TEXAS INSTRUMENTS

SN74AHC1G09
SCLS724F – MAY 2011 – REVISED FEBRUARY 2024

SN74AHC1G09 Single 2–Input Positive-AND Gate With Open-Drain Output

1 Features

- Operating range from 2V to 5.5V
- Low power consumption, 10µA maximum I_{CC}
- Maximum t_{pd} of 6ns at 5V
- ±8mA output drive at 5V
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Combining power good signals
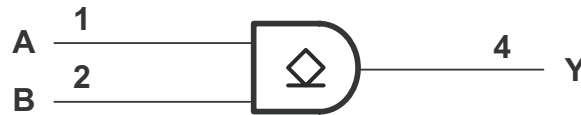- Enable digital signals

3 Description

The SN74AHC1G09 is a single 2-input positive-AND gate with an open drain output configuration. The device performs the Boolean logic $Y = A \times B$ in positive logic.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE[3]
SN74AHC1G09	DBV (SOT-23, 5)	2.9 mm × 2.8 mm	2.9 mm × 1.6 mm
	DCK (SC70, 5)	2 mm × 2.1 mm	2 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

Logic Diagram

⚠️ An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

Not to scale
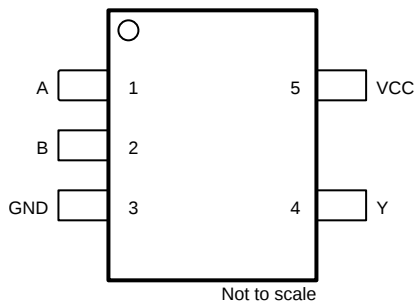
Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SC70 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input
B	2	I	Input
GND	3	—	Ground
V_{CC}	5	—	Power pin
Y	4	O	Output

(1)   I = input, O = output

Product Folder Links: *SN74AHC1G09*

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage[2]		−0.5	7	V
V_O	Output voltage[2]		−0.5	V_{CC} + 0.7	V
I_{IK}	Input clamp current	(V_I < 0)	−20		mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})	−20		mA
I_O	Continuous output current	(V_O = 0 to V_{CC})	−25	+25	mA
	Continuous current through V_{CC} or GND		−50	+50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

		SN74AHC1G09		UNIT
THERMAL METRIC[1]		**DBV (SOT-23)**	**DCK (SC70)**	**UNIT**
		5 PINS	**5 PINS**	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 50 µA	2 V				0.1	V
		3 V				0.1	
		4.5 V				0.1	
	I_{OL} = 4 mA	3 V	T_A = 25°C			0.36	
			T_A = −40°C to +85°C			0.44	
			T_A = −55°C to +125°C			0.55	
	I_{OL} = 8 mA	4.5 V	T_A = 25°C			0.36	
			T_A = −40°C to +85°C			0.44	
			T_A = −55°C to +125°C			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V	T_A = 25°C			±0.1	µA
			T_A = −40°C to +85°C			±1	
			T_A = −55°C to +125°C			±2	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V	T_A = 25°C			1	µA
			T_A = −40°C to +85°C			10	
			T_A = −55°C to +125°C			20	
C_i	V_I = V_{CC} or GND	5 V	T_A = 25°C		4	10	pF
			T_A = −55°C to +125°C			10	

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PD}	A or B	Y	C_L = 15 pF	T_A = 25°C		3.6	7	ns
				T_A = −40°C to +85°C	1		8	
				T_A = −55°C to +125°C	1		8.5	
	A or B	Y	C_L = 50 pF	T_A = 25°C		6.5	11	ns
				T_A = −40°C to +85°C	1.5		12	
				T_A = −55°C to +125°C	1.5		12.5	

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PD}	A or B	Y	C_L = 15 pF	T_A = 25°C		2.5	5	ns
				T_A = –40°C to +85°C	1		6	
				T_A = –55°C to +125°C	1		6.5	
	A or B	Y	C_L = 50 pF	T_A = 25°C		4.6	7.5	ns
				T_A = –40°C to +85°C	1.5		8	
				T_A = –55°C to +125°C	1.5		8.5	

5.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	5	pF

5.9 Typical Characteristics
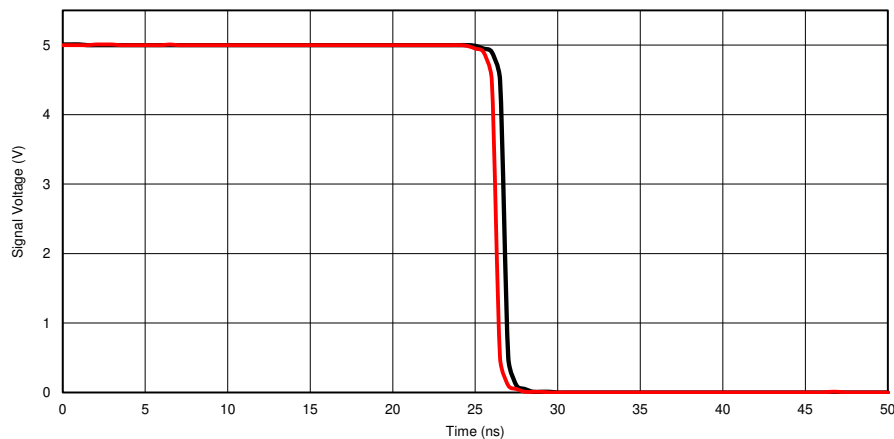
Figure 5-1. TPD Across V_{CC} at 25°C

Product Folder Links: *SN74AHC1G09*

6 Parameter Measurement Information

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

F. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD}.

G. t_{PZL} is measured at $V_{CC}/2$.

H. t_{PLZ} is measured at V_{OL} + 0.3 V.

Figure 6-1. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74AHC1G09*

7 Detailed Description

7.1 Overview

The SN74AHC1G09 device contains one open-drain positive-AND gate with a maximum sink current of 8 mA. A wide operating range of 2 V to 5.5 V enables this device to be used in many different systems, and a low t_{pd} qualifies this device to be used in high-speed applications.

7.2 Functional Block Diagram
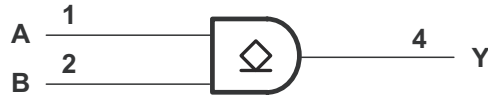
7.3 Feature Description

The wide operating voltage range of 2 V to 5 V allows the SN74AHC1G09 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation. The device is also equipped with Schmitt-trigger inputs, which increase the ability of the device to reject noise.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AHC1G09.

Table 7-1. Function Table

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H(Z)
L	X	L
X	L	L

Product Folder Links: *SN74AHC1G09*

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC1G09 is used in the following example in a basic power sequencing configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements to protect the device from malfunctioning.
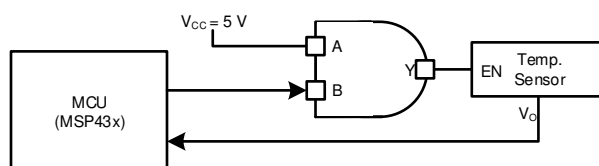
8.2 Typical Application

Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
    *   Rise time and fall time specifications. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
    *   Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
    *   Inputs are overvoltage-tolerant, allowing them to go as high as (V_I maximum) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Absolute Maximum Conditions:
    *   Load currents should not exceed (I_O maximum) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
    *   Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

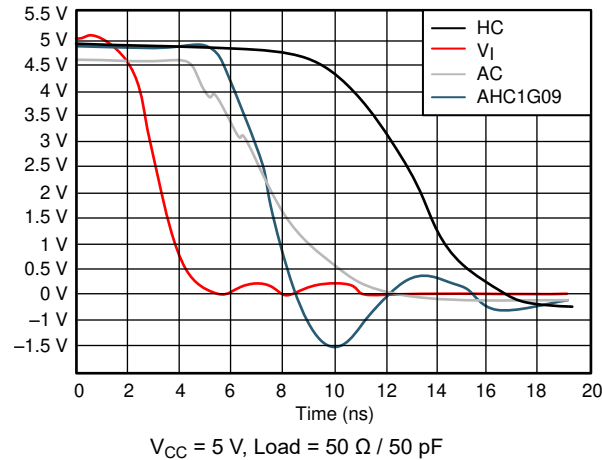
$V_{CC} = 5\ V$, Load = 50 Ω / 50 pF

Figure 8-2. I_{CC} vs Input Voltage

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended; if there are multiple V_{CC} pins, then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

The following are the rules that must be observed under all circumstances:
- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that should be applied to any particular unused input depends on the function of the device. Generally the unused inputs will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.
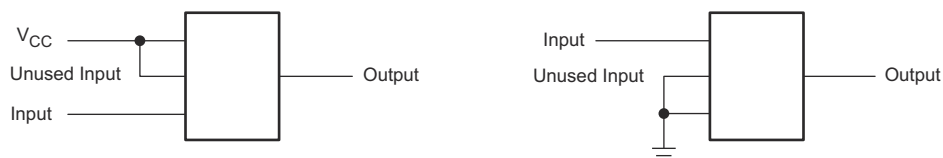
8.4.2 Layout Example

Figure 8-3. Layout Diagram

Product Folder Links: *SN74AHC1G09*

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Introduction to Logic* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2023) to Revision F (February 2024)	Page
• Updated RθJA values: DBV = 206 to 278, all values in °C/W...5	

Changes from Revision D (September 2016) to Revision E (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.................1	
• Updated RθJA values: DCK = 252 to 289.2, all values in °C/W 5	

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC1G09DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(38QH, 3BWF, A093, A09G, A09J)
SN74AHC1G09DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(38QH, 3BWF, A093, A09G, A09J)
SN74AHC1G09DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(1R8, AJ3, AJG, AJ J)
SN74AHC1G09DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(1R8, AJ3, AJG, AJ J)

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC1G09 :

- Automotive : SN74AHC1G09-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G09DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G09DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G09DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHC1G09DCKR	SC70	DCK	5	3000	210.0	185.0	35.0

2.4
1.8

1.4
1.1

B

A

PIN 1
INDEX AREA

1

5

2X 0.65

1.3

2

NOTE 4

(0.15)

1.3

2.15
1.85

(0.1)

3

4

5X 0.33
0.15

0.1 M C A B
NOTE 5

C

0.1 C

1.1 MAX

4X 0°-12°

(0.9)

0.1
0.0 TYP

4X 4°-15°

0.15

GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

0.46
0.26 TYP

SEATING PLANE

4214834/G   11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

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5X (0.95)

PKG

1

5X (0.4)

2

2X (0.65)

3

(R0.05) TYP

5

SYMM

(1.3)

4

(2.2)
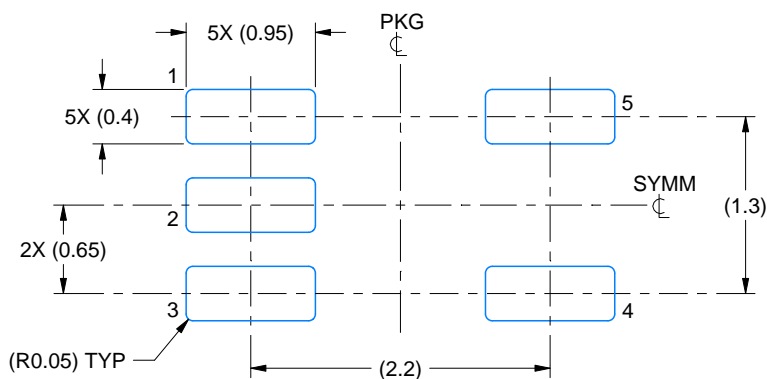
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK OPENING

METAL

EXPOSED METAL

0.07 MAX ARROUND

NON SOLDER MASK DEFINED (PREFERRED)

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

0.07 MIN ARROUND

SOLDER MASK DEFINED
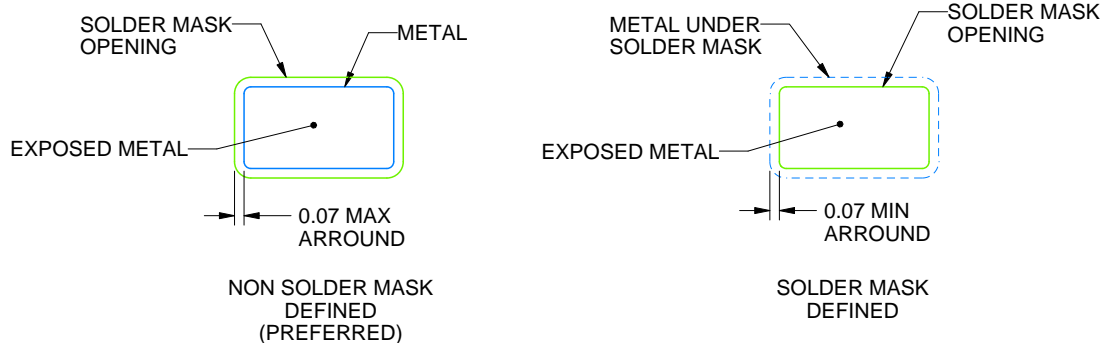
SOLDER MASK DETAILS

4214834/G   11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DCK0005A

PKG

5X (0.95)

1

5X (0.4)

5

2

SYMM

(1.3)

2X(0.65)

3

4

(R0.05) TYP

(2.2)

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G   11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

4214839/K   08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

PKG

5X (1.1)

1

5X (0.6)

2

5

SYMM

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K   08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER