









SN74AHC1G00

SCLS313Q - MARCH 1996 - REVISED JANUARY 2024

# **SN74AHC1G00 Single 2-Input Positive-NAND Gate**

#### 1 Features

- Operating range: 2 V to 5.5 V
- Maximum t<sub>pd</sub> of 6.5 ns at 5 V
- Low power consumption: maximum  $I_{CC}$  of 10  $\mu A$
- ±8-mA output drive at 5 V
- Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

## 3 Description

The SN74AHC1G00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### **Package Information**

PART NUMBER PACKAGE <sup>(1)</sup>		PACKAGE SIZE(2)	BODY SIZE(2)
	DBV (SOT-23, 5)	2.9 mm x 2.8 mm	2.9 mm x 1.6 mm
	DCK (SC-70, 5)	2 mm x 2.1 mm	2 mm × 1.25 mm
	DRL (SOT, 5)	1.6 mm × 1.6 mm	1.6 mm × 1.2 mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and (2) includes pins, where applicable.



Logic Diagram (Positive Logic)

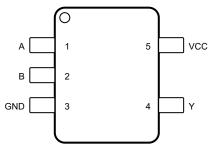


## **Table of Contents**

1 Features1	7.2 Functional Block Diagram	<u>ç</u>
2 Applications1	7.3 Feature Description	
3 Description1	7.4 Device Functional Modes	ç
4 Pin Configuration and Functions3	8 Application and Implementation	.10
5 Specifications4	8.1 Typical Application	. 10
5.1 Absolute Maximum Ratings4	8.2 Power Supply Recommendations	
5.2 ESD Ratings	8.3 Layout	. 12
5.3 Recommended Operating Conditions4	9 Device and Documentation Support	
5.4 Thermal Information5	9.1 Documentation Support	. 13
5.5 Electrical Characteristics5	9.2 Receiving Notification of Documentation Updates	.13
5.6 Switching Characteristics: V <sub>CC</sub> = 3.3 V ± 0.3 V6	9.3 Support Resources	. 13
5.7 Switching Characteristics: V <sub>CC</sub> = 5 V ± 0.5 V7	9.4 Trademarks	
5.8 Operating Characteristics7	9.5 Electrostatic Discharge Caution	13
5.9 Typical Characteristics7	9.6 Glossary	
6 Parameter Measurement information8	10 Revision History	. 13
7 Detailed Description9	11 Mechanical, Packaging, and Orderable	
7.1 Overview9	Information	. 14



## **4 Pin Configuration and Functions**



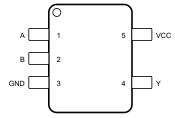


Figure 4-2. DCK Package 5-Pin SC70 Top View

Figure 4-1. DBV Package 5-Pin SOT-23 Top View

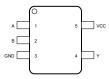


Figure 4-3. DRL Package 5-Pin SOT Top View

**Table 4-1. Pin Functions** 

P	IN	TYPE <sup>(1)</sup>	DESCRIPTION			
NO.	NAME	IIFE\/	DESCRIPTION			
1	Α	I	A input			
2	В	I	B input			
3	GND	_	Ground			
4	Y	0	Output			
5	V <sub>CC</sub>	_	Power			

(1) Signal Types: I = Input, O = Output, I/O = Input or Output



## **5 Specifications**

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage	Input voltage		7	V
V <sub>O</sub> (2)	Output voltage	Output voltage		V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)		-20	mA
I <sub>OK</sub>	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25	mA
	Continuous current through V <sub>CC</sub> or	GND		±50	mA
TJ	Maximum junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
	Input voltage	V <sub>CC</sub> = 5.5 V		1.65	
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 2 V		-50	μΑ
$I_{OH}$	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	IIIA
		V <sub>CC</sub> = 2 V		50	μA
$I_{OL}$	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 V \pm 0.5 V$		8	IIIA
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	ns/V
ΔυΔν	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20	115/ V

Product Folder Links: SN74AHC1G00

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
T <sub>A</sub> Operating free-air temperature	-40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

#### **5.4 Thermal Information**

			SN74AHC1G00				
	THERMAL METRIC(1)		DCK (SC70)	DRL (SOT)	UNIT		
		5 PINS	5 PINS	5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	256	°C/W		
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	180.5	205.8	130	°C/W		
R <sub>θJB</sub>	Junction-to-board thermal resistance	184.4	176.2	152	°C/W		
ΨЈТ	Junction-to-top characterization parameter	115.4	117.6	9.9	°C/W		
ΨЈВ	Junction-to-board characterization parameter	183.4	175.1	152	°C/W		
R <sub>0JC(bot)</sub>	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	°C/W		

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

#### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>	AMETER <sup>(1)</sup> TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
		T <sub>A</sub> = 25°C		1.9	2		
		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	2 V	1.9			
		$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$		1.9			
		T <sub>A</sub> = 25°C		2.9	3		
	I <sub>OH</sub> = -50 μA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	3 V	2.9			
		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2.9			
		T <sub>A</sub> = 25°C		4.4	4.5		V
V <sub>OH</sub> High level output voltage		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	4.5 V	4.4			
		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		4.4			
		T <sub>A</sub> = 25°C		2.58			
	I <sub>OH</sub> = -4 mA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	3 V	2.48			
		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		2.48			
		T <sub>A</sub> = 25°C		3.94			
	I <sub>OH</sub> = –8 mA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	4.5 V	3.8			
		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		3.8			

Copyright © 2024 Texas Instruments Incorporated

Submit Document Feedback

## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER <sup>(1)</sup>	TEST CO	NDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT	
			T <sub>A</sub> = 25°C				0.1		
			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	2 V			0.1	-	
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				0.1		
			T <sub>A</sub> = 25°C				0.1		
		I <sub>OL</sub> = 50 μA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	3 V			0.1		
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				0.1		
			T <sub>A</sub> = 25°C				0.1		
$V_{OL}$	Low level output voltage		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	4.5 V			0.1	- 1	
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				0.1		
			T <sub>A</sub> = 25°C	3 V 4.5 V			0.36		
		I <sub>OL</sub> = 4 mA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$				0.44	-	
			$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$				0.44		
			T <sub>A</sub> = 25°C				0.36		
		I <sub>OL</sub> = 8 mA	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$				0.44		
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				0.44		
			T <sub>A</sub> = 25°C				±0.1	μА	
$I_{\parallel}$	Input leakage current	V <sub>I</sub> = 5.5 V or GND	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	0 V to 5.5 V			±1		
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				±1		
			T <sub>A</sub> = 25°C				1		
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	5.5 V			10	μA	
			$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$				10		
			T <sub>A</sub> = 25°C			2	10	-	
$C_{i}$	Input Capacitance	$V_I = V_{CC}$ or GND	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	5 V			10		
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$				10		

<sup>(1)</sup> Recommended  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ 

# 5.6 Switching Characteristics: $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP	MAX	UNIT
				25°C		5.5	7.9	
t <sub>PLH</sub>				-40°C to +85°C	1		9.5	
	A or B	Y	C <sub>L</sub> = 15 pF	-40°C to +125°C	1		10.5	ns
	AOIB	ı	C[ - 13 pi	25°C		5.5	7.9	115
t <sub>PHL</sub>				-40°C to +85°C	1		9.5	
				-40°C to +125°C	1		10.5	
				25°C		8	11.4	
t <sub>PLH</sub>				-40°C to +85°C	1		13	
	A or B	Y	C <sub>L</sub> = 50 pF	-40°C to +125°C	1		14	ns
t <sub>PHL</sub>	AOIB	Ť	CL = 30 pr	25°C		8	11.4	115
				-40°C to +85°C	1		13	
				-40°C to +125°C	1		14	

<sup>(1)</sup> Recommended  $T_A = -40$ °C to +125°C

Product Folder Links: SN74AHC1G00

## 5.7 Switching Characteristics: $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP	MAX	UNIT
				25°C		3.7	5.5	
t <sub>PLH</sub>				-40°C to +85°C	1		6.5	
	A or B	Y	C <sub>L</sub> = 15 pF	-40°C to +125°C	1		7	ns
	AOIB	1	т С <sub>L</sub> – 13 рг	25°C		3.7	5.5	115
t <sub>PHL</sub>				-40°C to +85°C	1		6.5	
				-40°C to +125°C	1		7	
				25°C		5.2	7.5	
t <sub>PLH</sub>				-40°C to +85°C	1		6.5	
	A or B	Y	C <sub>L</sub> = 50 pF	-40°C to +125°C	1		9	no
	AUB	ĺ	OL - 30 PF	25°C		5.2	7.5	ns
t <sub>PHL</sub>				-40°C to +85°C	1		6.5	
				-40°C to +125°C	1		9	

<sup>(1)</sup> Recommended  $T_A = -40^{\circ}C$  to +125°C

## 5.8 Operating Characteristics

 $V_{CC}$  = 5 V,  $T_A$  = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load, f = 1 MHz		9.5		pF

## **5.9 Typical Characteristics**

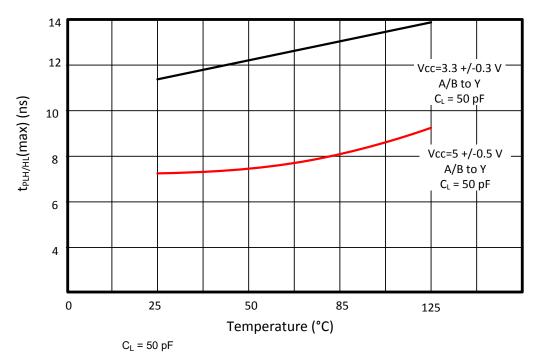
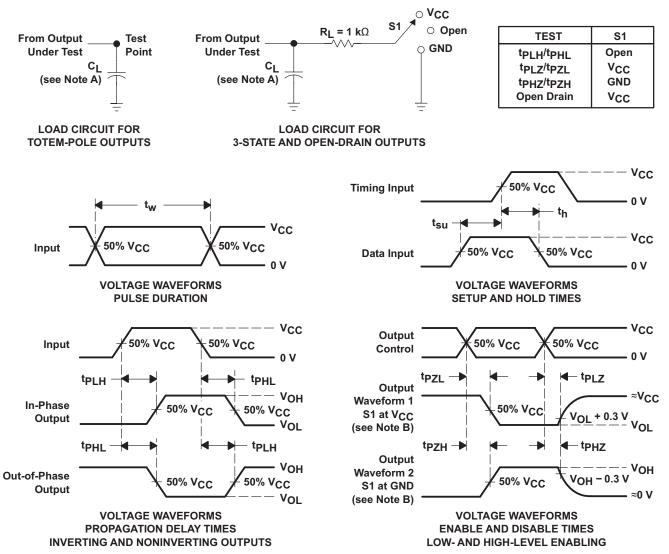


Figure 5-1. Propagation Delay vs Temperature



### **6 Parameter Measurement information**



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

Product Folder Links: SN74AHC1G00



## 7 Detailed Description

#### 7.1 Overview

The SN74AHC1G00 device performs the NAND Boolean function  $Y = \overline{A} \times \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic. The device has a wide operating range of  $V_{CC}$  from 2 V to 5 V.

## 7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Logic)

## 7.3 Feature Description

The SN74AHC1G00 device has wide operating voltage range for logic system from 2 V to 5 V. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption of 10-uA (maximum) makes this device a good choice for portable and battery power-sensitive applications. The Schmitt trigger action on all inputs have noise rejection capabilities.

#### 7.4 Device Functional Modes

Table 7-1. Function Table

INPU	OUTPUT <sup>(2)</sup>	
Α	В	Υ
Н	Н	L
L	X	Н
X	L	Н

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Typical Application



Figure 8-1. Typical Application

#### 8.1.1 Design Requirements

This SN74AHC1G00 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

## 8.1.2 Detailed Design Procedure

- · Recommended input conditions:
  - Specified high and low levels. See V<sub>IH</sub> and V<sub>IL</sub> in Section 5.3.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>.
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V<sub>CC</sub>.

Product Folder Links: SN74AHC1G00



## 8.1.3 Application Curve

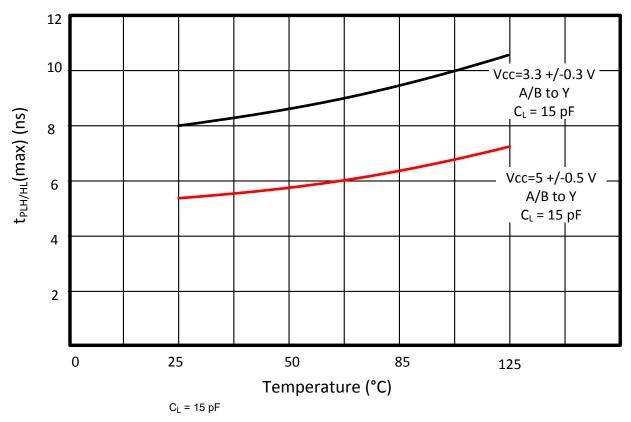


Figure 8-2. Propagation Delay vs Temperature

#### 8.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 5.3.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 8.3 Layout

#### 8.3.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float.

In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following are the rules must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the input and output, so they also cannot float when disabled.

#### 8.3.2 Layout Example



Figure 8-3. Layout Recommendation

Copyright © 2024 Texas Instruments Incorporated Product Folder Links: SN74AHC1G00

## 9 Device and Documentation Support

## 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Introduction to Logic application report
- · Texas Instruments, Implications of Slow or Floating CMOS Inputsapplication note

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossarv

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision P (October 2023) to Revision Q (January 2024)

**Page** 

#### Changes from Revision O (April 2016) to Revision P (October 2023)

Pag

- Updated the numbering format for tables, figures, and cross-references throughout the document......

Copyright © 2024 Texas Instruments Incorporated



## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74AHC1G00

www.ti.com 7-Oct-2025

## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AHC1G00DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(35XH, 3BSF, A003, A00G, A00J, A 00L, A00S)
SN74AHC1G00DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(35XH, 3BSF, A003, A00G, A00J, A 00L, A00S)
SN74AHC1G00DBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DBVT	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 125	(A003, A00G, A00J, A00S)
SN74AHC1G00DBVTG4.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DCK3	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	AAY
SN74AHC1G00DCK3.A	Last Time Buy	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 125	AAY
SN74AHC1G00DCKR	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QP, AA3, AAG, AA J, AAL, AAS)
SN74AHC1G00DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QP, AA3, AAG, AA J, AAL, AAS)
SN74AHC1G00DCKRE4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKRG4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKT	Obsolete	Production	SC70 (DCK)   5	-	-	Call TI	Call TI	-40 to 125	(AA3, AAG, AAJ, AA S)
SN74AHC1G00DCKTG4	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKTG4.A	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DRLR	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(AAB, AAS)
SN74AHC1G00DRLR.A	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(AAB, AAS)

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

## PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74AHC1G00:

Automotive: SN74AHC1G00-Q1

NOTE: Qualified Version Definitions:

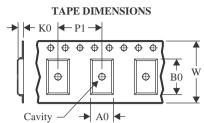
Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 8-Nov-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3



www.ti.com 8-Nov-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025