

SN74AHC125-Q1 Automotive Quadruple Bus Buffer Gate with 3-State Outputs

1 Features

- Qualified for automotive applications
- EPIC™ (Enhanced-Performance Implanted CMOS) process
- Operating range 2-V to 5.5-V V_{CC}
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Flow meters
- Programmable logic controllers
- Power on Ethernet® (PoE)
- [Motor drives and controls](#)
- [Electronic point-of-sale](#)

3 Description

The SN74AHC125-Q1 is a quadruple bus buffer gate featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

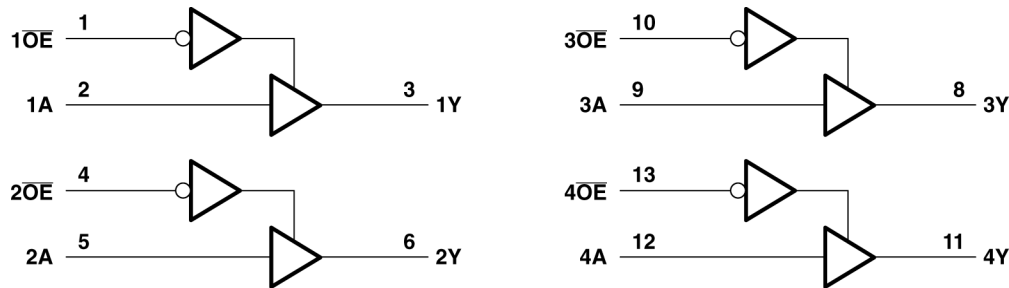
To put the device in the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE ¹	PACKAGE SIZE ²
SN74AHC125-Q1	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	BQA (WQFN, 14)	3mm × 2.5mm

(1) For more information, see [Section 9](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	6 Parameter Measurement Information	7
2 Applications	1	7 Detailed Description	8
3 Description	1	7.1 Functional Block Diagram.....	8
4 Pin Configuration and Functions	3	7.2 Device Functional Modes.....	8
5 Specifications	4	8 Device and Documentation Support	9
5.1 Absolute Maximum Ratings.....	4	8.1 Documentation Support.....	9
5.2 ESD Ratings.....	4	8.2 Receiving Notification of Documentation Updates.....	9
5.3 Recommended Operating Conditions.....	4	8.3 Support Resources.....	9
5.4 Thermal Information.....	5	8.4 Trademarks.....	9
5.5 Electrical Characteristics.....	5	8.5 Electrostatic Discharge Caution.....	9
5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	8.6 Glossary.....	9
5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	9 Mechanical, Packaging, and Orderable Information	9
5.8 Noise Characteristics.....	6	10 Revision History	9
5.9 Operating Characteristics.....	6		

4 Pin Configuration and Functions

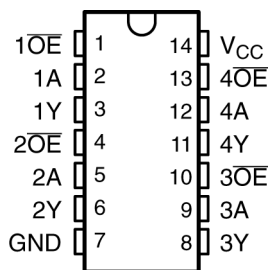


Figure 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

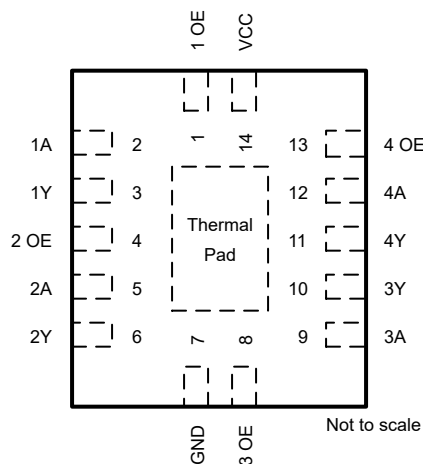


Figure 4-2. BQA Package, 14-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1 OE	1	I	Output enable
1A	2	I	Input
1Y	3	O	Output
2 OE	4	I	Output enable
2A	5	I	Input
2Y	6	O	Output
3 OE	8	I	Output enable
3A	9	I	Input
3Y	10	I	Output
4 OE	13	I	Output enable
4A	12	I	Input
4Y	11	O	Output
GND	7	—	Ground
V _{CC}	14	I	Supply voltage
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

- (1) I = input, O = output
(2) For BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I ¹	Input voltage range	-0.5	7	V
V_O ¹	Output voltage range	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$(V_I < 0)$		-20 mA
I_{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20 mA
I_O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±25 mA
	Continuous current through V_{CC} or GND			±50 mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽³⁾	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2 \text{ V}$	1.5	V
		$V_{CC} = 3 \text{ V}$	2.1	
		$V_{CC} = 5.5 \text{ V}$	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 2 \text{ V}$	0.5	V
		$V_{CC} = 3 \text{ V}$	0.9	
		$V_{CC} = 5.5 \text{ V}$	1.65	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2 \text{ V}$	-50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	-8	
I_{OL}	Low-level output current	$V_{CC} = 2 \text{ V}$	50	mA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	ns/V

over operating free-air temperature range (unless otherwise noted)¹

	MIN	MAX	UNIT
T _A Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC	SN74AHC125-Q1			UNIT
	D (SOIC)	PW (TSSOP)	BQA (WQFN)	
	14 PINS	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance ⁽¹⁾	86	147.7	88.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4mA	3 V	2.58			2.48		
	I _{OH} = -8mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4mA	3 V			0.36		0.5	
	I _{OL} = 8mA	4.5 V			0.36		0.5	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	μA
C _i	V _I = V _{CC} or GND	5 V		4	10			pF

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15pF		5.6	8	1	9.5	ns
t _{PHL}					5.6	8	1	9.5	
t _{PZH}	OE	Y	C _L = 15pF		5.4	8	1	9.5	ns
t _{PZL}					5.4	8	1	9.5	
t _{PHZ}	OE	Y	C _L = 15pF		7	9.7	1	11.5	ns
t _{PLZ}					7	9.7	1	11.5	
t _{PLH}	A	Y	C _L = 50pF		8.1	11.5	1	13	ns
t _{PHL}					8.1	11.5	1	13	
t _{PZH}	OE	Y	C _L = 50pF		7.9	11.5	1	13	ns
t _{PZL}					7.9	11.5	1	13	

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{pF}$	9.5	13.2		1	15	ns
t_{PLZ}				9.5	13.2		1	15	

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{pF}$	3.8	5.5		1	6.5	ns
t_{PHL}				3.8	5.5		1	6.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{pF}$	3.6	5.1		1	6	ns
t_{PZL}				3.6	5.1		1	6	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{pF}$	4.6	6.8		1	8	ns
t_{PLZ}				4.6	6.8		1	8	
t_{PLH}	A	Y	$C_L = 50\text{pF}$	5.3	7.5		1	8.5	ns
t_{PHL}				5.3	7.5		1	8.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{pF}$	5.1	7.1		1	8	ns
t_{PZL}				5.1	7.1		1	8	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{pF}$	6.1	8.8		1	10	ns
t_{PLZ}				6.1	8.8		1	10	

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

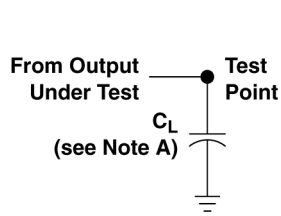
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

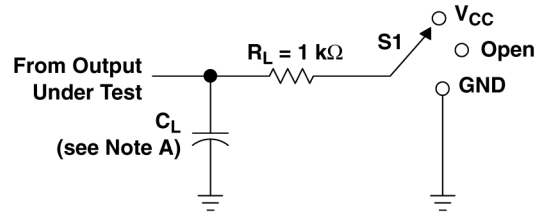
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	$f = 1\text{MHz}$	14	pF

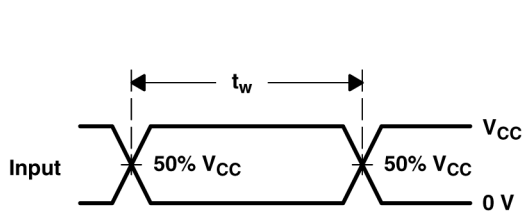
6 Parameter Measurement Information



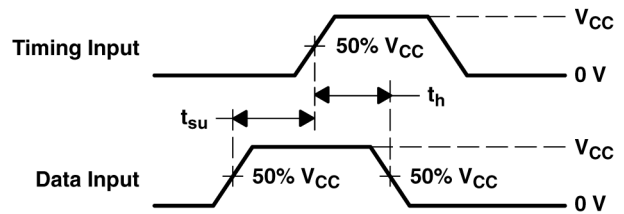
**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**



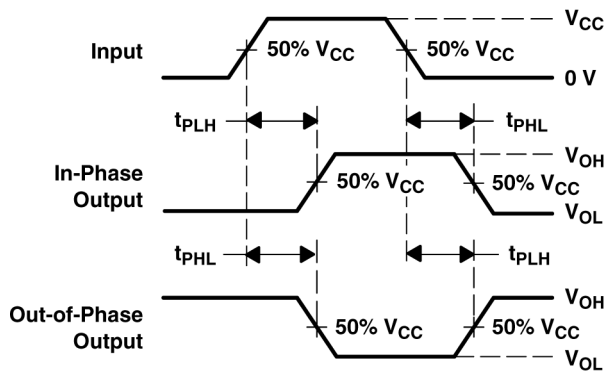
**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**



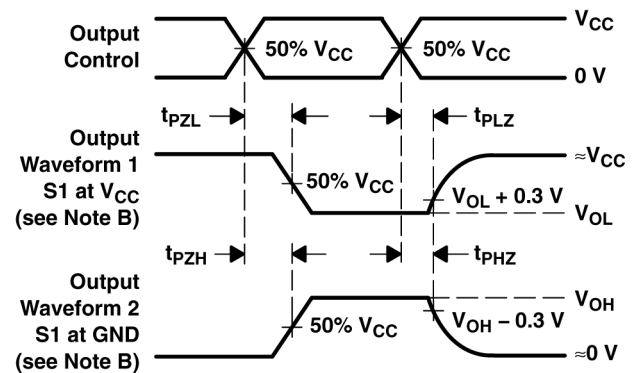
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Functional Block Diagram

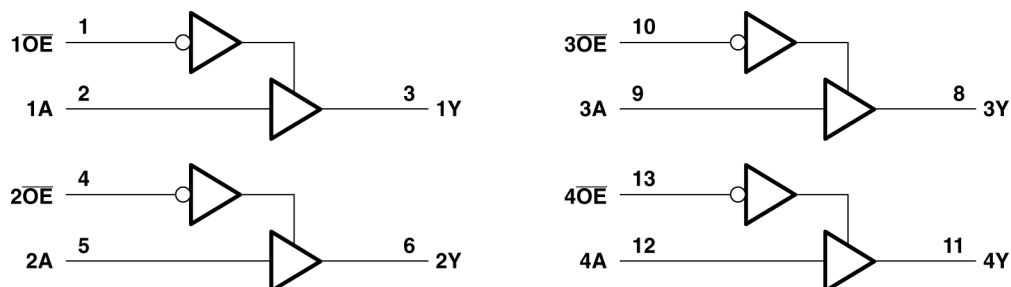


Figure 7-1. Logic Diagram (Positive Logic)

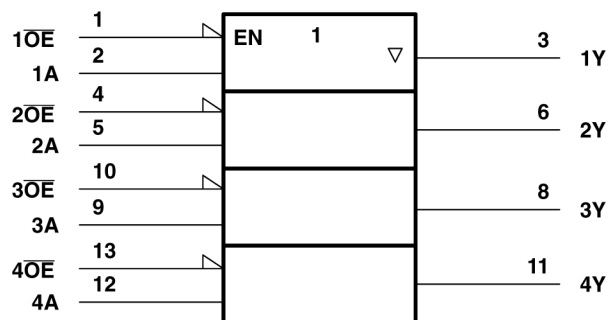


Figure 7-2. Logic Symbol†

†

7.2 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

Ethernet® is a registered trademark of Xerox Corporation.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2023) to Revision C (April 2024)	Page
• Added the BQA package to the data sheet.	1

Changes from Revision A (April 2008) to Revision B (June 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Added BQA package to <i>Package Information</i> table.....	1
• Updated thermal values for PW package from RθJA = 113 to 147.7, all values in °C/W	5
• Added thermal value for BQA package: RθJA = 88.3, all values in °C/W.....	5

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC125QDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125Q
SN74AHC125QDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125Q
SN74AHC125QPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125Q
SN74AHC125QPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125Q
SN74AHC125QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AHC125Q
SN74AHC125QPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AHC125Q
SN74AHC125QWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC125Q
SN74AHC125QWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC125Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC125-Q1 :

- Catalog : [SN74AHC125](#)
- Enhanced Product : [SN74AHC125-EP](#)
- Military : [SN54AHC125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

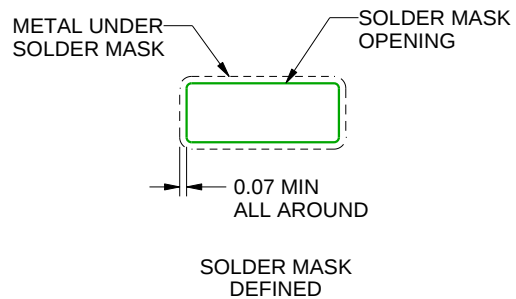
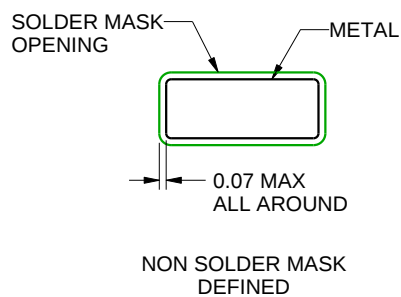
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

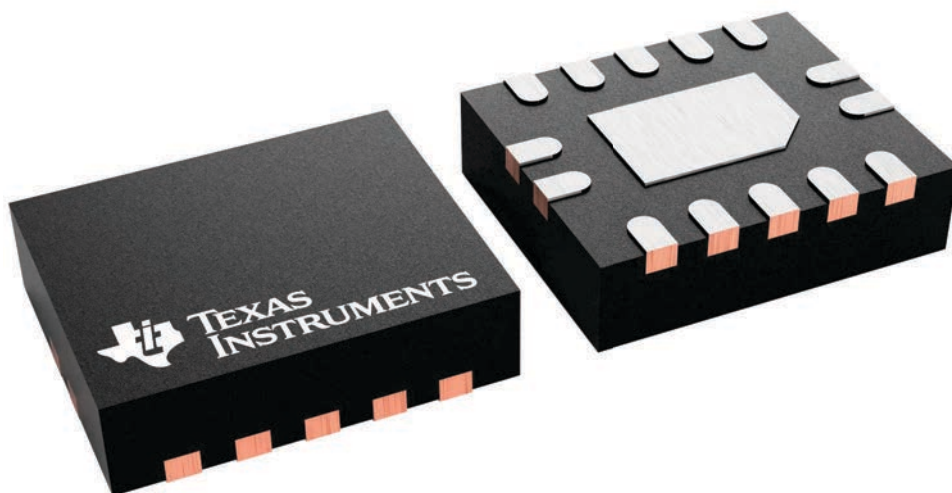
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



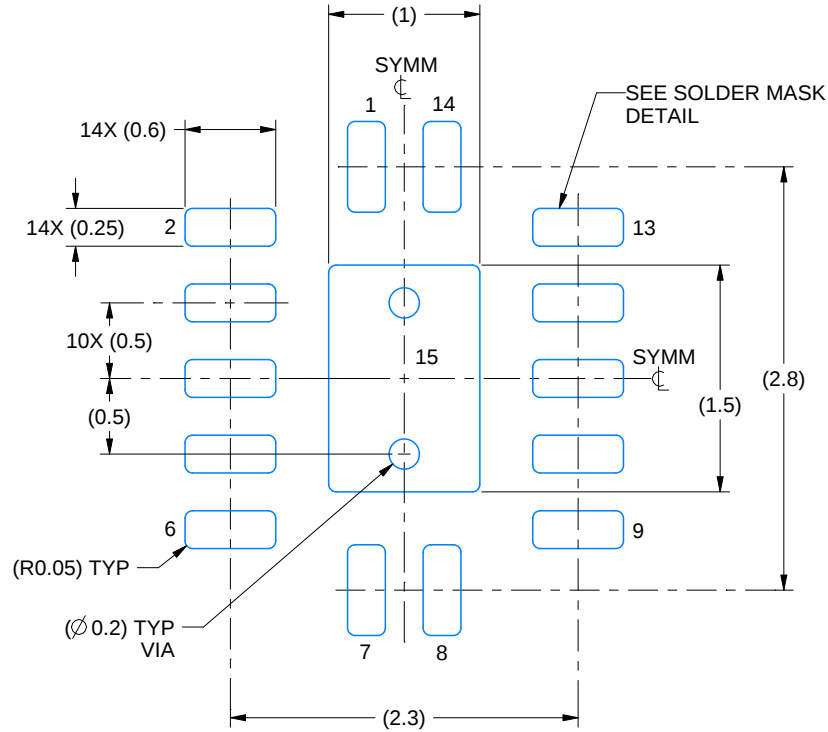
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

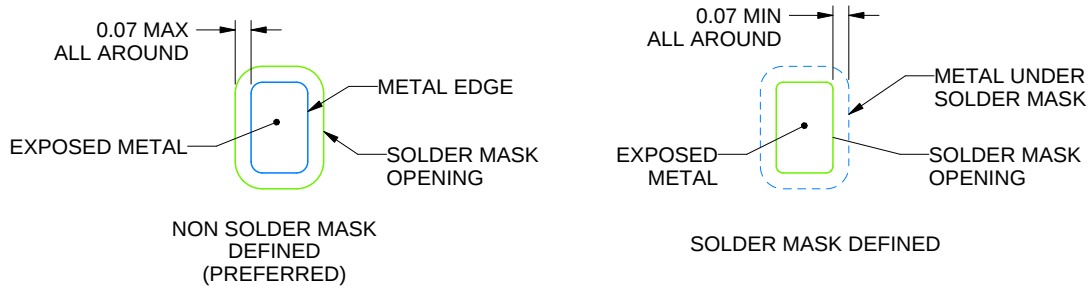
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

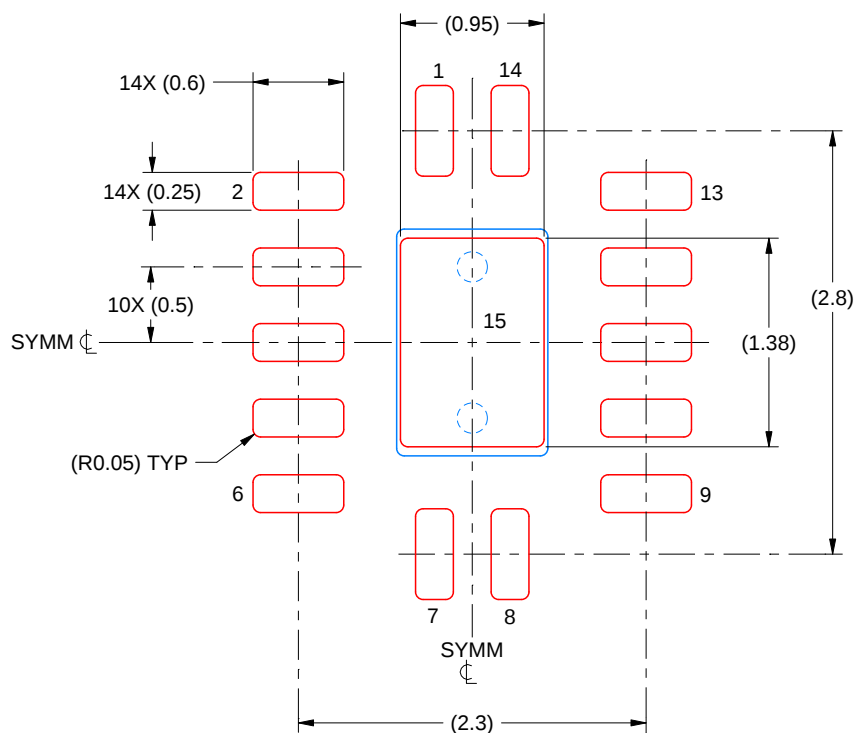
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



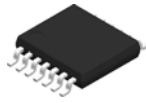
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated