

# SN54AHC05, SN74AHC05 HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

SCLS357H – MAY 1997 – REVISED JULY 2003

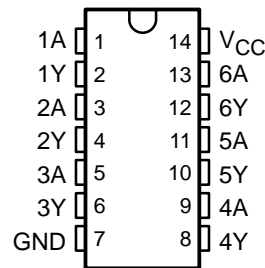
- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

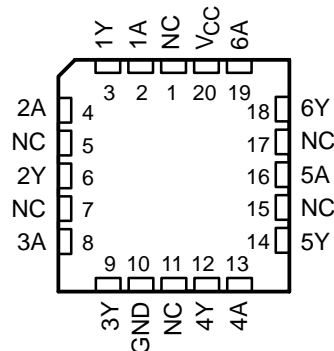
The 'AHC05 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ .

The open-drain outputs require pullup resistors to perform correctly. They can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

SN54AHC05 . . . J OR W PACKAGE  
SN74AHC05 . . . D, DB, DGV, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC05 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC05N	SN74AHC05N
	SOIC – D	Tube	SN74AHC05D	AHC05
		Tape and reel	SN74AHC05DR	
	SSOP – DB	Tape and reel	SN74AHC05DBR	HA05
	TSSOP – PW	Tube	SN74AHC05PW	HA05
		Tape and reel	SN74AHC05PWR	
TVSOP – DGV	Tape and reel	SN74AHC05DGVR	HA05	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC05J	SNJ54AHC05J
	CFP – W	Tube	SNJ54AHC05W	SNJ54AHC05W
	LCCC – FK	Tube	SNJ54AHC05FK	SNJ54AHC05FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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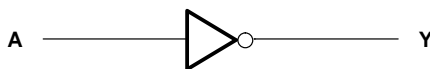
**SN54AHC05, SN74AHC05  
HEX INVERTERS  
WITH OPEN-DRAIN OUTPUTS**

SCLS357H – MAY 1997 – REVISED JULY 2003

**FUNCTION TABLE  
(each inverter)**

INPUT A	OUTPUT Y
H	L
L	H

**logic diagram, each inverter (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package .....	86°C/W
DB package .....	96°C/W
DGV package .....	127°C/W
N package .....	80°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN54AHC05, SN74AHC05**  
**HEX INVERTERS**  
**WITH OPEN-DRAIN OUTPUTS**  
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**recommended operating conditions (see Note 3)**

		SN54AHC05		SN74AHC05		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5		V
		V <sub>CC</sub> = 3 V		2.1		
		V <sub>CC</sub> = 5.5 V		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		V
		V <sub>CC</sub> = 3 V		0.9		
		V <sub>CC</sub> = 5.5 V		1.65		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4		
		V <sub>CC</sub> = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100		ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC05		SN74AHC05		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	0.1	0.1	V	
		3 V			0.1	0.1	0.1			
		4.5 V			0.1	0.1	0.1			
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.5	0.44			
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.5	0.44			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	±1*	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2	20	20	μA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2.5	10	10	pF		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC05		SN74AHC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 15 pF		2.9**	7.1**	1**	8.5**	1	8.5	ns
t <sub>PZL</sub>					4**	7.1**	1**	8.5**	1	8.5	
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 50 pF		4.7	10.6	1	12	1	12	ns
t <sub>PZL</sub>					5.8	10.6	1	12	1	12	

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**SN54AHC05, SN74AHC05  
HEX INVERTERS  
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**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC05		SN74AHC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 15 pF	2.2*	5.5*	1*	6.5*	1	6.5	ns	
t <sub>PZL</sub>				2.9*	5.5*	1*	6.5*	1	6.5		
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 50 pF	3.4	7.5	1	8.5	1	8.5	ns	
t <sub>PZL</sub>				4.2	7.5	1	8.5	1	8.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

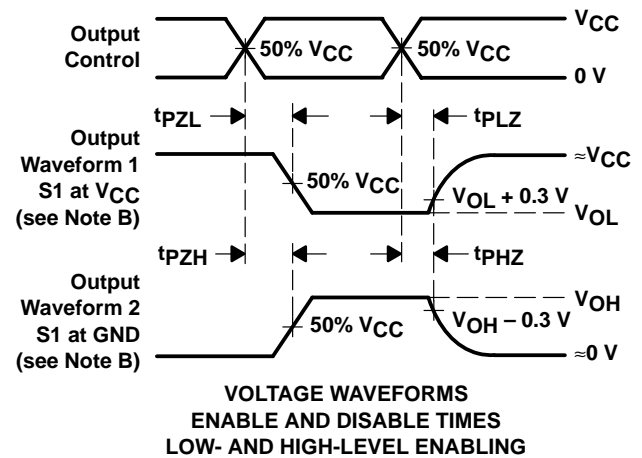
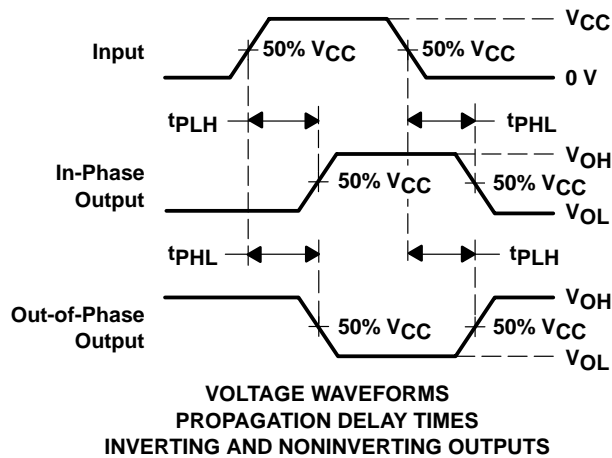
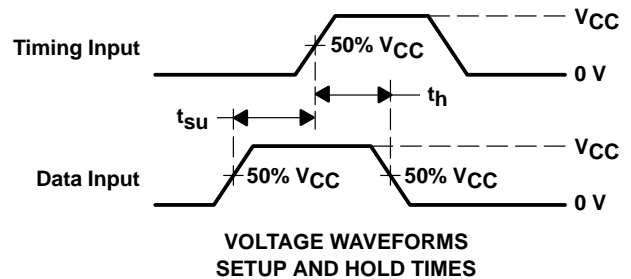
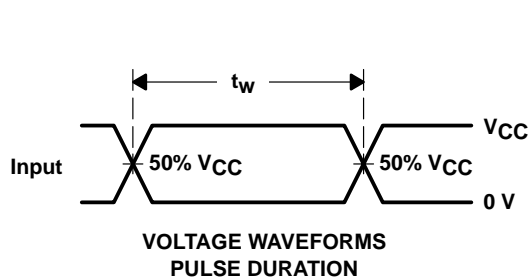
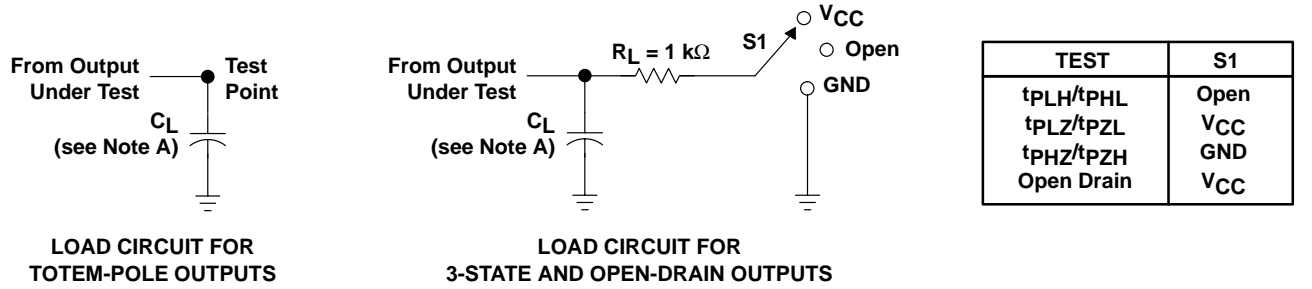
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	3	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 3 ns, t<sub>f</sub> ≤ 3 ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AHC05D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	AHC05
<a href="#">SN74AHC05DBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05
SN74AHC05DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05
<a href="#">SN74AHC05DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC05
SN74AHC05DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC05
<a href="#">SN74AHC05N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC05N
SN74AHC05N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC05N
<a href="#">SN74AHC05PW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HA05
<a href="#">SN74AHC05PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05
SN74AHC05PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC05DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC05DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC05DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC05PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC05N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC05N.A	N	PDIP	14	25	506	13.97	11230	4.32



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220762/A 05/2024

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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