









SN54AHC00, SN74AHC00

SCLS227M - OCTOBER 1995 - REVISED MAY 2024

SNx4AHC00 Quadruple 2-Input Positive-NAND Gates

1 Features

- Operating range 2V to 5.5V
- Latch-up performance exceeds 250mA per JESD

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

3 Description

The 'AHC00 devices perform the Boolean function Y $= \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information

	201100		
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	J (CDIP, 14)	19.55mm x 7.9mm	19.56mm × 6.67mm
SN54AHC00	W (CFP, 14)	9.21mm x 9mm	9.21mm × 6.3mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 1.58mm
	DB (SSOP, 14)	6.20mm × 7.8mm	6.20mm × 1.95mm
	DGV (TVSOP, 14)	3.60mm × 6.4mm	3.60mm × 1.05mm
SN74AHC00	N (PDIP, 14)	19.30mm × 9.4mm	19.30mm × 6.30mm
SN/4AHC00	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 1.95mm
	PW (SOP, 14)	5.00mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.5mm	3.50mm × 3.5mm
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and (2) includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.





Table of Contents

1 Features1	7.1 Functional Block Diagram
2 Applications 1	7.2 Device Functional Modes
3 Description1	8 Application and Implementation10
4 Pin Configuration and Functions3	8.1 Power Supply Recommendations10
5 Specifications5	8.2 Layout10
5.1 Absolute Maximum Ratings5	9 Device and Documentation Support1
5.2 ESD Ratings5	9.1 Documentation Support1
5.3 Recommended Operating Conditions5	9.2 Receiving Notification of Documentation Updates 1
5.4 Thermal Information6	9.3 Support Resources1
5.5 Electrical Characteristics6	9.4 Trademarks1
5.6 Switching Characteristics, V _{CC} = 3.3 V ± 0.3 V6	9.5 Electrostatic Discharge Caution1
5.7 Switching Characteristics, V _{CC} = 5 V ± 0.5 V7	9.6 Glossary1
5.8 Noise Characteristics7	10 Revision History1
5.9 Operating Characteristics7	11 Mechanical, Packaging, and Orderable
6 Parameter Measurement Information8	Information12
7 Detailed Description9	



4 Pin Configuration and Functions

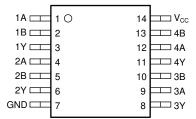


Figure 4-1. SN54AHC00 J or W Package, 14-Pin CDIP or CFP (Top View); SN74AHC00 D, DB, DGV, N, NS, or PW Package, 14-Pin SOIC, SSOP, TVSOP, PDIP, SOP, or TSSOP (Top View)

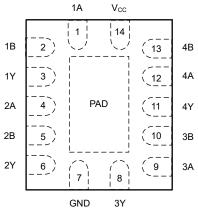
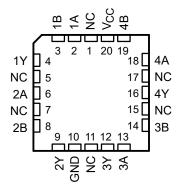


Figure 4-2. SN74AHC00 RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)



NC - No internal connection

Figure 4-3. SN54AHC00 FK Package, 20-Pin LCCC (Top View)



Table 4-1. Pin Functions

	PIN				
	SN74AHC00	SN54	AHC00	TYPE ⁽¹⁾	DESCRIPTION
NAME	D, DB, DGV, N, NS, PW, RGY, BQA	J, W	FK		DESSAI HOIV
1A	1	1	2	I	1A Input
1B	2	2	3	I	1B Input
1Y	3	3	4	0	1Y Output
2A	4	4	6	I	2A Input
2B	5	5	8	I	2B Input
2Y	6	6	9	0	2Y Output
GND	7	7	10	_	Ground Pin
3A	8	8	13	I	3A Input
3B	9	9	14	I	3B Input
3Y	10	10	12	0	3Y Output
4A	11	11	18	I	4A Input
4B	12	12	19	I	4B Input
4Y	13	13	16	0	4Y Output
V _{CC}	14	14	20	_	Power Pin
NC	_	_	1, 5, 7, 11, 15, 17	_	No Connection

⁽¹⁾ I = input, O = output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I (2)	Input voltage range		-0.5	7	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20	mA
Io	Continuous output current	(V _O = 0 to V _{CC})		±25	mA
	Continuous current through V _{CC}	or GND		±50	mA
T _{stg}	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
V (ESD)	Lieulostalic discharge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AH	C00	SN74AH	C00	UNIT
			MIN	MAX	MIN	MAX	UNII
V _{CC}	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
V_{IH}	High-level input voltage	V _{CC} = 3V	2.1		2.1		V
		V _{CC} = 5.5 V	3.85		3.85		
		V _{CC} = 2 V		0.5		0.5	
V_{IL}	Low-level Input voltage	V _{CC} = 3 V		0.9		0.9	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	5.5	0	5.5	V
Vo	Output voltage		0	V _{CC}	0	V _{CC}	V
		V _{CC} = 2 V		-50		-50	
I _{OH}	High-level output current	V_{CC} = 3.3 V ± 0.3 V		-4		-4	mA
		V _{CC} = 5 V ± 0.5 V		-8		-8	
		V _{CC} = 2 V		50		50	
I_{OL}	Low-level output current	V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V _{CC} = 5 V ± 0.5 V		8		8	
A4/A.,	Innut Transition rise or fell reta	V _{CC} = 3.3 V ± 0.3 V		100		100	no/\/
Δt/Δv	Input Transition rise or fall rate	V _{CC} = 5 V ± 0.5 V 20			20	ns/V	
T _A	Operating free-air temperature	,	– 55	125	-40	125	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Information

			SN74AHC00							
	THERMAL METRIC(1)		DB	DGV	N	NS	PW	RGY	BQA	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	96	127	80	76	147.7	87.1	88.3	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

						T _A = -55° 125°		T _A = -40° 85°C		T _A = -40° 125°C		
PARAMETER	TEST CONDITIONS	Vcc	T _A = 25°C		;	0154411000		SN74AHC00		Recommended		UNIT
						SN54AHC00		SN/4AHC00		SN74AHC00		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		2 V	1.9	2		1.9		1.9		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		3.8		
	I _{OL} = 50 μA	2 V			0.1		0.1		0.1		0.1	
		3 V			0.1		0.1		0.1		0.1	
V _{OL}		4.5 V			0.1	,	0.1		0.1	,	0.1	V
	I _{OH} = 4 mA	3 V			0.36	,	0.5		0.44	,	0.5	
	I _{OH} = 8 mA	4.5 V			0.36		0.5		0.44	,	0.5	
I ₁	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		±1	μA
Icc	$V_1 = V_{CC} \text{ or } $ $I_O = 0$	5.5 V			2		20		20		20	μA
Ci	V _I = V _{CC} or GND	5 V		2	10				10			pF

⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

5.6 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

				LOAD T _A = 25°C 125°C		T _A = -55°C TO		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE			•	03		Recommended		UNIT		
	((001101)	OAI AGITANGE				HC00	SN74AHC00		SN74AHC00			
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t _{PLH}	A or P	V	C = 15 pE	5.5 ⁽¹⁾	7.9 ⁽¹⁾	1 ⁽¹⁾	9.5 <mark>(1)</mark>	1	9.5	1	9.5	no	
t _{PHL}	A or B	T C	ļ ř	C _L = 15 pF	5.5 ⁽¹⁾	7.9 ⁽¹⁾	1 ⁽¹⁾	9.5 <mark>(1)</mark>	1	9.5	1	9.5	ns
t _{PLH}	A or B	Υ	C _L = 50 pF	8	11.4	1	13	1	13	1	13	ns	
t _{PHL}	AOIB	l I	С[– 30 рі	8	11.4	1	13	1	13	1	13	115	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

						T _A = -55°C TO		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C 125°C		125 C 05 C			Recommended		UNIT	
	(0.)	(551151)	0,,				SN54AHC00		SN74AHC00		SN74AHC00	
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	3.7 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	6.5	
t _{PHL}	AOIB	,		3.7 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	6.5	ns
t _{PLH}	A or B	Y	C _L = 50 pF	5.2	7.5	1	8.5	1	8.5	1	8.5	ns
t _{PHL}	AUID	'		C _L = 50 pF	5.2	7.5	1	8.5	1	8.5	1	8.5

5.8 Noise Characteristics

 $V_{CC} = 5 \text{ V}, C_{L} = 50 \text{ pF}, T_{A} = 25^{\circ}\text{C}^{(1)}$

	PARAMETER	SN	UNIT		
	FARAMETER	MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.3	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.3	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.6		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

⁽¹⁾ Characteristics are for surface-mount packages only.

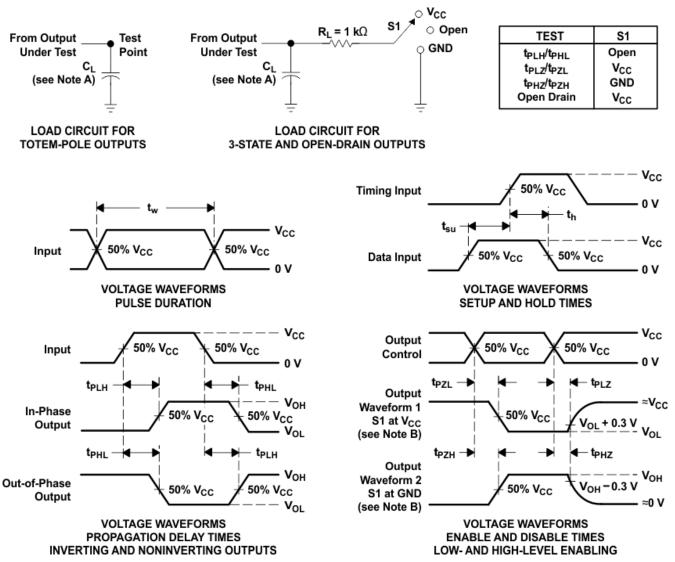
5.9 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST (CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF



6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated



7 Detailed Description

7.1 Functional Block Diagram



Figure 7-1. Logic Diagram, Each Gate (Positive Logic)

7.2 Device Functional Modes

Table 7-1. Function Table (Each Gate)

	INPUTS ⁽¹⁾			
Α	В	OUTPUT Y		
Н	Н	L		
L	X	Н		
X	L	Н		

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in Section 5.3.

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Layout Example*.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example

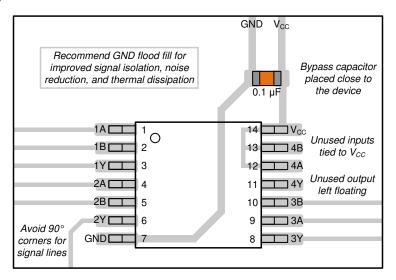


Figure 8-1. Example Layout for the SN74AHC00

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated



9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC00	Click here	Click here	Click here	Click here	Click here
SN74AHC00	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (June 2023) to Revision L (February 2024)

Page

Updated RθJA value: RGY = 47 to 87.1, all values in °C/W6



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN54AHC00 SN74AHC00

www.ti.com

12-Dec-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9682201Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9682201Q2A SNJ54AHC 00FK
5962-9682201QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QC A SNJ54AHC00J
5962-9682201QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QD A SNJ54AHC00W
SN74AHC00BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	AHC00
SN74AHC00DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00DGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00DRG4.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC00N
SN74AHC00N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC00N
SN74AHC00NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00
SN74AHC00PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	HA00
SN74AHC00PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00PWRG3	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HA00





www.ti.com

12-Dec-2025

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AHC00PWRG3.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00RGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SN74AHC00RGYRG4.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00
SNJ54AHC00FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9682201Q2A SNJ54AHC 00FK
SNJ54AHC00FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9682201Q2A SNJ54AHC 00FK
SNJ54AHC00J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QC A SNJ54AHC00J
SNJ54AHC00J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QC A SNJ54AHC00J
SNJ54AHC00W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QD A SNJ54AHC00W
SNJ54AHC00W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682201QD A SNJ54AHC00W

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

www.ti.com 12-Dec-2025

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC00, SN74AHC00:

Catalog: SN74AHC00

Automotive: SN74AHC00-Q1, SN74AHC00-Q1

Enhanced Product: SN74AHC00-EP, SN74AHC00-EP

Military: SN54AHC00

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications



www.ti.com 6-Nov-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC00BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC00DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC00DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC00DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC00DRG4	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC00NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC00PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC00RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



www.ti.com 6-Nov-2025



*All dimensions are nominal

ar arriversorers are membras							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC00BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC00DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC00DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC00DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC00DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC00NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC00PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC00PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74AHC00RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74AHC00RGYRG4	VQFN	RGY	14	3000	360.0	360.0	36.0

PACKAGE MATERIALS INFORMATION

www.ti.com 6-Nov-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9682201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9682201QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC00N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC00N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC00FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC00FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC00W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHC00W.A	W	CFP	14	25	506.98	26.16	6220	NA

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com

PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025