

SN74ACT11-Q1 Automotive Triple 3-Input AND Gates

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in [wettable flank](#) QFN package
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 8ns max at $V_{CC} = 5V$

2 Applications

- [Combine power good signals](#)
- [Combine enable signals](#)

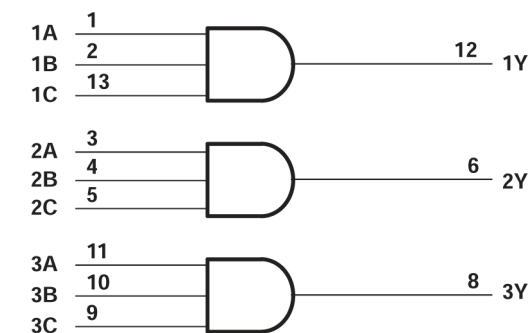
3 Description

The SN74ACT11-Q1 device contains three independent 3-input AND gates. These devices perform the Boolean function $Y = A \cdot B \cdot C$ in positive logic.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74ACT11-Q1	BQA (WQFN, 14)	3mm x 2.5mm	3mm x 2.5mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Gate (Positive Logic)



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4 Pin Configuration and Functions

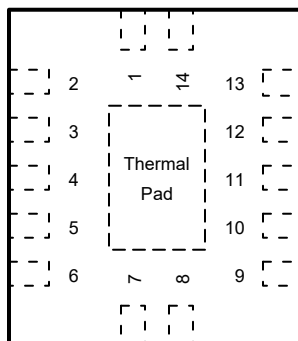


Figure 4-1. SN74ACT11-Q1 BQB Package (Transparent Top View)

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
2A	3	I	Channel 2, Input A
2B	4	I	Channel 2, Input B
2C	5	I	Channel 2, Input C
2Y	6	O	Channel 2, Output Y
GND	7	G	Ground
3Y	8	O	Channel 3, Output Y
3C	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
3A	11	I	Channel 3, Input C
1Y	12	O	Channel 1, Output Y
1C	13	I	Channel 1, Input C
V _{CC}	14	P	Positive Supply
Thermal pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) I = input, O = output, P = power, G = ground

(2) BQA Package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < -0.5V or V _I > V _{CC} + 0.5V		±20	mA
I _{OK}	Output clamp current	V _O < -0.5V or V _O > V _{CC} + 0.5V		±50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±50	mA
	Continuous output current through V _{CC} or GND			±200	mA
T _J	Operating junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	V
V _{IH}	High-level input voltage		2		V
V _{IL}	Low-Level input voltage			0.8	V
V _I	Input Voltage		0	V _{CC}	V
V _O	Output Voltage		0	V _{CC}	V
I _{OH}	High-level output current			-50	mA
I _{OL}	Low-level output current			50	mA
Δt/Δv	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
PW (TSSOP)	14	145.7	76.5	102.0	18.8	100.7	-	°C/W
BQA (WQFN)	14	91.3	99.4	61.0	14.5	60.8	37.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted); typical at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\mu\text{A}$	4.5V	4.4	4.499		V
		5.5V	5.4	5.499		
	$I_{OH} = -24\text{mA}$	4.5V	3.7	4.16		
	$I_{OH} = -24\text{mA}$	5.5V	4.7	5.18		
	$I_{OH} = -75\text{mA}^{(1)}$	5.5V	3.85			
V_{OL}	$I_{OH} = 50\mu\text{A}$	4.5V		0.001	0.1	V
		5.5V		0.001	0.1	
	$I_{OH} = 24\text{mA}$	4.5V		0.16	0.5	
	$I_{OH} = 24\text{mA}$	5.5V		0.14	0.5	
	$I_{OH} = 75\text{mA}^{(1)}$	5.5V			1.65	
I_I	$V_I = 5.5\text{V}$ or GND	0V to 5.5V		± 0.03	± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V		0.08	1	μA
ΔI_{CC}	$V_I = V_{CC} - 2.1\text{V}$; Any Input	4.5V to 5.5V			100	μA
C_I	$V_I = V_{CC}$ or GND	5V		2		pF
C_{PD}	$C_L = 50\text{pF}$, $F = 1\text{MHz}$	5V		20		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

5.6 Switching Characteristics

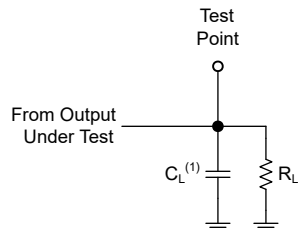
$C_L = 50\text{ pF}$; over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, or C	Y	$C_L = 50\text{pF}$	5V		5	8	ns
t_{PHL}	A, B, or C	Y	$C_L = 50\text{pF}$	5V		5.2	7.8	ns
t_r		Y	$C_L = 50\text{pF}$	5V		2.8	4.7	ns
t_f				5V		2.6	4.1	ns

6 Parameter Measurement Information

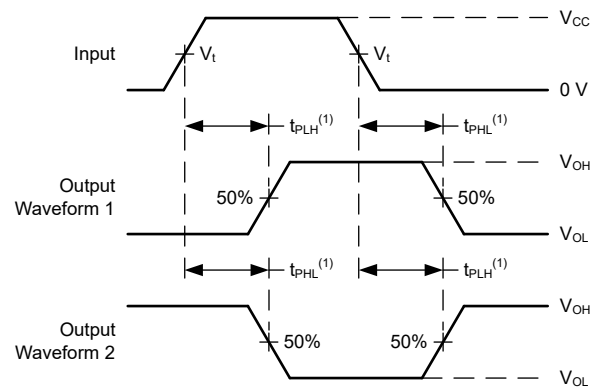
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f < 2.5\text{ns}$, $V_t = 1.5\text{V}$. For push-pull outputs, $R_L = 500\Omega$.

The outputs are measured individually with one input transition per measurement.



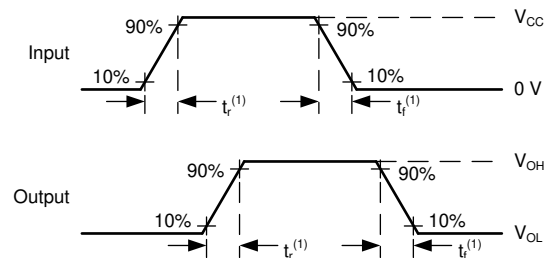
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

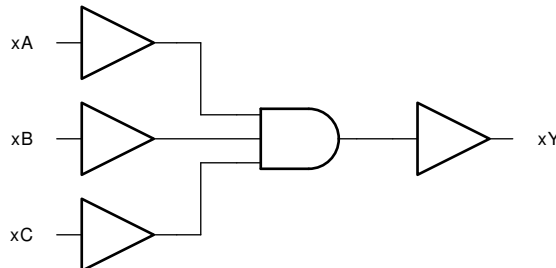
Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function $Y = A \bullet B \bullet C$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

7.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

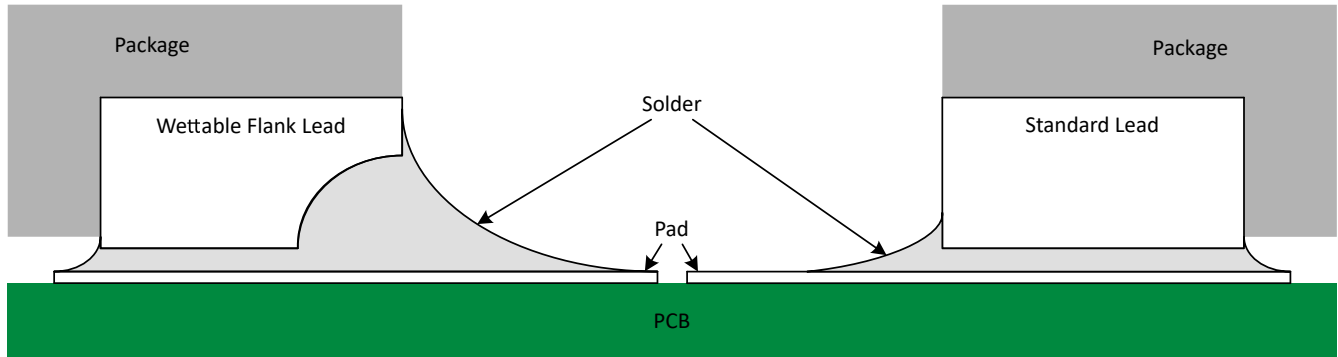


Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 7-1](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.4 Clamp Diode Structure

As shown in [Figure 7-2](#), the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

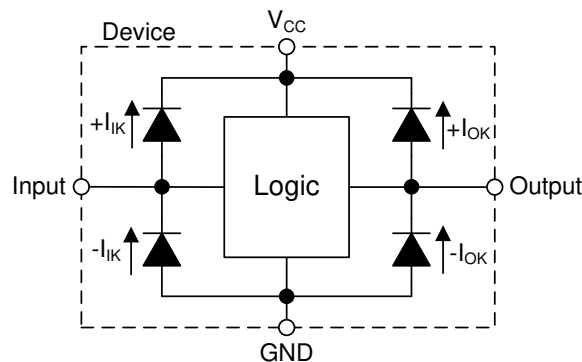


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table (Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

8.2 Typical Application

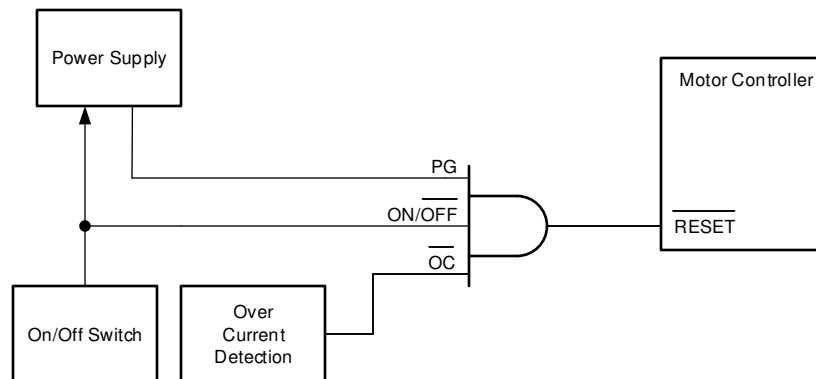


Figure 8-1. Typical application schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC11 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in .CMOS Power Consumption and Cpd Calculation

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SSL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC11, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HC11 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in *Layout*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC11 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

8.2.3 Application Curves

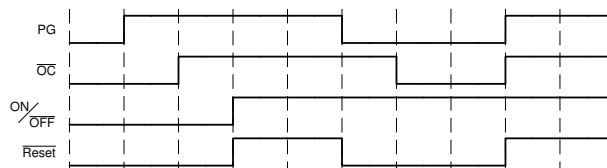


Figure 8-2. Typical application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1 μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer signals that must branch separately

8.4.2 Layout Example

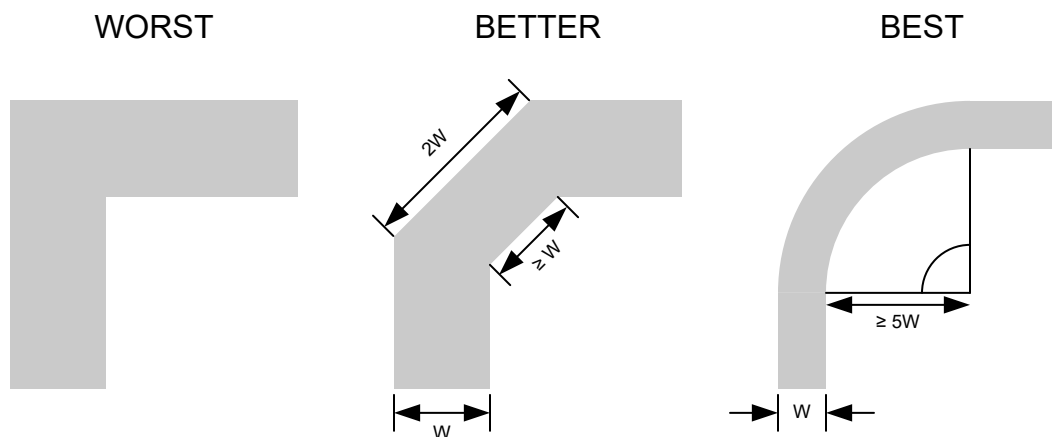


Figure 8-3. Example Trace Corners for Improved Signal Integrity

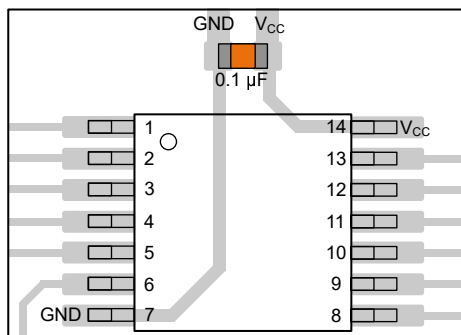


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

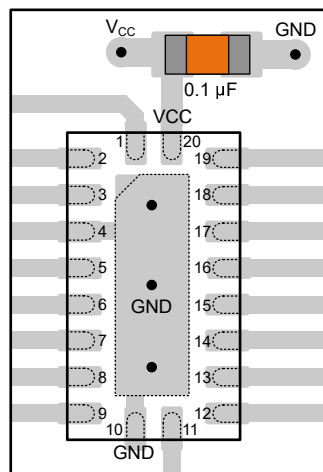


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

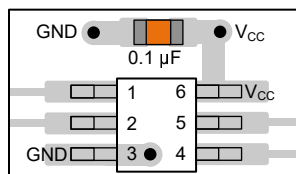


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

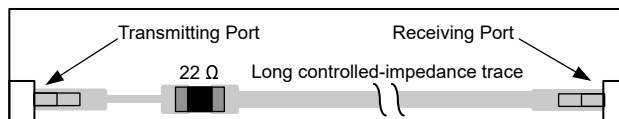


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74ACT11-Q1	Click here	Click here	Click here	Click here	Click here
SN74ACT11-Q1	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2025	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT11PWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT11Q
SN74ACT11PWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT11Q
SN74ACT11WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD11Q
SN74ACT11WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD11Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ACT11-Q1 :

- Catalog : [SN74ACT11](#)
- Military : [SN54ACT11](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

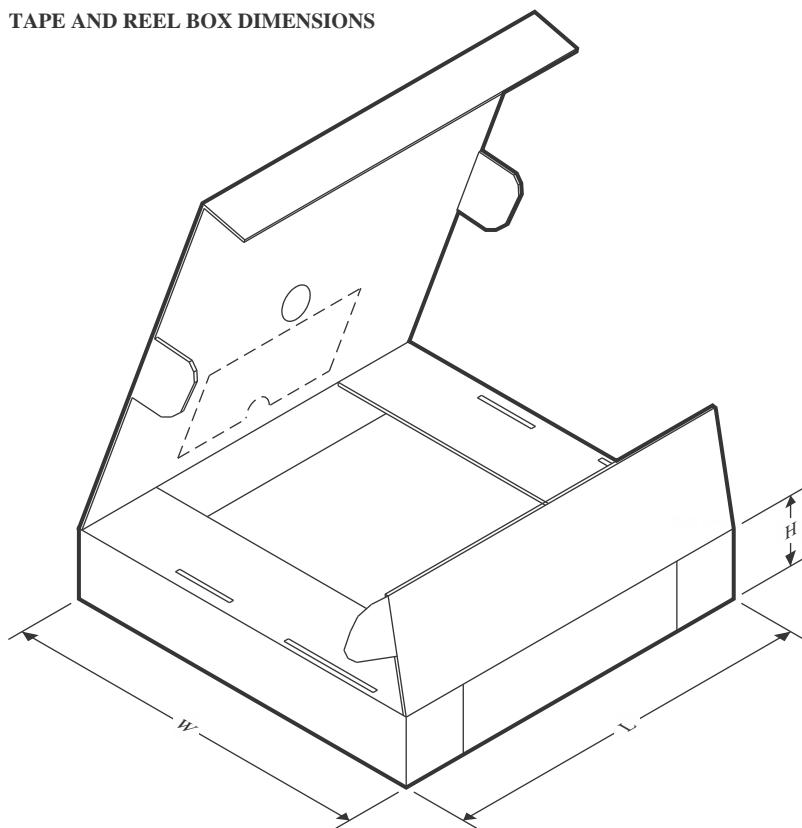
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT11PWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT11WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT11PWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74ACT11WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

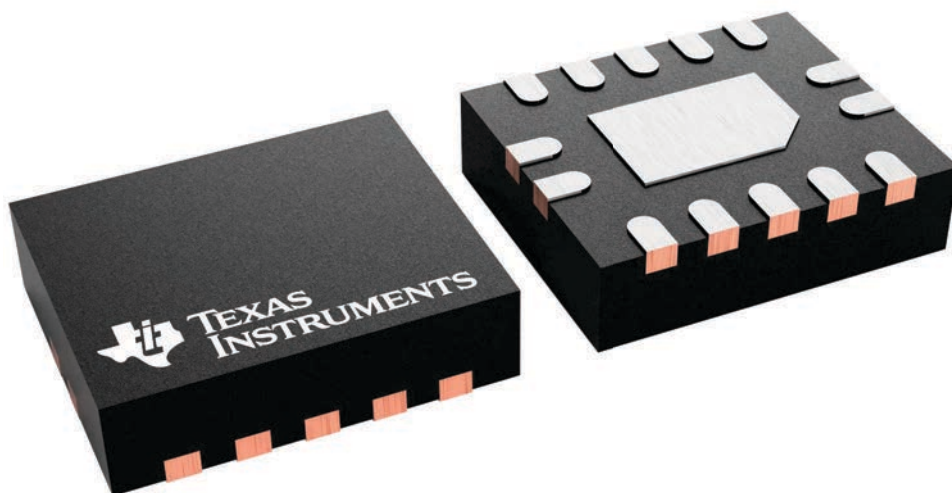
BQA 14

WQFN - 0.8 mm max height

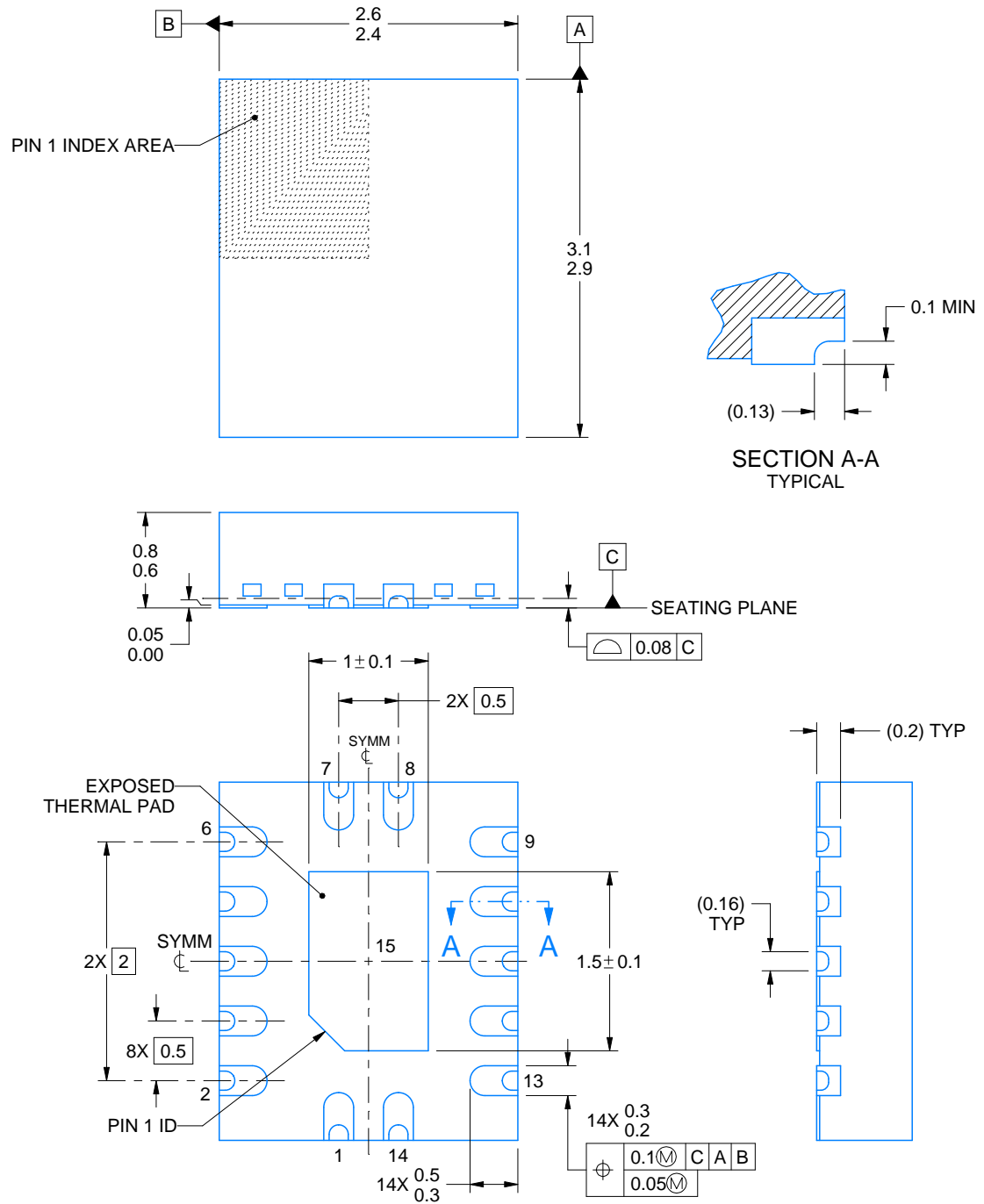
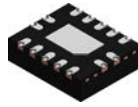
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



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NOTES:

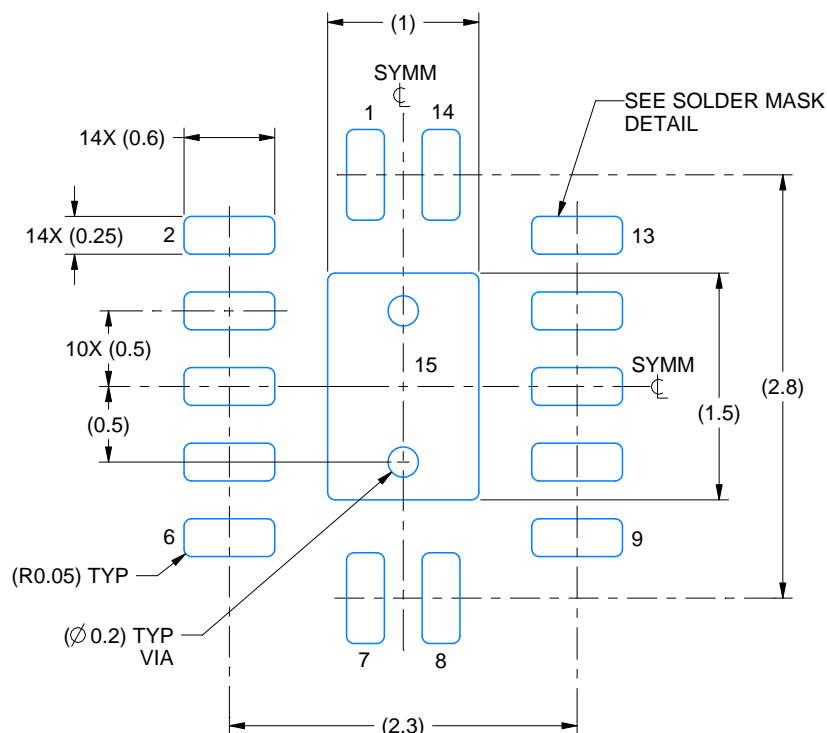
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

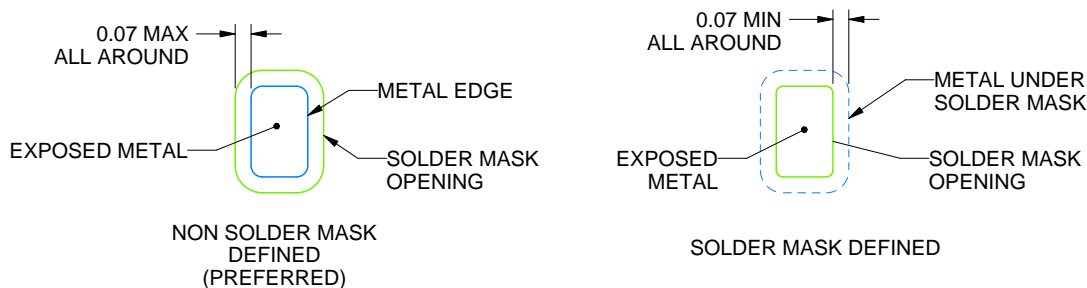
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

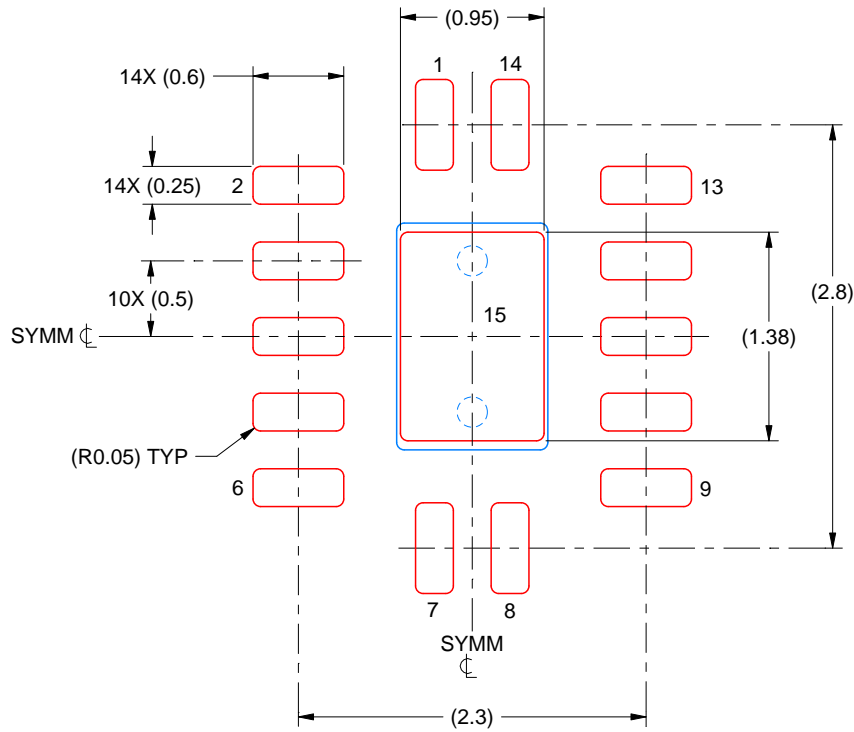
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

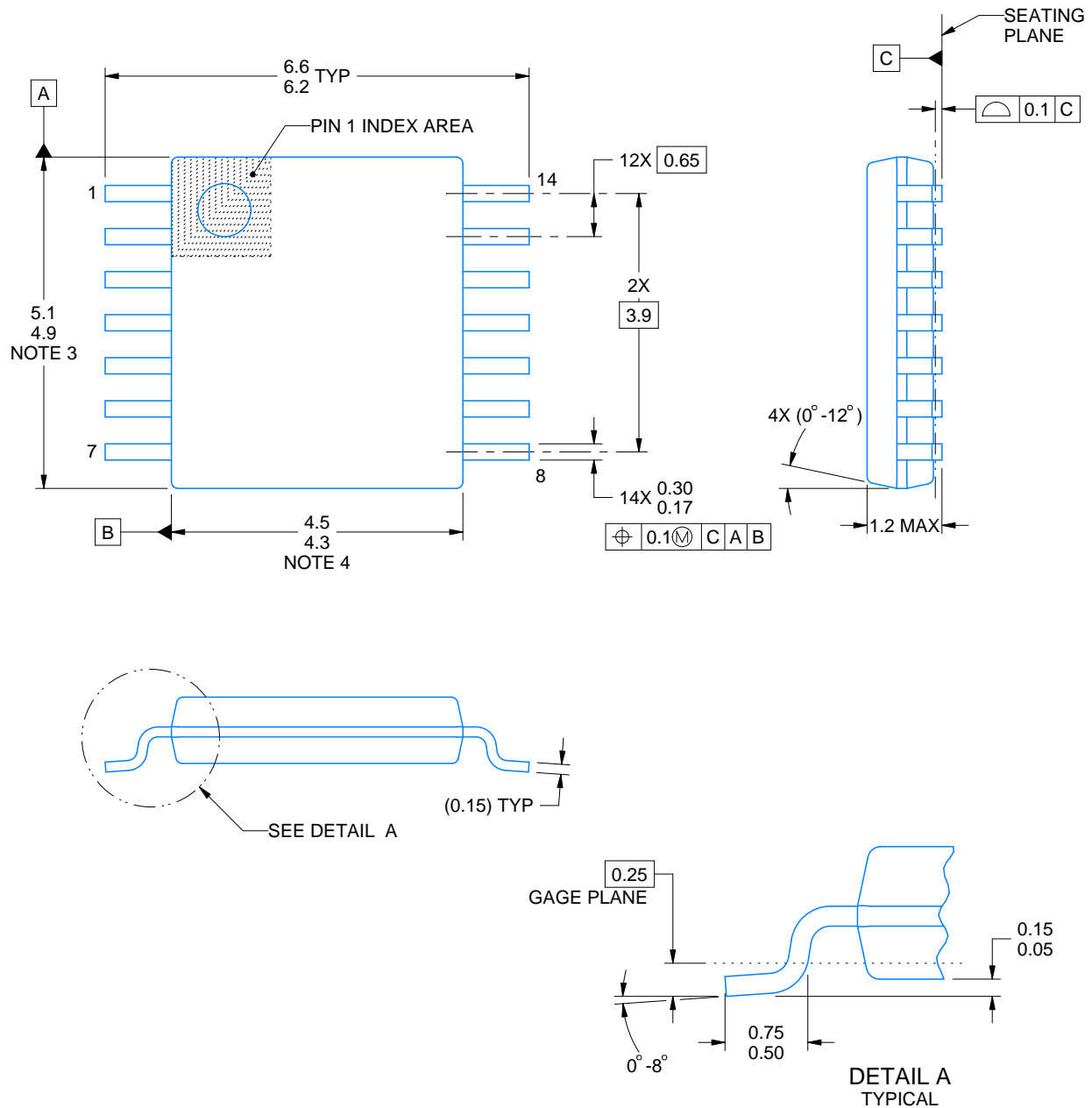
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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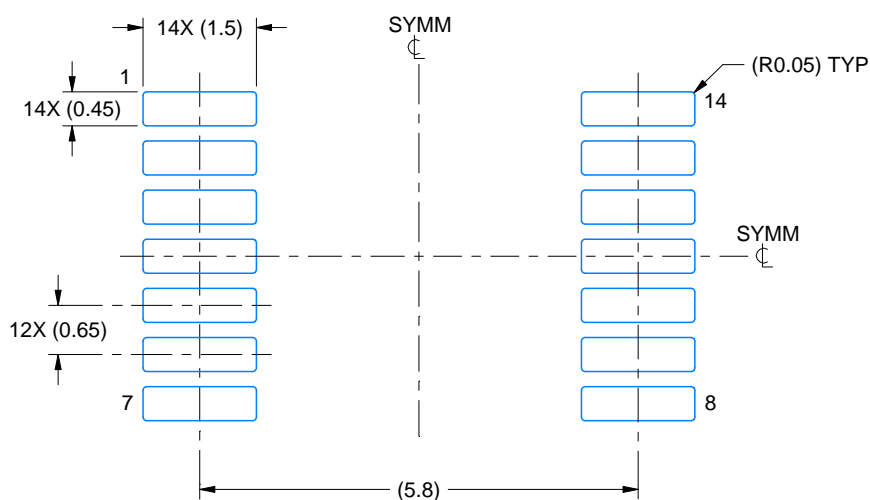
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

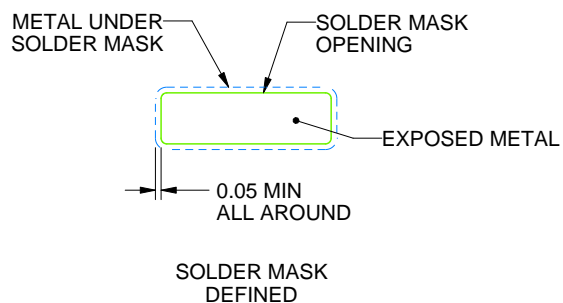
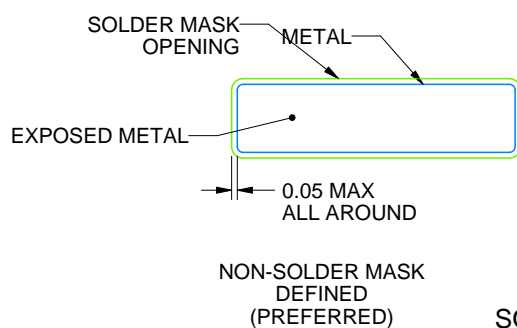
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

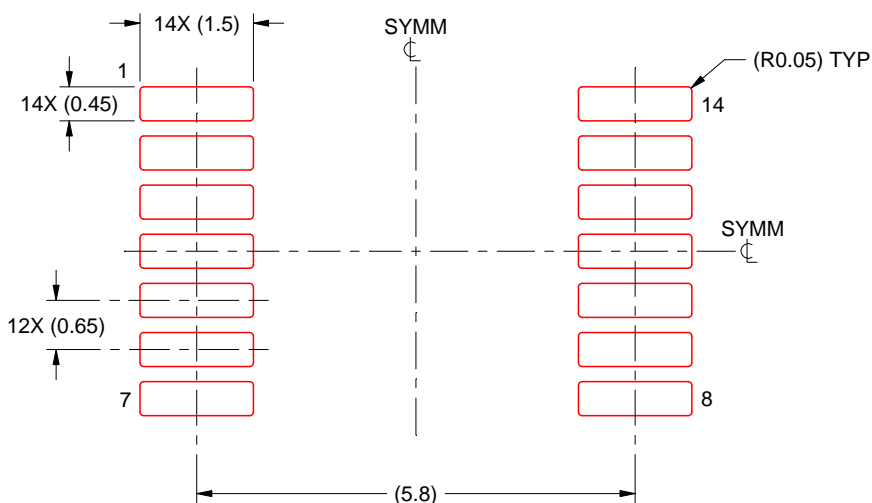
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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