TEXAS INSTRUMENTS

SN74AC8541
SCAS962B – NOVEMBER 2023 – REVISED SEPTEMBER 2024

SN74AC8541 Octal Buffers or Drivers With 3-State Outputs

1 Features

- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 6ns at 5V, 50pF load

2 Applications

- Enable or disable a digital signal
- Eliminate slow or noisy input signals
- Hold a signal during controller reset
- Debounce a switch

3 Description

The SN74AC8541 contains eight independent logic buffers with Schmitt-trigger inputs. The outputs can simultaneously be put into the high-impedance state using either of the provided output enable pins ($\overline{OE1}$ or $\overline{OE2}$).
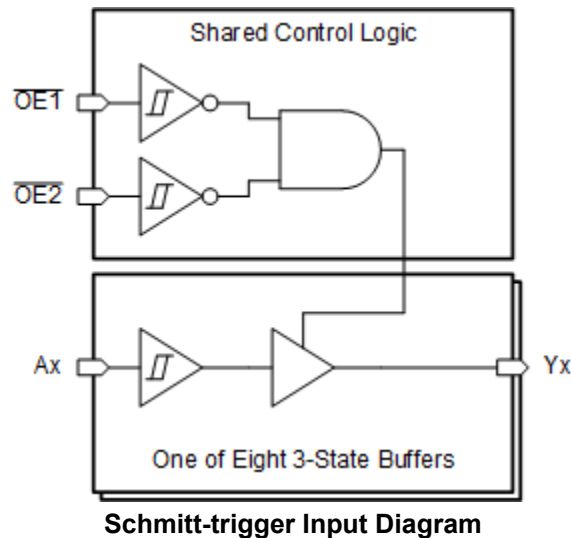
Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE[3]
SN74AC8541	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	RKS (VQFN, 20)	4.5 mm × 2.5 mm	4.5 mm × 2.5 mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.
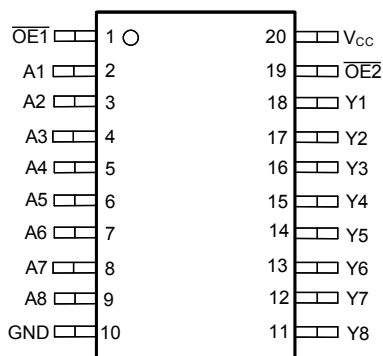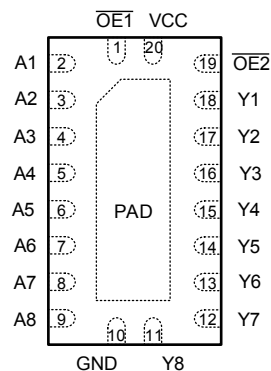

Schmitt-trigger Input Diagram

Table of Contents

4 Pin Configuration and Functions

**Figure 4-1. DGS or PW Package,
20-Pin SOT or TSSOP
(Top View)**

**Figure 4-2. RKS Package,
20-Pin VQFN
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE1}$	1	I	Output enable input 1, active low
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
Y8	11	O	Output for channel 8
Y7	12	O	Output for channel 7
Y6	13	O	Output for channel 6
Y5	14	O	Output for channel 5
Y4	15	O	Output for channel 4
Y3	16	O	Output for channel 3
Y2	17	O	Output for channel 2
Y1	18	O	Output for channel 1
$\overline{OE2}$	19	I	Output enable input 2, active low
V_{CC}	20	P	Positive supply
Thermal Pad[2]	—	—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1)   I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2)   RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range[2]		-0.5	V_{CC} + 0.5 V	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5 V	V
I_{IK}	Input clamp current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature		-65	150	°C

(1)   Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2)   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.5	6	V
V_I [1]	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		-1	mA
		V_{CC} = 2.5 V		-2	
		V_{CC} = 3.3 V		-12	
		V_{CC} = 5 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		1	mA
		V_{CC} = 2.5 V		2	
		V_{CC} = 3.3 V		12	
		V_{CC} = 5 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	1.5 V ≤ V_{CC} ≤ 5.5 V		Unlimited	
		3 V < V_{CC} ≤ 5.5 V		Unlimited	
T_A	Operating free-air temperature		-40	125	°C

(1)   All unused inputs of the device must be held at VCC or GND for proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AC8541			UNIT
		DGS (VSSOP)	PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.5	126.2	72.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.1	68.7	77.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	77.3	45.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	22.3	13.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78	76.9	45.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	29.4	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted); typical values measured at T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	1.5 V	0.61	0.89	1.17	V
		1.8 V	0.72	1.03	1.33	
		2.5 V	0.8	1.29	1.61	
		3 V	0.8	1.8	2.2	
		4.5 V	1.5	2.6	3.2	
		5 V	2.6	2.9	3.4	
		5.5 V	1.6	3.2	3.9	
V_{T-}	Negative-going input threshold voltage	1.5 V	0.26	0.48	0.7	V
		1.8 V	0.37	0.54	0.70	
		2.5 V	0.5	0.7	0.84	
		3 V	0.5	0.8	1.2	
		4.5 V	0.9	1.4	1.8	
		5 V	1.6	1.6	2.4	
		5.5 V	1.1	1.8	2.3	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.5 V	0.22	0.41	0.6	V
		1.8 V	0.28	0.49	0.69	
		2.5 V	0.3	0.60	0.83	
		3 V	0.3	1	1.2	
		4.5 V	0.4	1.2	1.4	
		5 V	0.5	1.3	1.5	
		5.5 V	0.5	1.4	1.6	

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted); typical values measured at T_A = 25°C

PARAMETER	TEST CONDITIONS	V$_{CC}$	MIN	TYP	MAX	UNIT
V$_{OH}$	I$_{OH}$ = -50µA	1.5 V	1.4	1.49		V
		1.8 V	1.7	1.79		
		2.5 V	2.4	2.49		
		3 V	2.9	2.99		
		4.5 V	4.4	4.49		
		5.5 V	5.4	5.49		
	I$_{OH}$ = -1mA	1.8 V	1.44			
	I$_{OH}$ = -2mA	2.5 V	2			
	I$_{OH}$ = -4mA	3 V	2.4			
	I$_{OH}$ = -12mA	3 V	2.4			
	I$_{OH}$ = -24mA	4.5 V	3.7			
	I$_{OH}$ = -24mA	5.5 V	4.7			
	I$_{OH}$ = -75mA	5.5 V				
	I$_{OH}$ = -50mA	5.5 V	3.85			
V$_{OL}$	I$_{OL}$ = 50µA	1.5 V		0.01	0.1	V
		1.8 V		0.01	0.1	
		2.5 V		0.01	0.1	
		3 V		0.01	0.1	
		4.5 V		0.01	0.1	
		5.5 V		0.01	0.1	
	I$_{OL}$ = 1mA	1.8 V			0.36	
	I$_{OL}$ = 2mA	2.5 V			0.5	
	I$_{OL}$ = 4mA	3 V			0.5	
	I$_{OL}$ = 12mA	3 V			0.5	
	I$_{OL}$ = 24mA	4.5 V			0.5	
	I$_{OL}$ = 24mA	5.5 V			0.5	
	I$_{OL}$ = 50mA	5.5 V			1.65	
	I$_{OL}$ = 75mA	5.5 V			1.65	
I$_I$	V$_I$ = 5.5 V or GND	0 V to 5.5 V			±1	µA
I$_{OZ}$	V$_O$ = V$_{CC}$ or GND	5.5 V			±5	µA
I$_{CC}$	V$_I$ = V$_{CC}$ or GND, I$_O$ = 0	5.5 V			20	µA
C$_I$	V$_I$ = V$_{CC}$ or GND	5 V		9		pF
C$_O$	V$_O$ = V$_{CC}$ or GND	5 V		15		pF
C$_{PD}$ [1] [2]	F = 1MHz	5 V		60		pF

(1) C$_{PD}$ is used to determine the dynamic power consumption, per channel

(2) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where F$_I$= input frequency, C$_L$= output load capacitance, V$_{CC}$= supply voltage

5.6 Switching Characteristics

C$_L$ = 50pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t$_{PLH}$	A	Y	1.5 V		14.5	25.6			26.5			26.8	ns
t$_{PHL}$	A	Y	1.5 V		14.8	27.5			28.4			28.8	ns
t$_{PZH}$	$\overline{OE}$	Y	1.5 V		17.6	35			36.8			37.7	ns

5.6 Switching Characteristics (continued)

C_L = 50pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZL}	$\overline{OE}$	Y	1.5 V	19.2	36.3				37.7			38.1	ns
t_{PHZ}	$\overline{OE}$	Y	1.5 V	22.3	32.7				33.8			34.3	ns
t_{PLZ}	$\overline{OE}$	Y	1.5 V	14	21.8				22.3			22.3	ns
t_{PLH}	A	Y	1.8 V	10.1	16.4				17.7			18.5	ns
t_{PHL}	A	Y	1.8 V	10.9	18.6				19.8			20.6	ns
t_{PZH}	$\overline{OE}$	Y	1.8 V	12.8	22.7				24.7			25.9	ns
t_{PZL}	$\overline{OE}$	Y	1.8 V	14.1	24.2				26			26.9	ns
t_{PHZ}	$\overline{OE}$	Y	1.8 V	17.7	23.3				25.8			25.8	ns
t_{PLZ}	$\overline{OE}$	Y	1.8 V	10.6	15.3				15.9			16	ns
t_{PLH}	A	Y	2.5 V	6.4	9.5				10.6			11.3	ns
t_{PHL}	A	Y	2.5 V	7.1	11.4				12.4			13.1	ns
t_{PZH}	$\overline{OE}$	Y	2.5 V	8.3	13.5				15.1			16.2	ns
t_{PZL}	$\overline{OE}$	Y	2.5 V	9.3	15.1				16.7			17.4	ns
t_{PHZ}	$\overline{OE}$	Y	2.5 V	7.6	10.5				11.4			11.9	ns
t_{PLZ}	$\overline{OE}$	Y	2.5 V	5.4	7.9				8.7			8.9	ns
t_{PLH}	A	Y	3.3 V	5.3	7.6				8.6			9.2	ns
t_{PHL}	A	Y	3.3 V	5.9	9.4				10.2			10.8	ns
t_{PZH}	$\overline{OE}$	Y	3.3 V	7.2	11.2				12.4			13.2	ns
t_{PZL}	$\overline{OE}$	Y	3.3 V	7.7	12.5				13.6			14.5	ns
t_{PHZ}	$\overline{OE}$	Y	3.3 V	6.3	8.4				9.3			10	ns
t_{PLZ}	$\overline{OE}$	Y	3.3 V	4.7	6.6				7.1			7.7	ns
t_{PLH}	A	Y	5 V	3.9	5.3				6			6.4	ns
t_{PHL}	A	Y	5 V	4.5	7				7.6			8	ns
t_{PZH}	$\overline{OE}$	Y	5 V	5.6	8.3				9.2			9.8	ns
t_{PZL}	$\overline{OE}$	Y	5 V	5.8	8.8				9.6			10.2	ns
t_{PHZ}	$\overline{OE}$	Y	5 V	5	6.3				6.8			6.8	ns
t_{PLZ}	$\overline{OE}$	Y	5 V	3.5	4.5				4.9			5.2	ns

5.7 Typical Characteristics
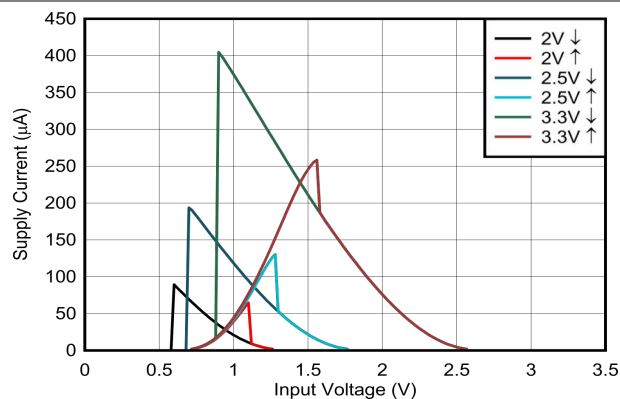
$T_A = 25°C$ (unless otherwise noted)

Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply
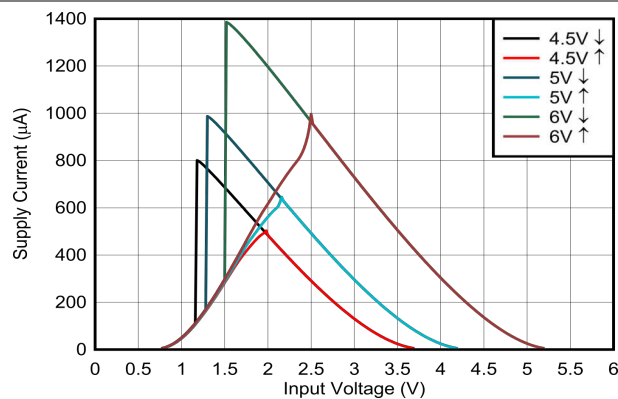
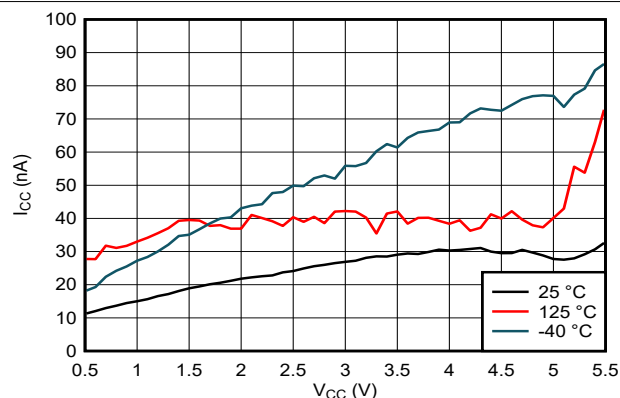**Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply**

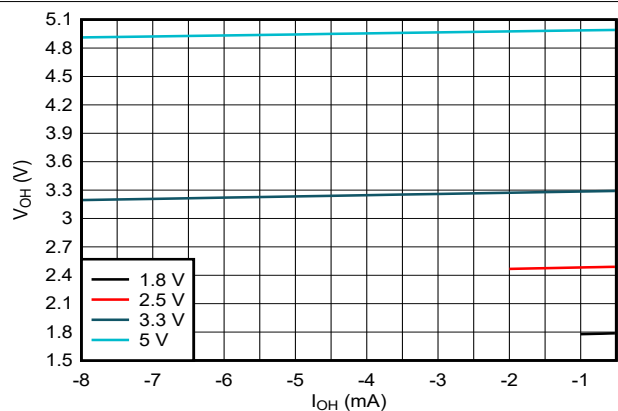**Figure 5-3. Supply Current Across Supply Voltage**
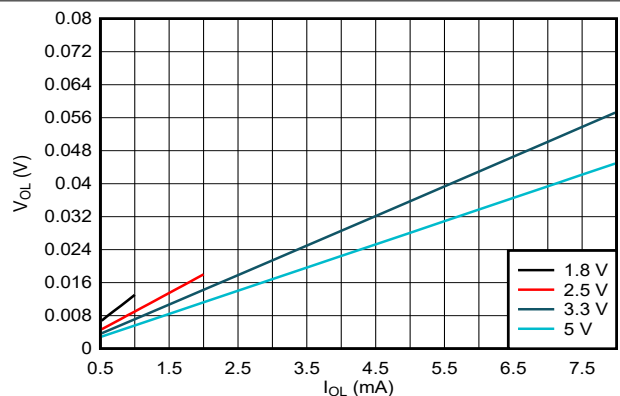
Figure 5-4. Output Voltage vs Current in HIGH State
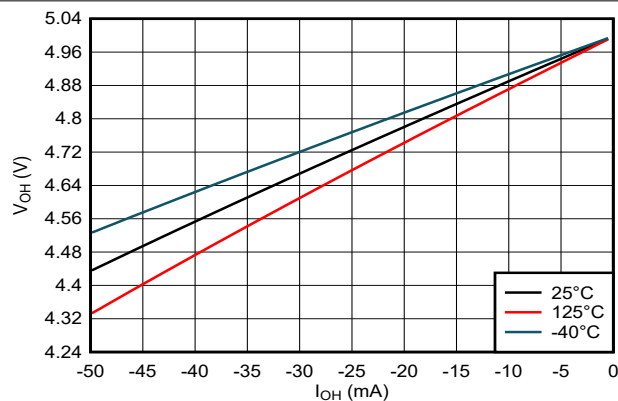
Figure 5-5. Output Voltage vs Current in LOW State

Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

Product Folder Links: *SN74AC8541*

5.7 Typical Characteristics (continued)

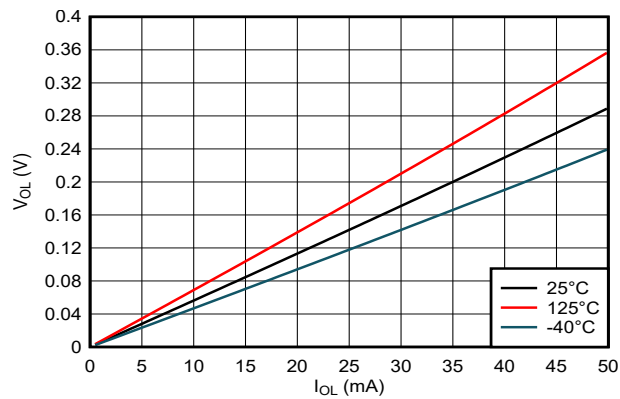T_A = 25°C (unless otherwise noted)

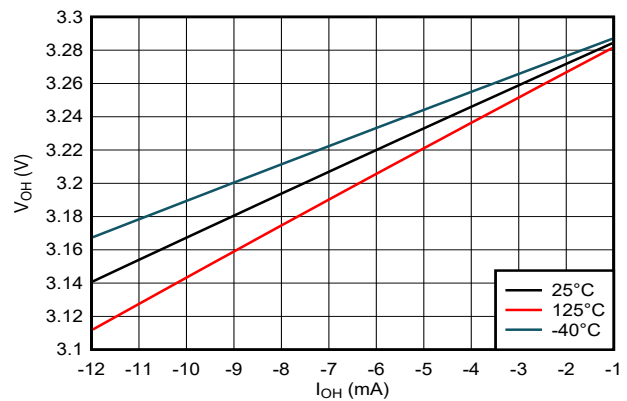Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

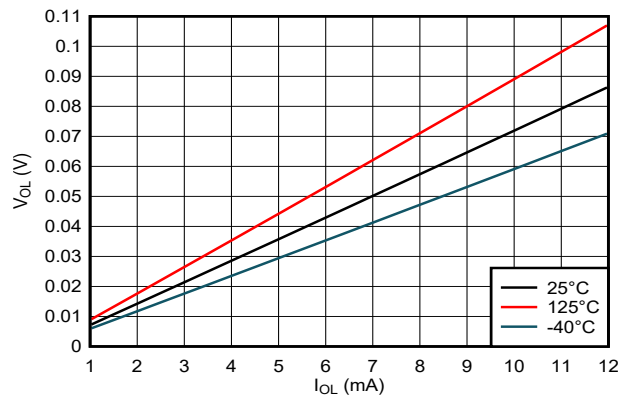Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply
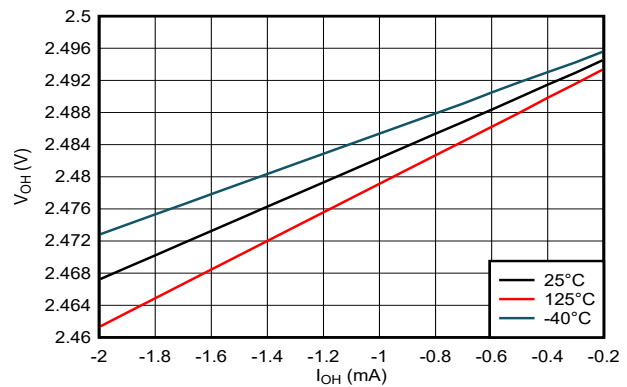

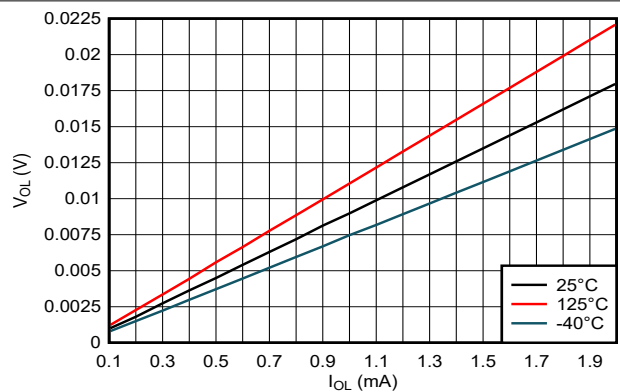Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

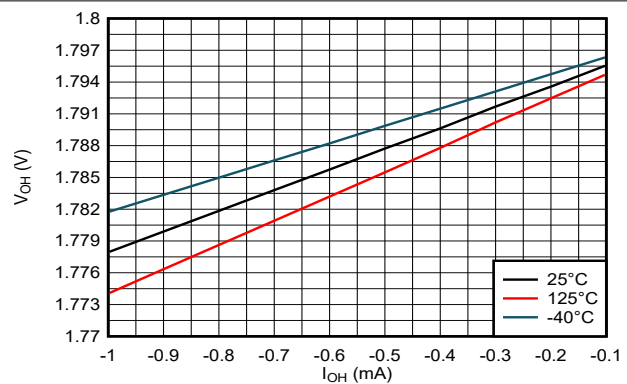Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

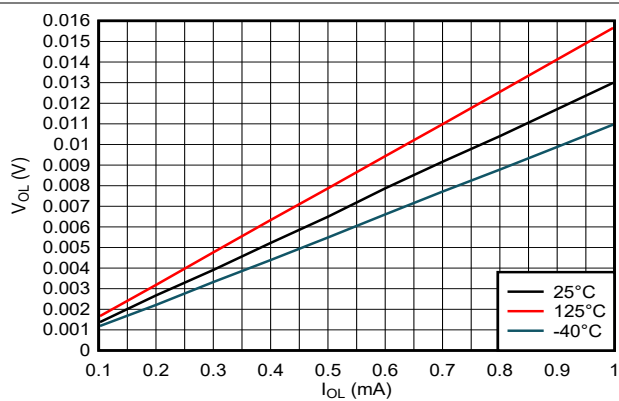**Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

Product Folder Links: *SN74AC8541*

6 Detailed Description

6.1 Overview

The SN74AC8541 contains eight buffers with 3-state outputs and Schmitt-trigger inputs. The active low output enable pins ($\overline{OE1}$ and $\overline{OE2}$) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.
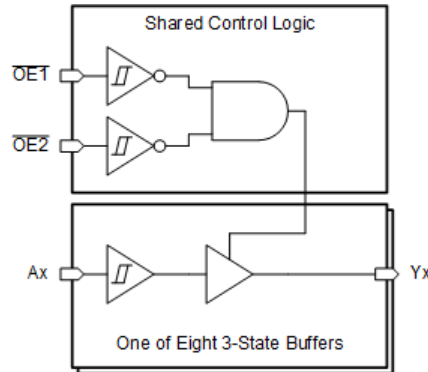
6.2 Functional Block Diagram

Figure 6-1. Schmitt-trigger Input Diagram

6.3 Device Functional Modes

Table 6-1. Function Table

INPUTS[1]			OUTPUT[2]
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

(1) L = input low, H = input high, X = don't care
(2) L = output low, H = output high, Z = high impedance

6.4 Feature Description

6.4.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state.

The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

6.4.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

6.4.3 Clamp Diode Structure

As shown in Figure 6-2, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
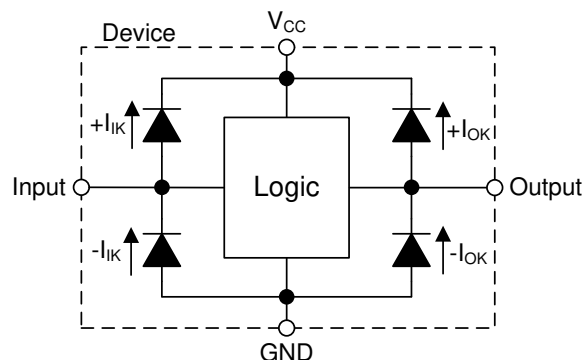
Figure 6-2. Electrical Placement of Clamping Diodes for Each Input and Output

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SN74AC8541 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

7.2 Typical Application

Figure 7-1. Typical Application Block Diagram

7.3 Design Requirements

7.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.
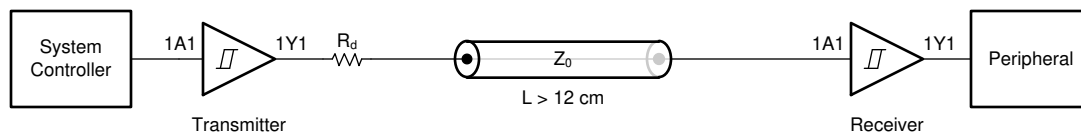
The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC8541 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC8541 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC8541 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC8541 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> **CAUTION**
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

7.3.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC8541 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AC8541 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

7.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

Submit Document Feedback   15

Product Folder Links: *SN74AC8541*

7.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC8541 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

7.5 Application Curves
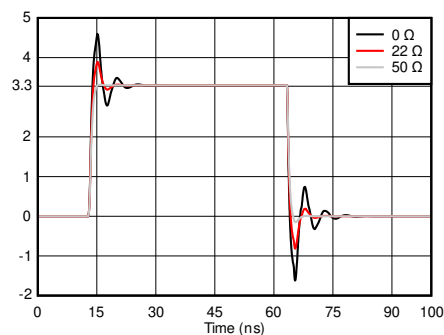
Figure 7-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

7.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.7 Layout

7.7.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

Product Folder Links: *SN74AC8541*

7.7.2 Layout Example

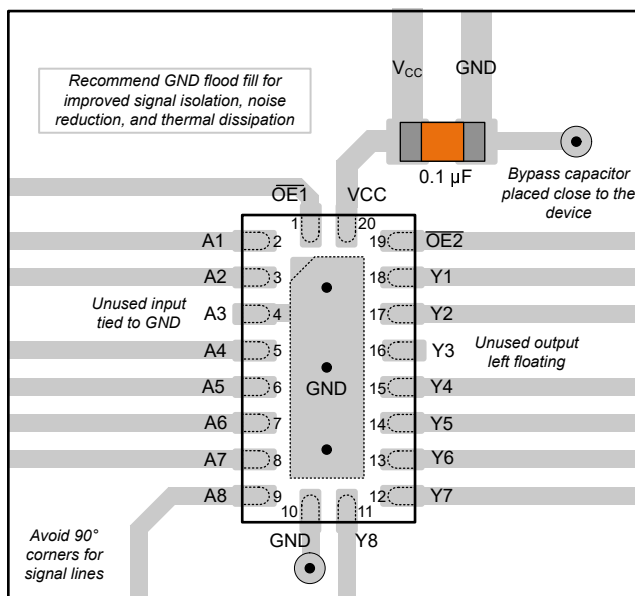**Figure 7-3. Example Layout for the SN74AC8541 in the RKS Package**

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision A (March 2024) to Revision B (September 2024)	**Page**
• Updated input transition rise or fall rate in *Recommended Operating Conditions* table and diagram in *Description* and *Functional Block Diagram* sections.. 1	

Changes from Revision * (November 2023) to Revision A (March 2024)	**Page**
• Added DGS and PW packages to *Device Information* table, *Pin Configuration and Functions* section and *Thermal Information* table...1	

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC8541DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8541
SN74AC8541DGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8541
SN74AC8541PWR	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC8541
SN74AC8541PWR.A	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC8541
SN74AC8541RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC8541
SN74AC8541RKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC8541

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC8541 :

• Automotive : SN74AC8541-Q1

NOTE: Qualified Version Definitions:

  • Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC8541DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AC8541PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC8541RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC8541DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AC8541PWR	TSSOP	PW	20	3000	353.0	353.0	32.0
SN74AC8541RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

6.6
6.4
NOTE 3

2X

5.85

10

11

20X 0.30
0.19

B

4.5
4.3
NOTE 4

⊕ 0.1Ⓜ C A B

C SEATING PLANE

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0.75
0.50

0°-8°

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PIN 1 INDEX AREA

A

5.1
4.7 TYP

1

20

18X 0.5

5.2
5.0
NOTE 3

2X 4.5

10

11

B

3.1
2.9

20X 0.275
0.165

⊕ 0.1 Ⓜ C A B

C

⌓ 0.1 C

SEATING PLANE

4X (0°-15°)

SEE DETAIL A

4X (7°-15°)

(0.15) TYP

0.25
GAGE PLANE

0°-8°

0.7
0.4

1.1 MAX

0.15
0.05

DETAIL A
TYPICAL

4226367/A   10/2020

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

20X (1.45)

SYMM

1

20

20X (0.3)

(R0.05) TYP

18X (0.5)

SYMM

10

11

(4.4)

LAND PATTERN EXAMPLE
SCALE: 16X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

EXPOSED METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

EXPOSED METAL

SOLDER MASK DETAILS

4226367/A   10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

20X (1.45)

20X (0.3)

1

(R0.05) TYP

(18X 0.5)

10

SYMM

20

SYMM

11

(4.4)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A   10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RKS 20

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4226872/A

A

2.6
2.4

B

PIN 1 INDEX AREA

4.6
4.4

// 0.1 C

1.0
0.8

C

SEATING PLANE

0.05
0.00

◁ 0.08 C

1±0.1

2X 0.5

14X 0.5

10   11

9   12   EXPOSED
THERMAL PAD

2X
3.5

3±0.1

(0.2) TYP

2   19

PIN 1 ID
(OPTIONAL)

1   20

20X 0.30
0.18

20X 0.5
0.3

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ

4222490/B 02/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
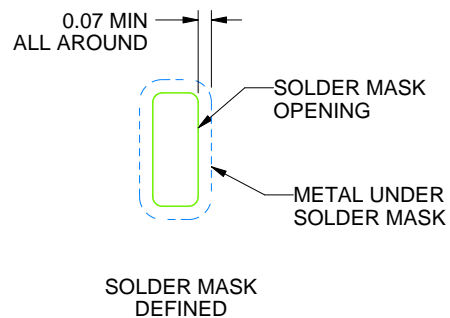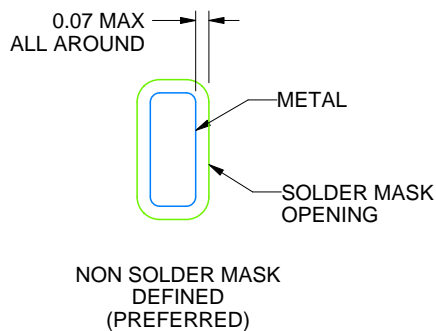
RKS0020A

(1)

SYMM

1   20

20X (0.6)

2

20X (0.24)

19

(1.25)

SYMM

(3)

(4.3)

16X (0.5)

(R0.05) TYP

9

12

(⌀ 0.2) VIA
TYP

10   11

(2.3)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
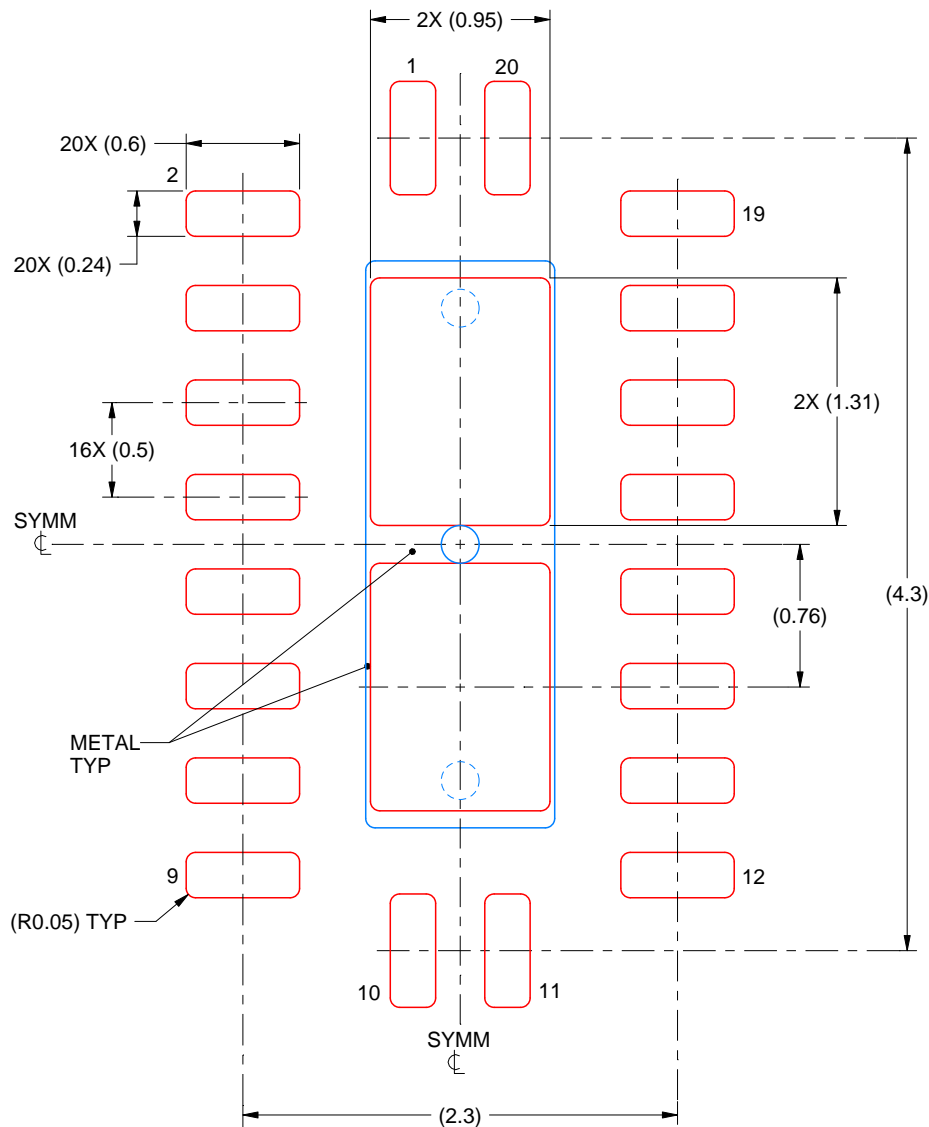
4222490/B   02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

2X (0.95)

1

20

20X (0.6)

2

20X (0.24)

19

16X (0.5)

SYMM
℄

2X (1.31)

(4.3)

(0.76)

METAL
TYP

9

(R0.05) TYP

12

10

11

SYMM
℄

(2.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B   02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
    design recommendations.

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