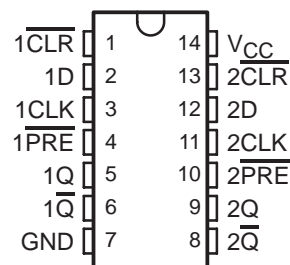


SN74AC74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 10 ns at 5 V**

**D PACKAGE
(TOP VIEW)**



† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74AC74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

T _A	PACKAGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D Tape and reel	SN74AC74MDREP	SAC74MEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H§	H§
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\overline{Q}_0

§ This configuration is nonstable; that is, it does not persist when either \overline{PRE} or \overline{CLR} returns to its inactive (high) level.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



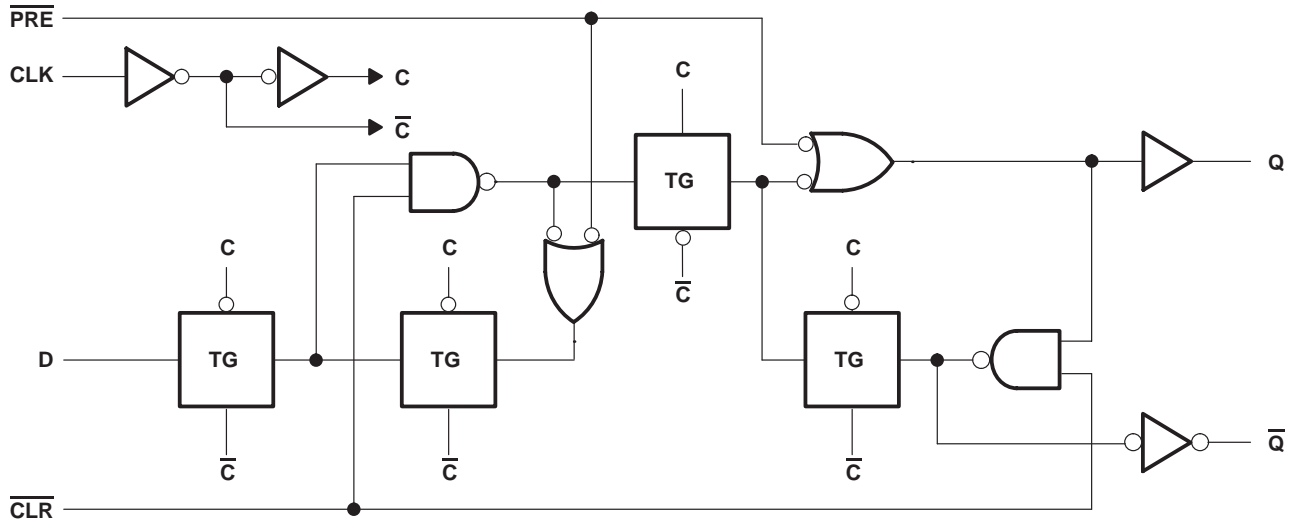
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SN74AC74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Package thermal impedance, θ_{JA} (see Note 2)	86°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1	V
		V _{CC} = 4.5 V	3.15	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9	V
		V _{CC} = 4.5 V	1.35	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V	-12	mA
		V _{CC} = 4.5 V	-24	
		V _{CC} = 5.5 V	-24	
I _{OL}	Low-level output current	V _{CC} = 3 V	12	mA
		V _{CC} = 4.5 V	24	
		V _{CC} = 5.5 V	24	
Δt/Δv	Input transition rise or fall rate		8	ns/V
T _A	Operating free-air temperature	-55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	3 V	2.9	4.49	2.9	V		
		4.5 V	4.4	5.49	4.4			
		5.5 V	5.4	5.49	5.4			
	I _{OH} = -12 mA	3 V	2.56		2.4			
		4.5 V	3.86		3.7			
		5.5 V	4.86		4.7			
V _{OL}	I _{OL} = 50 μA	3 V	0.002	0.1	0.1	V		
		4.5 V	0.001	0.1	0.1			
		5.5 V	0.001	0.1	0.1			
	I _{OL} = 12 mA	3 V		0.36	0.5			
		4.5 V		0.36	0.5			
		5.5 V		0.36	0.5			
I _I	Data pins	V _I = V _{CC} or GND	5.5 V		±0.1	±1	μA	
	Control pins				±0.1	±1		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		2	40	μA		
C _i	V _I = V _{CC} or GND	5 V		3		pF		

SN74AC74-EP

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	100		70		MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5.5	8		ns
		CLK	5.5	8		
t_{su}	Setup time, data before $\text{CLK}\uparrow$	Data	4	5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0	0.5		
t_h	Hold time, data after $\text{CLK}\uparrow$	0.5	0.5			ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	140		95		MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4.5	5.5		ns
		CLK	4.5	5.5		
t_{su}	Setup time, data before $\text{CLK}\uparrow$	Data	3	4		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0	0.5		
t_h	Hold time, data after $\text{CLK}\uparrow$	0.5	0.5			ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
			MIN	TYP	MAX				
f_{max}			100	125		70		MHz	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	3.5	8	12	1	13		ns
t_{PHL}			4	10.5	12	1	14		
t_{PLH}	CLK	Q or \overline{Q}	4.5	8	13.5	1	17.5		ns
t_{PHL}			3.5	8	14	1	13.5		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

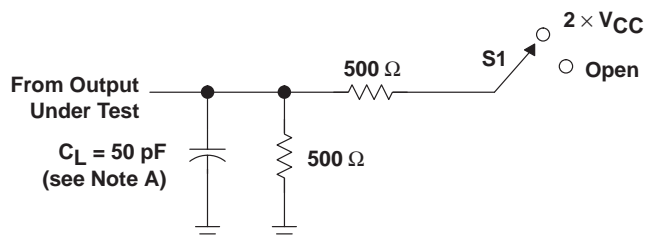
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
			MIN	TYP	MAX				
f_{max}			140	160		95		MHz	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	2.5	6	9	1	9.5		ns
t_{PHL}			3	8	9.5	1	10.5		
t_{PLH}	CLK	Q or \overline{Q}	3.5	6	10	1	12		ns
t_{PHL}			2.5	6	10	1	10		

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF

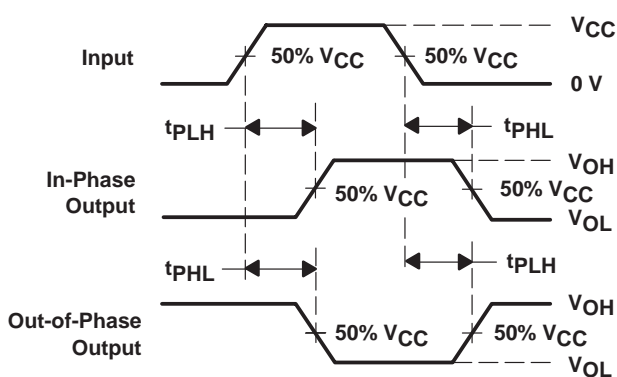


PARAMETER MEASUREMENT INFORMATION

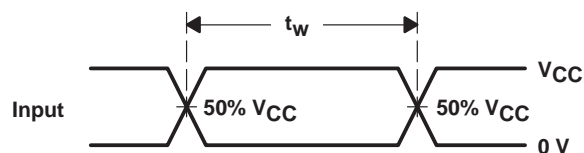


LOAD CIRCUIT

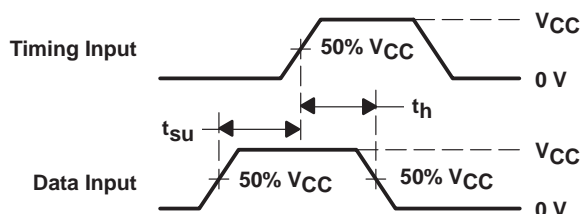
TEST	S1
t_{PLH}/t_{PHL}	Open



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC74MDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAC74MEP
SN74AC74MDREP.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAC74MEP
V62/04617-01XE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAC74MEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AC74-EP :

- Catalog : [SN74AC74](#)

- Automotive : [SN74AC74-Q1](#)

- Military : [SN54AC74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC74MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC74MDREP	SOIC	D	14	2500	353.0	353.0	32.0

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Last updated 10/2025