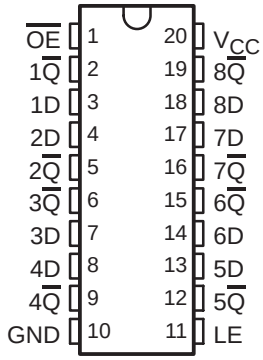
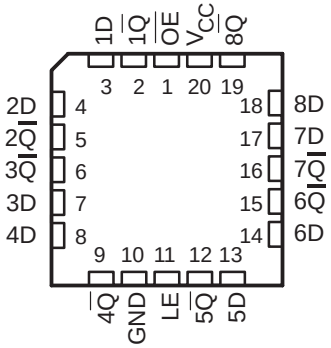
- **2-V to 6-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 6 V**
- **Max $t_{pd}$ of 10.5 ns at 5 V**
- **3-State Inverting Outputs Drive Bus Lines Directly**
- **Full Parallel Access for Loading**

**SN54AC533 . . . J OR W PACKAGE**
**SN74AC533 . . . DB, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AC533 . . . FK PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’AC533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

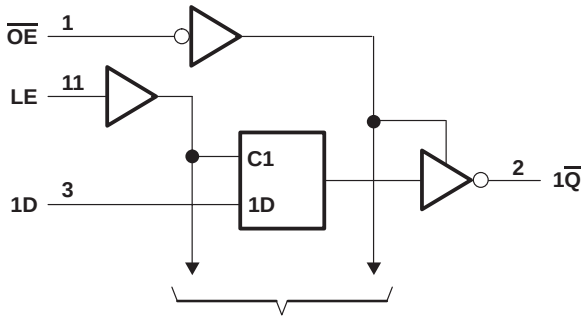
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | PDIP − N | Tube | SN74AC533N | SN74AC533N |
| | SOIC − DW | Tube | SN74AC533DW | AC533 |
| | | Tape and reel | SN74AC533DWR | |
| | SOP − NS | Tape and reel | SN74AC533NSR | AC533 |
| | SSOP − DB | Tape and reel | SN74AC533DBR | AC533 |
| | TSSOP − PW | Tube | SN74AC533PW | AC533 |
| | | Tape and reel | SN74AC533PWR | |
| −55°C to 125°C | CDIP − J | Tube | SNJ54AC533J | SNJ54AC533J |
| | CFP − W | Tube | SNJ54AC533W | SNJ54AC533W |
| | LCCC − FK | Tube | SNJ54AC533FK | SNJ54AC533FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

## logic diagram (positive logic)




**To Seven Other Channels**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 6 | 2 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | 3.15 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | 1.35 | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | −12 | | −12 | mA |
| | | $V_{CC}$ = 4.5 V | | −24 | | −24 | |
| | | $V_{CC}$ = 5.5 V | | −24 | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | 12 | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | 24 | | 24 | |
| | | $V_{CC}$ = 5.5 V | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 8 | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = −12 mA | 3 V | 2.56 | | | 2.4 | | 2.46 | | |
| | $I_{OH}$ = −24 mA | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 3 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±5 | | ±2.5 | μA |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 80 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 6 | | 8 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 5.5 | | 7.5 | | 6 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 2.5 | | 1 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 4.5 | | 6.5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 6 | | 4.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 2.5 | | 1 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | $\overline{Q}$ | 2 | 14 | 1 | 17.5 | 1.5 | 16 | ns |
| $t_{PHL}$ | | | 2 | 13 | 1 | 16 | 1.5 | 14.5 | |
| $t_{PLH}$ | LE | $\overline{Q}$ | 2 | 14.5 | 1 | 18 | 1.5 | 16.5 | ns |
| $t_{PHL}$ | | | 2 | 13 | 1 | 16 | 1.5 | 14.5 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 2 | 12.5 | 1 | 15.5 | 1.5 | 14 | ns |
| $t_{PZL}$ | | | 2 | 12.5 | 1 | 15.5 | 1.5 | 14 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 2 | 13 | 1 | 16 | 1.5 | 14.5 | ns |
| $t_{PLZ}$ | | | 2 | 13 | 1 | 16 | 1.5 | 14.5 | |

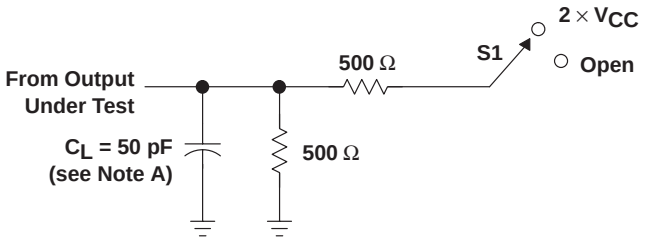
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | SN54AC533 | | SN74AC533 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | $\overline{Q}$ | 2 | 10 | 1 | 12.5 | 1.5 | 11 | ns |
| $t_{PHL}$ | | | 2 | 9.5 | 1 | 12 | 1.5 | 10.5 | |
| $t_{PLH}$ | LE | $\overline{Q}$ | 2 | 10.5 | 1 | 13 | 1.5 | 11.5 | ns |
| $t_{PHL}$ | | | 2 | 10 | 1 | 13 | 1.5 | 11 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 2 | 9.5 | 1 | 12 | 1.5 | 10.5 | ns |
| $t_{PZL}$ | | | 2 | 9.5 | 1 | 12 | 1.5 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 2 | 10 | 1 | 12.5 | 1.5 | 11 | ns |
| $t_{PLZ}$ | | | 2 | 10 | 1 | 12.5 | 1.5 | 11 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

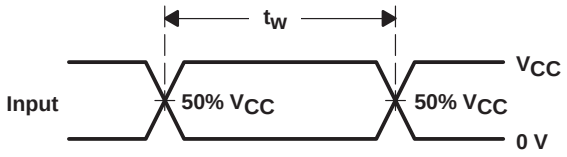
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 1 MHz | 40 | pF |

## PARAMETER MEASUREMENT INFORMATION

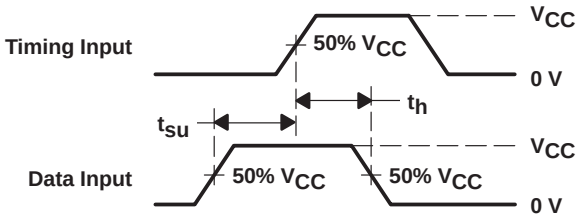



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |

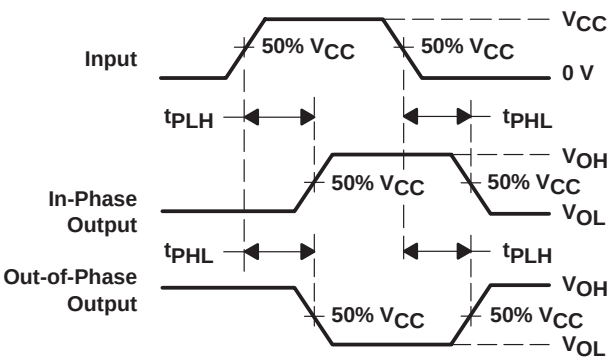
LOAD CIRCUIT



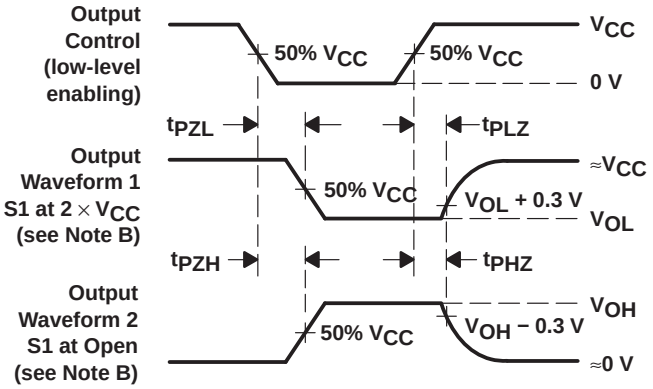

VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AC533DW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC533 |
| SN74AC533DW.A | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC533 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

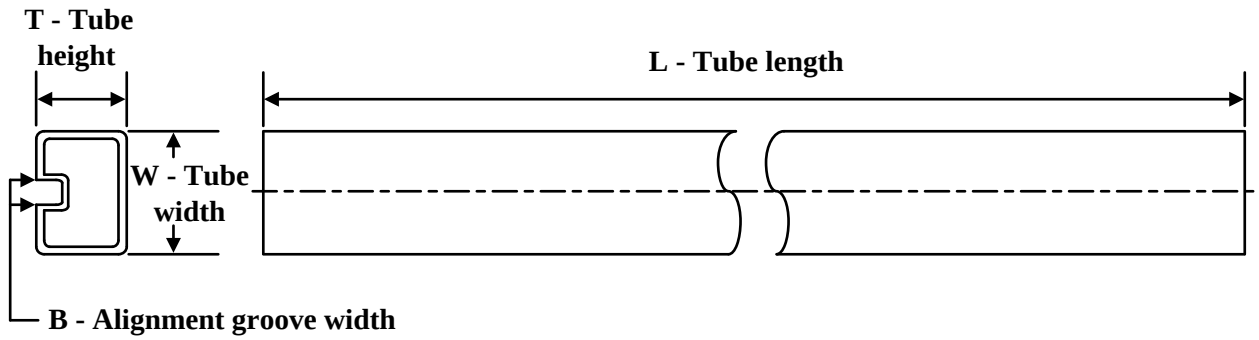
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

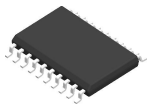
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74AC533DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74AC533DW.A | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

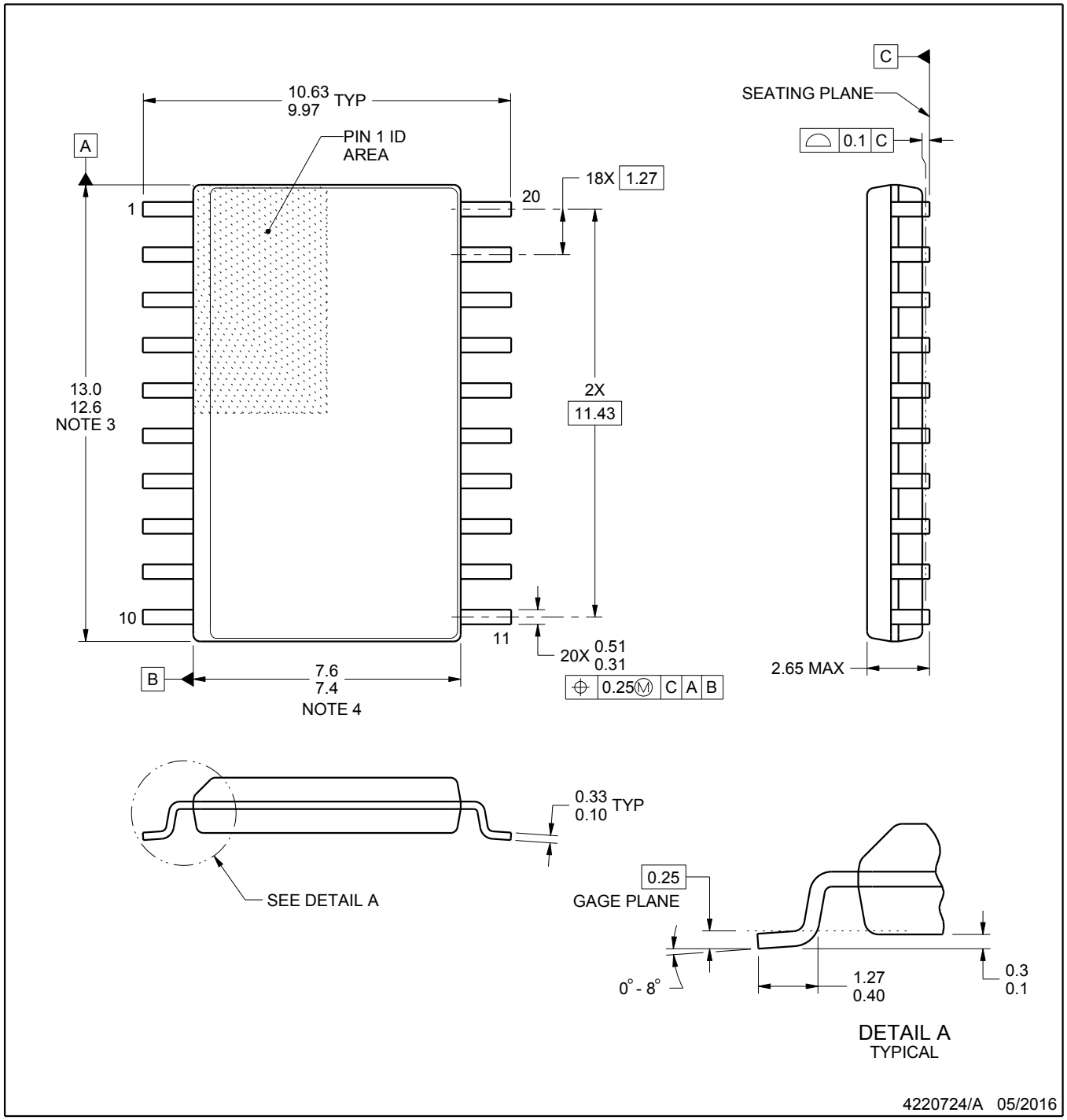


# PACKAGE OUTLINE

## DW0020A

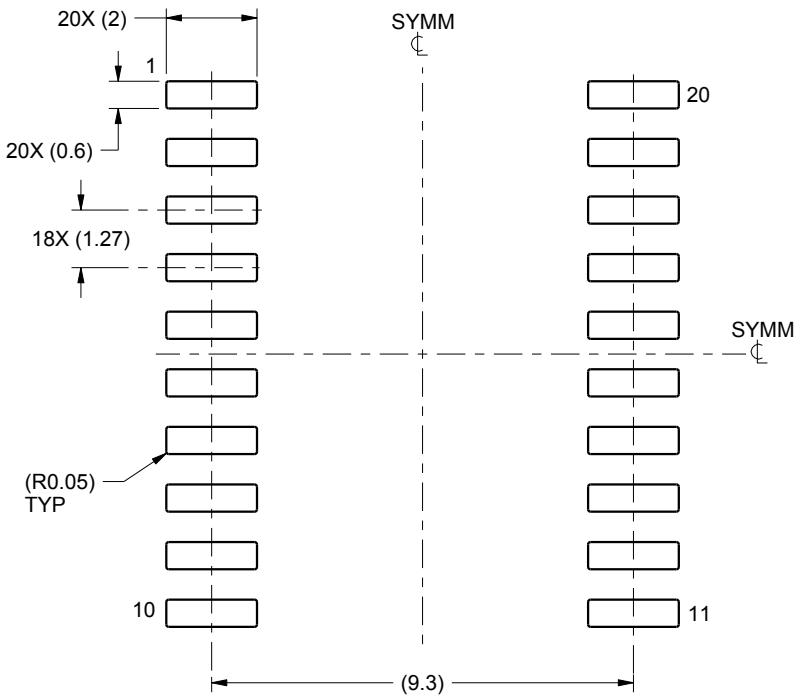
## SOIC - 2.65 mm max height

SOIC

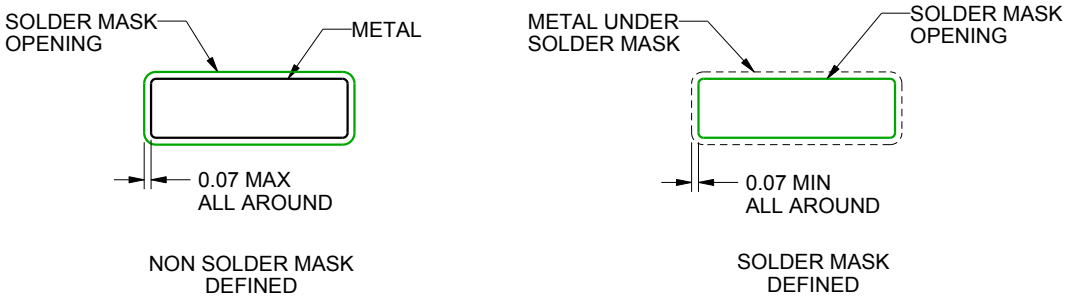



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

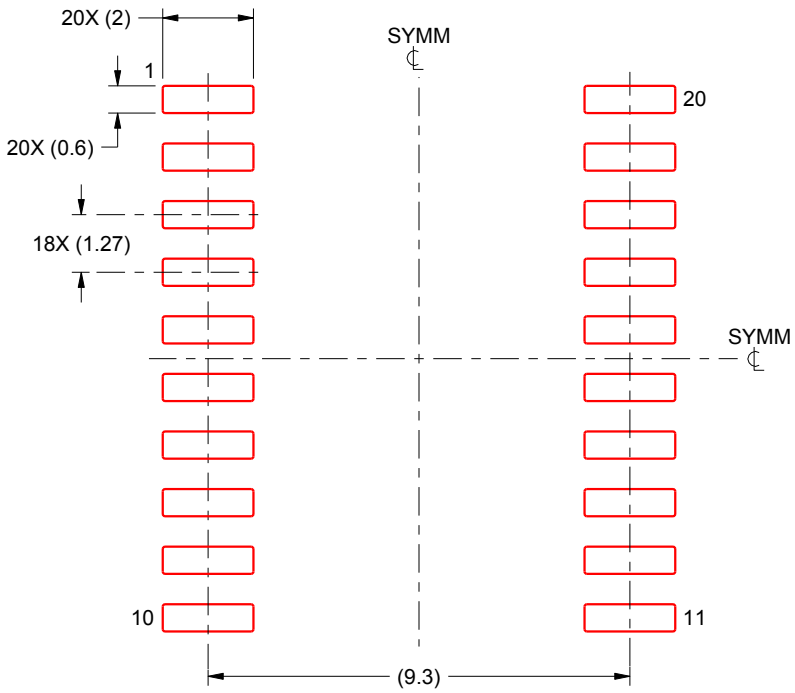



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025