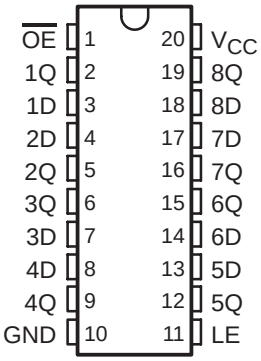
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 9.5 ns at 5 V**
- **3-State Noninverting Outputs Drive Bus Lines Directly**
- **Full Parallel Access for Loading**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DW PACKAGE
(TOP VIEW)



description/ordering information

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

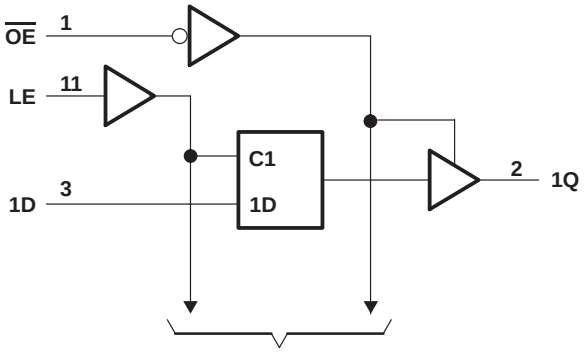
T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	SOIC − DW	Tape and reel	SN74AC373MDWREP	SAC373MEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 58°C/W
Storage temperature range, T_{stg} (see Note 3) . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Long-term high−temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12	mA
		V_{CC} = 4.5 V		−24	
		V_{CC} = 5.5 V		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature		−55	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
	I_{OH} = −12 mA		3 V	2.56			2.4		
	I_{OH} = −24 mA		4.5 V	3.86			3.7		
			5.5 V	4.86			4.7		
V_{OL}	I_{OL} = 50 μA		3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
	I_{OL} = 12 mA		3 V			0.36		0.5	
	I_{OL} = 24 mA		4.5 V			0.36		0.5	
			5.5 V			0.36		0.5	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.25		±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		80	μA
C_i	V_I = V_{CC} or GND		5 V		4.5				pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	5.5		6.5		ns
t_{su}	Setup time, data before LE↓	5.5		6.5		ns
t_h	Hold time, data after LE↓	1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	4		5		ns
t_{su}	Setup time, data before LE↓	4		5		ns
t_h	Hold time, data after LE↓	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.5	10	13.5	1	16.5	ns
t_{PHL}			1.5	9.5	13.0	1	16	
t_{PLH}	LE	Q	1.5	10	13.5	1	16.5	ns
t_{PHL}			1.5	9.5	12.5	1	15	
t_{PZH}	$\overline{OE}$	Q	1.5	9	11.5	1	14	ns
t_{PZL}			1.5	8.5	11.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	1.5	10	12.5	1	16	ns
t_{PLZ}			1.5	8	11.5	1	13	

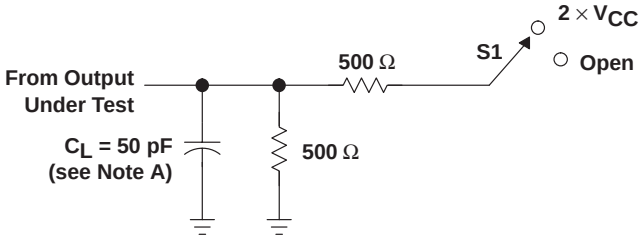
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.5	7	9.5	1	11.5	ns
t_{PHL}			1.5	7	9.5	1	11.5	
t_{PLH}	LE	Q	1.5	7.5	9.5	1	12	ns
t_{PHL}			1.5	7	9.5	1	11	
t_{PZH}	$\overline{OE}$	Q	1.5	7	8.5	1	10.5	ns
t_{PZL}			1.5	6.5	8.5	1	10	
t_{PHZ}	$\overline{OE}$	Q	1.5	8	11	1	13.5	ns
t_{PLZ}			1.5	6.5	8.5	1	10.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

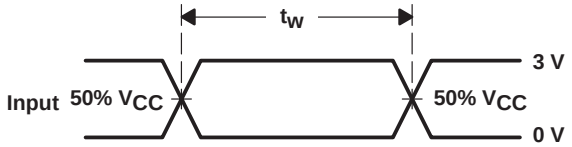
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION

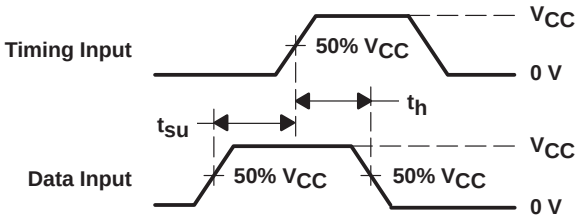


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



VOLTAGE WAVEFORMS



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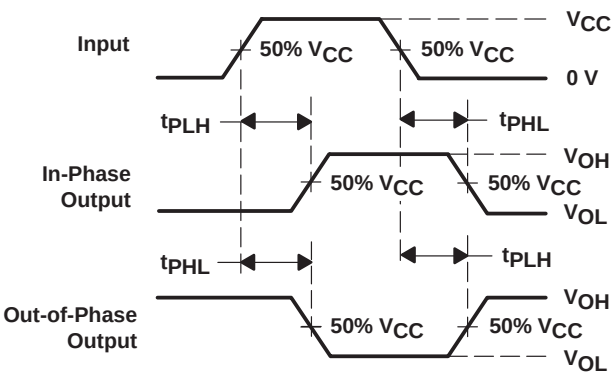
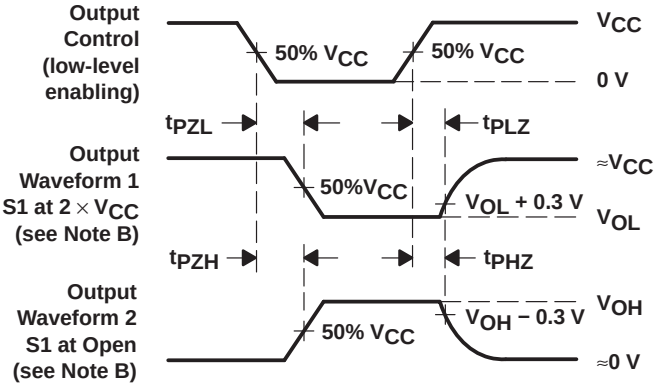


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC373MDWREP	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAC373MEP
V62/04621-01XE	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SAC373MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74AC373-EP :

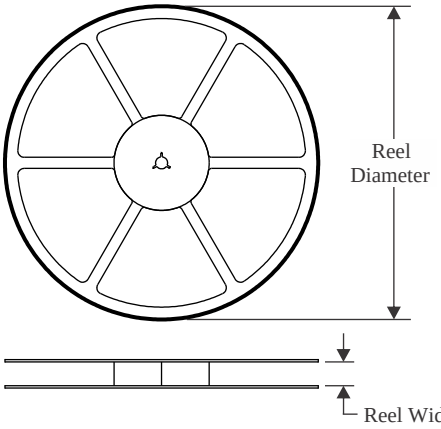
- Catalog : SN74AC373
- Military : SN54AC373

NOTE: Qualified Version Definitions:

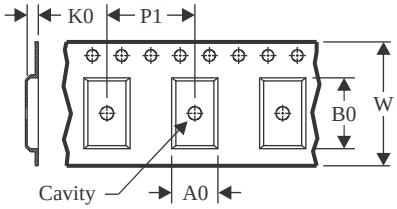
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

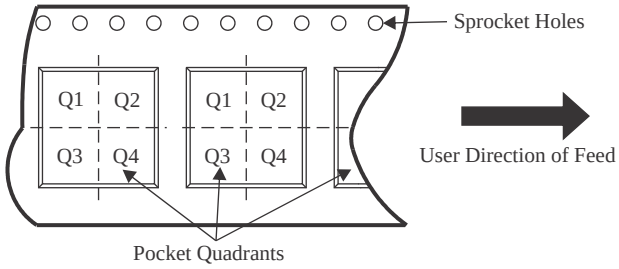


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

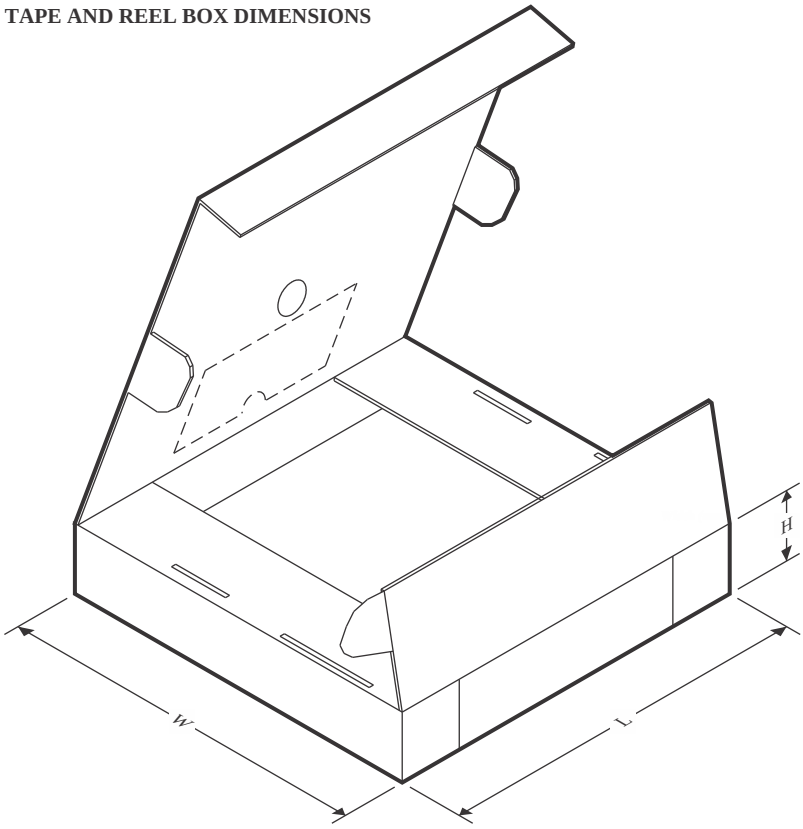
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373MDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC373MDWREP	SOIC	DW	20	2000	356.0	356.0	45.0

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Last updated 10/2025