







SN74AC14-Q1

SCAS915B - JUNE 2011 - REVISED JULY 2024

SN74AC14-Q1 Automotive Hex Schmitt-Trigger Inverter

1 Features

- Qualified for automotive applications
- 2V to $6V\ V_{CC}$ operation
- Inputs accept voltages to 6V

2 Description

This Schmitt-trigger device contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC14-Q1	BQA (WQFN, 14)	3.00mm × 2.50mm	3.00mm × 2.50mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm x 4.4mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.





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3 Pin Configuration and Functions

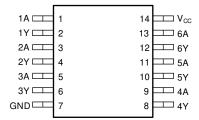


Figure 3-1. PW Package, 14-Pin TSSOP (Top View)

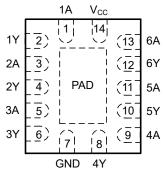


Figure 3-2. BQA Package, 14-Pin WQFN (Top View)

PIN		1/0	DESCRIPTION
NAME	N.O.	1/0	DESCRIPTION
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	_	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{CC}	14	_	Positive Supply
NC		_	Not internally connected
Thermal Pad	(1)	_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQA package only.



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ⁽²⁾	Input voltage range		-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_1 < 0 \text{ or } V_1 > V_{CC})$		±20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20	mA
Io	Continuous output current	(V _O = 0 to V _{CC})		±50	mA
	Continuous current through V _{CC} or	GND		±200	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommend Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

	1 3 1		MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	V
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
I _{OH}		V _{CC} = 3 V		-12	
	High-level output current	V _{CC} = 4.5 V		-24	mA
		V _{CC} = 5.5 V		-24	
		V _{CC} = 3 V		12	
I _{OL}	Low-level output current	V _{CC} = 4.5 V		24	mA
		V _{CC} = 5.5 V		24	
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.3 Thermal Information

		SN74AC14-Q1			
	THERMAL METRIC(1)		PW (TSSOP)	UNIT	
		14 PINS	14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.4	148	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: SN74AC14-Q1

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v	T _A = 25°C			MIN MAX		UNIT
PARAMETER		V _{cc}	MIN	TYP	MAX	IVIIIN	WAX	ONII
V _{T+}		3 V	0.8	1.8	2.2	0.8	2.2	
Positive-going		4.5 V	1.5	2.6	3.2	1.5	3.2	V
threshold		5.5 V	1.6	3.2	3.9	1.6	3.9	
V _{T-}		3 V	0.5	8.0	1	0.5	1.2	
Negative-going		4.5 V	0.9	1.4	1.8	0.9	1.8	V
threshold		5.5 V	1.1	1.8	2.3	1.1	2.3	
ΔV_{T}		3 V	0.3	1	1.2	0.3	1.2	
Hysteresis		4.5 V	0.4	1.2	1.4	0.4	1.4	V
(V _{T+} - V _{T-})		5.5 V	0.5	1.4	1.6	0.5	1.6	
		3 V	2.9			2.9		
	I _{OH} = -50 μA	4.5 V	4.4			4.4		
V		5.5 V	5.4			5.4		V
V _{OH}	I _{OH} = -12 mA	3 V	2.56			2.4		V
	I _{OH} = -24 mA	4.5 V	3.86			3.7		
		5.5 V	4.86			4.7		
		3 V			0.1		0.1	
	I _{OL} = 50 μA	4.5 V			0.1		0.1	
V		5.5 V			0.1		0.1	V
V _{OL}	I _{OL} = 12 mA	3 V			0.36		0.5	V
	L = 24 mA	4.5 V			0.36		0.5	
	I _{OL} = 24 mA	5.5 V			0.36		0.5	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40	μΑ
C _i	V _I = V _{CC} or GND	5 V		4.5		-		pF

4.5 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	T _A = 25°C		MIN MAX		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	IVIIIV IVIAX	IVIAA	UNII
t _{PLH}	A	V	1.5	5	10	1.5	12	no
t _{PHL}		ř	1.5	5	8.5	1.5	10	ns

4.6 Switching Characteristics, V_{CC} = 3.3 V \pm 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	T _A = 25°C		MIN MAX		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	IVIIIN	IVIAA	UNII
t _{PLH}	A	V	1.5	6	13.5	1.0	16	20
t _{PHL}		ľ	1.5	6	11.5	1.0	14	ns



4.7 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

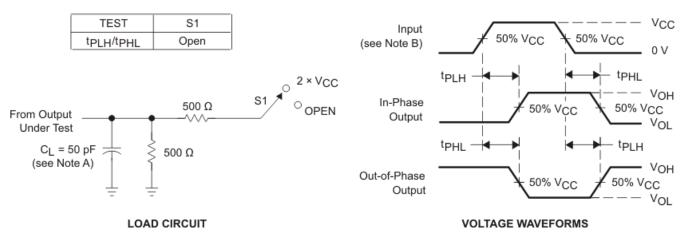
	PARAMETER		TEST CONDITIONS		
C_{pd}	Power dissipation capacitance	C _L = 50 pF,	f = 1 MHz	30	pF

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5 Parameter Measurement Information



- C_I includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms



6 Detailed Description

6.1 Overview

This Schmitt-trigger device contain six independent inverters. They perform the Boolean function Y = A/. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

6.2 Functional Block Diagram



Figure 6-1. Logic Diagram Each Inverter (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table

INPUT	OUTPUT
Α	Y
Н	L
L	Н

Product Folder Links: SN74AC14-Q1



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.2.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, $0.1\mu F$ is recommended; if there are multiple V_{CC} pins, then $0.01\mu F$ or $0.022\mu F$ is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A $0.1\mu F$ and a $1\mu F$ are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Section 7.2.2 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

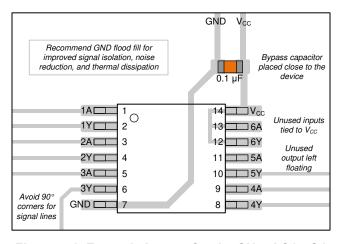


Figure 7-1. Example Layout for the SN74AC14-Q1



8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74AC14-Q1	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2023) to Revision B (July 2024) Page • Added BQA package size to Package Information table, Pin Configuration and Functions section, and Thermal Information table. 1 • Added package size to Package Information table. 1 • Updated RθJA values: PW = 113 to 148, all values in °C/W. 4 • Updated Layout Example image. 9

Changes from Revision * (June 2011) to Revision A (May 2023)

Pag

Added Package Information table, Pin Functions table, and Thermal Information table......

Product Folder Links: SN74AC14-Q1



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/			Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AC14QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q
SN74AC14QPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q
SN74AC14WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q
SN74AC14WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AC14-Q1:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Catalog : SN74AC14

Military: SN54AC14

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

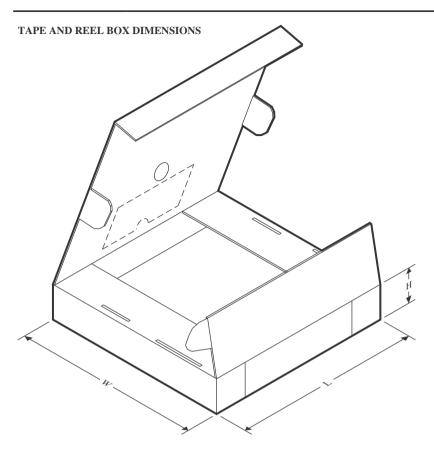


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC14QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC14WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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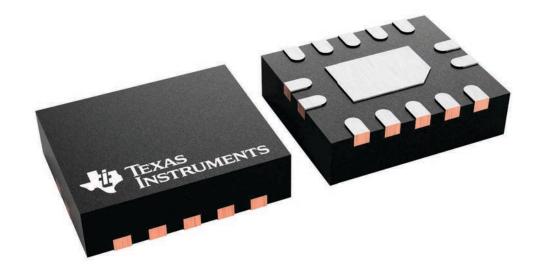
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC14QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC14WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

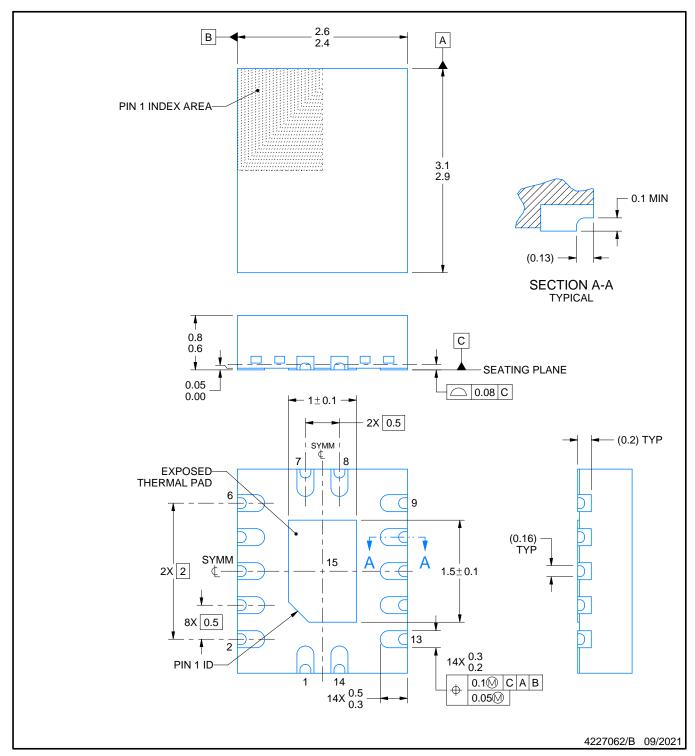
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

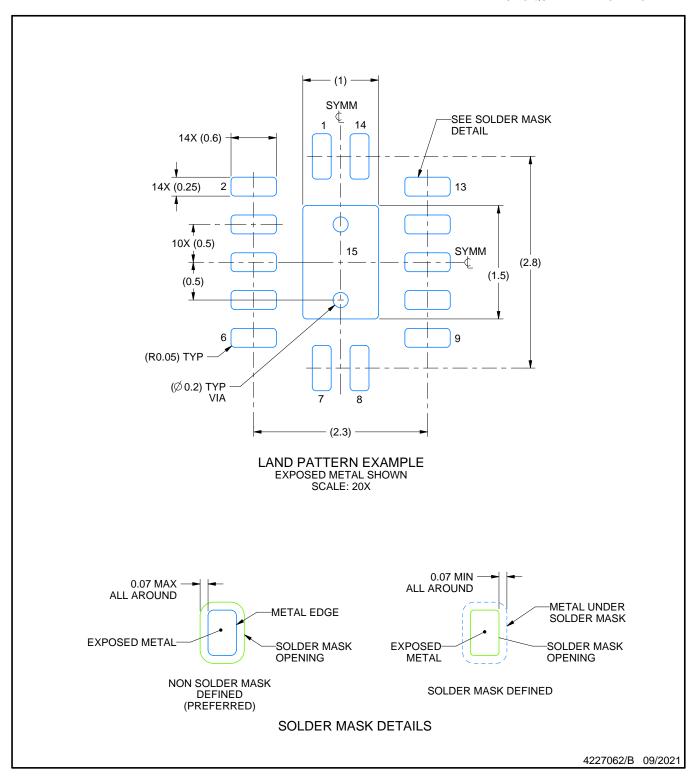


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

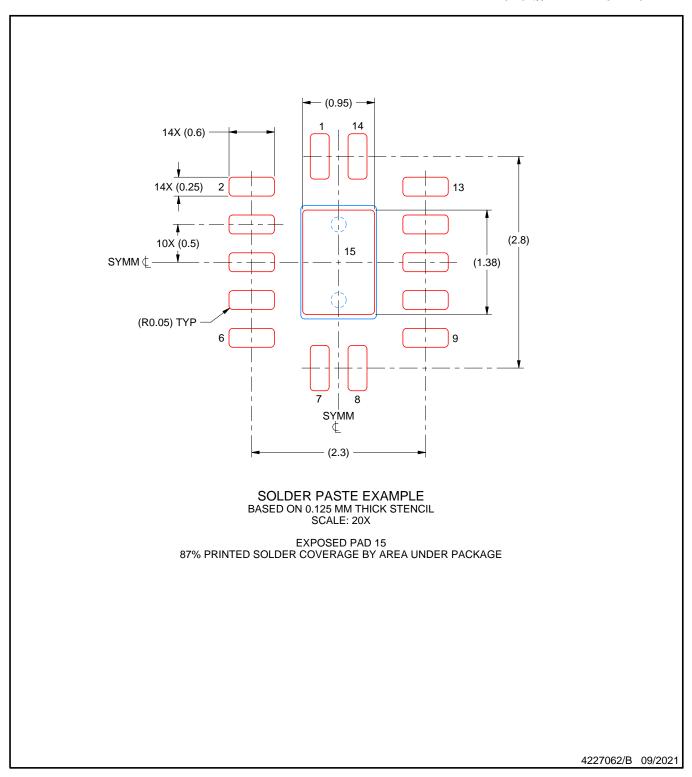


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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