## SN54ABTH25245, SN74ABTH25245 25- $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS251F - JUNE 1992 - REVISED MAY 1997

- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> =  $25^{\circ}$ C
- High-Impedance State During Power Up and Power Down
- **Designed to Facilitate Incident-Wave** Switching for Line Impedances of 25  $\Omega$  or Greater
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic** Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) DIPs

#### description

The 'ABTH25245 are 25- $\Omega$  octal bus transceivers designed for asynchronous communication between data buses. They improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

These devices allow noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that both buses are effectively isolated. When OE is low, the device is active.

These transceivers are capable of sinking 188 mA of  $I_{OL}$  current, which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more-reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all narameters



SN54ABTH2524	5 JT PACKAGE
SN74ABTH25245	DW OR NT PACKAGE
(TOP	VIEW)

	_		-
A1		$\cup_{24}$	DIR
GND	2	23	] B1
A2	[]3	22	] B2
A3	4	21	Vcc
GND	5	20	] вз
A4	6	19	] B4
A5	<b>[</b> 7	18	] B5
GND	8]]	17	] B6
A6	9	16	V <sub>CC</sub>
A7	10	15	] в7
GND	[ 11	14	] B8
A8	[12	. 13	

#### SN54ABTH25245 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

Copyright © 1997, Texas Instruments Incorporated

#### description (continued)

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH25245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ABTH25245 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

FUNCTION TABLE										
INP	UTS									
OE	DIR	OPERATION								
L	L	B data to A bus								
L	Н	A data to B bus								
Н	Х	Isolation								

#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.



#### logic diagram (positive logic)



**To Seven Other Channels** 

Pin numbers shown are for the DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	$-0.5$ V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$-0.5$ V to 7 V
Voltage range applied to any output in the disabled or power-off state, V <sub>O</sub>	. –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V <sub>O</sub>	. $-0.5$ V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mÅ
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Current into any output in the low state, IO: SN74ABTH25245 (A port)	376 mA
SN74ABTH25245 (B port)	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	81°C/W
NT package	67°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



## SN54ABTH25245, SN74ABTH25245 25- $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS251F - JUNE 1992 - REVISED MAY 1997

#### recommended operating conditions (see Note 3)

				SN54ABTI	125245	SN74ABTH	125245	
				MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage			4.5	5.5	4.5	5.5	V
VIH	High-level input voltage			2		2		V
VIL	Low-level input voltage				0.8		0.8	V
VI	Input voltage			0	Vcc	0	VCC	V
IК	Input clamp current		<u> </u>		-18	mA		
			A port	40	~ –80		-80	m۸
ЧОН	riigh-level output current		B port	40	-32		-32	IIIA
			A port	na	188		188	mA
OL		current		90g	64		64	1110
A+/A\/	Input transition rise or fall rate		Control inputs	Q	4		4	nc//
	input transition rise of fail fate	A or B ports		10		10	115/ V	
$\Delta t / \Delta V_{CC}$	Power-up ramp rate			200		200		μs/V
TA	Operating free-air temperature			-55	125	-40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



## SN54ABTH25245, SN74ABTH25245 25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS251F - JUNE 1992 - REVISED MAY 1997

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST CO	NDITIONS	SN54	ABTH2	5245	SN74	ABTH2	5245	LINUT	
					TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.2			-1.2	V	
	A port	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = –3 mA	2.7			2.7				
	Apon	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -80 mA	2.4			2.4				
∨он		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = –3 mA	2.5			2.5			V	
	B port	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = –3 mA	3			3				
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA	2*			2				
	A port		I <sub>OL</sub> = 94 mA			0.55			0.55		
VOL	Apon	VCC = 4.3 V	I <sub>OL</sub> = 188 mA			0.7			0.7	V	
	B port	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA			0.55*			0.55		
V <sub>hys</sub>					100			100		mV	
I.	Control inputs	$V_{CC} = 0$ to 5.5 V,	$V_{I} = V_{CC} \text{ or } GND$			1±1			±1	uА	
Ч	A or B ports	$V_{CC}$ = 2.1 V to 5.5 V,	$V_{I} = V_{CC} \text{ or } GND$		N.	±20			±20	μΛ	
44 15	A or P porto	A or R ports $V_{00} = 4.5 V_{00}$		V <sub>I</sub> = 0.8 V	100	P		100			
'I(noid)	A of B ports	VCC = 4.3 V	V <sub>I</sub> = 2 V	-100	E		-100			μΛ	
IOZPU <sup>‡</sup>	:	$V_{CC} = 0$ to 2.1 V, $V_{O} = 0$	0.5 V to 2.7 V, $\overline{OE} = X$		3	±50			±50	μΑ	
IOZPD <sup>‡</sup>	:	$V_{CC} = 2.1 V \text{ to } 0, V_{O} = 0$	0.5 V to 2.7 V, OE = X	8		±50			±50	μA	
loff		$V_{CC} = 0,$	VI or VO $\leq$ 4.5 V	Q		±100			±100	μA	
ICEX	_	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V			50			50	μA	
١ <sub>O</sub> §	B port	V <sub>CC</sub> = 5.5 V,	$V_{O} = 2.5 V$	-50		-210	-50		-210	mA	
		$V_{CC} = 5.5 V_{.}$	Outputs high			500			500	μΑ	
ICC		Outputs open,	Outputs low			20			20	mA	
VI		$V_I = V_{CC}$ or GND	Outputs disabled			500			500	μΑ	
$\Delta I_{CC}$ V <sub>CC</sub> = 5.5 V, One input at 3.4 V Other inputs at V <sub>CC</sub> or GND		at 3.4 V, SND			1			1	mA		
Ci	Control inputs	V <sub>CC</sub> = 5 V,	$V_I = V_{CC} \text{ or } GND$		4			4		pF	
Cio	A or B ports	V <sub>CC</sub> = 5 V,	$V_{O} = V_{CC} \text{ or } GND$		11.5			11.5		pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



#### SN54ABTH25245, SN74ABTH25245 **25-** $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS251F - JUNE 1992 - REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER			V( Tj	CC = 5 V A = 25°C	, ;	SN54ABTH25245	SN74ABTH	125245	UNIT
	(INFOT)	(001-01)	MIN	TYP	MAX	MIN MAX	MIN	MAX	
<sup>t</sup> PLH	A or B	RorA	1	2.3	3.5	1 1	1	3.9	200
<sup>t</sup> PHL	AUB	DOLA	1	2.4	3.5	1 &	1	4.3	115
<sup>t</sup> PZH		A or B	1.5	3.7	5.4	1.5	1.5	6.5	-
<sup>t</sup> PZL	ÛE		1.4	4	5.8	1.4	1.4	6.8	115
<sup>t</sup> PHZ		A or P	2	4.3	6.1	2	2	7.2	
<sup>t</sup> PLZ	UE	A or B	2	3.9	5.8	<b>Q</b> 2	2	6.4	115

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



#### SN54ABTH25245, SN74ABTH25245 25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS251F – JUNE 1992 – REVISED MAY 1997

7 V **S1** O Open **500** Ω **From Output**  $\Lambda \Lambda A$ TEST **S**1 **Under Test** C GND Open tPLH/tPHL  $C_1 = 50 \text{ pF}$ tPLZ/tPZL 7 V **500** Ω (see Note A) tPHZ/tPZH Open LOAD CIRCUIT 3 V **Timing Input** 1.5 V 0 V tw t<sub>su</sub> th 3 V 3 V Input 1.5 V 1.5 V **Data Input** 1.5 V 1.5 V 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATION SETUP AND HOLD TIMES 3 V 3 V Output 1.5 V 1.5 V Input 1.5 V 1.5 V Control 0 V 0 V <sup>t</sup>PZL <sup>t</sup>PHL <sup>t</sup>PLH <sup>t</sup>PLZ Output VOH 3.5 V Waveform 1 1.5 V 1.5 V 1.5 V Output VOI + 0.3 V S1 at 7 V VOL VOL (see Note B) <sup>t</sup>PHZ <sup>t</sup>PLH <sup>t</sup>PHL – <sup>t</sup>PZH <sup>-</sup> Output VOH Vон Waveform 2 V<sub>OH</sub> – 0.3 V 1.5 V 1.5 V 1.5 V Output S1 at Open ≈ 0 V VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES** ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

#### PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





Texas

STRUMENTS

#### TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH25245DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABTH25245DWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1



www.ti.com

# PACKAGE MATERIALS INFORMATION

15-Jul-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH25245DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74ABTH25245DWRG4	SOIC	DW	24	2000	350.0	350.0	43.0

## TEXAS INSTRUMENTS

www.ti.com

15-Jul-2025

## TUBE



## - B - Alignment groove width

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
SN74ABTH25245DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABTH25245DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated