

SN54ABT16260, SN74ABTH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art **EPIC-II^B**™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The SN54ABT16260 and SN74ABTH16260 are 12-bit to 24-bit multiplexed D-type latches used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A_1 – A_{12} , $1B_1$ – $1B_{12}$, and $2B_1$ – $2B_{12}$) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus-transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable ($LE1B$, $LE2B$, $LEA1B$, and $LEA2B$) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

SN54ABT16260 . . . WD PACKAGE
SN74ABTH16260 . . . DL PACKAGE
(TOP VIEW)

$\overline{OEA}$	1	56	$\overline{OE2B}$
$LE1B$	2	55	$LEA2B$
$2B_3$	3	54	$2B_4$
GND	4	53	GND
$2B_2$	5	52	$2B_5$
$2B_1$	6	51	$2B_6$
V_{CC}	7	50	V_{CC}
A_1	8	49	$2B_7$
A_2	9	48	$2B_8$
A_3	10	47	$2B_9$
GND	11	46	GND
A_4	12	45	$2B_{10}$
A_5	13	44	$2B_{11}$
A_6	14	43	$2B_{12}$
A_7	15	42	$1B_{12}$
A_8	16	41	$1B_{11}$
A_9	17	40	$1B_{10}$
GND	18	39	GND
A_{10}	19	38	$1B_9$
A_{11}	20	37	$1B_8$
A_{12}	21	36	$1B_7$
V_{CC}	22	35	V_{CC}
$1B_1$	23	34	$1B_6$
$1B_2$	24	33	$1B_5$
GND	25	32	GND
$1B_3$	26	31	$1B_4$
$LE2B$	27	30	$LEA1B$
SEL	28	29	$\overline{OE1B}$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II^B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN54ABT16260, SN74ABTH16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABT16260 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH16260 is characterized for operation from -40°C to 85°C .

Function Tables

B TO A ($\overline{OEB} = \text{H}$)

INPUTS						OUTPUT A
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

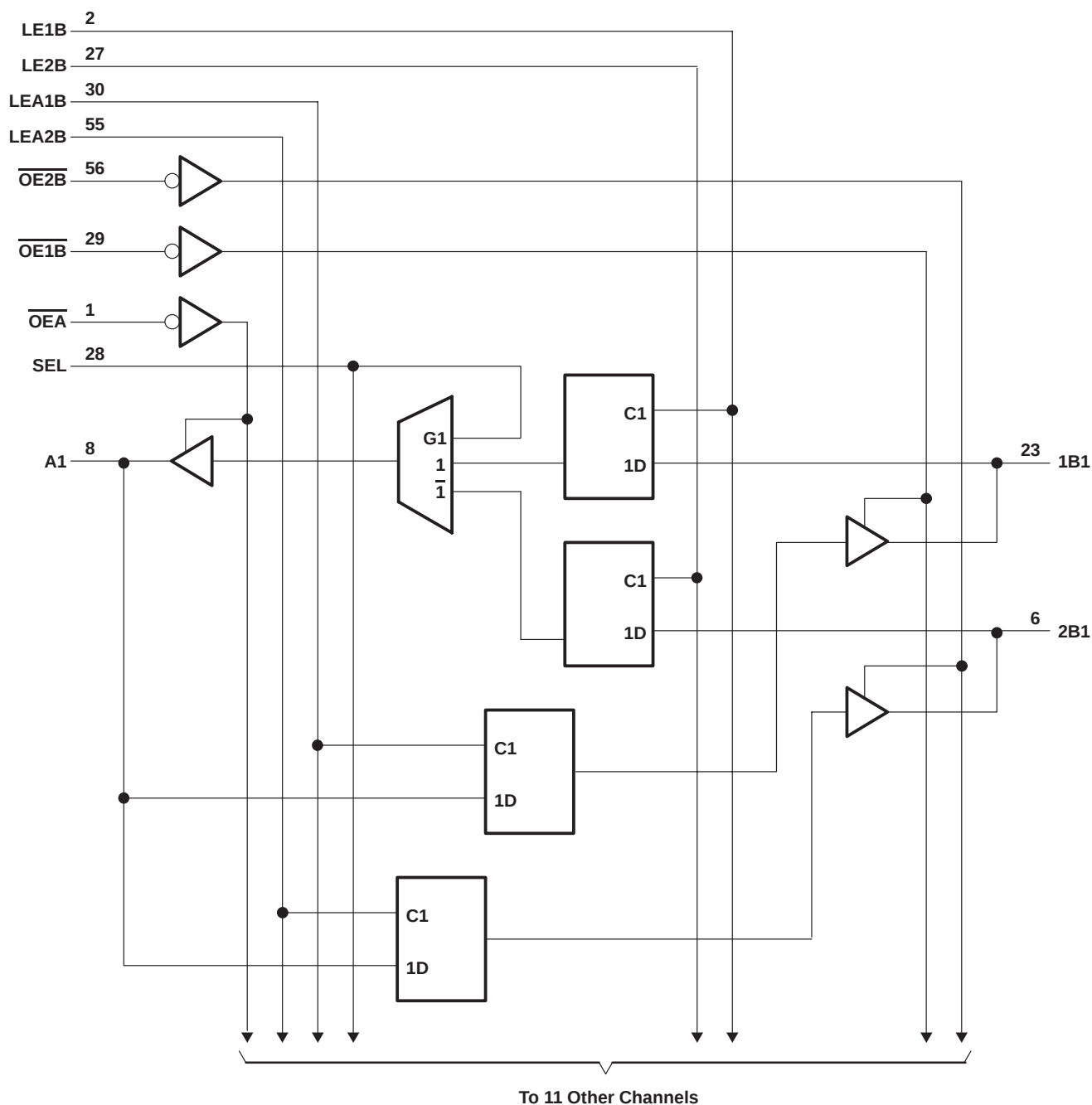
A TO B ($\overline{OEA} = \text{H}$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

SN54ABT16260, SN74ABTH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

logic diagram (positive logic)



To 11 Other Channels

SN54ABT16260, SN74ABTH16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16260	96 mA
SN74ABTH16260	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16260		SN74ABTH16260		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT16260, SN74ABTH16260
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT16260		SN74ABTH16260		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
		V _{CC} = 4.5 V	2			2				
			2*					2		
V _{OL}		V _{CC} = 4.5 V			0.36		0.5			V
					0.55*				0.55	
V _{hys}			100							mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND			±20		±100		±20	
I _I (hold)	A or B ports	V _{CC} = 4.5 V				100		100		μA
						–100		–100		
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZH} §		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I _{OZL} §		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			–10		–10		–10	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA
I _O ¶		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–225	–50	–225	–50	–225	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			1.5		1.5		1.5	mA
					63		63		63	
					1		1		1	
ΔI _{CC} #		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i		V _I = 2.5 V or 0.5 V			3					pF
C _{io}		V _O = 2.5 V or 0.5 V			11.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT16260, SN74ABTH16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS204C – JUNE 1992 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}^\dagger$		SN54ABT16260		SN74ABTH16260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t_{SU}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		2		1.5		ns
t_H	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1.5		1		ns

[†] These values apply only to the SN74ABTH16260.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16260					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1	3.1	5.3	1	5.9	ns
t _{PHL}			1	3.4	5.4	1	6.3	
t _{PLH}	LE	A or B	1.1	3.2	5.4	1.1	6.6	ns
t _{PHL}			1.1	3.3	5.3	1.1	5.9	
t _{PLH}	SEL (B1)	A	1.3	3.2	5.1	1.3	5.4	ns
	SEL (B2)		1.1	3.4	5.4	1.1	6.3	
t _{PHL}	SEL (B1)		1.5	3.1	4.6	1.5	5	
	SEL (B2)		1.6	3.6	5.3	1.6	6.2	
t _{PZH}	$\overline{\text{OE}}$	A or B	1	3.3	5.6	1	6.4	ns
t _{PZL}			1.6	3.8	5.9	1.6	6.5	
t _{PHZ}	$\overline{\text{OE}}$	A or B	2.2	4.1	5.9	2.2	7.5	ns
t _{PLZ}			1.3	3.2	5	1.3	5.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABTH16260					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1	3.1	4.8	1	5.6	ns
t _{PHL}			1	3.4	5	1	5.9	
t _{PLH}	LE	A or B	1.1	3.2	4.9	1.1	5.8	ns
t _{PHL}			1.1	3.3	4.9	1.1	5.3	
t _{PLH}	SEL (B1)	A	1.3	3.2	4.6	1.3	5.3	ns
	SEL (B2)		1.1	3.4	4.9	1.1	6	
t _{PHL}	SEL (B1)		1.5	3.1	4.4	1.5	4.4	
	SEL (B2)		1.6	3.6	5.1	1.6	5.9	
t _{PZH}	$\overline{\text{OE}}$	A or B	1	3.3	4.7	1	5.7	ns
t _{PZL}			1.6	3.8	5.1	1.6	5.8	
t _{PHZ}	$\overline{\text{OE}}$	A or B	2.2	4.1	5.4	2.2	6.4	ns
t _{PLZ}			1.3	3.2	4.4	1.3	4.8	



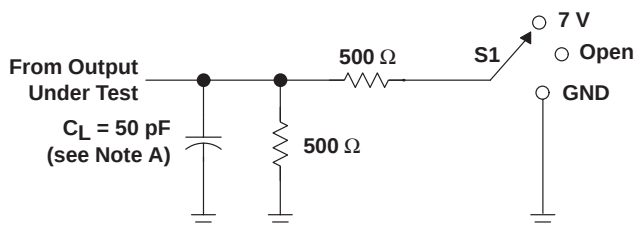
SN54ABT16260, SN74ABTH16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH 3-STATE OUTPUTS

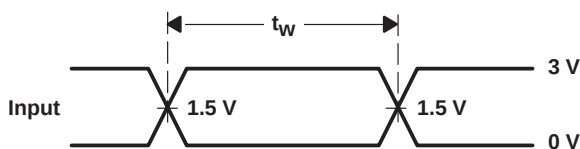
SCBS204C – JUNE 1992 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION

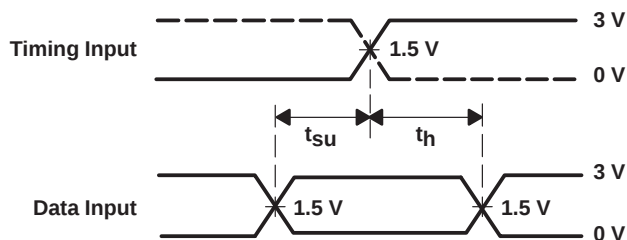


LOAD CIRCUIT

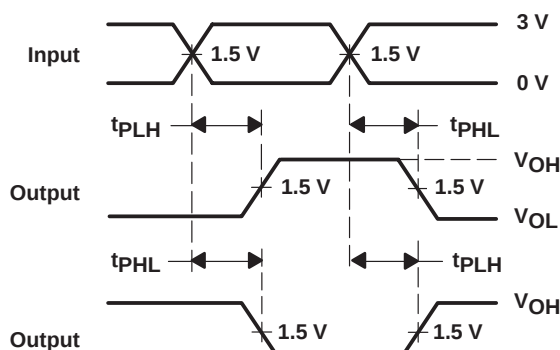
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



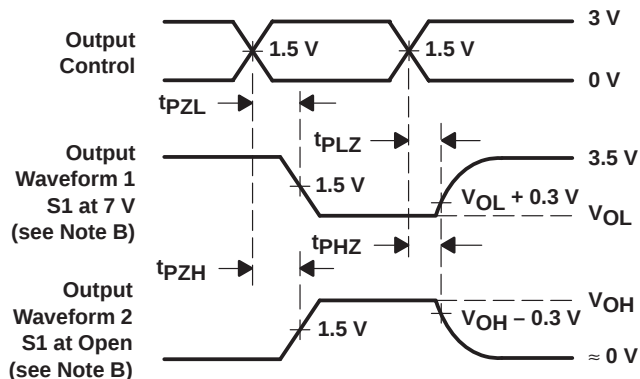
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABTH16260DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16260
SN74ABTH16260DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16260
SN74ABTH16260DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16260
SN74ABTH16260DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16260

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16260DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16260DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABTH16260DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABTH16260DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated