

HIGH-SPEED DIFFERENTIAL RECEIVERS

Check for Samples: [SN65LVDS33](#), [SN65LVDT33](#), [SN65LVDS34](#), [SN65LVDT34](#)

FEATURES

- 400-Mbps Signaling Rate⁽¹⁾ and 200-Mxfr/s Data Transfer Rate
- Operates With a Single 3.3-V Supply
- -4 V to 5 V Common-Mode Input Voltage Range
- Differential Input Thresholds $< \pm 50$ mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range
- Integrated 110- Ω Line Termination Resistors On LVDT Products
- TSSOP Packaging (33 Only)
- Complies With TIA/EIA-644 (LVDS)
- Active Failsafe Assures a High-Level Output With No Input
- Bus-Pin ESD Protection Exceeds 15 kV HBM
- Input Remains High-Impedance on Power Down
- TTL Inputs Are 5 V Tolerant
- Pin-Compatible With the AM26LS32, SN65LVDS32B, μ A9637, SN65LVDS9637B

⁽¹⁾ The signalling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

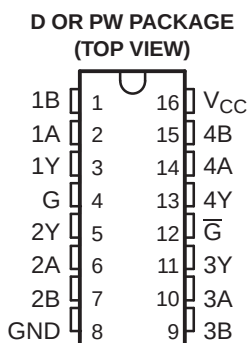
DESCRIPTION

This family of four LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

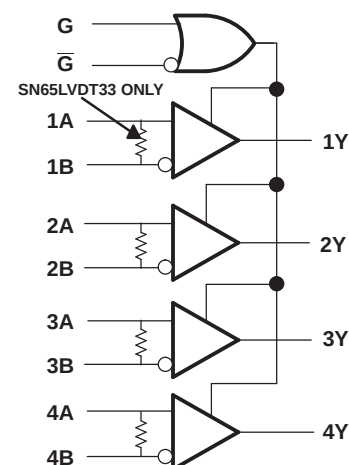
Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ± 50 mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals usually necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

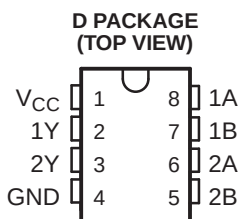
SN65LVDS33D, SN65LVDT33D SN65LVDS33PW, SN65LVDT33PW



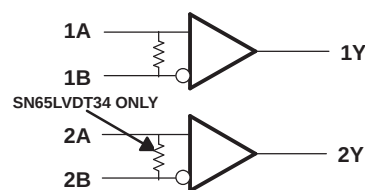
logic diagram (positive logic)



SN65LVDS34D, SN65LVDT34D



logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS⁽¹⁾

PART NUMBER ⁽²⁾	NUMBER OF RECEIVERS	TERMINATION RESISTOR	SYMBOLIZATION
SN65LVDS33D	4	No	LVDS33
SN65LVDS33PW	4	No	LVDS33
SN65LVDT33D	4	Yes	LVDT33
SN65LVDT33PW	4	Yes	LVDT33
SN65LVDS34D	2	No	LVDS34
SN65LVDT34D	2	Yes	LVDT34

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Add the suffix R for taped and reeled carrier.

DESCRIPTION (CONTINUED)

The receivers can withstand ± 15 kV human-body model (HBM) and ± 600 V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

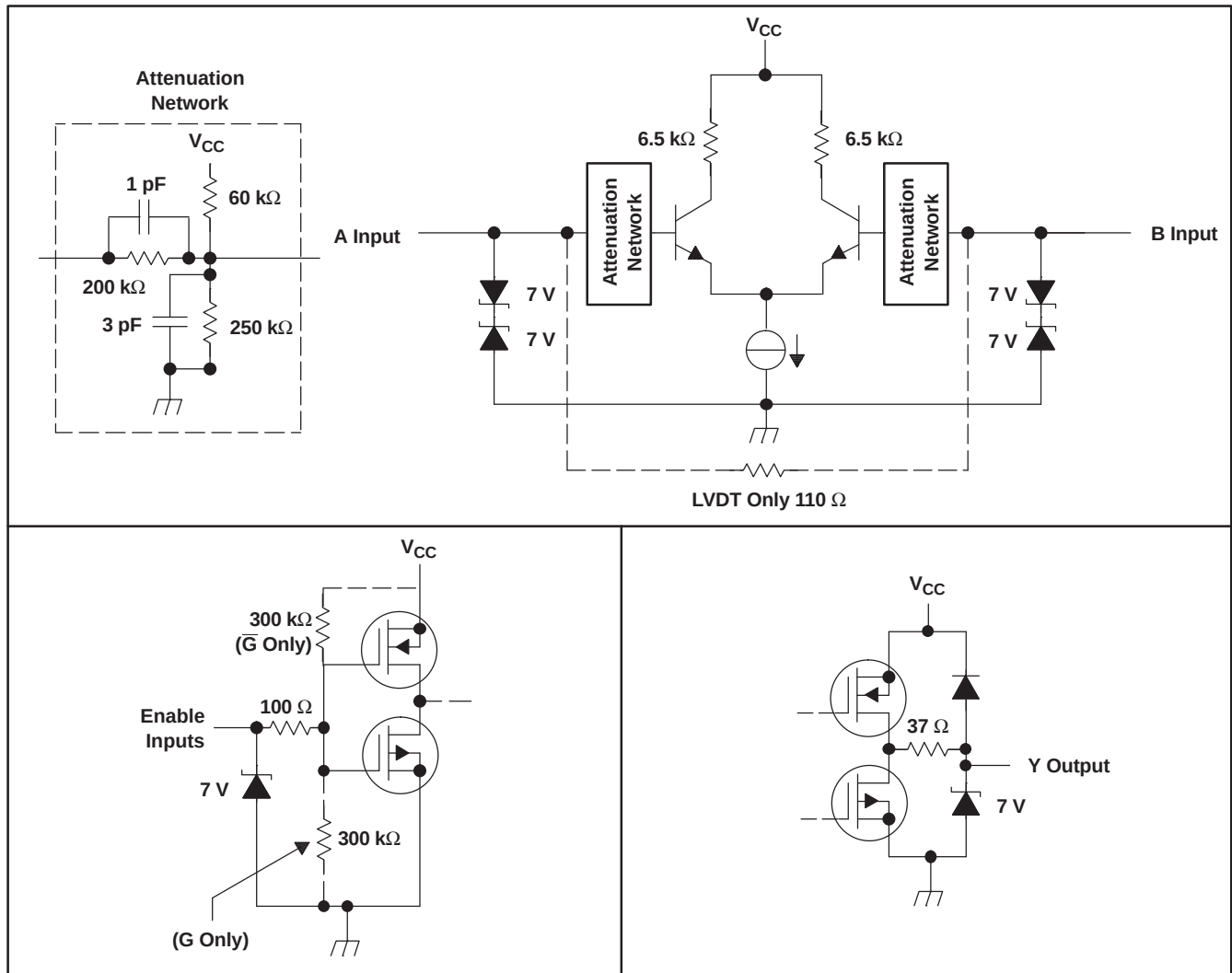
The SN65LVDS33, SN65LVDT33, SN65LVDS34 and SN65LVDT34 are characterized for operation from -40°C to 85°C .

Table 1. Function Tables⁽¹⁾

SN65LVDS33 and SN65LVDT33				SN65LVDS34 and SN65LVDT34	
DIFFERENTIAL INPUT	ENABLES		OUTPUT	DIFFERENTIAL INPUT	OUTPUT
$V_{ID} = V_A - V_B$	G	$\bar{G}$	Y	$V_{ID} = V_A - V_B$	Y
$V_{ID} \geq -32$ mV	H	X	H	$V_{ID} \geq -32$ mV	H
	X	L	H	-100 mV $< V_{ID} \leq -32$ mV	?
-100 mV $< V_{ID} \leq -32$ mV	H	X	?	$V_{ID} \leq -100$ mV	L
	X	L	?	Open	H
$V_{ID} \leq -100$ mV	H	X	L		
	X	L	L		
X	L	H	Z		
Open	H	X	H		
	X	L	H		

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
Supply voltage range, V_{CC} ⁽²⁾		–0.5 V to 4 V
Voltage range	Enables or Y	–1 V to 6 V
	A or B	–5 V to 6 V
	$ V_A - V_B $ (LVDT)	1 V
Electrostatic discharge	A, B, and GND ⁽³⁾	Class 3, A: 15 kV, B: 500 V
Charged-device mode	All pins ⁽⁴⁾	±500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
PW16	774 mW	6.2 mW/°C	402 mW
D16	950 mW	7.6 mW/°C	494 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables		5	V
V_{IL}	Low-level input voltage	Enables		0.8	V
$ V_{ID} $	Magnitude of differential input voltage	LVDS		3	V
		LVDT		0.8	
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)	–4		5	V
T_A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT1}	Positive-going differential input voltage threshold		V _{IB} = −4 V or 5 V, See Figure 1 and Figure 2			50	mV
V _{IT2}	Negative-going differential input voltage threshold				−50		
V _{IT3}	Differential input failsafe voltage threshold		See Table 2 and Figure 5	−32		−100	mV
V _{ID(HYS)}	Differential input voltage hysteresis, V _{IT1} − V _{IT2}				50		mV
V _{OH}	High-level output voltage		I _{OH} = −4 mA	2.4			V
V _{OL}	Low-level output voltage		I _{OL} = 4 mA			0.4	V
I _{CC}	Supply current	SN65LVDx33	G at V _{CC} , No load, Steady-state		16	23	mA
			G at GND		1.1	5	
		SN65LVDx34	No load, Steady-state		8	12	
I _I	Input current (A or B inputs)	SN65LVDS	V _I = 0 V, Other input open			±20	μA
			V _I = 2.4 V, Other input open			±20	
			V _I = −4 V, Other input open			±75	
			V _I = 5 V, Other input open			±40	
		SN65LVDT	V _I = 0 V, Other input open			±40	μA
			V _I = 2.4 V, Other input open			±40	
			V _I = −4 V, Other input open			±150	
			V _I = 5 V, Other input open			±80	
I _{ID}	Differential input current (I _{IA} − I _{IB})	SN65LVDS	V _{ID} = 100 mV, V _{IC} = −4 V or 5 V			±3	μA
		SN65LVDT	V _{ID} = 200 mV, V _{IC} = −4 V or 5 V	1.55		2.22	mA
I _{I(OFF)}	Power-off input current (A or B inputs)	SN65LVDS	V _A or V _B = 0 V or 2.4 V, V _{CC} = 0 V			±20	μA
			V _A or V _B = −4 or 5 V, V _{CC} = 0 V			±50	
		SN65LVDT	V _A or V _B = 0 V or 2.4 V, V _{CC} = 0 V			±30	
			V _A or V _B = −4 V or 5 V, V _{CC} = 0 V			±100	
I _{IH}	High-level input current (enables)		V _{IH} = 2 V			10	μA
I _{IL}	Low-level input current (enables)		V _{IL} = 0.8 V			10	μA
I _{OZ}	High-impedance output current			−10		10	μA
C _I	Input capacitance, A or B input to GND		V _I = 0.4 sin (4E6πt) + 0.5 V		5		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{PLH(1)}$	Propagation delay time, low-to-high-level output	See Figure 3	2.5	4	6	ns
$t_{PHL(1)}$	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe deactivate time	$C_L = 10$ pF, See Figure 3 and Figure 6			9	ns
t_{d2}	Delay time, failsafe activate time		0.3		1.5	μ s
$t_{sk(p)}$	Pulse skew ($ t_{PHL(1)} - t_{PLH(1)} $)	See Figure 3		200		ps
$t_{sk(o)}$	Output skew ⁽²⁾			150		ps
$t_{sk(pp)}$	Part-to-part skew ⁽³⁾				1	ns
t_r	Output signal rise time			0.8		ns
t_f	Output signal fall time			0.8		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			3.8	9	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	9	ns

- (1) All typical values are at 25°C and with a 3.3-V supply.
- (2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.
- (3) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

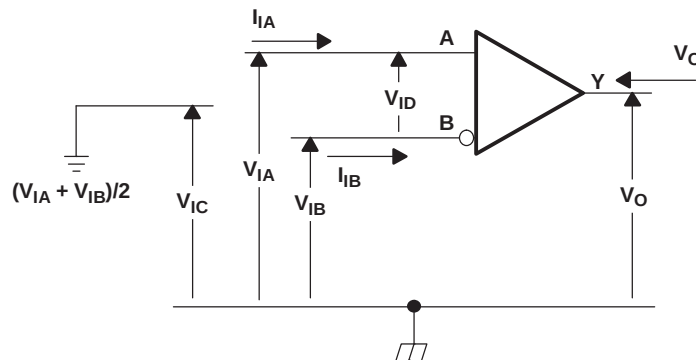
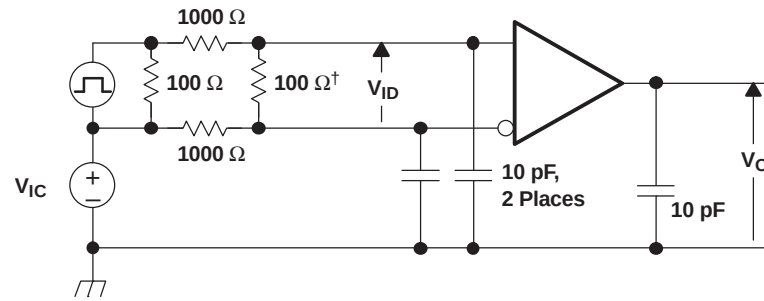
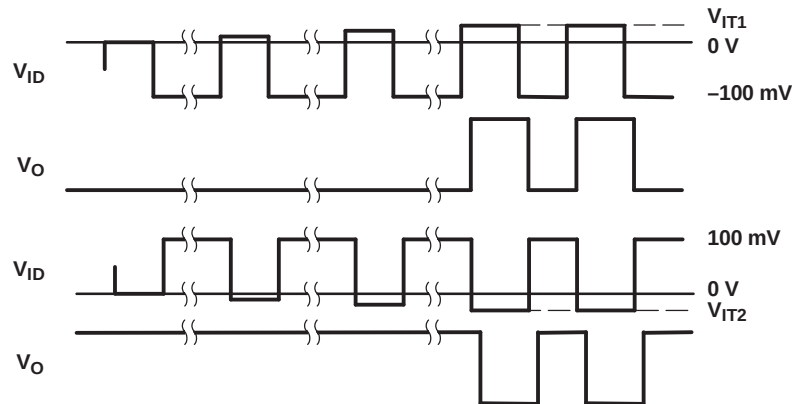


Figure 1. Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



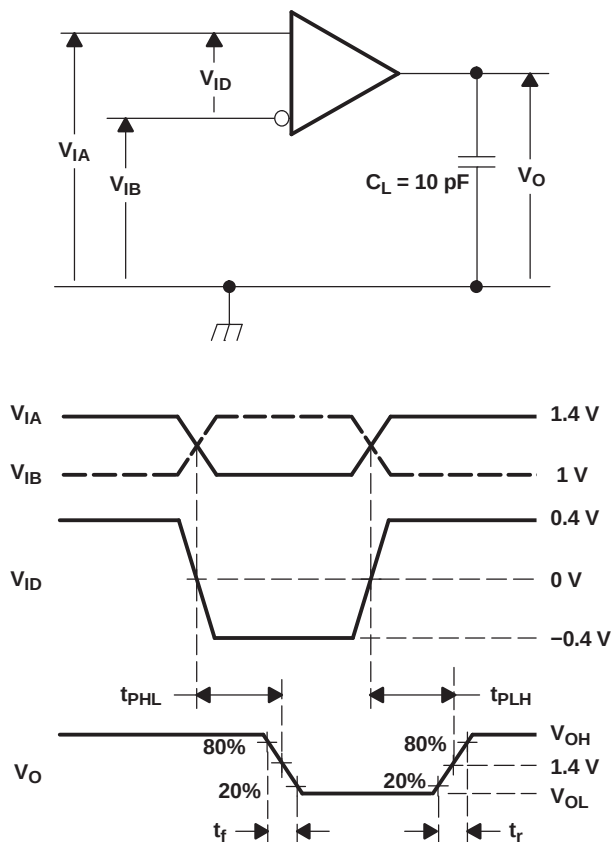
† Remove for testing LVDT device.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions

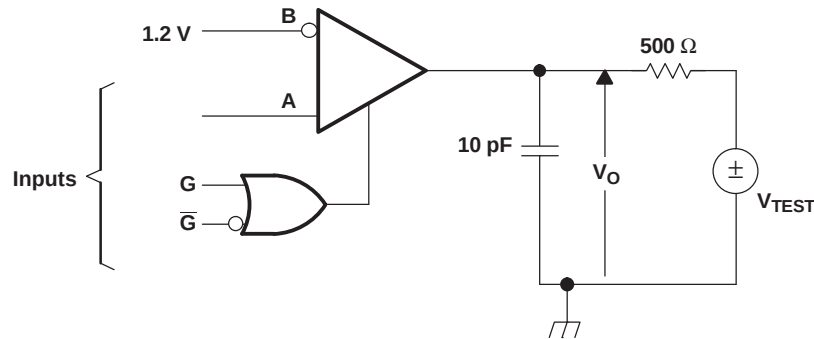
PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = $10 \pm 0.2 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

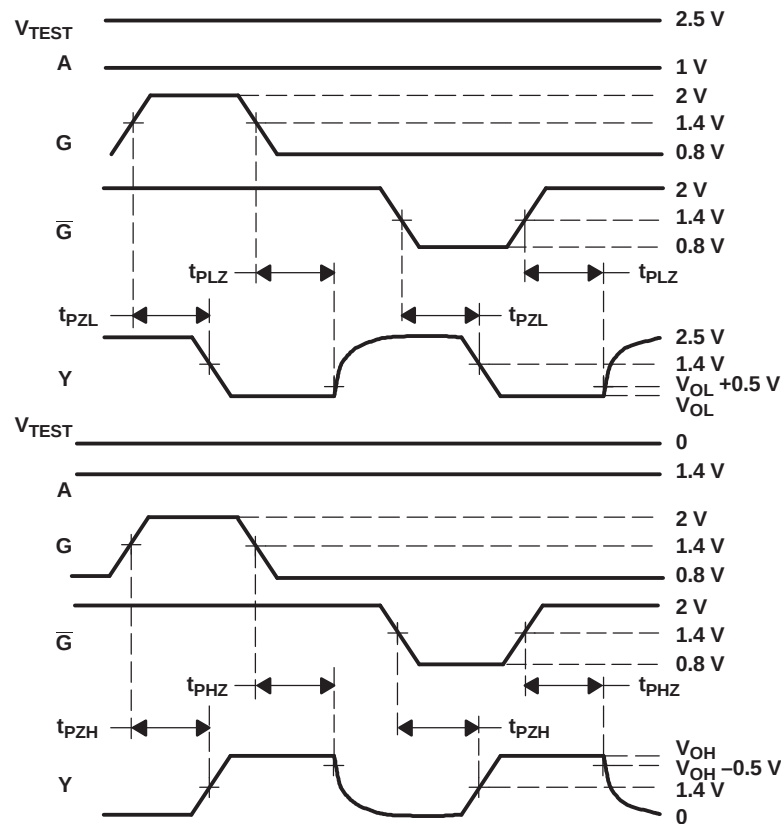
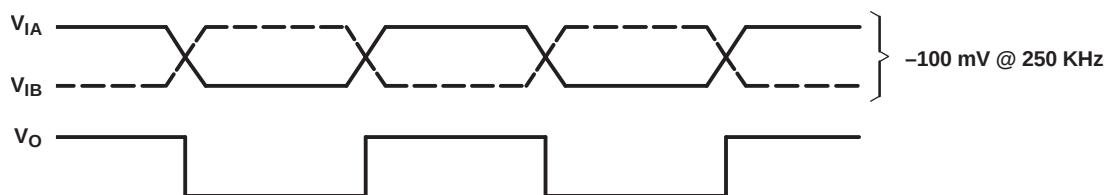


Figure 4. Enable/Disable Time Test Circuit and Waveforms

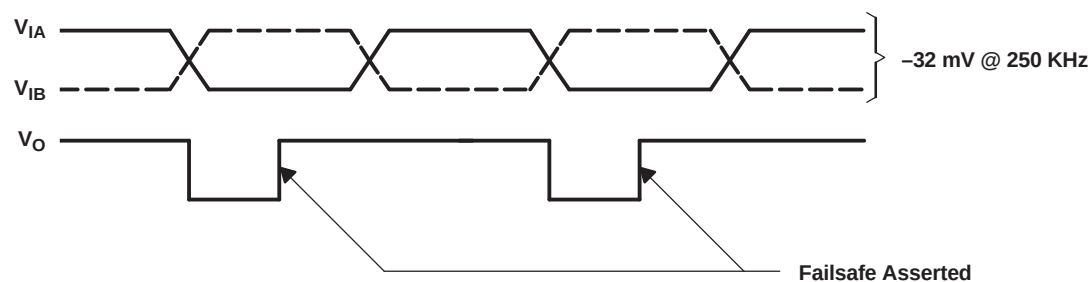
Table 2. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES ⁽¹⁾		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
-4000	-3900	-100	-3950	L
-4000	-3968	-32	-3984	H
4900	5000	-100	4950	L
4968	5000	-32	4984	H

(1) These voltages are applied for a minimum of 1.5 μ s.



a) No Failsafe



b) Failsafe Asserted

Figure 5. V_{IT3} Failsafe Threshold Test

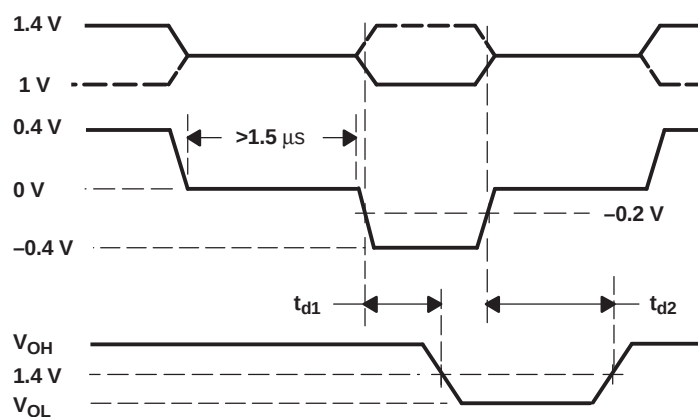


Figure 6. Waveforms for Failsafe Activate and Deactivate

TYPICAL CHARACTERISTICS

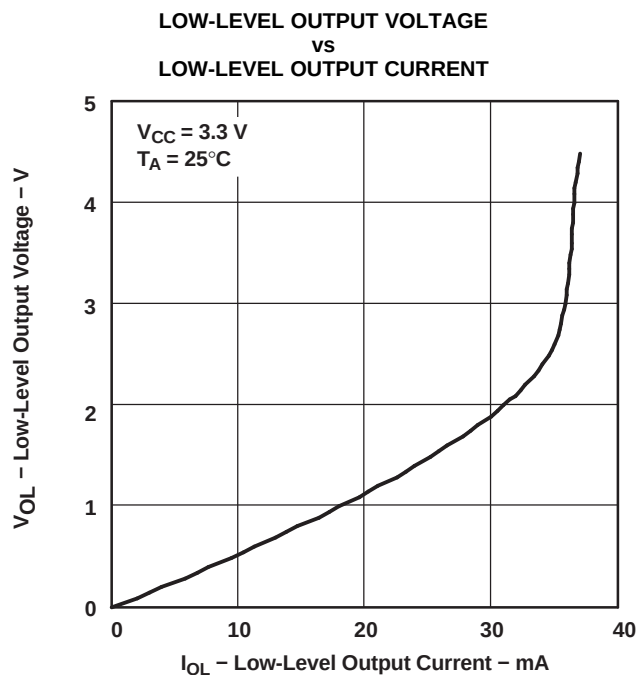


Figure 7.

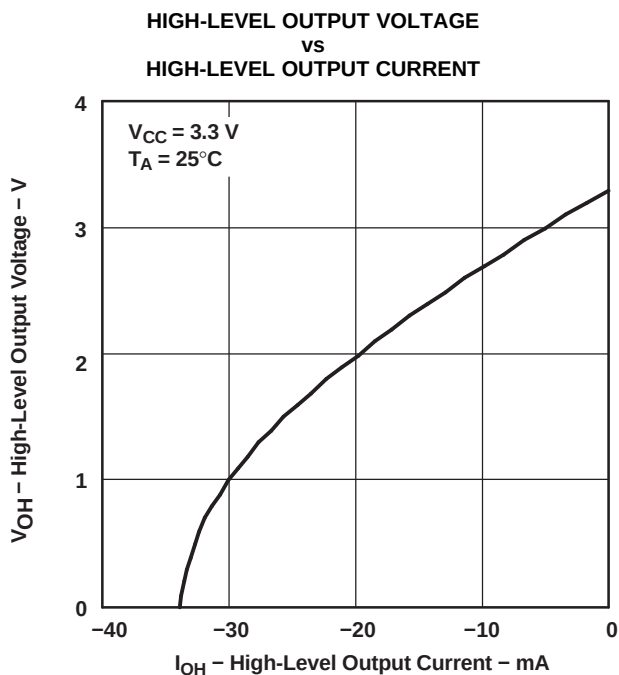


Figure 8.

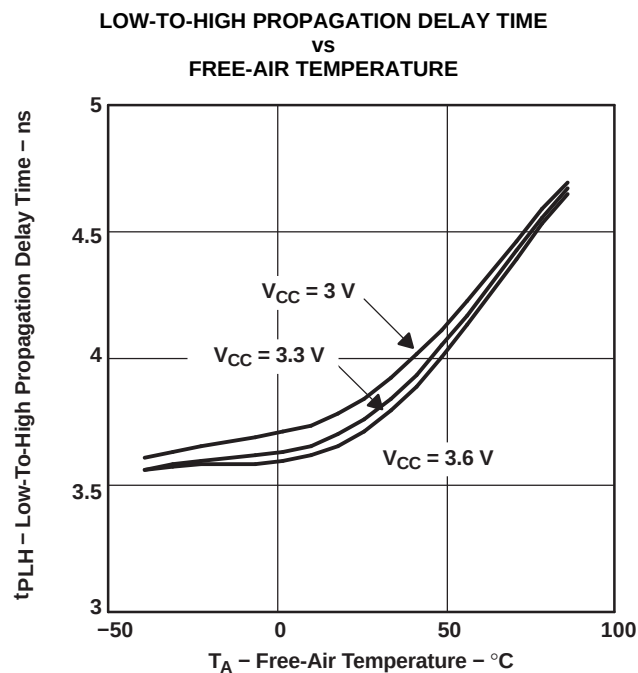


Figure 9.

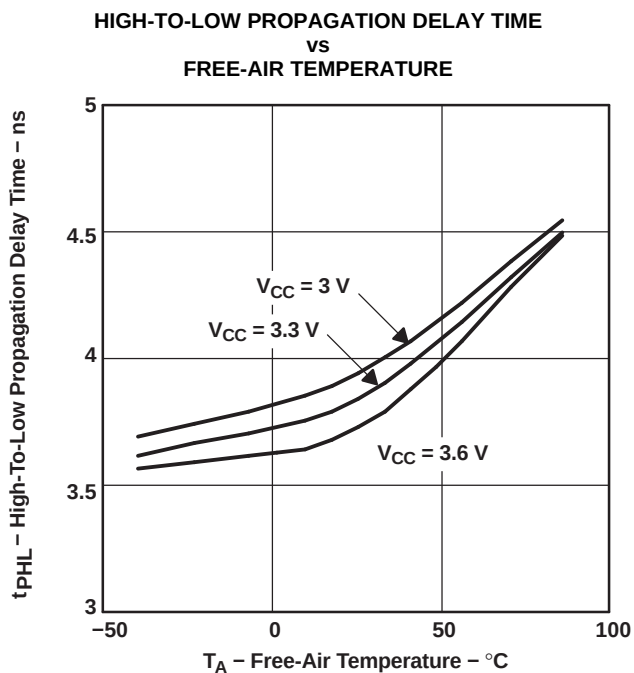


Figure 10.

TYPICAL CHARACTERISTICS (continued)

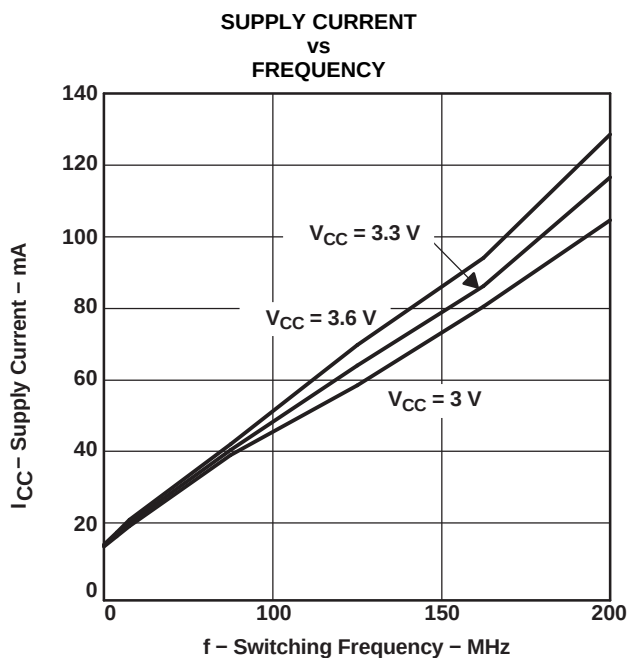
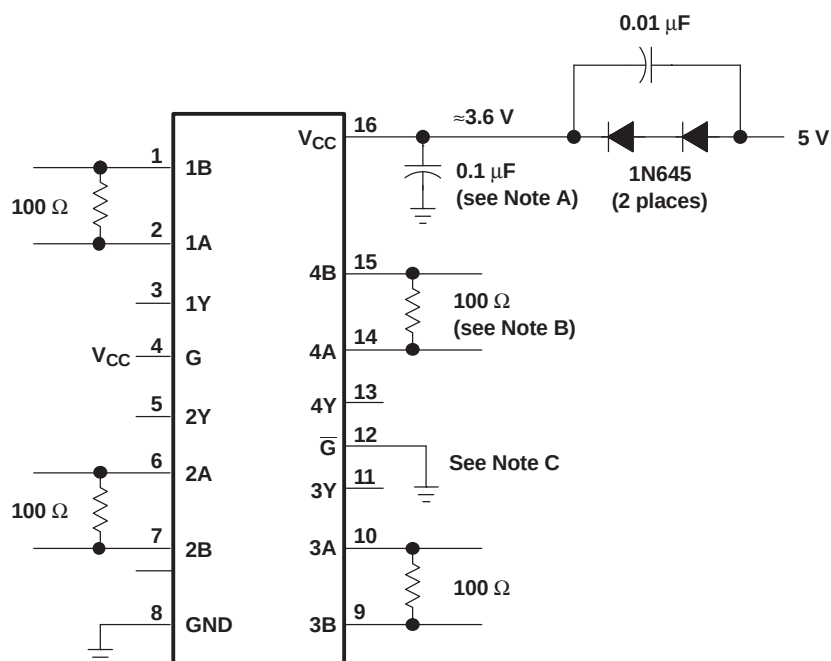


Figure 11.

APPLICATION INFORMATION



- Place a 0.1-μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- The termination resistance value should match the nominal characteristic impedance of the transmission media with $\pm 10\%$.
- Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation With 5-V Supply

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signalling Design Notes* ([SLLA014](#))
- *Interface Circuits for TIA/EIA-644 (LVDS)* ([SLLA038](#))
- *Reducing EMI With LVDS* ([SLLA030](#))
- *Slew Rate Control of LVDS Circuits* ([SLLA034](#))
- *Using an LVDS Receiver With RS-422 Data* ([SLLA031](#))
- *Evaluating the LVDS EVM* ([SLLA033](#))

ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Failsafe Feature of the SN65LVDS32B*, ([SLLA082A](#)).

The following figure shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

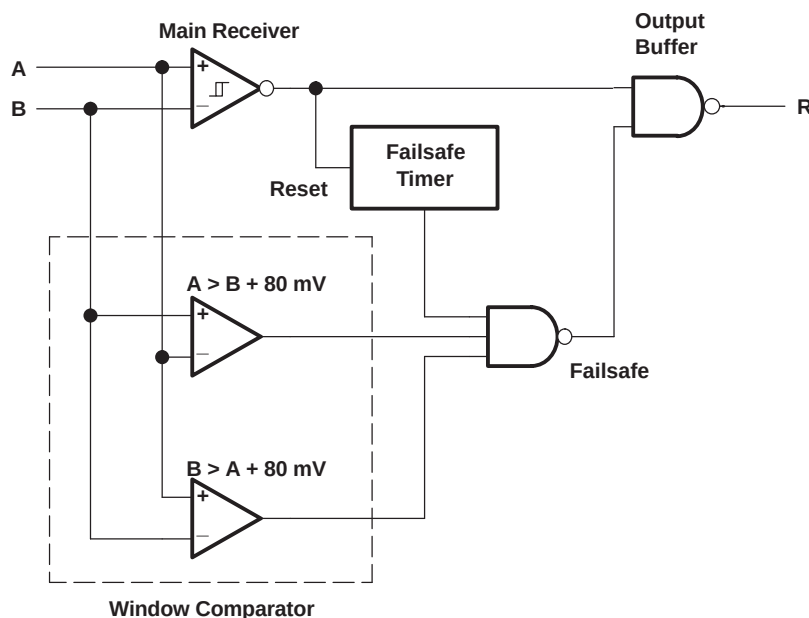


Figure 13. Receiver With Active Failsafe

ECL/PECL-TO-LVTTL CONVERSION WITH TI'S LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like

LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination ($V_{CC}-2\text{ V}$).

Figure 14 and Figure 15 show the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of $50\ \Omega$. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

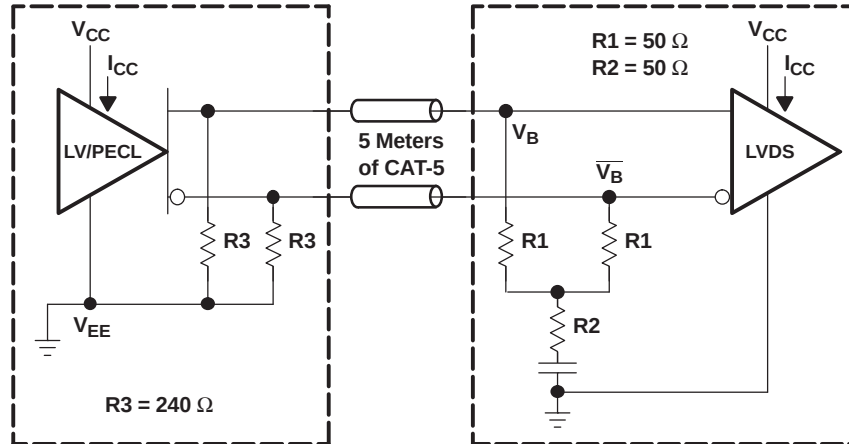


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

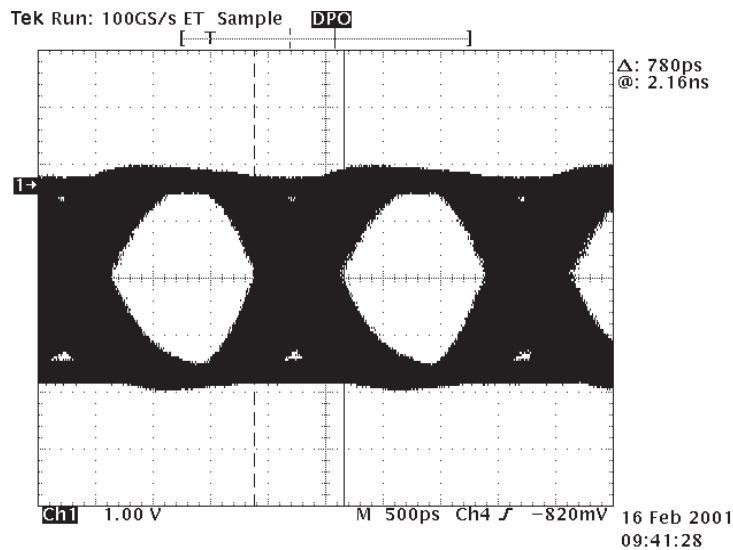


Figure 15. LV/PECL to Remote SN65LVDS33 at 500 Mbps Receiver Output (CH1)

TEST CONDITIONS

- $V_{CC} = 3.3\text{ V}$
- $T_A = 25^\circ\text{C}$ (ambient temperature)
- All four channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data.

EQUIPMENT

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

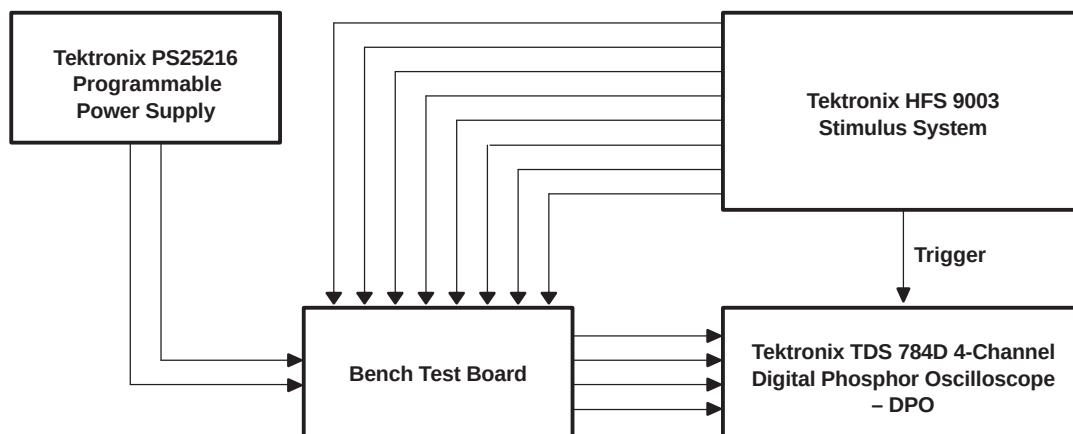


Figure 16. Equipment Setup

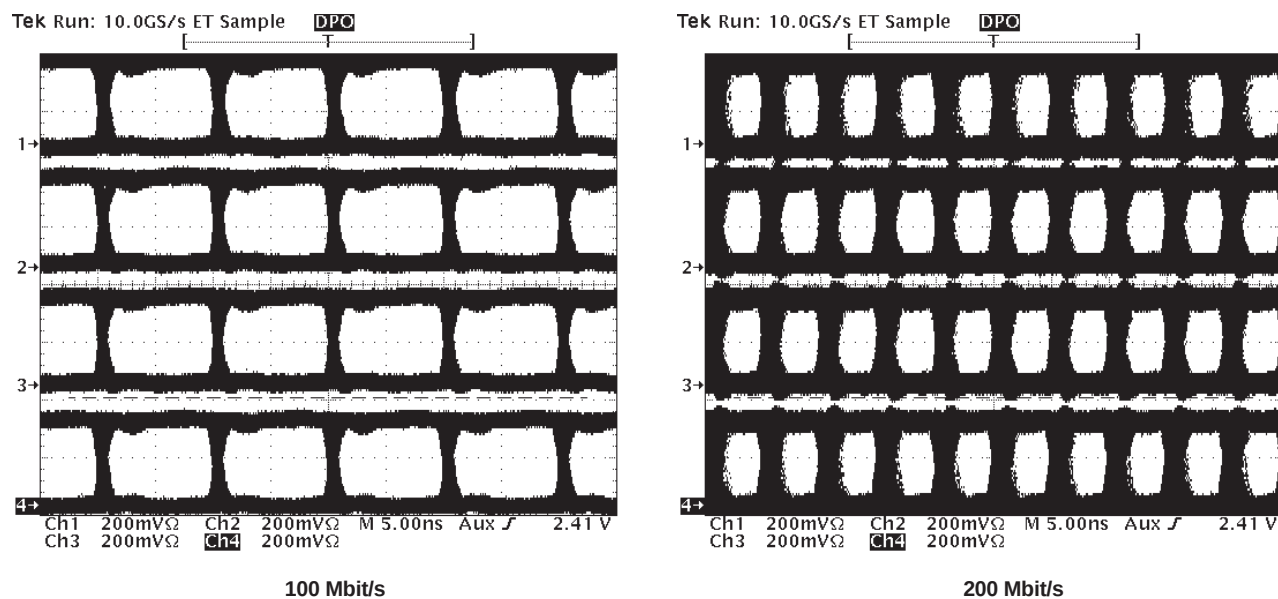


Figure 17. Typical Eye Pattern SN65LVDS33

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS33D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33D.B	Active	Production	null (null)	40 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS33D	LVDS33
SN65LVDS33DG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33DR.B	Active	Production	null (null)	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS33DR	LVDS33
SN65LVDS33DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33PW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33PW.B	Active	Production	null (null)	90 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS33PW	LVDS33
SN65LVDS33PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33
SN65LVDS33PWR.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS33PWR	LVDS33
SN65LVDS34D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34
SN65LVDS34D.B	Active	Production	null (null)	75 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS34D	LVDS34
SN65LVDS34DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34
SN65LVDS34DR.B	Active	Production	null (null)	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDS34DR	LVDS34
SN65LVDS34DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34
SN65LVDT33D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33
SN65LVDT33D.B	Active	Production	null (null)	40 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT33D	LVDT33
SN65LVDT33DG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33
SN65LVDT33PW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33
SN65LVDT33PW.B	Active	Production	null (null)	90 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT33PW	LVDT33
SN65LVDT33PWG4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33
SN65LVDT33PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33
SN65LVDT33PWR.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT33PWR	LVDT33
SN65LVDT33PWRG4.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT33PWRG4	LVDT33
SN65LVDT34D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34
SN65LVDT34D.B	Active	Production	null (null)	75 TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT34D	LVDT34
SN65LVDT34DG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34
SN65LVDT34DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDT34DR.B	Active	Production	null (null)	2500 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65LVDT34DR	LVDT34

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65LVDS33 :

- Enhanced Product : [SN65LVDS33-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

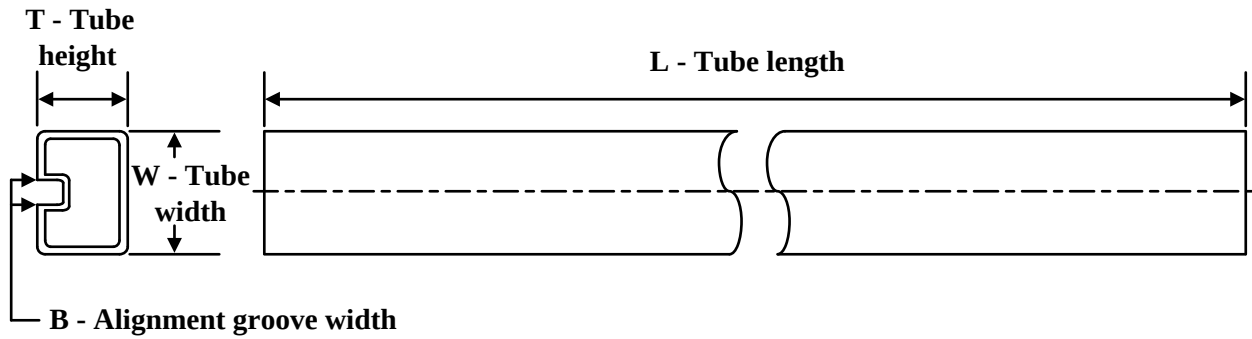
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS33DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS33PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS34DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT33PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT34DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS33DR	SOIC	D	16	2500	353.0	353.0	32.0
SN65LVDS33PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS34DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVDT33PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDT34DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE


*All dimensions are nominal

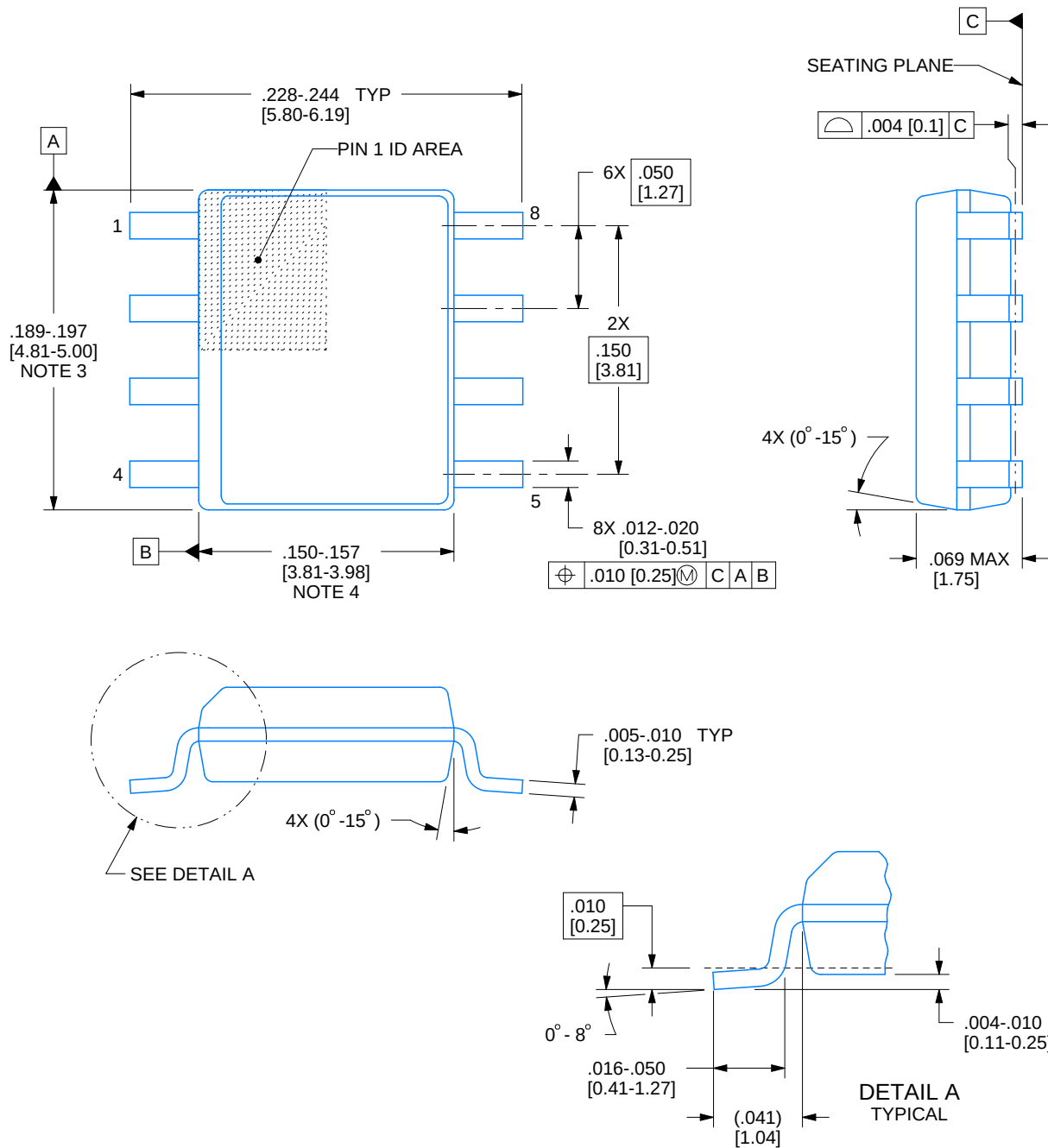
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDS33D	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS33DG4	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS33PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS34D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS34D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT33D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDT33DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDT33PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDT33PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDT34D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDT34D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT34DG4	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT34DG4	D	SOIC	8	75	505.46	6.76	3810	4

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

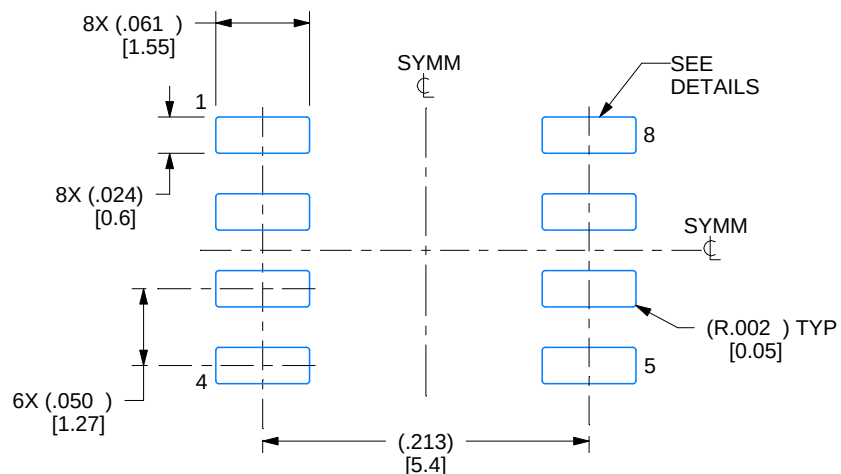
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

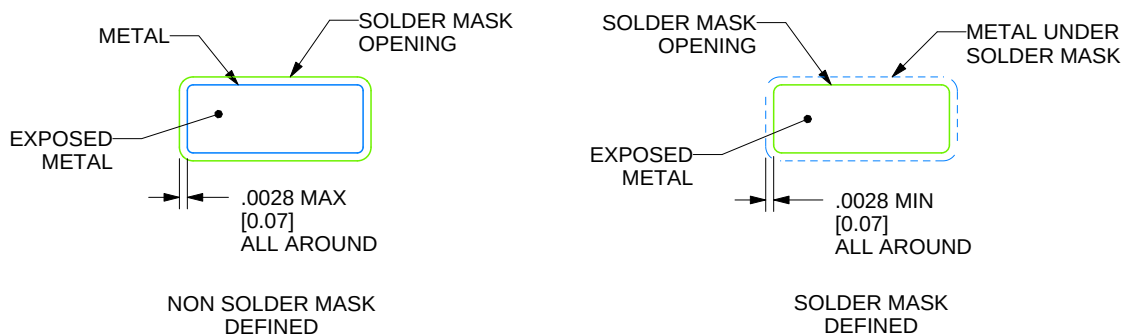
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

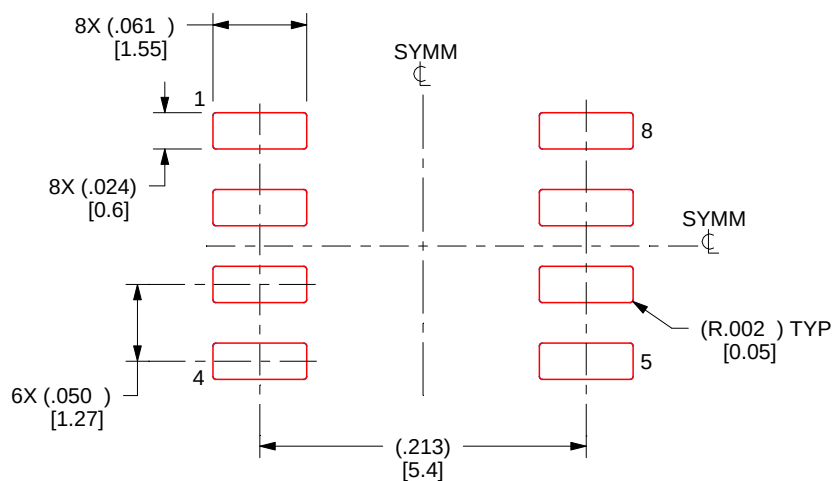
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

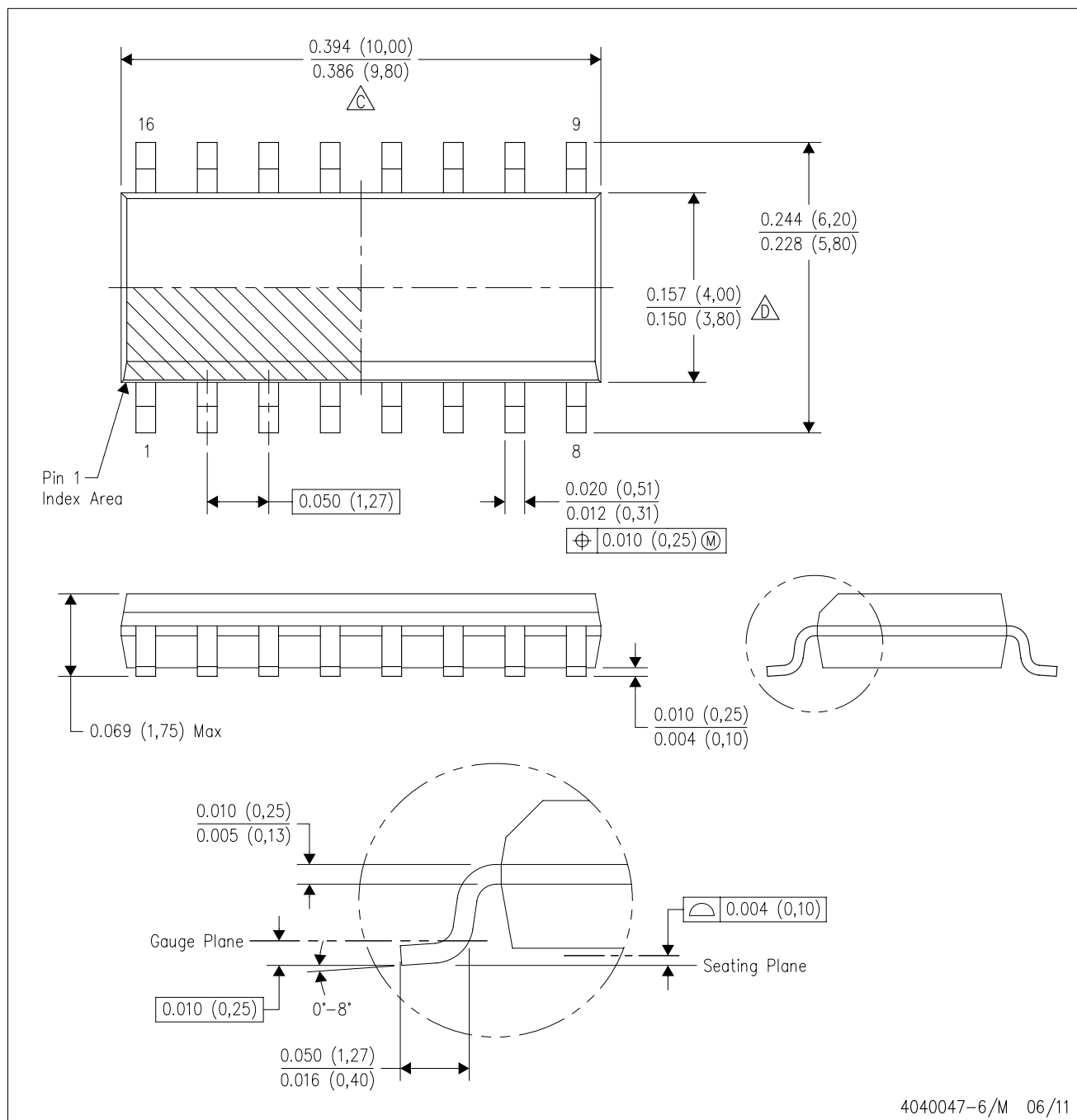
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

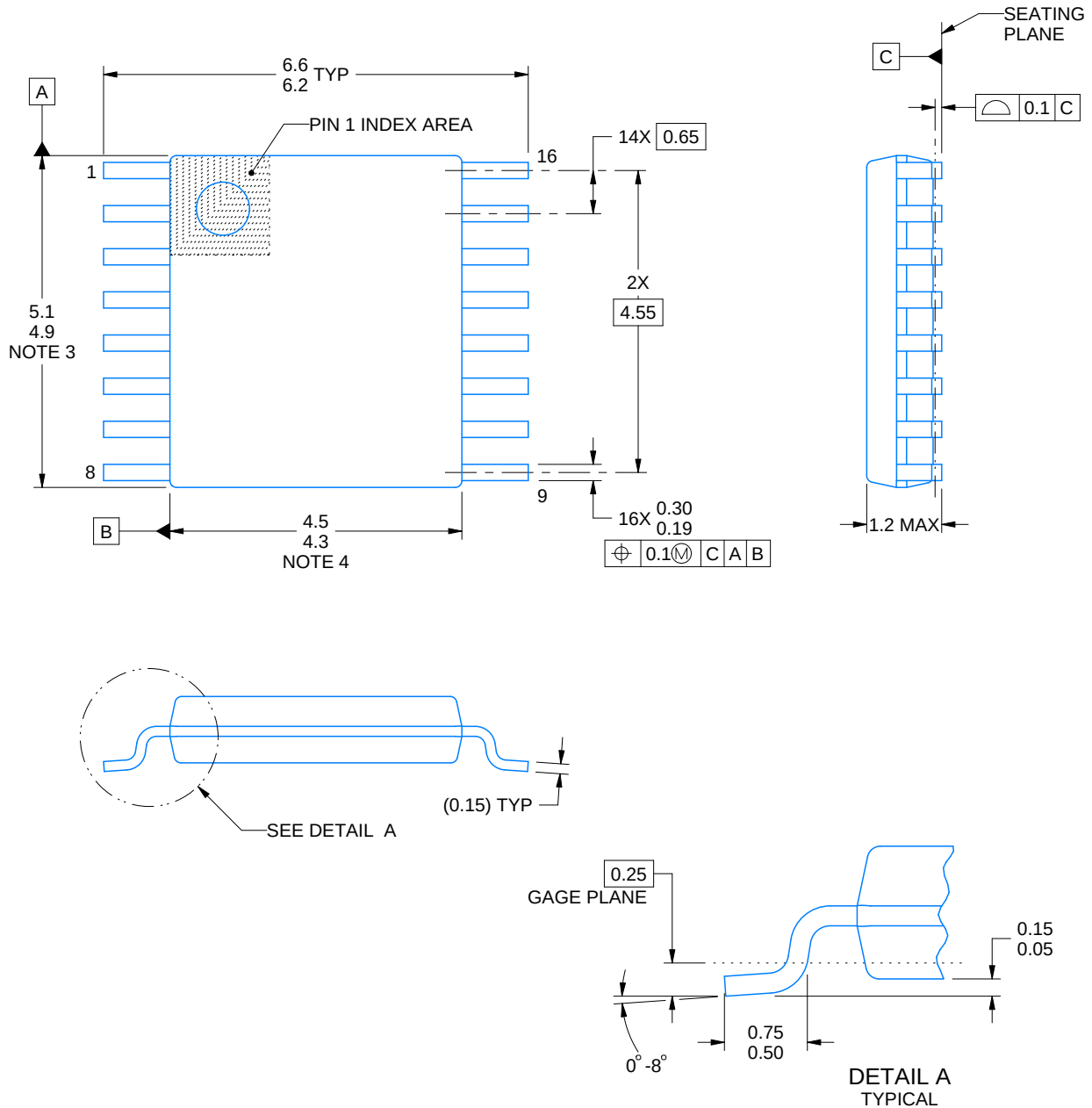
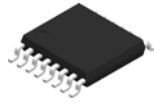
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

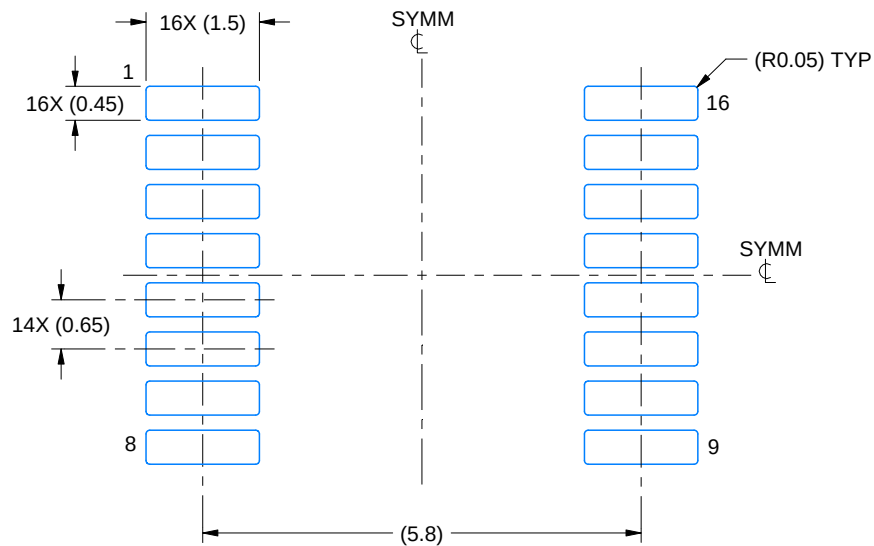
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

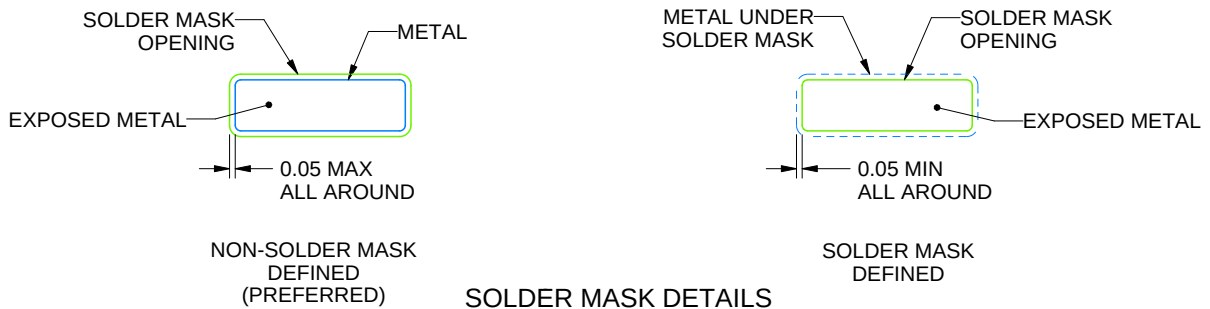
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

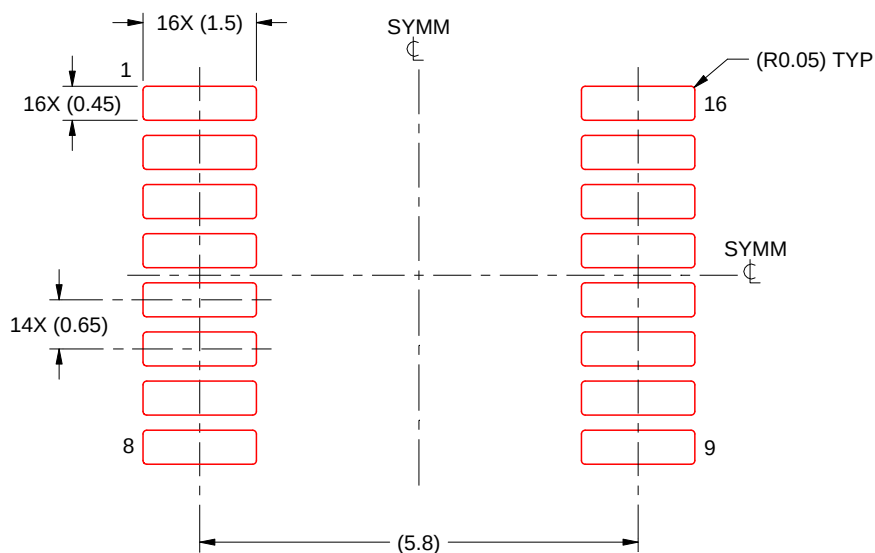
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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