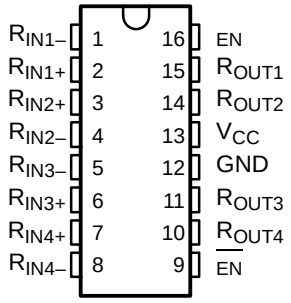
LVDS QUAD DIFFERENTIAL LINE RECEIVER

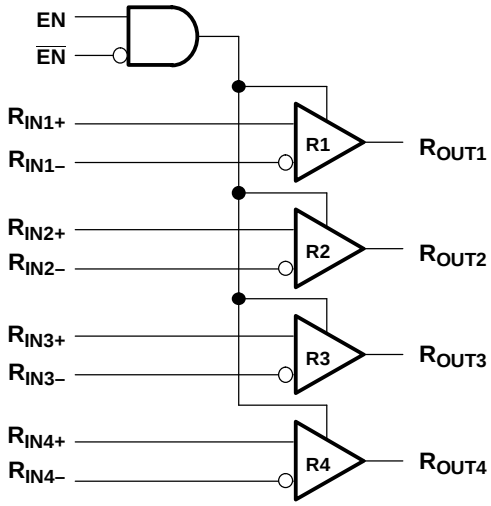
FEATURES

- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **50 ps Channel-to-Channel Skew (Typ)**
- **200 ps Differential Skew (Typ)**
- **Propagation Delay Times 2.7 ns (Typ)**
- **3.3-V Power Supply Design**
- **High Impedance LVDS Inputs on Power Down**
- **Low-Power Dissipation (40 mW at 3.3 V Static)**
- **Accepts Small Swing (350 mV) Differential Signal Levels**
- **Supports Open, Short, and Terminated Input Fail-Safe**
- **Industrial Operating Temperature Range (–40°C to 85°C)**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Available in SOIC and TSSOP Packages**
- **Pin-Compatible With DS90LV048A From National**

SN65LVDS048AD (Marked as LVDS048A)
SN65LVDS048APW (Marked as DL048A)
(TOP VIEW)



functional diagram



DESCRIPTION

The SN65LVDS048A is a quad differential line receiver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the quad differential receivers will provide a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS048A is characterized for operation from –40°C to 85°C.

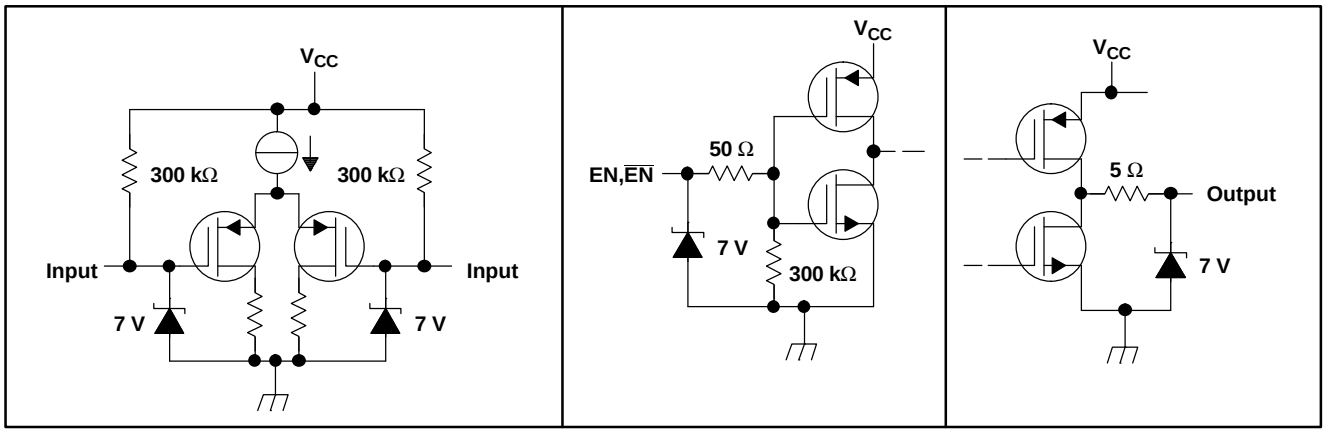
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TRUTH TABLE(1)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
$R_{IN+} - R_{IN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq 100$ mV	H	L or OPEN	H
$V_{ID} \leq -100$ mV			L
Open/short or terminated			H
X	All other conditions		Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		UNIT
V_{CC}	Supply voltage range	–0.3 V to 4 V
$V_I(R_{IN+}, R_{IN-})$	Input voltage range	–0.3 V to 4 V
	Enable input voltage (EN, $\overline{EN}$)	–0.3 V to (V_{CC} +0.3 V)
$V_O(R_{OUT})$	Output voltage	–0.3 V to (V_{CC} +0.3 V)
	Bus-pin (R_{IN+}, R_{IN-}) electrostatic discharge(3)	> 10 kV
	Continuous power dissipation	See Dissipation Rating Table
	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Receiver input voltage	GND		3	V
V_{IC}	Common-mode input voltage	$\frlvert V_{ID} \frrvert / 2$		$2.4 - \frlvert V_{ID} \frrvert / 2$	V
				V_{CC}– 0.8	
T_A	Operating free-air temperature	–40	25	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IT+}	Differential input high threshold voltage	V_{CM} = 1.2 V, 0.05 V, 2.35 V(3)				100	mV
V_{IT-}	Differential input low threshold voltage			–100			
$V_{(CMR)}$	Common mode voltage range	V_{ID} = 200 mV pk to pk(4)		0.1		2.3	V
I_{IN}	Input current	V_{IN} = 2.8 V	V_{CC} = 3.6 V or 0 V	–20	±1	20	µA
		V_{IN} = 0 V		–20	±1	20	µA
		V_{IN} = 3.6 V,	V_{CC} = 0 V	–20	±1	20	µA
V_{OH}	Output high voltage	I_{OH} = -0.4 mA, V_{ID} = 200 mV		2.7	3.2		V
		I_{OH} = -0.4 mA, input terminated		2.7	3.2		V
		I_{OH} = -0.4 mA, input shorted		2.7	3.2		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = -200 mV			0.05	0.25	V
I_{OS}	Output short circuit current	Enabled, V_{OUT} = 0 V(5)			–65	–100	mA
$I_{O(Z)}$	Output 3-state current	Disabled, V_{OUT} = 0 V or V_{CC}		–1		1	µA
V_{IH}	Input high voltage			2.0		V_{CC}	V
V_{IL}	Input low voltage			GND		0.8	V
I_I	Input current (enables)	V_{IN} = 0 V or V_{CC}, Other input = V_{CC} or GND		–10		10	µA
V_{IK}	Input clamp voltage	I_{CL} = –18 mA		–1.5	–0.8		V
I_{CC}	No load supply current, receivers enabled	EN = V_{CC}, Inputs open			8	15	mA
$I_{CC(Z)}$	No load supply current, receivers disabled	EN = GND, Inputs open			0.6	1.5	mA

(1) Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.
(2) All typical values are at 25°C and with a 3.3-V supply.
(3) V_{CC} is always higher than R_{IN+} and R_{IN-} voltage, R_{IN-} and R_{IN+} have a voltage range of -0.2 V to V_{CC}-V_{ID}/2. To be compliant with ac specifications the common voltage range is 0.1 V to 2.3 V.
(4) The VCMR range is reduced for larger V_{ID}, Example: If V_{ID} = 400 mV, the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V, but is supported only with inputs shorted and no external common-mode voltage applied. A V_{ID} up to V_{CC}-0 V may be applied to the R_{IN+} and R_{IN-} inputs with the common-mode voltage set to V_{CC}/2. Propagation delay and differential pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV < V_{ID} < 800 mV over the common-mode range.
(5) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time. Do not exceed maximum junction temperature specification.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PHL}	Differential propagation delay, high-to-low	C_L = 15 pF, V_{ID} = 200 mV (see Figure 1 and Figure 2)	1.9	2.7	3.7	ns
t_{PLH}	Differential propagation delay, low-to-high		1.9	2.9	3.7	ns
$t_{SK(p)}$	Differential pulse skew (t_{PHLD} - t_{PLHD})(3)			200	450	ps
$t_{SK(o)}$	Differential channel-to-channel skew; same device(4)			50	500	ps
$t_{SK(pp)}$	Differential part-to-part skew(5)				1	ns
$t_{SK(lim)}$	Differential part-to-part skew(6)				1.5	ns
t_r	Rise time			0.5	1	ns
t_f	Fall time			0.5	1	ns
t_{PHZ}	Disable time high to Z	R_L = 2 K Ω, C_L = 15 pF (see Figure 3 and Figure 4)		8	9	ns
t_{PLZ}	Disable time low to Z			6	8	ns
t_{PZH}	Enable time Z to high			8	10	ns
t_{PZL}	Enable time Z to low			7	8	ns
$f_{(MAX)}$	Maximum operating frequency(7)	All channels switching	200	250		MHz

(1) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r and t_f (0%–100%) ≤ 3 ns for R_{IN}.
(2) All typical values are at 25°C and with a 3.3-V supply.
(3) $t_{SK(p)}|t_{PLH} - t_{PHL}|$ is the magnitude difference in differential propagation delay time between the positive going edge andthe negative going edge of the same channel.
(4) $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device.
(5) $t_{SK(pp)}$ is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same VCC and within 5°C of each other within the operating temperature range.
(6) $t_{sk(lim)}$ part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{sk(lim)}$ is defined as |Min - Max| differential propagation delay.
(7) $f_{(MAX)}$ generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55%,V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

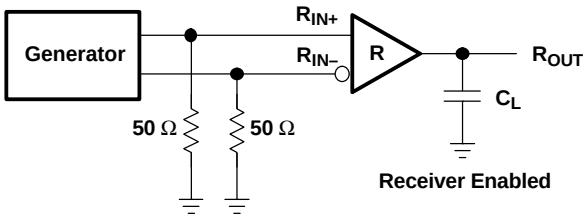


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

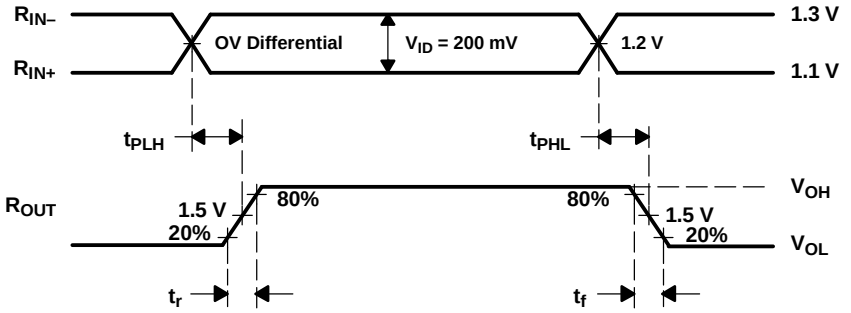
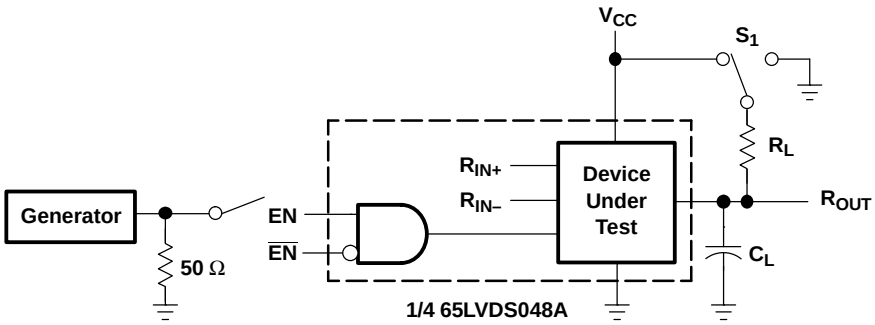


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



C_L Includes Load and Test Jig Capacitance.
$S_1 = V_{CC}$ for t_{PZL} and t_{PLZ} Measurements.
S_1 = GND for t_{PZH} and t_{PHZ} Measurements.

Figure 3. Receiver 3-State Delay Test Circuit

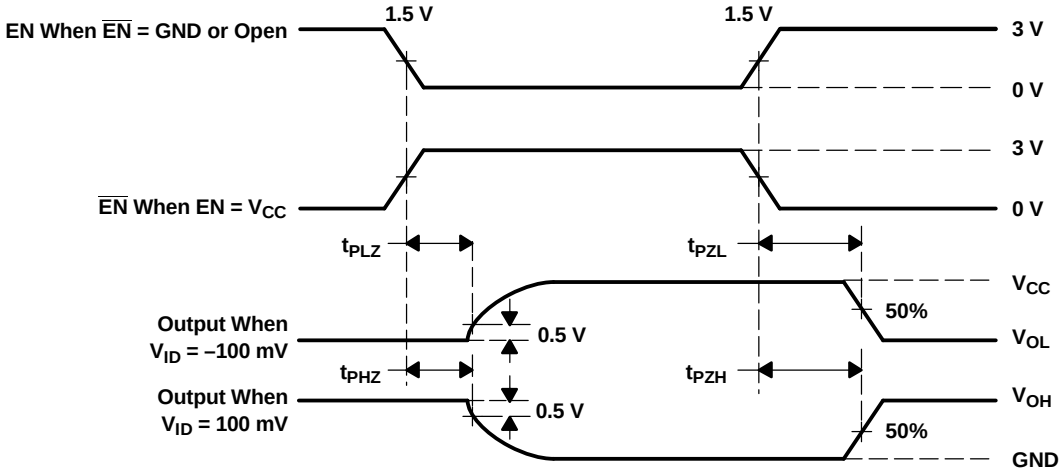


Figure 4. Receiver 3-State Delay Waveforms

TYPICAL CHARACTERISTICS

OUTPUT HIGH VOLTAGE
vs
POWER SUPPLY VOLTAGE

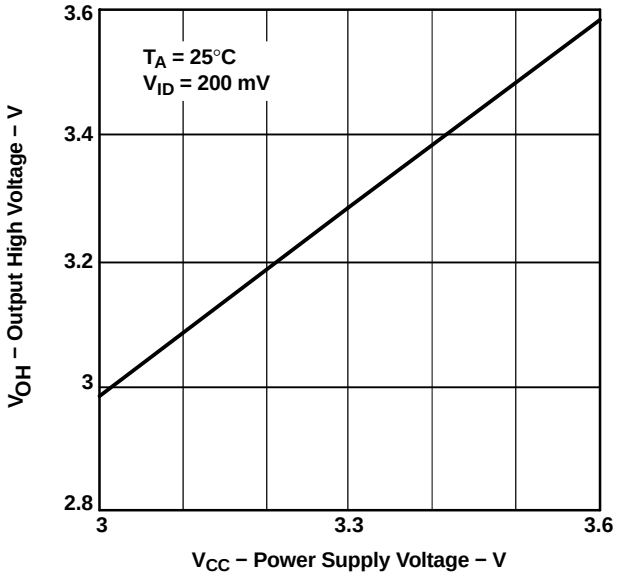


Figure 5.

OUTPUT LOW VOLTAGE
vs
POWER SUPPLY VOLTAGE

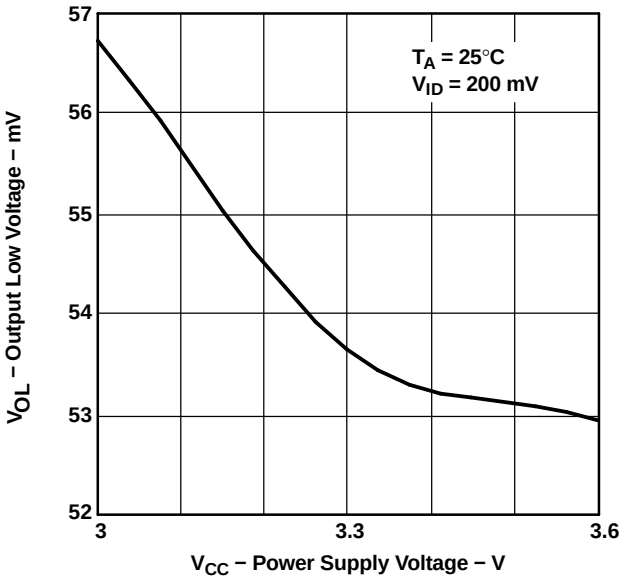


Figure 6.

OUTPUT SHORT CIRCUIT CURRENT
vs
POWER SUPPLY VOLTAGE

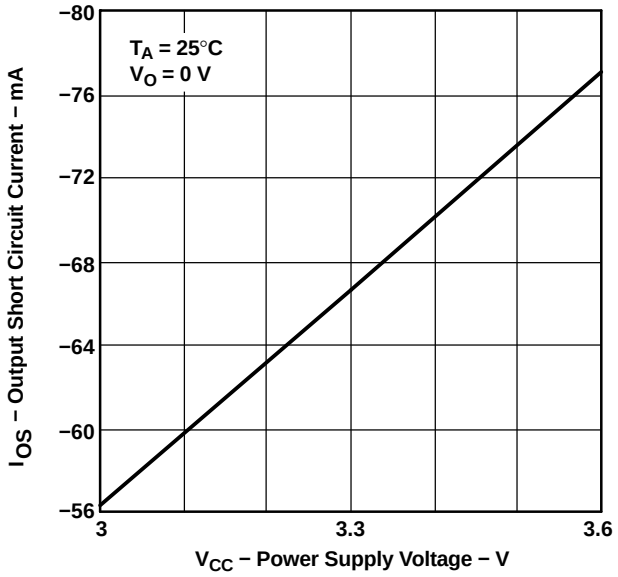


Figure 7.

DIFFERENTIAL TRANSITION VOLTAGE
vs
POWER SUPPLY VOLTAGE

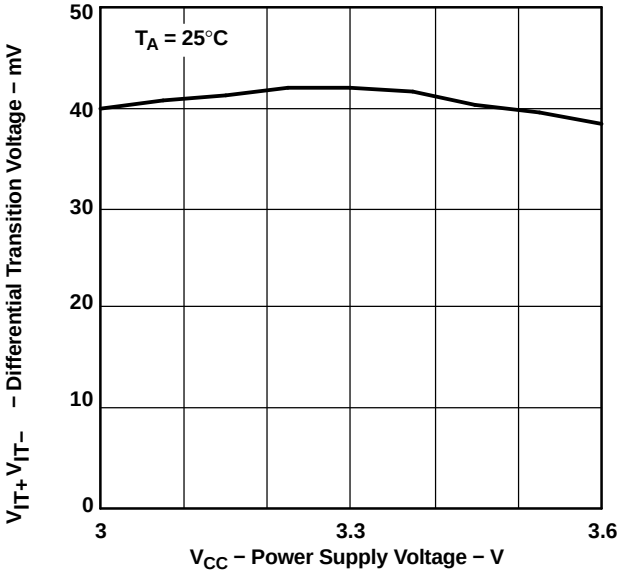


Figure 8.

TYPICAL CHARACTERISTICS (continued)

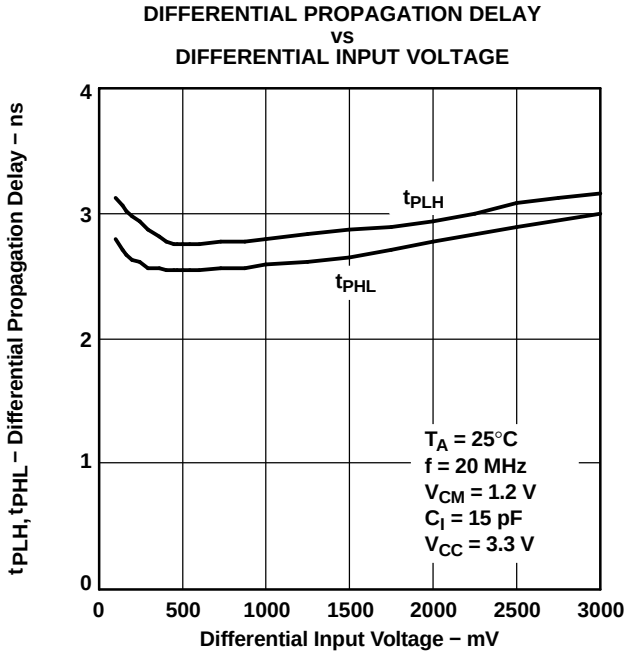


Figure 9.

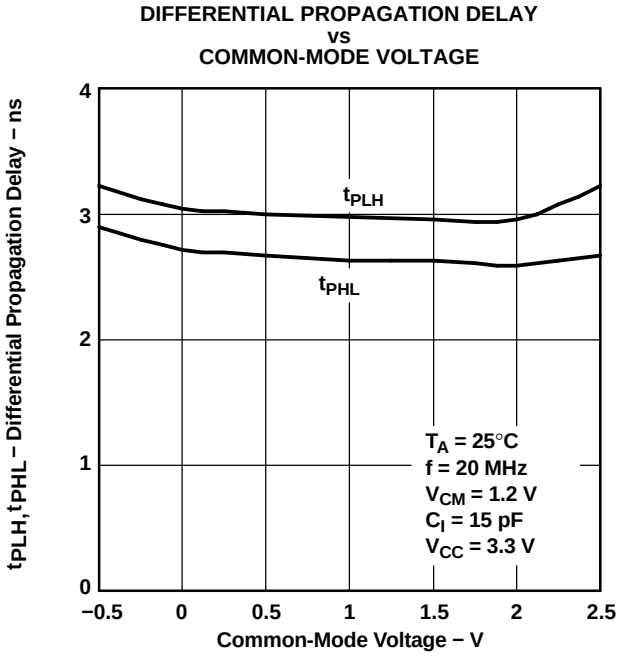


Figure 10.

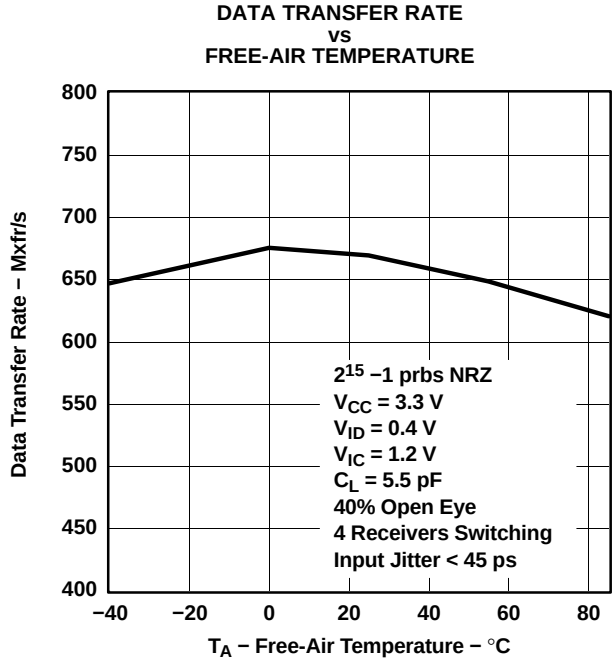


Figure 11.

APPLICATION INFORMATION

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

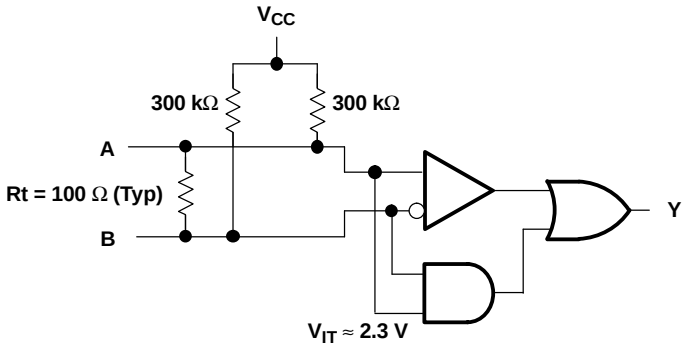


Figure 12. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS048AD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS048A
SN65LVDS048AD.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS048A
SN65LVDS048ADG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS048A
SN65LVDS048ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS048A
SN65LVDS048ADR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS048A
SN65LVDS048APW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A
SN65LVDS048APW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A
SN65LVDS048APWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A
SN65LVDS048APWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A
SN65LVDS048APWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A
SN65LVDS048APWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL048A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

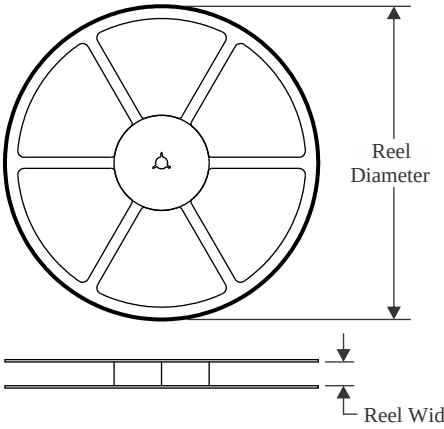
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

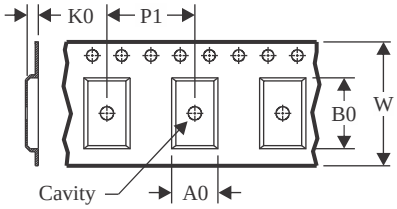
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

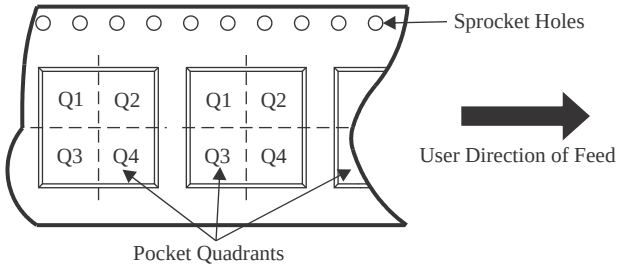


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

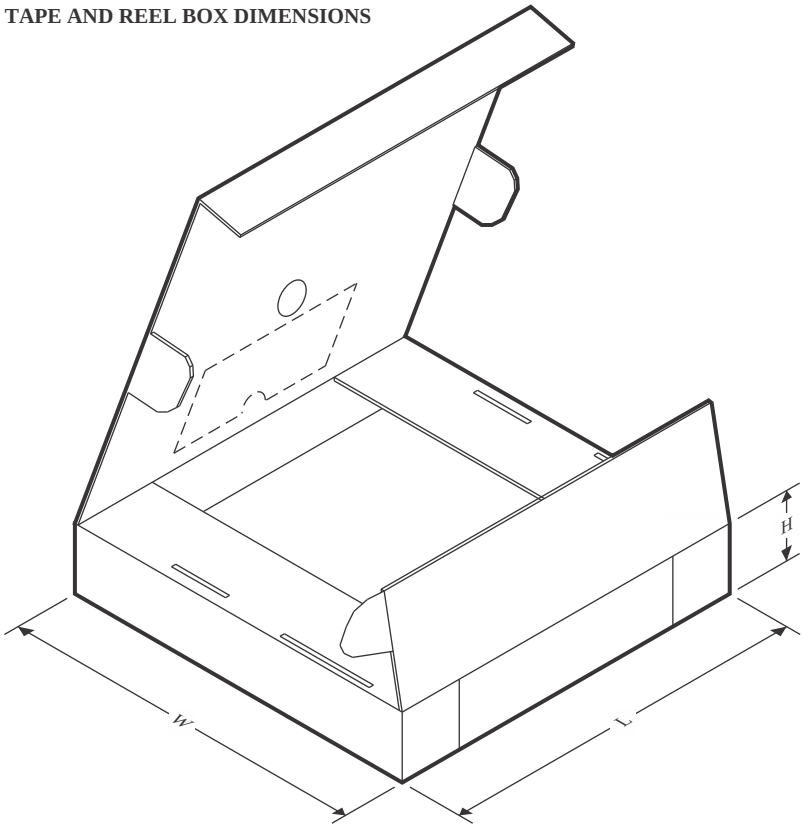
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS048ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS048APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

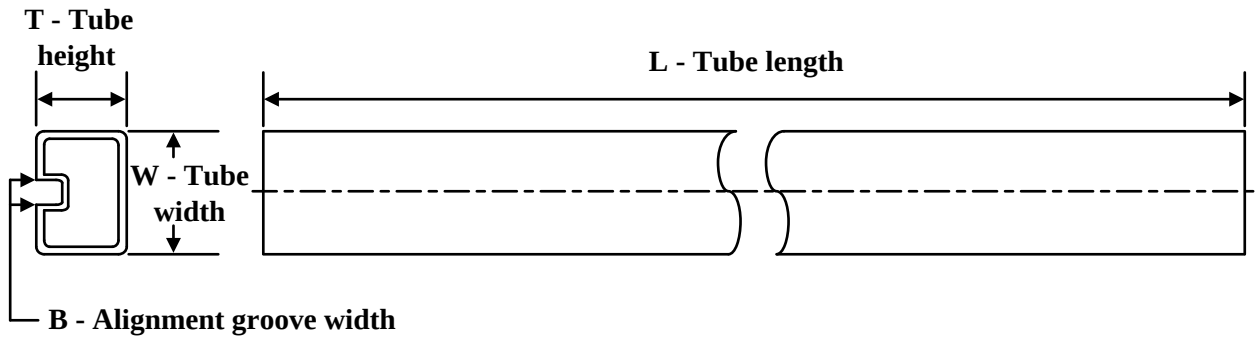
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS048ADR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS048APWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS048AD	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS048AD.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS048ADG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS048APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS048APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS048APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

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