LVDS QUAD DIFFERENTIAL LINE DRIVER

FEATURES

- **>400 Mbps (200 MHz) Signaling Rates**
- **Flow-Through Pinout Simplifies PCB Layout**
- **300 ps Maximum Differential Skew**
- **Propagation Delay Times 1.8 ns (Typical)**
- **3.3 V Power Supply Design**
- **±350 mV Differential Signaling**
- **High Impedance on LVDS Outputs on Power Down**
- **Conforms to TIA/EIA-644 LVDS Standard**
- **Industrial Operating Temperature Range (-40°C to 85°C)**
- **Available in SOIC and TSSOP Packages**

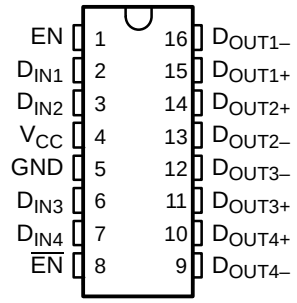
DESCRIPTION

The SN65LVDS047 is a quad differential linedriver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

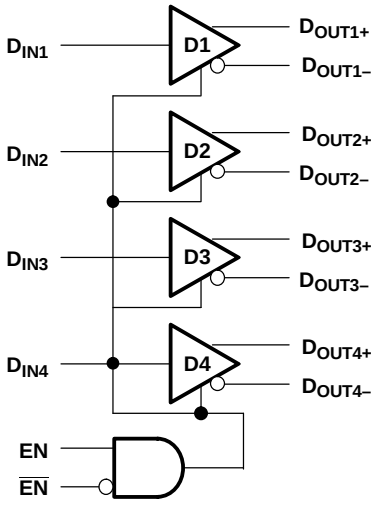
The intended application of this device and signaling technique is for point-to-point and multi-drop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS047 is characterized for operation from -40°C to 85°C.

D OR PW PACKAGE
(Marked as LVDS047)
(TOP VIEW)



functional block diagram



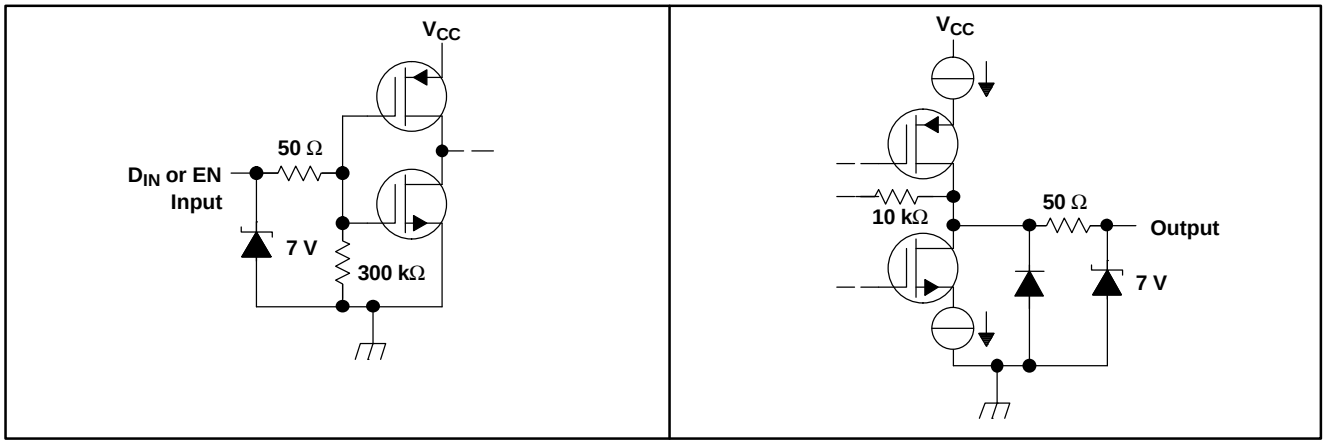
TRUTH TABLE(1)

INPUT	ENABLES		OUTPUTS	
D_{IN}	EN	$\overline{EN}$	D_{OUT+}	D_{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature (see (2) range (unless otherwise noted)

		UNIT
(V_{CC})	Supply voltage	-0.3 V to 4 V
V_I(D_{IN})	Input voltage range	-0.3 V to (V_{CC} +0.3 V)
(EN, $\overline{EN}$)	Enable input voltage	-0.3 V to (V_{CC} +0.3 V)
V_O(D_{OUT+},D_{OUT-})	Output voltage	-0.5 V to (V_{CC} +0.5 V)
(D_{OUT+},D_{OUT-})	Bus-pin--electrostatic discharge, see (3)	>10 kV
(D_{OUT+},(D_{OUT-})	Short circuit duration	Continuous
	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq$ 25°C POWER RATING	OPERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	-40	25	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (see (1) and (2)) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
V_{OD}	Differential output voltage	R_L = 100 Ω, see Figure 1	250	310	450	mV
$n\|V_{OD}\|$	Change in magnitude of V_{OD} for complementary output states			1	35	$\|mV\|$
$V_{OC(SS)}$	Steady-state, common-mode output voltage		1.125	1.17	1.375	V
$nV_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1	25	$\|mV\|$
V_{OH}	Output high voltage			1.33	1.6	V
V_{OL}	Output low voltage		0.90	1.02		V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		GND		0.8	V
I_{IH}	Input high current	V_{IN} = V_{CC} or 2.5 V	-10	3	10	µA
I_{IL}	Input low current	V_{IN} = GND or 0.4 V	-10	1	10	µA
V_{IK}	Input clamp voltage	I_{CL} = -18 mA	-1.5	-0.8		V
I_{OS}	Output short circuit current, see (4)	Enabled, D_{IN} = V_{CC}, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V		-3.1	-9	mA
I_{OSD}	Differential output short circuit current, see (4)	Enabled, V_{OD} = 0 V			-9	mA
I_{OFF}	Power-off leakage	V_O = 0 V or 3.6 V, V_{CC} = 0 V or Open	-1		1	µA
I_{OZ}	Output 3-state current	EN = 0.8 V and $\overline{EN}$ = 2 V, V_O = 0 V or V_{CC}	-1		1	µA
I_{CC}	No load supply current, drivers enabled	D_{IN} = V_{CC} or GND		7		mA
I_{CCL}	Loaded supply current, drivers enabled	R_L = 100 Ω all channels, D_{IN} = V_{CC} or GND (all inputs)		20	26	mA
$I_{CC(Z)}$	No load supply current, drivers disabled	D_{IN} = V_{CC} or GND, EN = GND, $\overline{EN}$ = V_{CC}		0.5	1.3	mA

(1) Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.
(2) The SN65LVDS047 is a current mode device and only functions within data sheet specifications when a resistive load is applied to the driver outputs, 90 Ω to 110 Ω typical range.
(3) All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (see (1), (2) and (3))(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(4)	MAX	UNIT
t_{PHL}	Differential propagation delay, high-to-low	R_L = 100 Ω,, C_L = 15 pF, see Figure 2 and Figure 3	1.4	1.8	2.8	ns
t_{PLH}	Differential propagation delay, low-to-high		1.4	1.8	2.8	ns
$t_{SK(p)}$	Differential pulse skew (t_{PHLD} - t_{PLHD}), see (5)			50	300	ps
$t_{SK(o)}$	Channel-to-channel skew, see (6)			40	300	ps
$t_{SK(pp)}$	Differential part-to-part skew, see (7)				1	ns
$t_{SK(lim)}$	Differential part-to-part skew, see (8)				1.2	ns
t_r	Rise time			0.5	1.5	ns
t_f	Fall time			0.5	1.5	ns
t_{PHZ}	Disable time high to Z	R_L = 100 Ω,, C_L = 15 pF, see Figure 4 and Figure 5		5.5	8	ns
t_{PLZ}	Disable time low to Z			5.5	8	ns
t_{PZH}	Enable time Z to high			8.5	12	ns
t_{PZL}	Enable time Z to low			8.5	12	ns
$f_{(MAX)}$	Maximum operating frequency, see (9)			250		MHz

(1) Generator waveform for all tests unless otherwise: f = 1 MHz, Z_o = 50 Ω, t_r < 1 ns, and t_f < 1 ns.
(2) C_L includes probe and jig capacitance.
(3) All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.
(4) All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.
(5) $t_{SK(p)}|t_{PHL}-t_{PLH}|$ is the magnitude difference in differential propagation delay time between the positive going edge andthe negative going edge of the same channel.
(6) $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device.
(7) $t_{SK(pp)}$ is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) $t_{SK(lim)}$ part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SK(lim)}$ is defined as|Min - Max| differential propagation delay.
(9) $f_{(MAX)}$ generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to55,V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

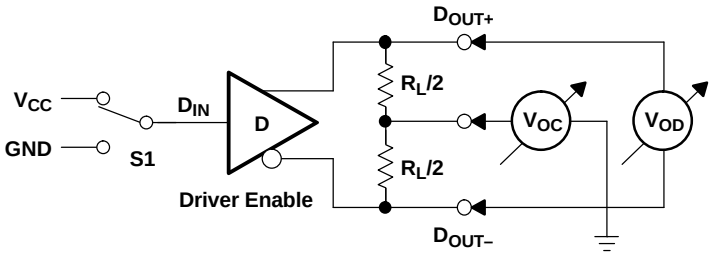


Figure 1. Driver V_{OD} and V_{OC} Test Circuit

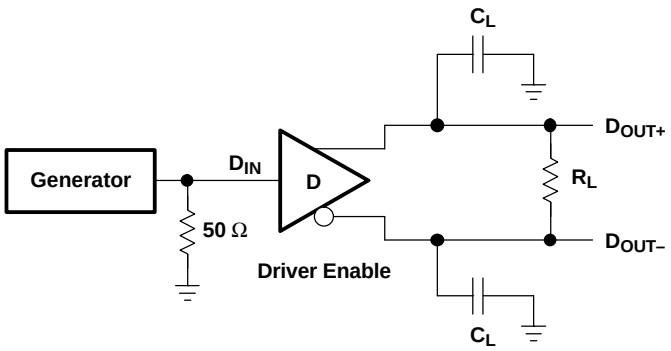


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

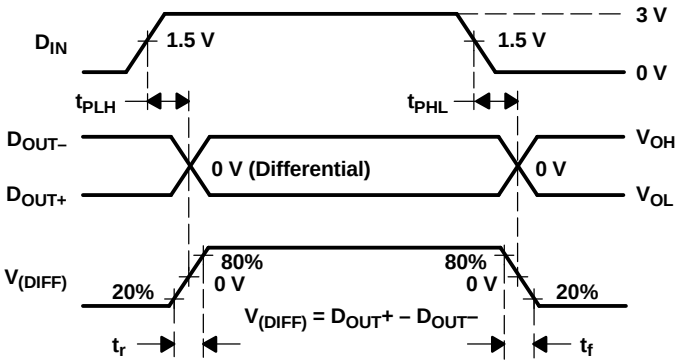


Figure 3. Driver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

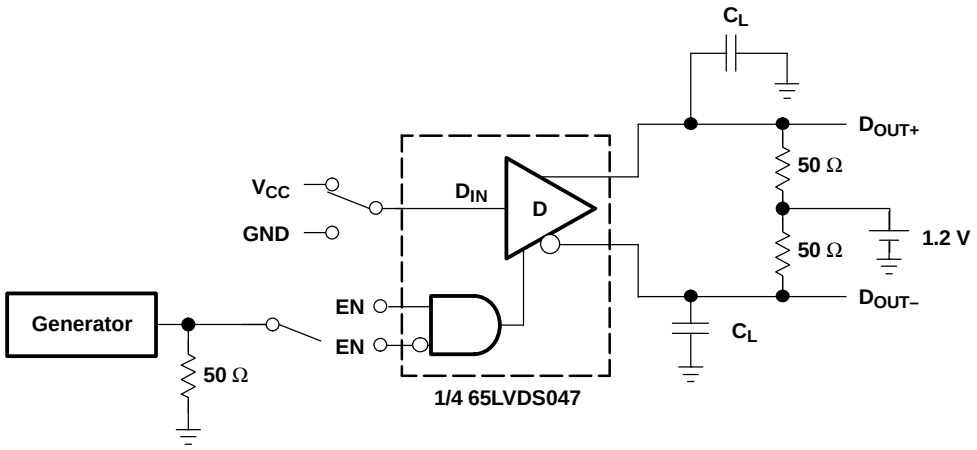


Figure 4. Driver 3-State Delay Test Circuit

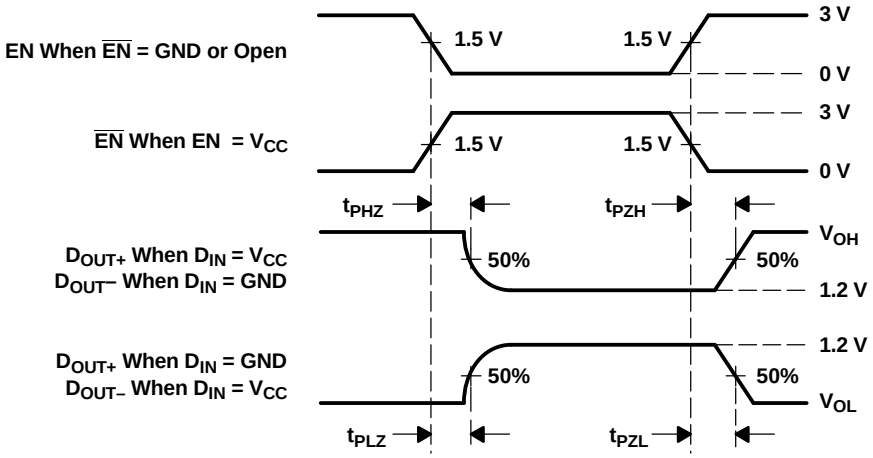


Figure 5. Driver 3-State Delay Waveform

TYPICAL CHARACTERISTICS

OUTPUT HIGH VOLTAGE
vs
POWER SUPPLY VOLTAGE

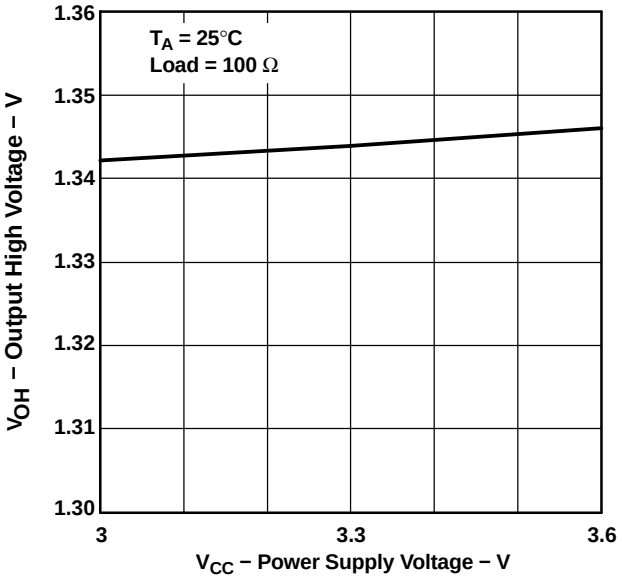


Figure 6.

OUTPUT LOW VOLTAGE
vs
POWER SUPPLY VOLTAGE

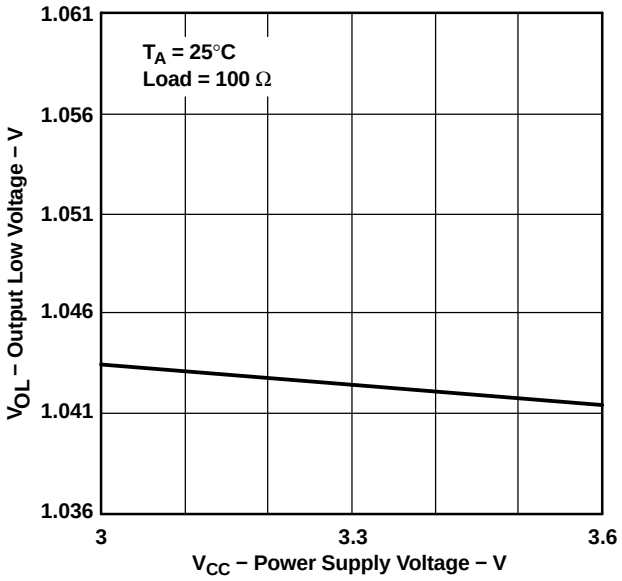


Figure 7.

OUTPUT SHORT CIRCUIT CURRENT
vs
POWER SUPPLY VOLTAGE

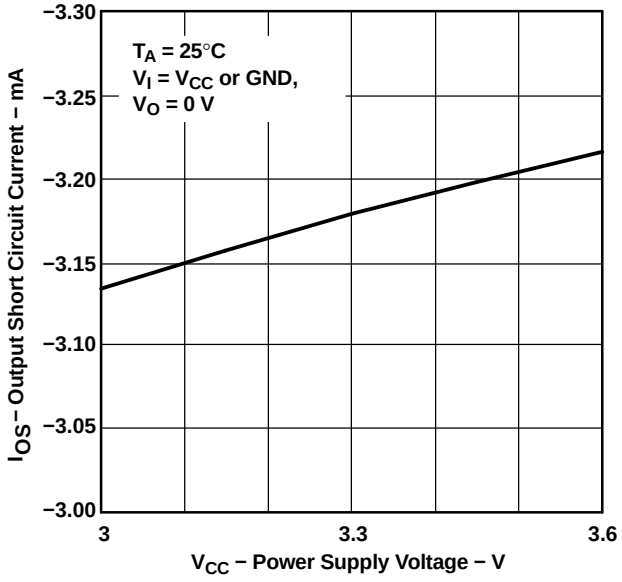


Figure 8.

DIFFERENTIAL OUTPUT VOLTAGE
vs
POWER SUPPLY VOLTAGE

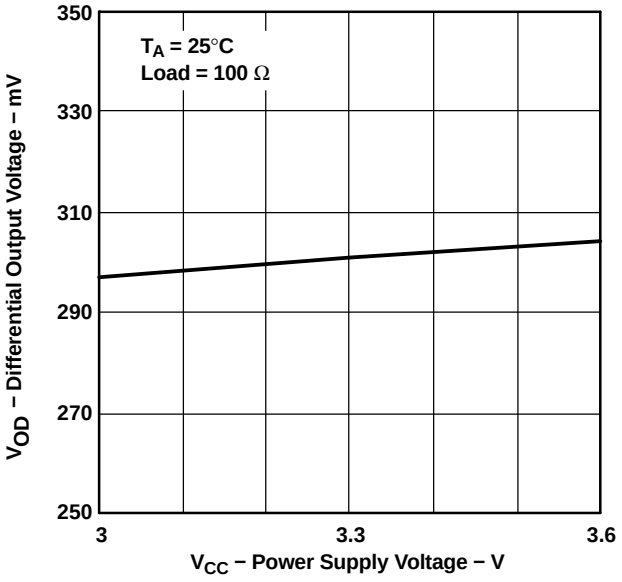


Figure 9.

TYPICAL CHARACTERISTICS (continued)

COMMON-MODE OUTPUT VOLTAGE
vs
POWER SUPPLY VOLTAGE

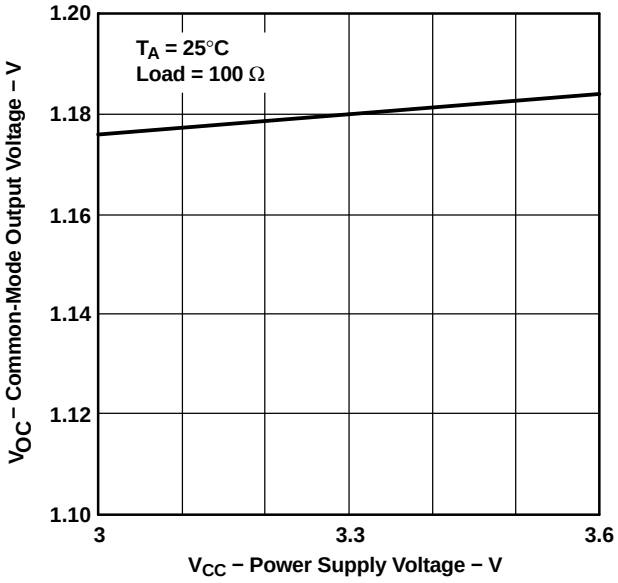


Figure 10.

POWER SUPPLY CURRENT
vs
FREQUENCY

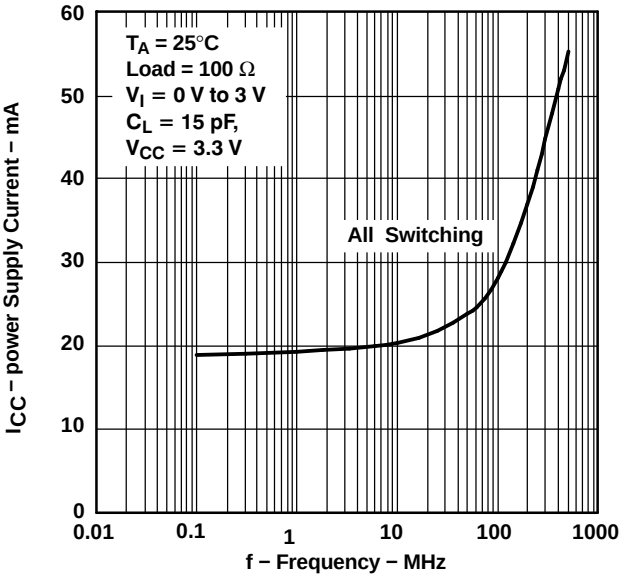


Figure 11.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS047D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047
SN65LVDS047PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS047

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

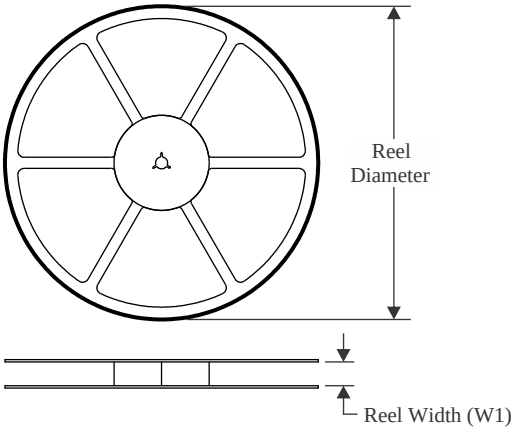
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

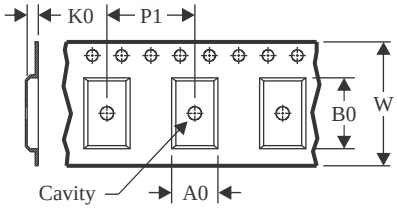
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

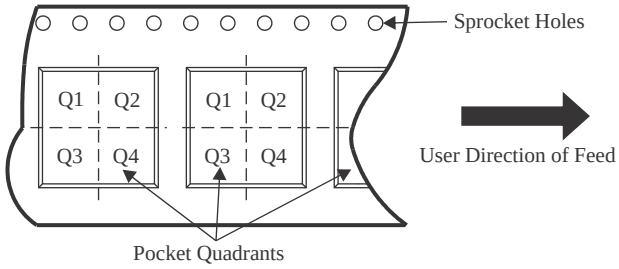


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

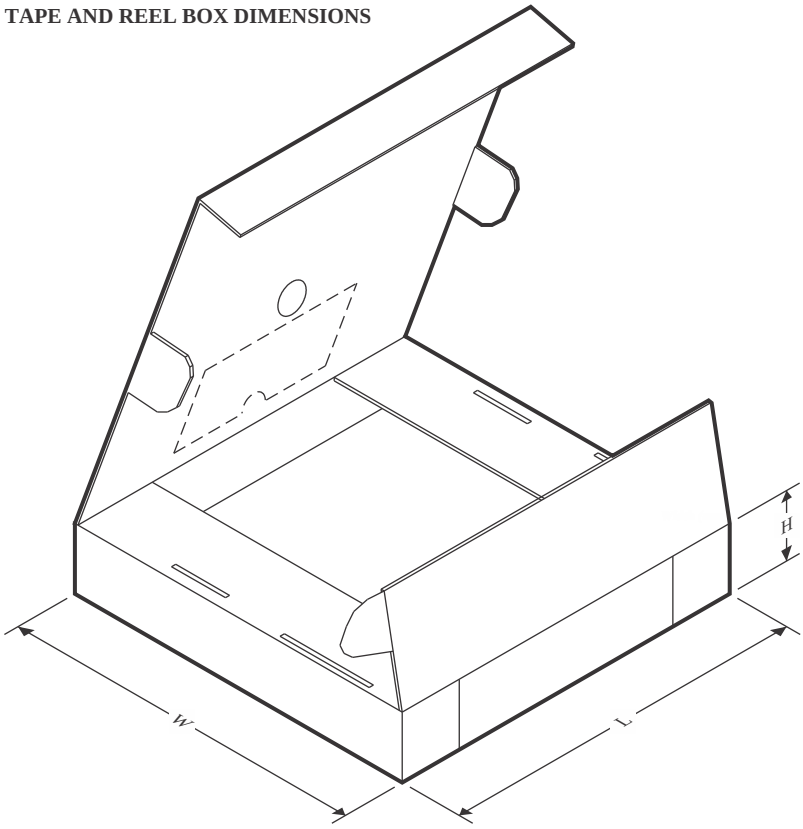
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS047DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS047PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

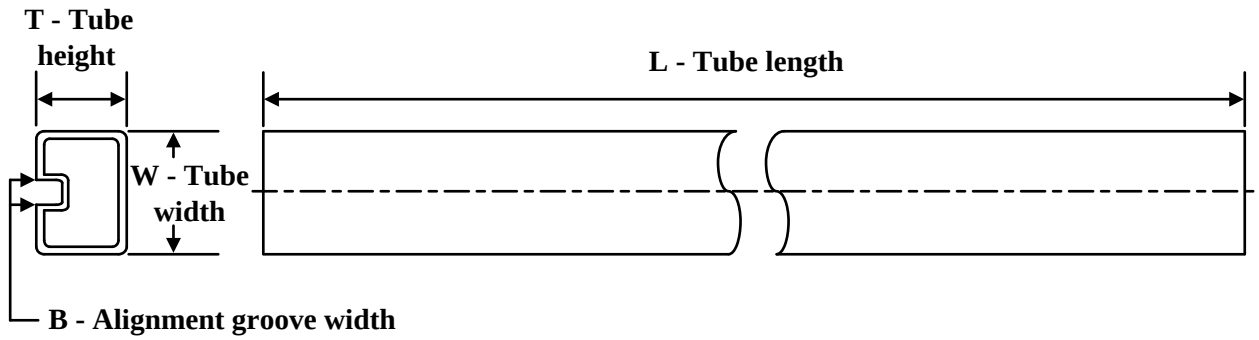
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS047DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS047PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

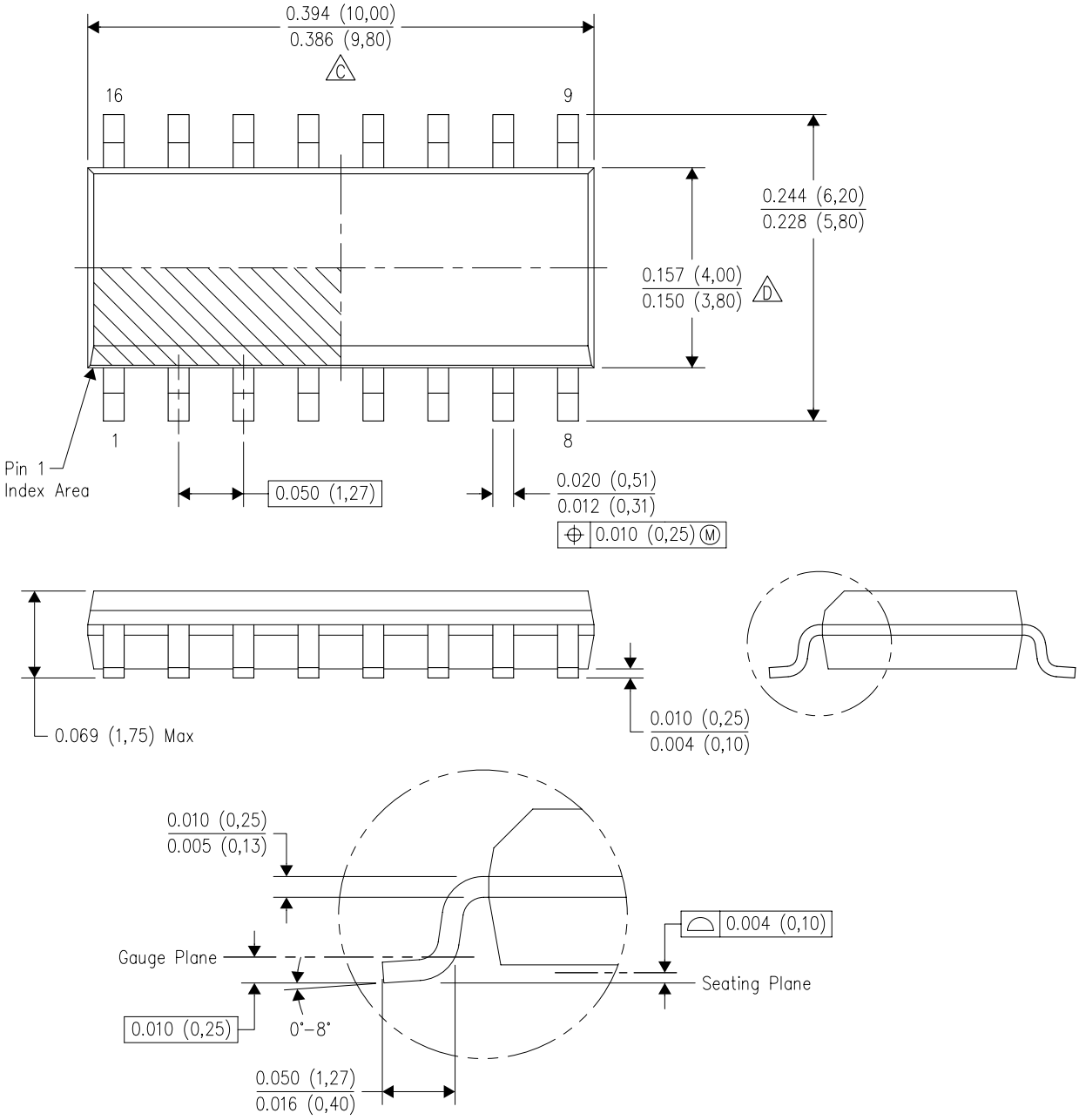
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS047D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS047D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS047DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS047PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS047PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS047PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



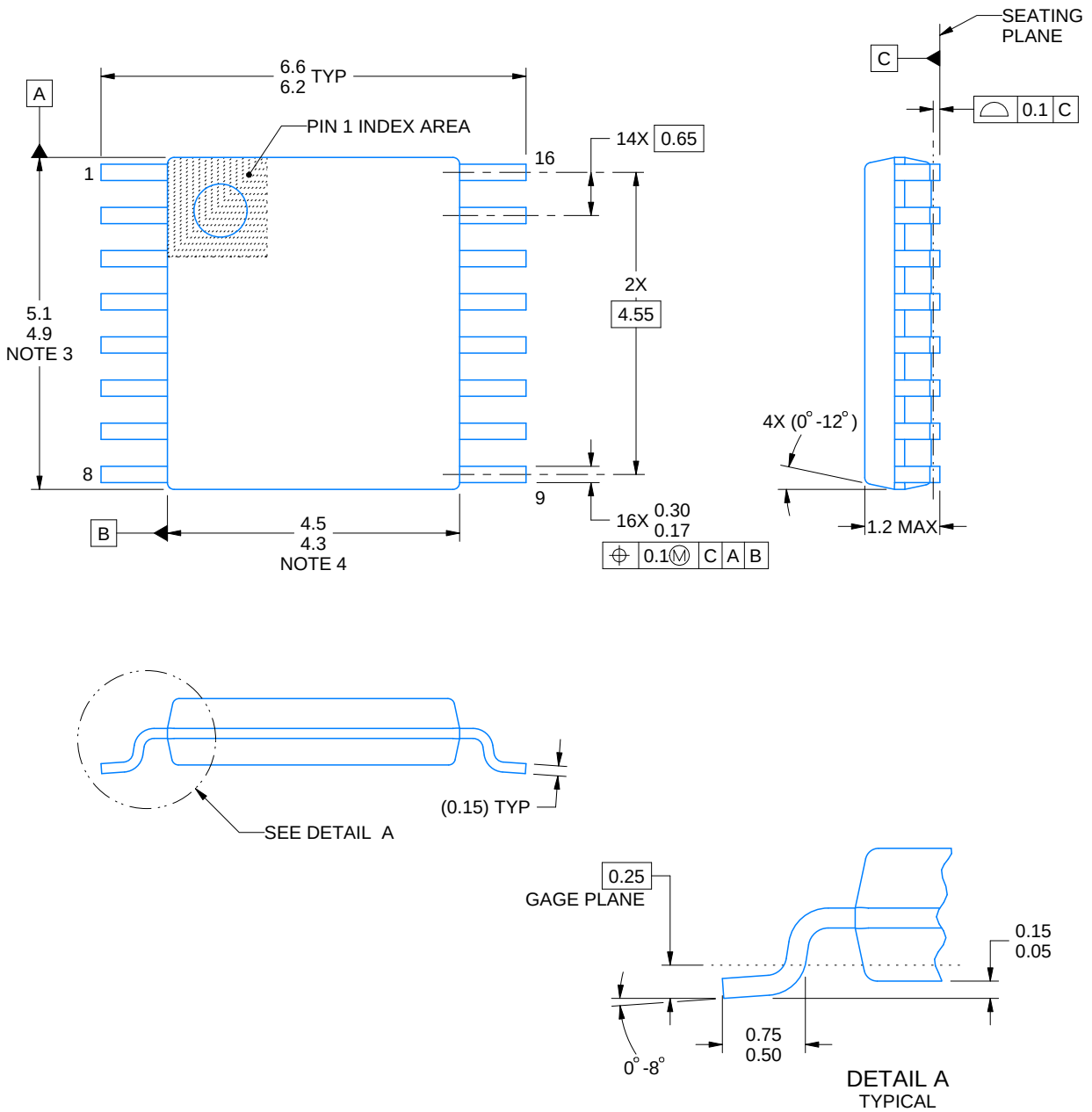
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

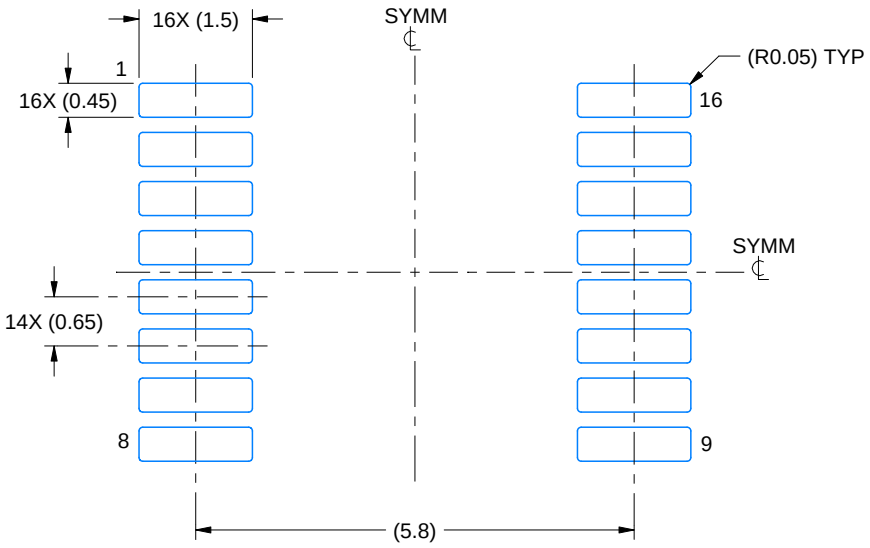
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



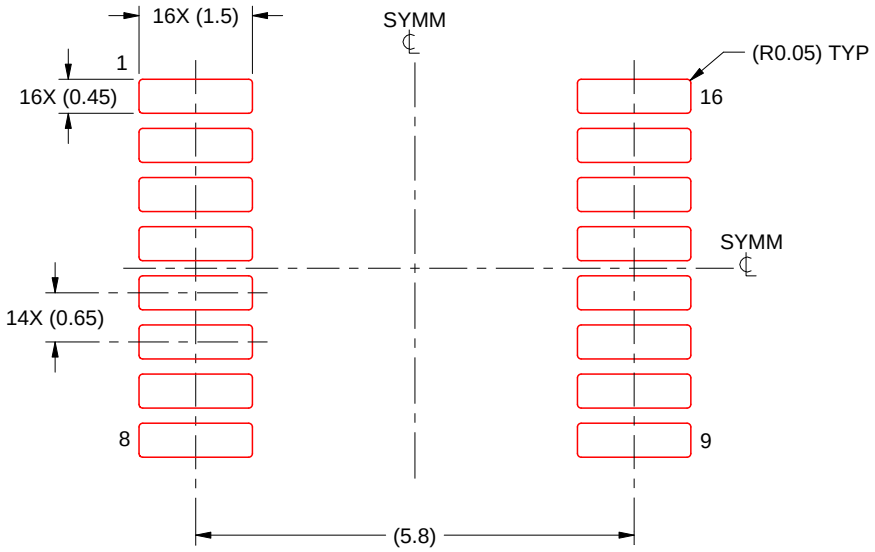
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265