

## SNx5LBC182 Differential Bus Transceiver

### 1 Features

- One-fourth unit load allows up to 128 devices on a bus
- Meets or exceeds the requirements of ANSI standard TIA/EIA-485-A and ISO 8482: 1987(E)
- Controlled driver output-voltage slew rates allow longer cable stub lengths
- Designed for signaling rates.
  - The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second) up to 250 kbps
- Low disabled supply current: 250- $\mu$ A maximum
- Thermal shutdown protection
- Open-circuit fail-safe receiver design
- Receiver input hysteresis: 70-mV typical
- Glitch-free power-up and power-down protection

### 2 Applications

- Utility meters
- [Industrial process control](#)
- [Building automation](#)

### 3 Description

The SN65LBC182 and SN75LBC182 are differential data line transceivers with a high level of ESD protection in the trade-standard footprint of the SN75176. They are designed for balanced transmission lines and meet ANSI standard TIA/EIA-485-A and ISO 8482. The SN65LBC182 and SN75LBC182 combine a 3-state, differential line driver and differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control.

The driver outputs and the receiver inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus. This port operates over a wide range of common-mode voltage, making the device suitable for party-line applications. The device also includes additional features for party-line data buses in electrically noisy environment applications such as industrial process control or power inverters.

The SN75LBC182 and SN65LBC182 bus pins also exhibit a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus. The high ESD tolerance protects the device for cabled connections. (For an even higher level of protection, see the SN65/75LBC184, literature number SLLS236.)

The differential driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled voltage transitions. The receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). Very low device supply current can be achieved by disabling the driver and the receiver.

The SN65LBC182 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the SN75LBC182 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

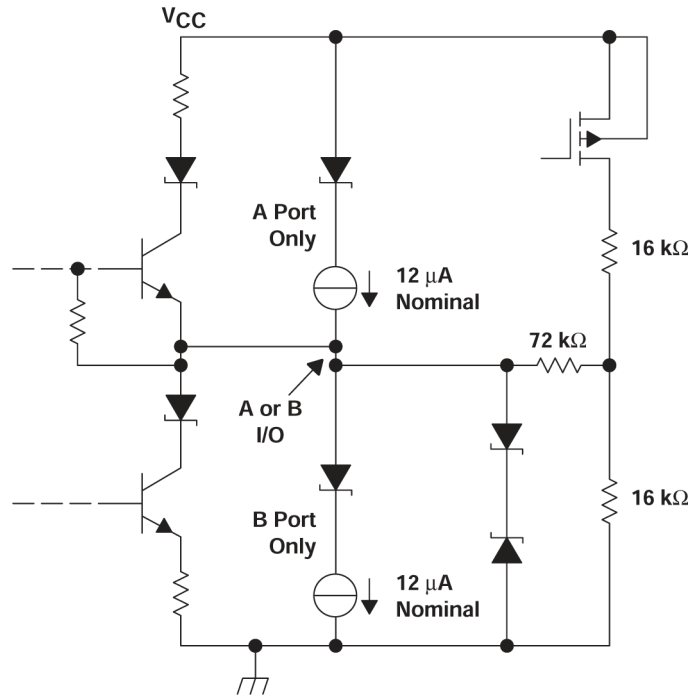
#### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| SN65LBC182, | P (PDIP, 8)            | 9.81 mm $\times$ 9.43 mm    |
| SN75LBC182  | D (SOIC, 8)            | 4.9 mm $\times$ 6 mm        |

(1) For more information, see [Section 11](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



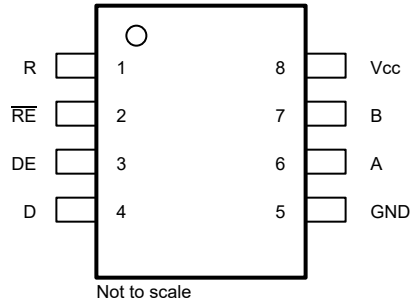


**Schematic of Inputs and Outputs**

## Table of Contents

|  |          |  |           |
|--|----------|--|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | <b>6 Parameter Measurement Information</b> .....       | <b>9</b>  |
| <b>2 Applications</b> .....                    | <b>1</b> | <b>7 Detailed Description</b> .....                    | <b>12</b> |
| <b>3 Description</b> .....                     | <b>1</b> | 7.1 Functional Block Diagram.....                      | 12        |
| <b>4 Pin Configuration and Functions</b> ..... | <b>4</b> | 7.2 Device Functional Modes.....                       | 12        |
| <b>5 Specifications</b> .....                  | <b>5</b> | <b>8 Application and Implementation</b> .....          | <b>13</b> |
| 5.1 Absolute Maximum Ratings .....             | 5        | 8.1 Application Information.....                       | 13        |
| 5.2 ESD Ratings.....                           | 5        | <b>9 Device and Documentation Support</b> .....        | <b>14</b> |
| 5.3 Dissipation Rating.....                    | 5        | 9.1 Receiving Notification of Documentation Updates... | 14        |
| 5.4 Recommended Operating Conditions.....      | 5        | 9.2 Support Resources.....                             | 14        |
| 5.5 Thermal Information.....                   | 6        | 9.3 Trademarks.....                                    | 14        |
| 5.6 Driver Electrical Characteristics.....     | 6        | 9.4 Electrostatic Discharge Caution.....               | 14        |
| 5.7 Receiver Electrical Characteristics.....   | 6        | 9.5 Glossary.....                                      | 14        |
| 5.8 Driver Switching Characteristics.....      | 7        | <b>10 Revision History</b> .....                       | <b>14</b> |
| 5.9 Receiver Switching Characteristics.....    | 7        | <b>11 Mechanical, Packaging, and Orderable</b>         |           |
| 5.10 Typical Characteristics.....              | 8        | <b>Information</b> .....                               | <b>14</b> |

## 4 Pin Configuration and Functions



**Figure 4-1. P (PDIP) or D (SOIC) Package (Top View)**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE | DESCRIPTION                        |
|-----------------|-----|------|------------------------------------|
| NAME            | NO. |      |                                    |
| R               | 1   | O    | Receiver Output                    |
| $\overline{RE}$ | 2   | I    | Active Low Receiver Enable Input   |
| DE              | 3   | I    | Active High Driver Enable Input    |
| D               | 4   | I    | Driver Input                       |
| GND             | 5   | GND  | Device GND                         |
| A               | 6   | I/O  | Non-Inverting Differential Bus I/O |
| B               | 7   | I/O  | Inverting Differential Bus I/O     |
| V <sub>CC</sub> | 8   | PWR  | Device VCC (4.75V to 5.25V)        |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|                                 |   | MIN                                 | MAX | UNIT |
|---------------------------------|---|-------------------------------------|-----|------|
| V <sub>CC</sub>                 | Supply voltage range, (see <sup>(2)</sup> ) | -0.5                                | 7   | V    |
| (A or B)                        | Voltage range at any bus terminal           | -15                                 | 15  | V    |
| V <sub>I</sub> (D, DE, R or RE) | Input voltage                               | -0.3                                | 7   | V    |
| I <sub>O</sub>                  | Receiver output current                     |                                     | ±20 | mA   |
|                                 | Continuous total power dissipation          | See <i>Dissipation Rating</i> table |     |      |

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

### 5.2 ESD Ratings

|                    |                         |   | VALUE     | UNIT |    |
|--------------------|-------------------------|---|-----------|------|----|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | A, B, GND | ±15  | kV |
|                    |                         |   | All pins  | ±3   |    |
|                    |                         | IEC 61000-4-2 contact discharge                                   | A, B, GND | ±8   | kV |
|                    |                         | IEC 61000-4-2 Air-gap discharge                                   | A, B, GND | ±15  | kV |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 5.3 Dissipation Rating

| PACKAGE <sup>(2)</sup> | T <sub>A</sub> ≤ 25°C POWER RATING | DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C POWER RATING | T <sub>A</sub> = 85°C POWER RATING |
|------------------------|------------------------------------|--|------------------------------------|------------------------------------|
| D                      | 725 mW                             | 5.8 mW/°C  | 464 mW                             | 377 mW                             |
| P                      | 1150 mW                            | 9.2 mW/°C  | 736 mW                             | 598 mW                             |

- This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

### 5.4 Recommended Operating Conditions

|   |            | MIN  | NOM | MAX  | UNIT |
|---|------------|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>   |            | 4.75 | 5   | 5.25 | V    |
| Voltage at any bus I/O terminal (separately or common mode) V <sub>I</sub> or V <sub>IC</sub> |            | -7   |     | 12   | V    |
| High-level input voltage, V <sub>IH</sub>   | D, DE, RE  | 2    |     | 0.8  | V    |
| Low-level input voltage, V <sub>IL</sub>  |            |      |     |      |      |
| Differential input voltage, V <sub>ID</sub> (see <sup>(1)</sup> )                             |            | -12  |     | 12   | V    |
| Output current, I <sub>O</sub>  | Driver     | -60  |     | 60   | mA   |
|   | Receiver   | -8   |     | 4    |      |
| Operating free-air temperature, T <sub>A</sub>  | SN65LBC182 | -40  |     | 85   | °C   |
|   | SN75LBC182 | 0    |     | 70   |      |

- Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

## 5.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | D (SOIC) | P (PDIP) | UNIT |
|-------------------------------|--|----------|----------|------|
|                               |  | 8-PINS   |          |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 116.7    | 84.3     | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 56.3     | 65.4     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 63.4     | 62.1     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 8.8      | 31.3     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 62.6     | 60.4     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.6 Driver Electrical Characteristics

over recommended operating conditions

| PARAMETER           | TEST CONDITIONS  |   | MIN                       | TYP <sup>(1)</sup>          | MAX      | UNIT    |    |
|---------------------|--|---|---------------------------|-----------------------------|----------|---------|----|
| $V_{IK}$            | Input clamp voltage  | $I_I = -18$ mA  | -1.5                      |                             |          | V       |    |
| $V_O$               | Output voltage   | $I_O = 0$   | 0                         |                             | $V_{CC}$ | V       |    |
| $ V_{OD} $          | Differential output voltage  | $R_L = 54 \Omega$ ,   | 1.5                       | 2.2                         | $V_{CC}$ | V       |    |
|                     |  | $V_{test} = -7$ V to 12 V,                                    | 1.5                       | 2.2                         | $V_{CC}$ | V       |    |
| $\Delta V_{OD}$     | Change in magnitude of differential output voltage                         | See <a href="#">Figure 6-1</a>                                | -0.2                      |                             | 0.2      | V       |    |
| $V_{OC(SS)}$        | Steady-state common-mode output voltage                                    |   | 1                         |                             | 3        |         |    |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage                          | See <a href="#">Figure 6-1</a> and <a href="#">Figure 6-4</a> | -0.2                      |                             | 0.2      |         |    |
| $V_{OC(PP)}$        | Peak-to-peak change in common-mode output voltage during state transitions |   | 0.8                       |                             |          | V       |    |
| $I_{OZ}$            | High-impedance output current  | See receiver input currents                                   |                           |                             |          |         |    |
| $I_{IH}$            | High-level input current (D, DE)   | $V_I = 2.4$ V   |                           |                             | 50       | $\mu$ A |    |
| $I_{IL}$            | Low-level input current (D, DE)  | $V_I = 0.4$ V   | -50                       |                             |          | $\mu$ A |    |
| $I_{OS}$            | Short-circuit output current   | $V_O = -7$ V to 12 V  | -250                      |                             | 250      | mA      |    |
| $I_{CC}$            | Supply current   | SN75LBC182  | No load, DE at $V_{CC}$ , | $\overline{RE}$ at $V_{CC}$ | 12       | 25      | mA |
|                     |  | SN65LBC182  |                           |                             | 12       | 30      |    |

(1) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

## 5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                            |                                   | MIN  | TYP <sup>(1)</sup> | MAX | UNIT |
|-----------|--|-----------------------------------|------|--------------------|-----|------|
| $V_{IT+}$ | Positive-going input threshold voltage     |                                   |      |                    | 0.2 | V    |
| $V_{IT-}$ | Negative-going input threshold voltage     |                                   | -0.2 |                    |     |      |
| $V_{hys}$ | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                                   |      | 70                 |     | mV   |
| $V_{IK}$  | Enable-input clamp voltage                 | $I_I = -18$ mA                    | -1.5 |                    |     | V    |
| $V_{OH}$  | High-level output voltage                  | $V_{ID} = 200$ mV, $I_O = -8$ mA, | 2.8  |                    |     | V    |
| $V_{OL}$  | Low-level output voltage                   | $V_{ID} = 200$ mV, $I_O = 4$ mA,  |      |                    | 0.4 | V    |

## 5.7 Receiver Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS                 | MIN                                    | TYP <sup>(1)</sup> | MAX     | UNIT    |
|-----------|--|---------------------------------|--|--------------------|---------|---------|
| $I_{OZ}$  | High-impedance-state output current          | $V_O = 0.4$ to $2.4$ V          |  |                    | $\pm 1$ | $\mu$ A |
| $I_I$     | Bus input current                            | $V_{IH} = 12$ V, $V_{CC} = 5$ V |  |                    | 250     | $\mu$ A |
|           |  | $V_{IH} = 12$ V, $V_{CC} = 0$ V | Other input at 0 V                     |                    | 250     |         |
|           |  | $V_{IH} = -7$ V, $V_{CC} = 5$ V |  | -200               |         |         |
|           |  | $V_{IH} = -7$ V, $V_{CC} = 0$ V |  | -200               |         |         |
| $I_{IH}$  | High-level input current ( $\overline{RE}$ ) | $V_{IH} = 2$ V                  |  |                    |         | 50      |
| $I_{IL}$  | Low-level input current ( $\overline{RE}$ )  | $V_{IL} = 0.8$ V                | -50                                    |                    |         | $\mu$ A |
| $I_{CC}$  | Supply current                               | No load                         | DE at 0 V, $\overline{RE}$ at 0 V      |                    | 3.5     | mA      |
|           |  |                                 | DE at 0 V, $\overline{RE}$ at $V_{CC}$ |                    | 175 250 |         |

(1) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

## 5.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS   | MIN  | TYP   | MAX  | UNIT    |
|-------------|--|---|------|-------|------|---------|
| $t_r$       | Differential output signal rise time             | $R_L = 54 \Omega$ ,<br>See <a href="#">Figure 6-3</a><br>$C_L = 50$ pF, | 0.25 | 0.72  | 1.2  | $\mu$ s |
| $t_f$       | Differential output signal fall time             |   | 0.25 | 0.73  | 1.2  |         |
| $t_{PLH}$   | Propagation delay time, low-to-high-level output |   |      |       | 1.3  |         |
| $t_{PHL}$   | Propagation delay time, high-to-low-level output |   |      |       | 1.3  |         |
| $t_{sk(p)}$ | Pulse skew ( $t_{PHL} - t_{PLH}$ )               |   |      | 0.075 | 0.15 |         |
| $t_{PZH}$   | Output enable time to high level                 | $R_L = 110 \Omega$ , See <a href="#">Figure 6-5</a>                     |      |       | 3.5  | $\mu$ s |
| $t_{PHZ}$   | Output disable time from high level              |   |      |       | 3.5  |         |
| $t_{PZL}$   | Output enable time to low level                  | $R_L = 110 \Omega$ , See <a href="#">Figure 6-6</a>                     |      |       | 3.5  | $\mu$ s |
| $t_{PLZ}$   | Output disable time from low level               |   |      |       | 3.5  |         |

## 5.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|-------------|--|---|-----|-----|-----|------|
| $t_r$       | Differential output signal rise time             | $C_L = 50$ pF, See <a href="#">Figure 6-7</a> |     | 20  |     | ns   |
| $t_f$       | Differential output signal fall time             |   |     | 20  |     |      |
| $t_{PLH}$   | Propagation delay time, low-to-high-level output |   |     |     | 150 |      |
| $t_{PHL}$   | Propagation delay time, high-to-low-level output |   |     |     | 150 |      |
| $t_{PZH}$   | Output enable time to high level                 | See <a href="#">Figure 6-8</a>                |     |     | 100 | ns   |
| $t_{PZL}$   | Output enable time to low level                  |   |     |     | 100 |      |
| $t_{PHZ}$   | Output disable time from high level              |   |     |     | 100 | ns   |
| $t_{PLZ}$   | Output disable time from low level               |   |     |     | 100 |      |
| $t_{sk(p)}$ | Pulse skew $ t_{PHL} - t_{PLH} $                 |   |     |     | 50  |      |

## 5.10 Typical Characteristics

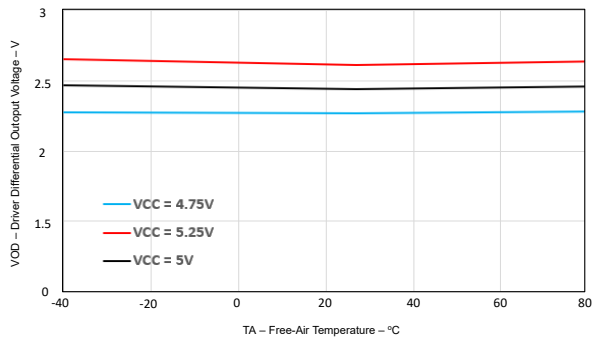


Figure 5-1. Driver Differential Output Voltage vs Temperature

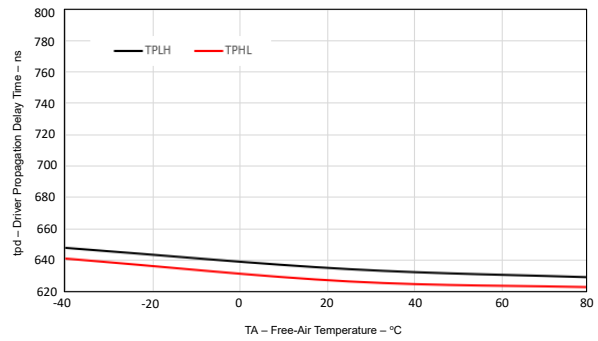


Figure 5-2. Driver Propagation Delay Time vs Temperature

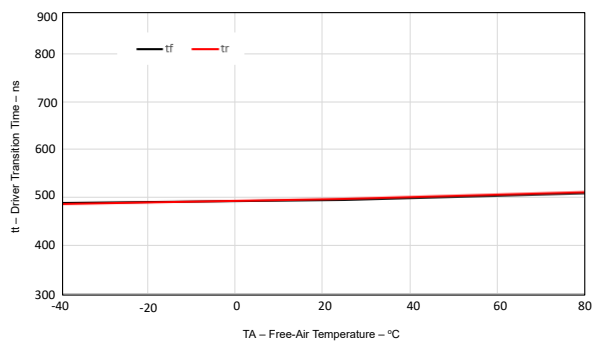


Figure 5-3. Driver Transition Time vs Temperature

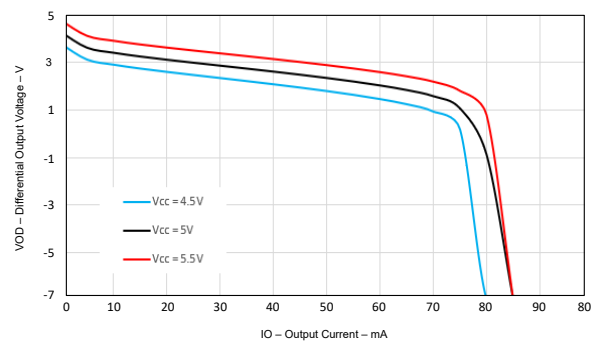


Figure 5-4. Differential Output Voltage vs Output Current

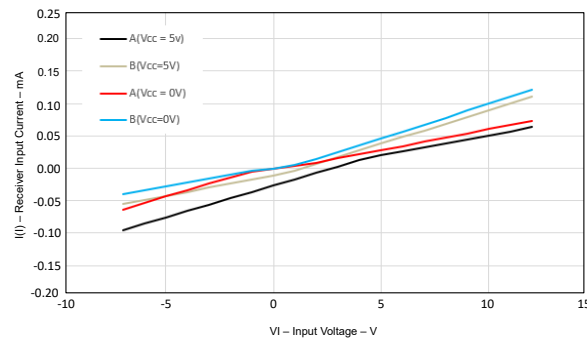
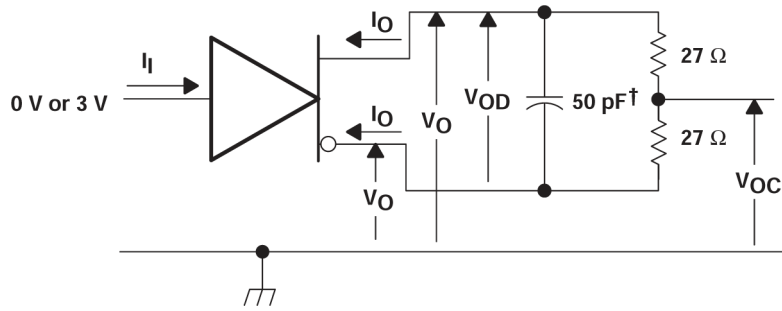


Figure 5-5. Receiver Input Current vs Input Voltage



## 6 Parameter Measurement Information



A. Includes probe and jig capacitance

Figure 6-1. Driver Test Circuit,  $v_{OD}$  And  $v_{OC}$  Without Common-Mode Loading

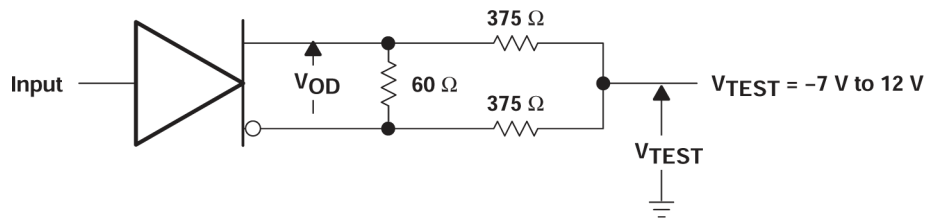
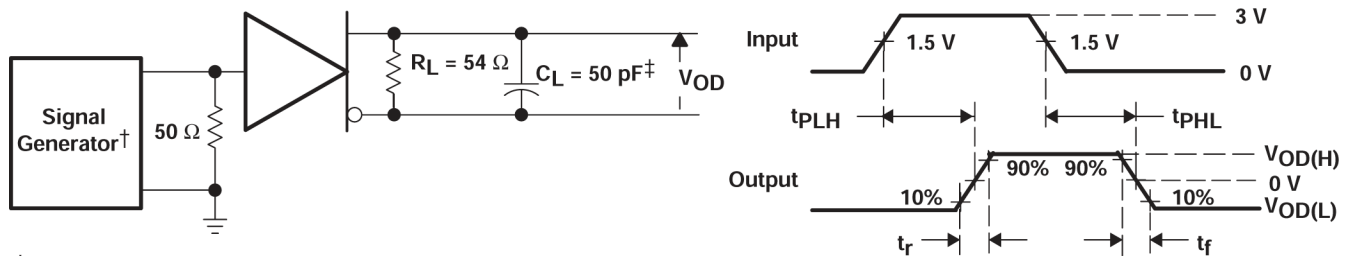


Figure 6-2. Driver Test Circuit,  $v_{OD}$  With Common-Mode Loading



A. PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$   
B. Includes probe and jig capacitance

Figure 6-3. Driver Switching Test Circuit and Waveforms

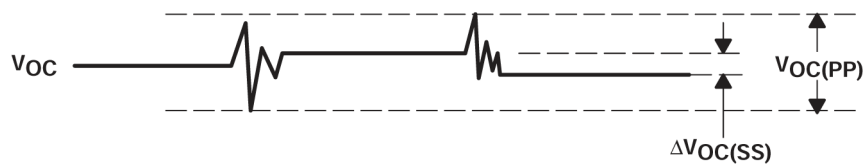
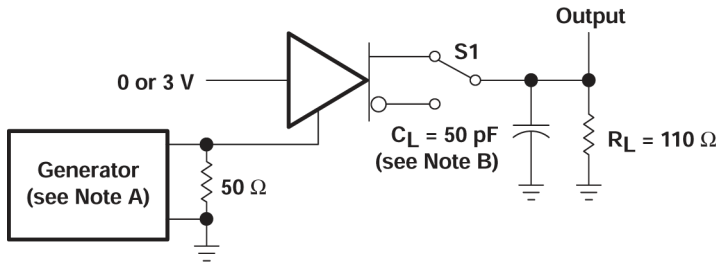
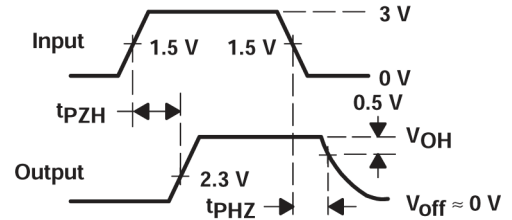


Figure 6-4.  $v_{OC}$  Definitions



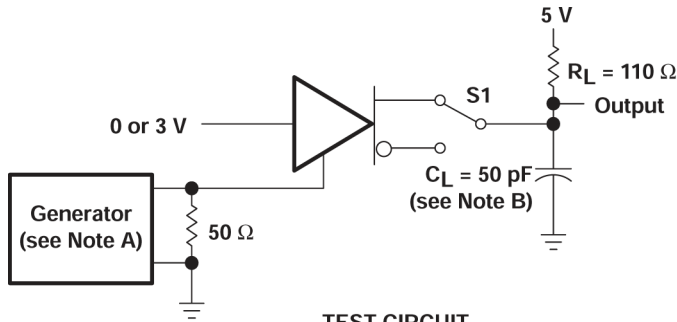
TEST CIRCUIT



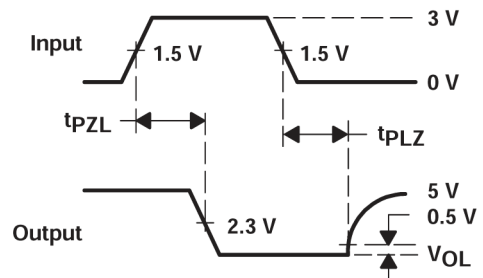
VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 6-5. Driver  $T_{PZH}$  And  $T_{PHZ}$  Test Circuit and Voltage Waveforms



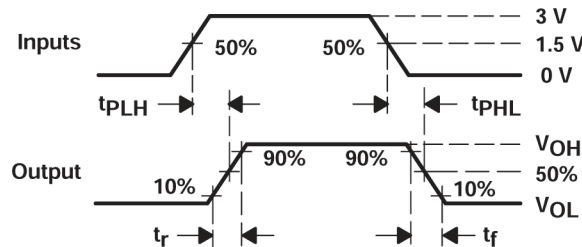
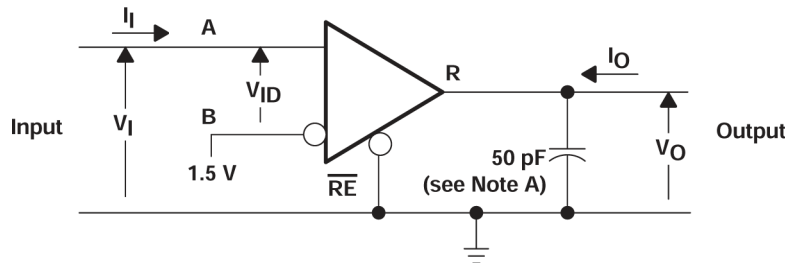
TEST CIRCUIT



VOLTAGE WAVEFORMS

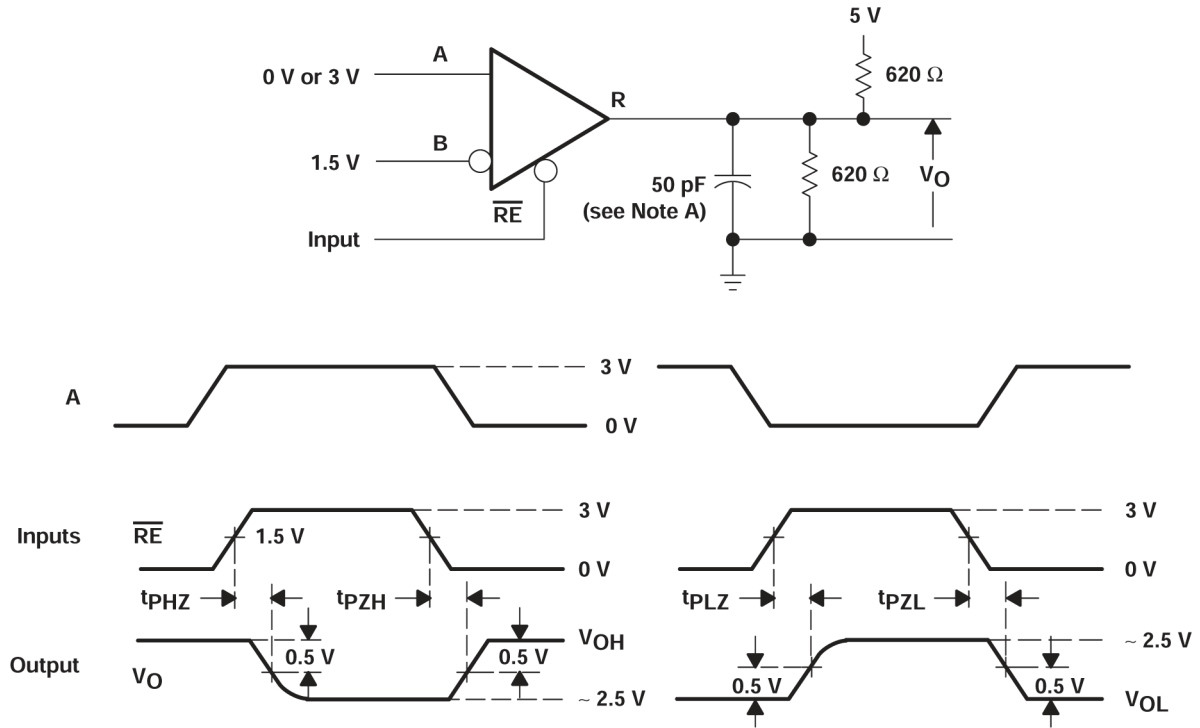
- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 6-6. Driver  $T_{PZL}$  And  $T_{PLZ}$  Test Circuit and Voltage Waveforms



- A. This value includes probe and jig capacitance ( $\pm 10\%$ ).

Figure 6-7. Receiver  $T_{PLH}$  And  $T_{PHL}$  Test Circuit and Voltage Waveforms

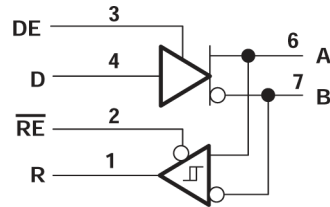


A. This value includes probe and jig capacitance ( $\pm 10\%$ ).

**Figure 6-8. Receiver  $T_{PZL}$ ,  $T_{PLZ}$ ,  $T_{PZH}$ , And  $T_{PHZ}$  Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Functional Block Diagram



### 7.2 Device Functional Modes

**Table 7-1. Function Tables Driver**

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | A       | B |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |
| Open       | H            | H       | L |

**Table 7-2. Function Tables Receiver**

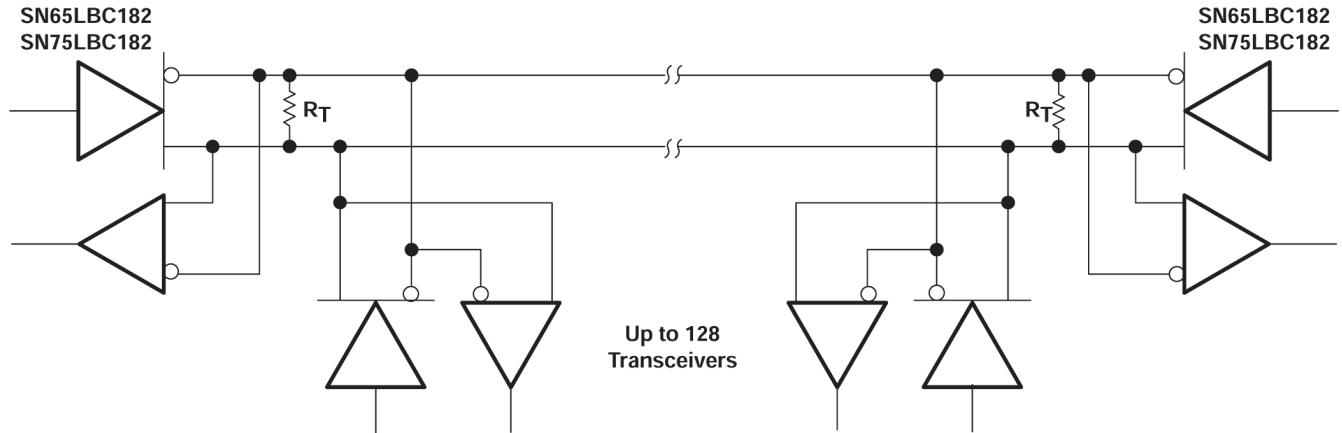
| DIFFERENTIAL<br>INPUTS                  | ENABLE<br>RE | OUTPUT<br>R |
|---|--------------|-------------|
| $V_{ID} \geq 0.2\text{ V}$              | L            | H           |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2\text{ V}$             | L            | L           |
| X                                       | H            | Z           |
| Open                                    | L            | H           |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information



- A. The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 8-1. Typical Application Circuit**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (March 2005) to Revision B (October 2023)                                     | Page |
|---|------|
| • Changed the numbering format for tables, figures, and cross-references throughout the document..... | 1    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65LBC182D</a>  | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | 6LB182              |
| <a href="#">SN65LBC182DR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6LB182              |
| SN65LBC182DR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6LB182              |
| SN65LBC182DRG4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6LB182              |
| <a href="#">SN65LBC182P</a>  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | 65LBC182            |
| SN65LBC182P.A                | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | 65LBC182            |
| <a href="#">SN75LBC182D</a>  | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 7LB182              |
| <a href="#">SN75LBC182DR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7LB182              |
| SN75LBC182DR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7LB182              |
| <a href="#">SN75LBC182P</a>  | Obsolete      | Production           | PDIP (P)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75LBC182            |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LBC182DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65LBC182DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75LBC182DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75LBC182DR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LBC182DR | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN65LBC182DR | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75LBC182DR | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN75LBC182DR | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65LBC182P   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN65LBC182P.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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