

# SN65HVD888 Bus-Polarity Correcting RS-485 Transceiver With IEC-ESD Protection

## 1 Features

- Exceeds requirements of EIA-485 standard
- Bus-polarity correction within 76ms ( $t_{FS}$ )
- Data rate: 300bps to 250kbps
- Works with two configurations:
  - Failsafe resistors only
  - Failsafe and differential termination resistors
- Up to 256 nodes on a bus (1/8 Unit Load)
- SOIC-8 Package for backward compatibility
- Bus-pin protection:
  - $\pm 16\text{kV}$  HBM protection
  - $\pm 12\text{kV}$  IEC61000-4-2 Contact discharge
  - $+4\text{kV}$  IEC61000-4-4 Fast transient burst

## 2 Applications

- E-Metering networks
- Industrial automation
- HVAC systems
- DMX512-networks
- Process control
- Battery-powered applications
- Motion control
- Telecom equipment

## 3 Description

The SN65HVD888 is a low-power RS-485 transceiver with automatic bus-polarity correction and transient protection. Upon hot plug-in, the device detects and corrects the bus polarity within the first 76ms of bus idling. On-chip transient protection protects the device against IEC61000 ESD and EFT transients. This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to Human-Body Model (HBM), Air-Gap Discharge, and Contact Discharge specifications.

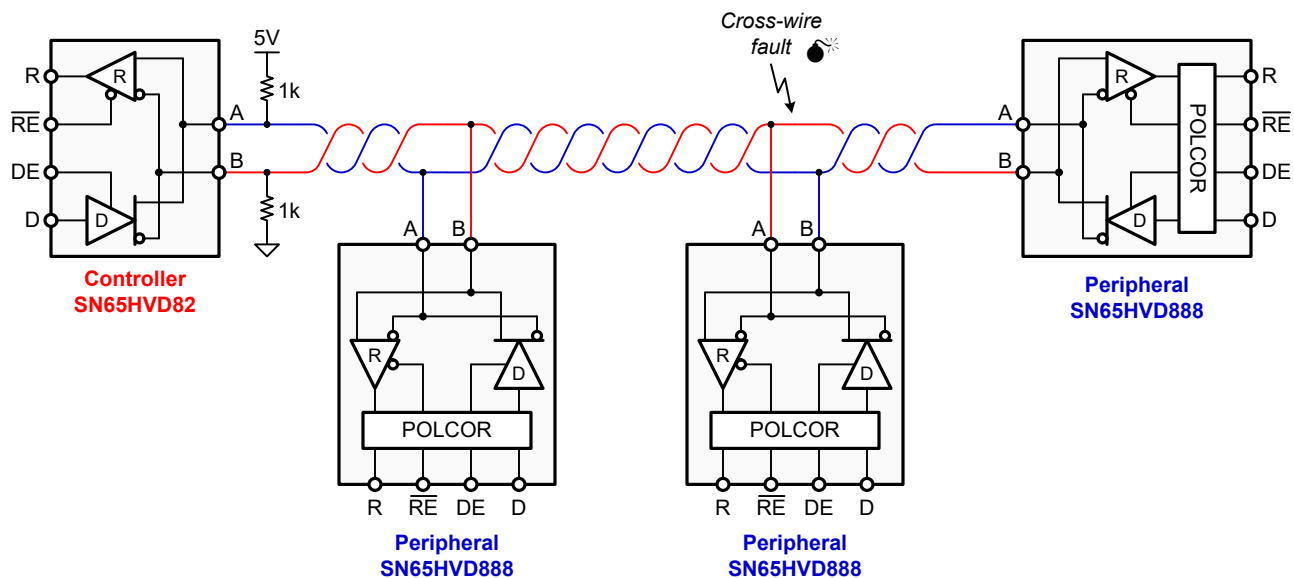
The device combines a differential driver and a differential receiver, which operate together from a single 5V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The SN65HVD888 is available in an SOIC-8 package, and is characterized from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN65HVD888	SOIC (8)	4.9mm × 6mm

(1) For all available packages, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



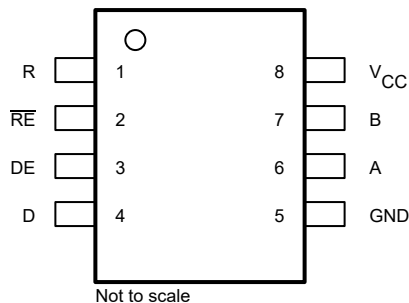
**Typical Network Application With Polarity Correction (POLCOR)**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.3 Feature Description.....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>15</b>
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	8.1 Application Information.....	<b>15</b>
<b>5 Specifications</b> .....	<b>4</b>	8.2 Typical Application.....	<b>21</b>
5.1 Absolute Maximum Ratings.....	<b>4</b>	8.3 Power Supply Recommendations.....	<b>22</b>
5.2 ESD Ratings: JEDEC Specifications.....	<b>4</b>	8.4 Layout.....	<b>22</b>
5.3 ESD Ratings: IEC Specifications.....	<b>4</b>	<b>9 Device and Documentation Support</b> .....	<b>24</b>
5.4 Recommended Operating Conditions.....	<b>5</b>	9.1 Device Support.....	<b>24</b>
5.5 Thermal Information.....	<b>5</b>	9.2 Receiving Notification of Documentation Updates.....	<b>24</b>
5.6 Electrical Characteristics.....	<b>6</b>	9.3 Support Resources.....	<b>24</b>
5.7 Power Dissipation Characteristics.....	<b>7</b>	9.4 Trademarks.....	<b>24</b>
5.8 Switching Characteristics.....	<b>7</b>	9.5 Electrostatic Discharge Caution.....	<b>24</b>
5.9 Typical Characteristics.....	<b>8</b>	9.6 Glossary.....	<b>24</b>
<b>6 Parameter Measurement information</b> .....	<b>9</b>	<b>10 Revision History</b> .....	<b>24</b>
<b>7 Detailed Description</b> .....	<b>11</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>25</b>
7.1 Overview.....	<b>11</b>		
7.2 Functional Block Diagram.....	<b>11</b>		

## 4 Pin Configuration and Functions



**Figure 4-1. D Package, 8-Pin SOIC (Top View)**

**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
RE	2	Digital input	Receiver enable, active low
V <sub>CC</sub>	8	Supply	4.5V to 5.5V supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

(see <sup>(1)</sup>)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	−0.5	7	V
	Input voltage at any logic pin	−0.3	5.7	V
	Voltage input, transient pulse, A and B, through 100Ω	−100	100	V
	Voltage at A or B inputs	−18	18	V
	Receiver output current	−24	24	mA
	Continuous total-power dissipation	See ( <a href="#">Thermal Information</a> ) table		
T <sub>J</sub>	Junction temperature		170	°C
T <sub>STG</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.4](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings: JEDEC Specifications

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500
		Machine model (MM)	±100

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 ESD Ratings: IEC Specifications

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±12000
		IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND	±4000
		IEC 60749-26 ESD (HBM), bus terminals and GND	±16000

## 5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>ID</sub>	Differential input voltage	–12		12	V
V <sub>I</sub>	Input voltage at any bus terminal (separate or common mode) <sup>(1)</sup>	–7		12	V
V <sub>IH</sub>	High-level input voltage (driver, driver-enable, and receiver-enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)	0		0.8	V
I <sub>O</sub>	Output current	Driver		60	mA
		Receiver		8	
C <sub>L</sub>	Differential load capacitance		50		pF
R <sub>L</sub>	Differential load resistance		60		Ω
1/t <sub>UI</sub>	Signaling rate	0.3		250	kbps
T <sub>J</sub>	Junction temperature	–40		150	°C
T <sub>A</sub> <sup>(2)</sup>	Operating free-air temperature (see <a href="#">Section 5.5</a> for additional information)	–40		125	°C

- (1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
- (2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65HVD888	UNIT
		D (SOIC)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	60.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	57.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Driver differential-output voltage magnitude	RL = 60 Ω, 375 Ω on each output from –7 to +12 V	See <a href="#">Figure 6-1</a>	1.5	2.5		V
		RL = 54 Ω (RS-485)	See <a href="#">Figure 6-2</a>	1.5	2.5		
		RL = 100 Ω (RS-422)		2	3		
Δ V <sub>OD</sub>	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL = 50 pF	See <a href="#">Figure 6-2</a>	–0.2	0	0.2	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	See <a href="#">Figure 6-2</a>	1	V <sub>CC</sub> / 2	3	V
ΔV <sub>OC</sub>	Change in differential driver common-mode output voltage	Center of two 27-Ω load resistors	See <a href="#">Figure 6-2</a>	–0.2	0	0.2	mV
V <sub>OC(PP)</sub>	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors	See <a href="#">Figure 6-2</a>		850		mV
C <sub>OD</sub>	Differential output capacitance				8		pF
V <sub>IT+</sub>	Positive-going receiver differential-input voltage threshold				35	100	mV
V <sub>IT–</sub>	Negative-going receiver differential-input voltage threshold			–100	–35		mV
V <sub>HYS</sub> <sup>(1)</sup>	Receiver differential-input voltage threshold hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )			40	60		mV
V <sub>OH</sub>	Receiver high-level output voltage	I <sub>OH</sub> = –8 mA		2.4	V <sub>CC</sub> – 0.3		V
V <sub>OL</sub>	Receiver low-level output voltage	I <sub>OL</sub> = 8 mA			0.2	0.4	V
I <sub>I</sub>	Driver input, driver enable, and receiver enable input current			–2		2	μA
I <sub>OZ</sub>	Receiver high-impedance output current	VO = 0 V or VCC, RE at VCC		–10		10	μA
I <sub>OS</sub>	Driver short-circuit output current	I <sub>OS</sub>   with V <sub>A</sub> or V <sub>B</sub> from –7 to +12 V				150	mA
I <sub>I</sub>	Bus input current (driver disabled)	V <sub>CC</sub> = 4.5 to 5.5 V or	V <sub>I</sub> = 12 V		75	125	μA
		V <sub>CC</sub> = 0 V, DE at 0 V	V <sub>I</sub> = –7 V	–100	–40		
I <sub>CC</sub>	Supply current (quiescent) –40°C to 85°C	Driver and receiver enabled	DE = V <sub>CC</sub> , RE = GND, No load		750	900	μA
		Driver enabled, receiver disabled	DE = V <sub>CC</sub> , RE = V <sub>CC</sub> , No load			650	
		Driver disabled, receiver enabled	DE = GND, RE = GND, No load			750	
		Driver and receiver disabled	DE = GND, D = GND RE = VCC, No load		0.4	5	
I <sub>CC</sub>	Supply current (quiescent) –40°C to 125°C	Driver and receiver enabled	DE = V <sub>CC</sub> , RE = GND, No load		750	990	μA
		Driver enabled, receiver disabled	DE = V <sub>CC</sub> , RE = V <sub>CC</sub> , No load			715	
		Driver disabled, receiver enabled	DE = GND, RE = GND, No load			825	
Supply current (dynamic)		See <a href="#">Figure 5-3</a>					

(1) Under any specific conditions,  $V_{IT+}$  is specified to be at least  $V_{HYS}$  higher than  $V_{IT-}$ .

## 5.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
PD	Power Dissipation driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>J</sub> = 150°C 50% duty cycle square-wave signal at 250 kbps signaling rate:	Unterminated	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF (driver)	164	mW
		RS-422 load	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF (driver)	247	
		RS-485 load	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF (driver)	316	

## 5.8 Switching Characteristics

3.3 ms > bit time > 4  $\mu\text{s}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t <sub>r</sub> , t <sub>f</sub>	Driver differential-output rise and fall times	RL = 54Ω, CL = 50pF	See <a href="#">Figure 6-3</a>	400	700	1200	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay	RL = 54Ω, CL = 50pF	See <a href="#">Figure 6-3</a>	90	700	1000	ns
t <sub>SK(P)</sub>	Driver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>	RL = 54Ω, CL = 50pF	See <a href="#">Figure 6-3</a>		25	200	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time		See <a href="#">Figure 6-4</a> and <a href="#">Figure 6-5</a>		50	500	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver enable time	Receiver enabled	See <a href="#">Figure 6-4</a> and <a href="#">Figure 6-5</a>		500	1000	ns
		Receiver disabled	See <a href="#">Figure 6-4</a> and <a href="#">Figure 6-5</a>		3	9	μs
RECEIVER							
t <sub>r</sub> , t <sub>f</sub>	Receiver output rise and fall times	CL = 15 pF	See <a href="#">Figure 6-6</a>		18	30	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Receiver propagation delay time	CL = 15 pF	See <a href="#">Figure 6-6</a>		85	195	ns
t <sub>SK(P)</sub>	Receiver pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>	CL = 15 pF	See <a href="#">Figure 6-6</a>		1	15	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Receiver disable time				50	500	
t <sub>PZL(1)</sub> , t <sub>PZH(1)</sub> , t <sub>PZL(2)</sub> , t <sub>PZH(2)</sub>	Receiver enable time	Driver enabled	See <a href="#">Figure 6-7</a>		20	130	ns
		Driver disabled	See <a href="#">Figure 6-8</a>		2	8	μs
t <sub>FS</sub>	Bus failsafe time	Driver disabled	See <a href="#">Figure 6-9</a>	44	58	76	ms

## 5.9 Typical Characteristics

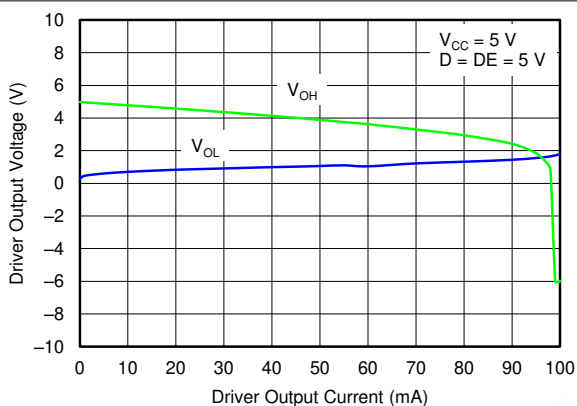


Figure 5-1. Driver Output Voltage vs Driver Output Current

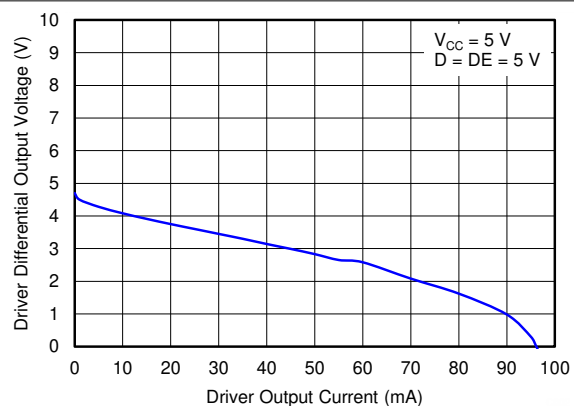


Figure 5-2. Driver Differential Output Voltage vs Driver Output Current

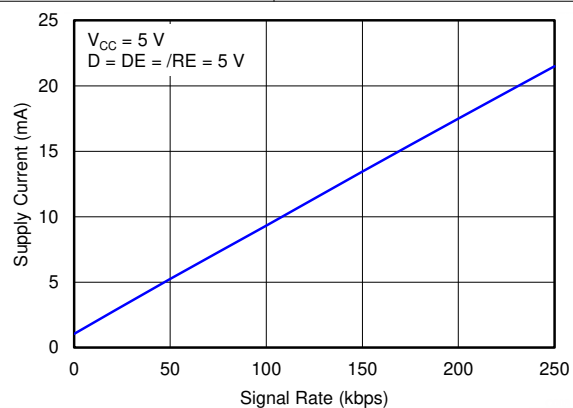
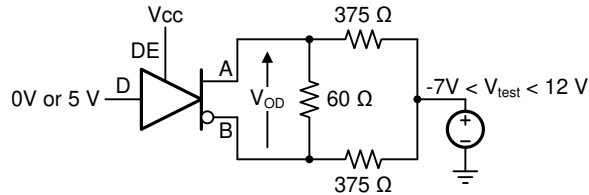


Figure 5-3. Supply Current vs Signaling Rate

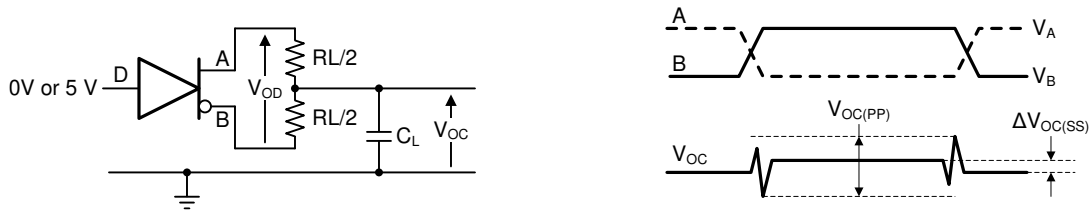


## 6 Parameter Measurement information

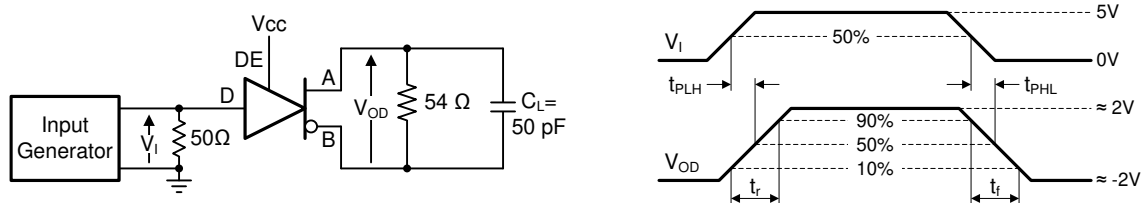
### Driver



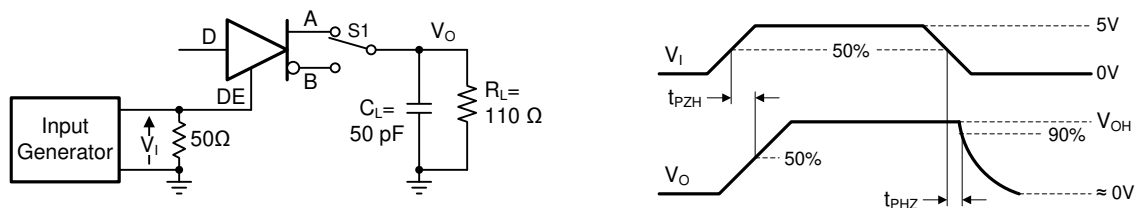
**Figure 6-1. Measurement of Driver Differential-Output Voltage With Common-Mode Load**



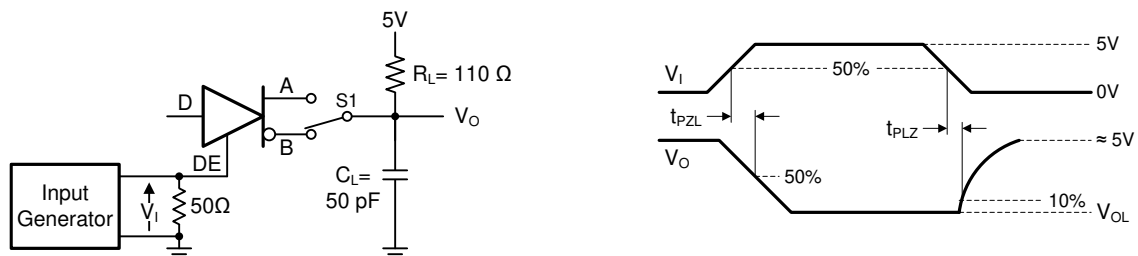
**Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load**



**Figure 6-3. Measurement of Driver Differential-Output Rise and Fall Times and Propagation Delays**

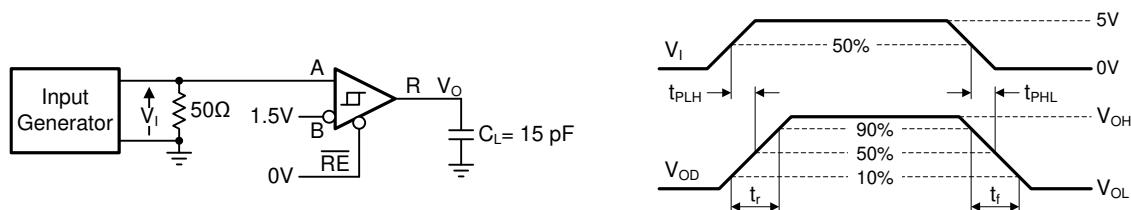


**Figure 6-4. Measurement of Driver Enable and Disable Times With Active-High Output and Pull-Down Load**

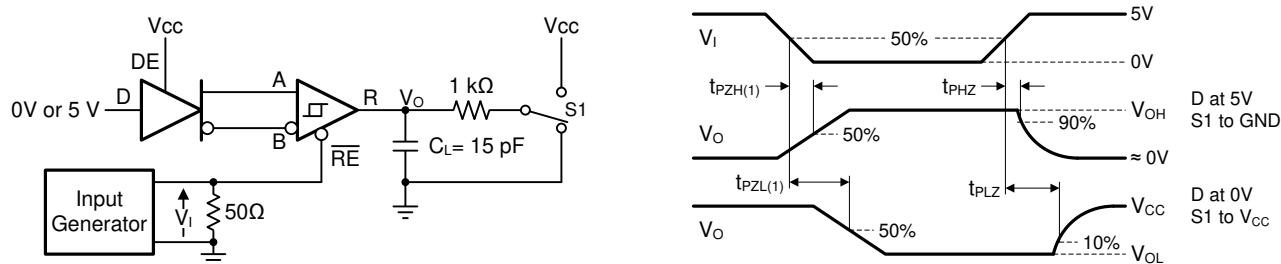


**Figure 6-5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pull-up Load**

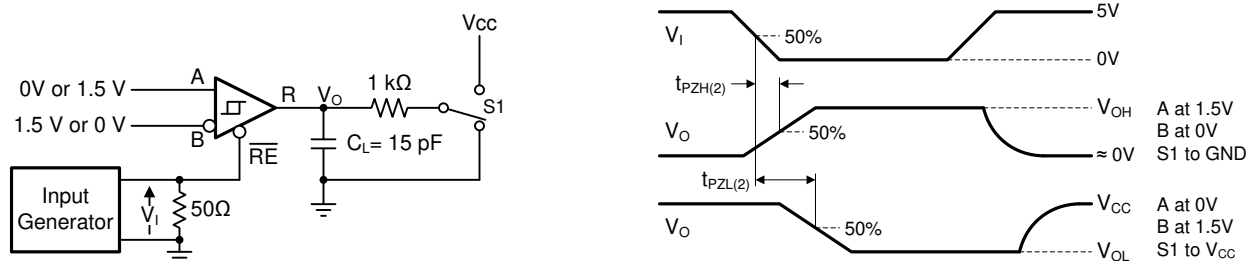
## Receiver



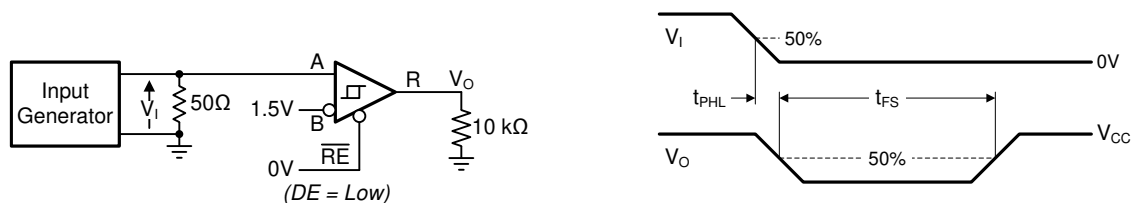
**Figure 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**



**Figure 6-7. Measurement of Receiver Enable and Disable Times With Driver Enabled**

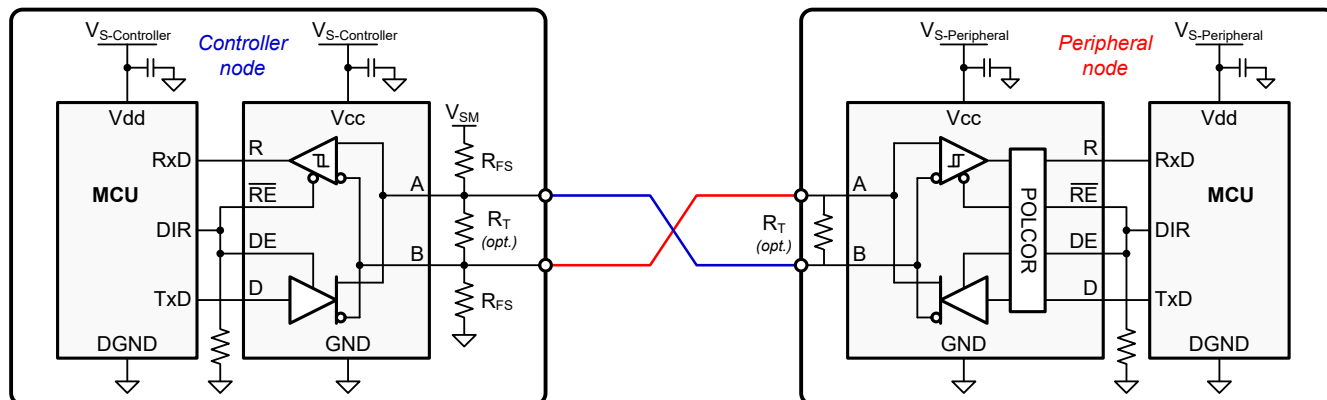


**Figure 6-8. Measurement of Receiver Enable Times With Driver Disabled**



**Figure 6-9. Measurement of Receiver Polarity-Correction Time With Driver Disabled**

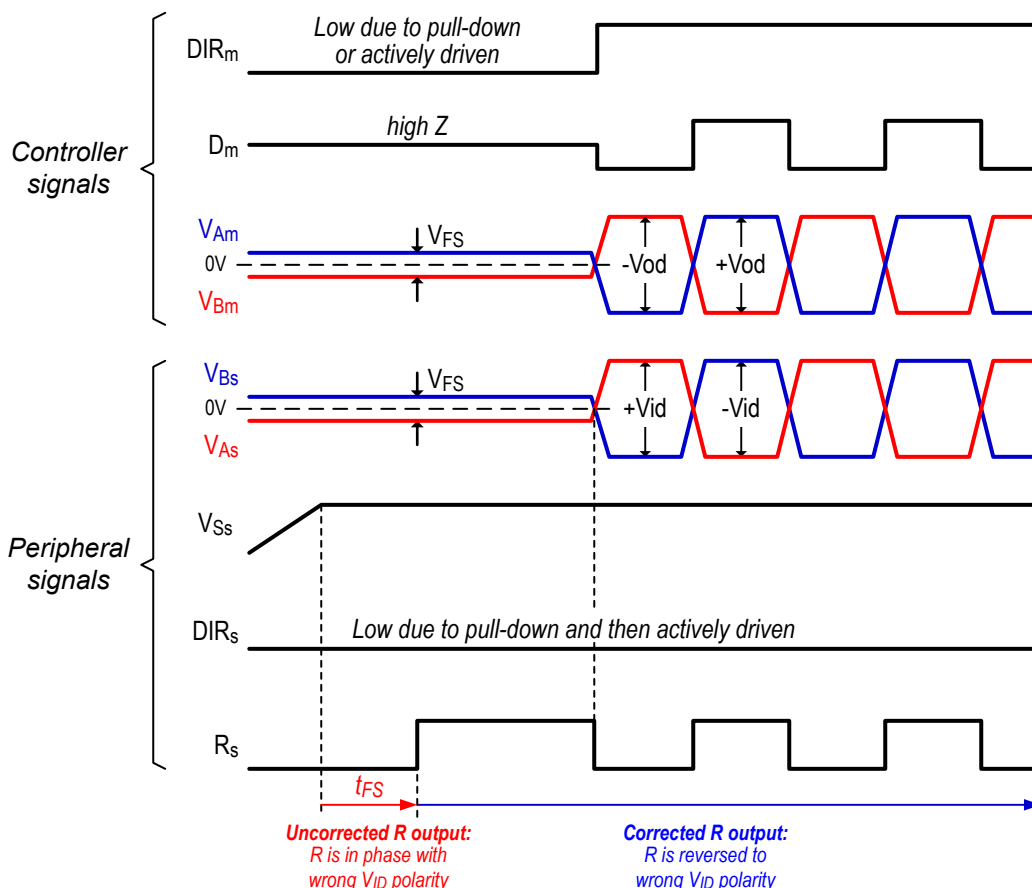




**Figure 7-1. Point-To-Point Data Link With Cross-Wire Fault**

Prior to initiating data transmission the controller transceiver must idle for a time span that exceeds the maximum failsafe time,  $t_{FS-max}$ , of a peripheral transceiver. This idle time is accomplished by driving the direction control line, DIR, low. After a time,  $t > t_{FS-max}$ , the controller begins transmitting data.

Because of the indicated cross-wire fault between controller and peripheral, the peripheral node receives bus signals with reversed polarity. Assuming the peripheral node has just been connected to the bus, the direction-control pin is pulled-down during power-up and then is actively driven low by the peripheral MCU. The polarity correction begins as soon as the peripheral supply is established and ends after approximately 44 to 76ms.



**Figure 7-2. Polarity Correction Timing Prior to a Data Transmission**

Initially the peripheral receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the peripheral receiver,  $R_S$ , turns low. After  $t_{FS}$  has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and  $R_S$  turns high.

At this point all incoming bus data with reversed polarity are polarity corrected within the transceiver. Because polarity correction is also applied to the transmit path, the data sent by the peripheral MCU are reversed by the POLCOR logic and then fed into the driver.

The reversed data from the peripheral MCU are reversed again by the cross-wire fault in the bus, and the correct bus polarity is reestablished at the controller end.

This process repeats each time the device powers up and detects an incorrect bus polarity.

## 7.4 Device Functional Modes

**Table 7-1. Driver Pin Functions**

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High
POLARITY-CORRECTING MODE <sup>(1)</sup>				
H	H	L	H	Actively drives bus Low
L	H	H	L	Actively drives bus High
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus Low

(1) The polarity-correcting mode is entered when  $V_{ID} < V_{IT-}$  and  $t > t_{FS}$  and  $DE = \text{low}$ . This state is latched when  $\overline{RE}$  turns from Low to High.

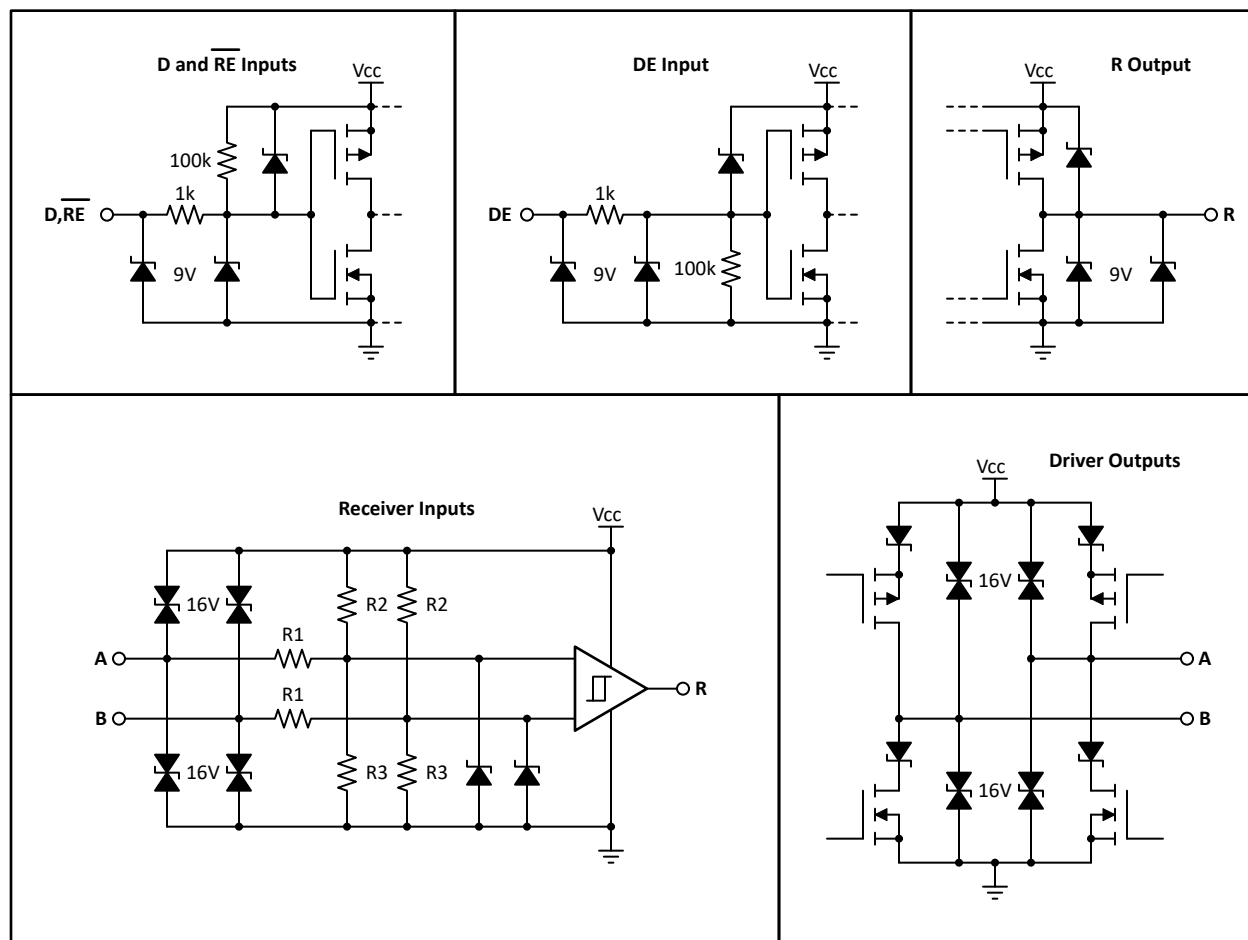
**Table 7-2. Receiver Pin Functions**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state
POLARITY-CORRECTING MODE <sup>(1)</sup>			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	H	Receive polarity corrected bus High
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled

**Table 7-2. Receiver Pin Functions (continued)**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
Open, short, idle Bus	L	?	Indeterminate bus state

- (1) The polarity-correcting mode is entered when  $V_{ID} < V_{IT-}$  and  $t > t_{FS}$  and  $DE = \text{low}$ . This state is latched when  $\overline{RE}$  turns from Low to High.

**Figure 7-3. Equivalent Input and Output Schematic Diagrams**

## 8 Application and Implementation

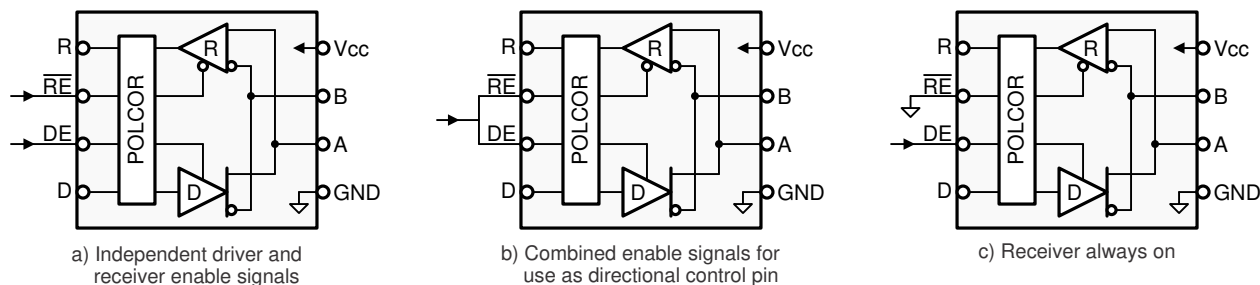
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Device Configuration

The SN65HVD888 is a half-duplex RS-485 transceiver operating from a single 5V  $\pm 10\%$  supply. The driver and receiver enable pins allow for the configuration of different operating modes.



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**Figure 8-1. Transceiver Configurations**

Using independent enable lines provides the most flexible control as the lines allow for the driver and the receiver to be turned on and turned off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not. Only this configuration allows the SN65HVD888 to enter low-power standby mode because it allows both the driver and receiver to be disabled simultaneously.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver enable to ground and controlling only the driver-enable input also uses only one control line. In this configuration a node not only receives the data on the bus sent by other nodes but also receives the data sent on the bus, enabling the node to verify the correct data has been transmitted.

#### 8.1.2 Bus Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with  $Z_0 = 100\Omega$ , and RS-485 cable with  $Z_0 = 120\Omega$ . Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000ft or 1200m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

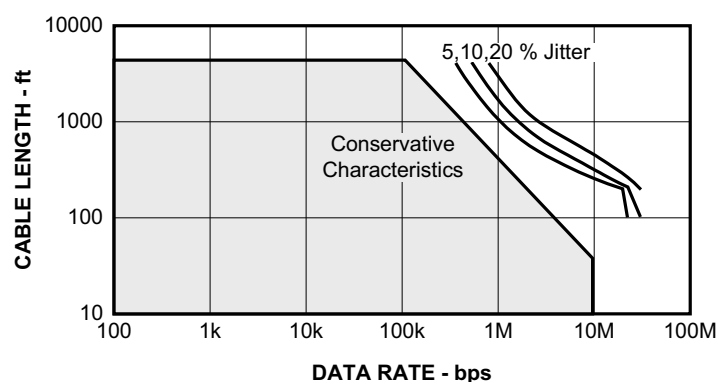
**Table 8-1. VID with a Failsafe Network and Bus Termination**

V <sub>CC</sub>	R <sub>L</sub> DIFFERENTIAL TERMINATION	R <sub>FS</sub> PULLUP	R <sub>FS</sub> PULLDOWN	V <sub>ID</sub>
5V	54Ω	560Ω	560Ω	230mV
		1KΩ	1KΩ	131mV
		4.7KΩ	4.7KΩ	29mV
		10KΩ	10KΩ	13mV

An external failsafe-resistor network must be used to ensure failsafe operation during an idle bus state. When the bus is not actively driven, the differential receiver inputs could float allowing the receiver output to assume a random output. A proper failsafe network forces the receiver inputs to exceed the V<sub>IT</sub> threshold, thus forcing the SN65HVD888 receiver output into the failsafe (high) state. [Table 8-1](#) shows the differential input voltage (V<sub>ID</sub>) for various failsafe networks with a 54-Ω differential bus termination.

### 8.1.3 Cable Length Versus Data Rate

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, applications such as e-metering often operate at rates of up to 250kbps even at distances of 4000ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

**Figure 8-2. Cable Length vs Data Rate Characteristic**

### 8.1.4 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for the short distance is because a stub presents a non-terminated piece of bus line which can introduce reflections if the distance is too long. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, thus leading to a maximum physical stub length of as shown in [Equation 1](#).

$$L_{\text{Stub}} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- $t_r$  is the 10/90 rise time of the driver
- $c$  is the speed of light ( $3 \times 10^8$  m/s or  $9.8 \times 10^8$  ft/s)
- $v$  is the signal velocity of the cable ( $v = 78\%$ ) or trace ( $v = 45\%$ ) as a factor of  $c$

Based on [Equation 1](#), with a minimum rise time of 400 ns, [Equation 2](#) shows the maximum cable-stub length of the SN65HVD888.

$$L_{\text{Stub}} \leq 0.1 \times 400 \times 10^{-9} \times 3 \times 10^8 \times 0.78 = 9.4 \text{ m (or 30.6 ft)} \quad (2)$$



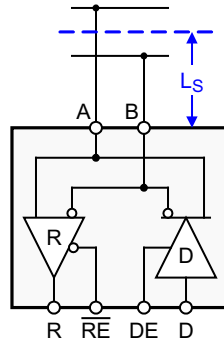


Figure 8-3. Stub Length

### 8.1.5 3 to 5V Interface

Interfacing the SN65HVD888 to a 3V controller is easy. Because the 5V logic inputs of the transceiver accept 3V input signals they can be directly connected to the controller I/O. The 5V receiver output, R, however must be level-shifted by a Schottky diode and a 10k resistor to connect to the controller input (see Figure 8-4). When R is high, the diode is reverse biased and the controller supply potential lies at the controller RxD input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2V lies at the controller RxD input.

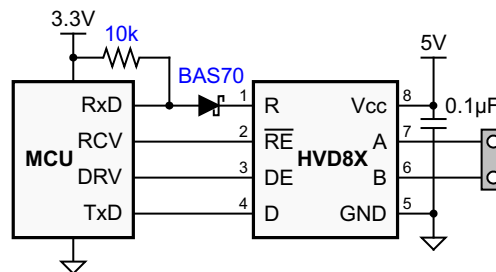


Figure 8-4. 3-V to 5-V Interface

### 8.1.6 Noise Immunity

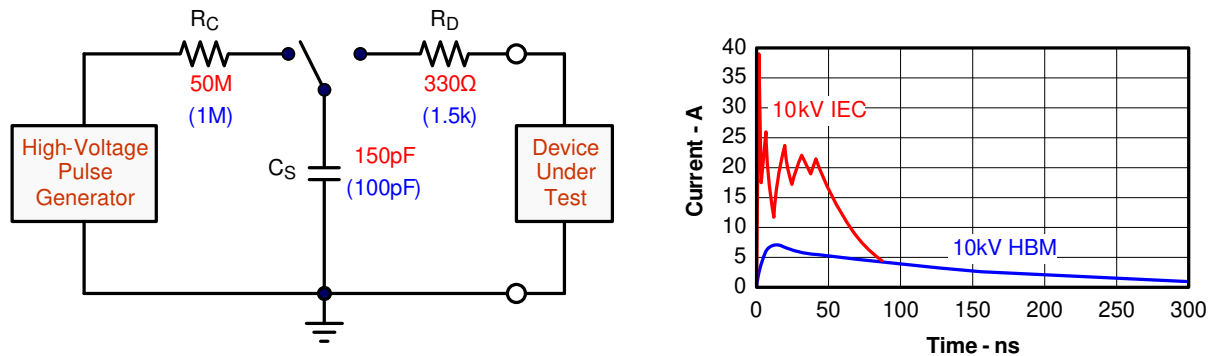
The input sensitivity of a standard RS-485 transceiver is  $\pm 200\text{mV}$ . When the differential input voltage,  $V_{ID}$ , is greater than  $+200\text{mV}$ , the receiver output turns high, for  $V_{ID} < -200\text{mV}$  the receiver outputs low.

The SN65HVD888 transceiver implements high receiver noise-immunity by providing a typical positive-going input threshold of 35mV and a minimum hysteresis of 40 mV. In the case of a noisy input condition therefore, a differential noise voltage of up to  $40\text{mV}_{PP}$  can be present without causing the receiver output to change states from high to low.

### 8.1.7 Transient Protection

The bus terminals of the SN65HVD888 transceiver family possess on-chip ESD protection against  $\pm 16\text{kV}$  HBM and  $\pm 12\text{kV}$  IEC61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_S$ , and 78% lower discharge resistance,  $R_D$  of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.



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**Figure 8-5. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)**

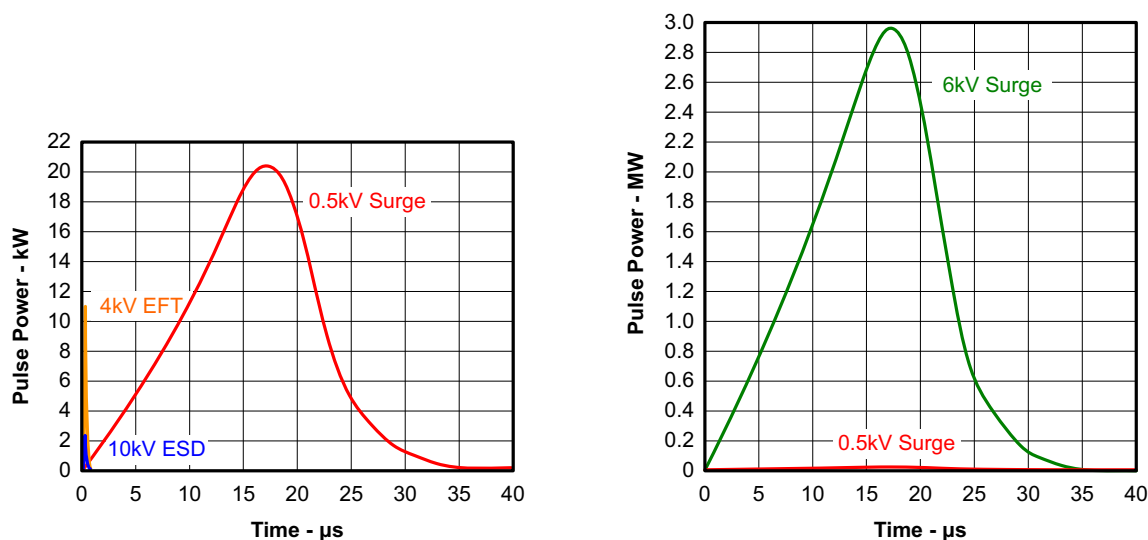
The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients. [Figure 6-9](#) suggests two circuit designs providing protection against short and long duration surge transients, in addition to ESD and Electrical Fast Transients (EFT) transients. [Table 8-2](#) lists the bill of materials for the external protection devices.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

[Figure 8-6](#) compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. In the diagram on the left of [Figure 8-6](#), the tiny blue blip in the bottom left corner represents the power of a 10kV ESD transient, which already dwarfs against the significantly higher EFT power spike, and certainly dwarfs against the 500V surge transient. This type of transient power is well representative of factory environments in industrial and process automation. The diagram on the right of [Figure 8-6](#) compares the enormous power of a 6kV surge transient, most likely occurring in e-metering applications of power generating and power grid systems, with the aforementioned 500V surge transient.

#### Note

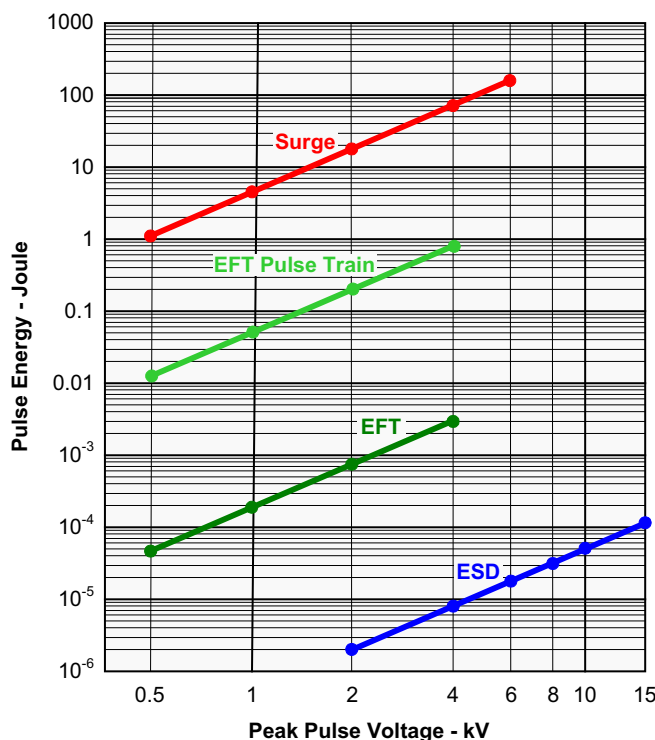
The unit of the pulse-power changes from kW to MW, thus making the power of the 500V surge transient almost dropping off the scale.



**Figure 8-6. Power Comparison of ESD, EFT, and Surge Transients**

In the case of surge transients, high-energy content is signified by long pulse duration and slow decaying pulse power

The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 8-7 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

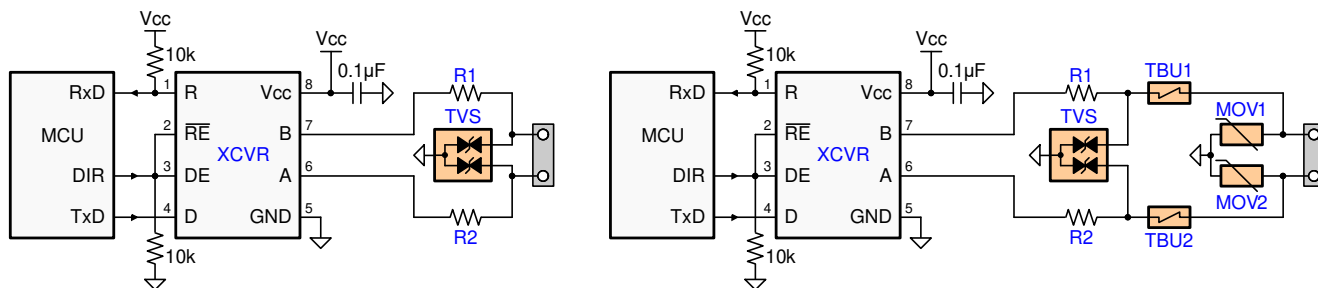


**Figure 8-7. Comparison of Transient Energies**

**Table 8-2. Bill of Materials**

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5V, 250kbps RS-485 Transceiver	SN65HVD888	TI
R1, R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

1. See the [Third-Party Products Disclaimer](#).



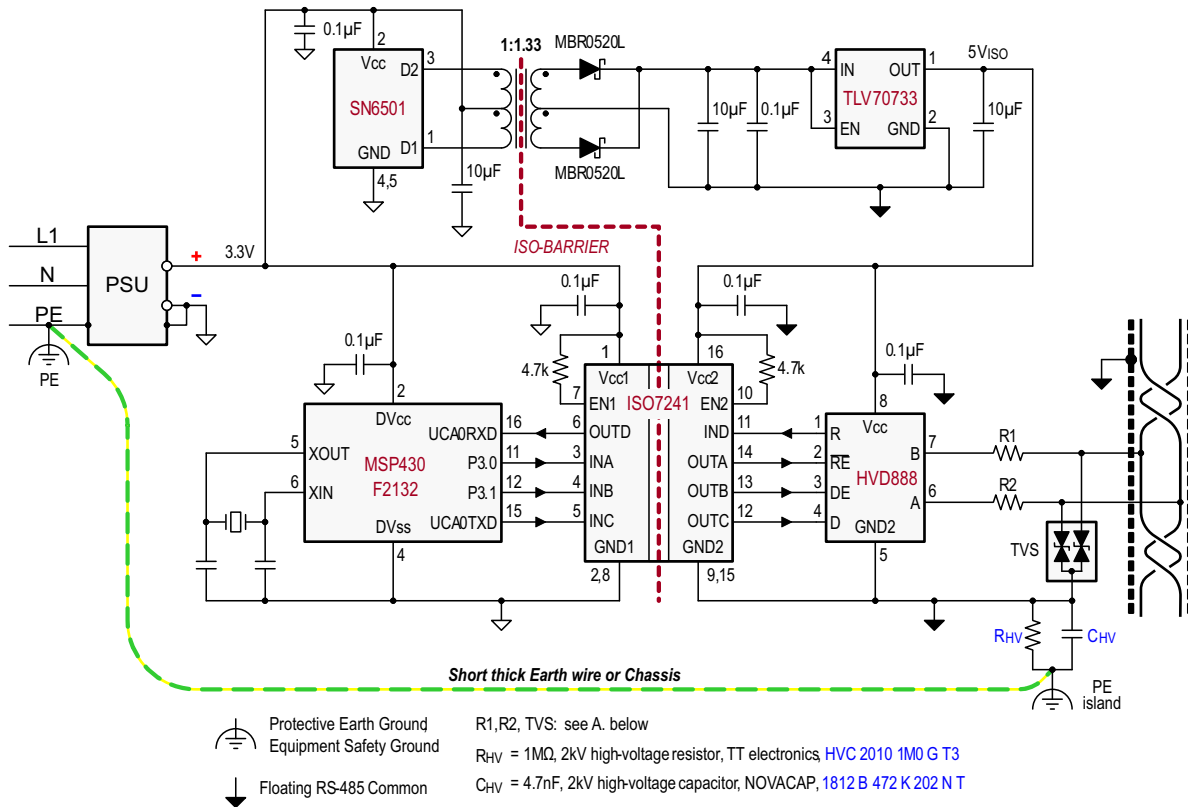
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**Figure 8-8. Transient Protections Against ESD, EFT, and Surge Transients**

The left circuit shown in [Figure 8-8](#) provides surge protection of  $\geq 500\text{V}$  transients, while the right protection circuits can withstand surge transients of  $5\text{kV}$ .

## 8.2 Typical Application

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver through a multi-channel, digital isolator (Figure 8-9).



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A. See Table 8-2.

**Figure 8-9. Isolated Bus Node With Transient Protection**

### 8.2.1 Design Requirements

Example Application: Isolated Bus Node with Transient Protection

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 12kV (per IEC 61000-4-2) and EFTs up to 4kV (per IEC 61000-4-4).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

### 8.2.2 Detailed Design Procedure

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7kΩ resistors to limit input currents during transient events.

While the transient protection is similar to the one in Figure 8-8 (left circuit), an additional high-voltage capacitor diverts transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This diversion is necessary as noise transients on the bus are usually referred to Earth potential.

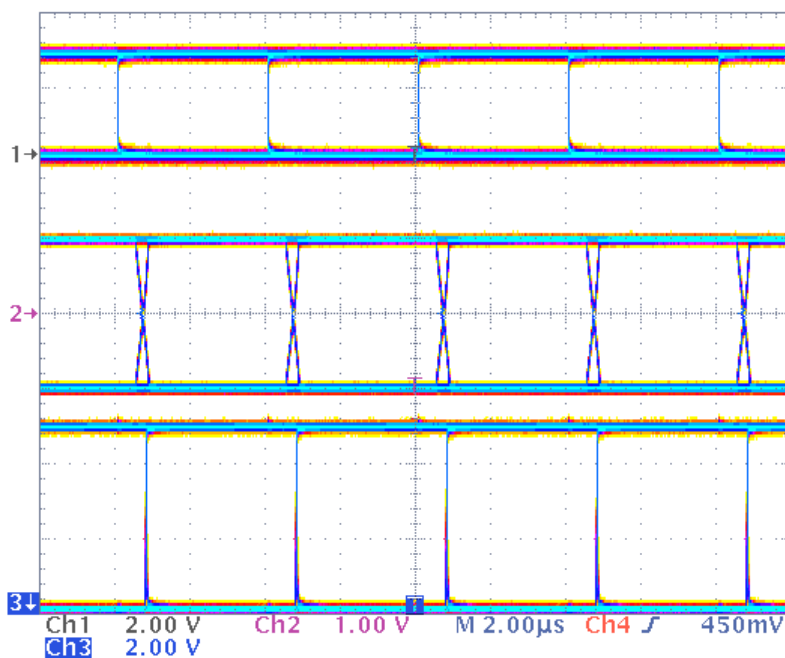
$R_{VH}$  refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge  $C_{HV}$ , if expected that fast transients might charge  $C_{HV}$  to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components,  $C_{HV}$  and  $R_{HV}$ , are connecting to the chassis at the other end.

### 8.2.3 Application Curve



**Figure 8-10. SN65HVD888 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250kbps Operation, PRBS Data Pattern**

## 8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

## 8.4 Layout

### 8.4.1 Layout Guidelines

#### 8.4.1.1 Design and Layout Considerations For Transient Protection

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design.

In order for PCB design to be successful, begin with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.

2. Use  $V_{CC}$  and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100 to 220nF bypass capacitors as close as possible to the  $V_{CC}$ -pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for  $V_{CC}$  and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1 to 10k pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
  - While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few-hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200mA.

#### 8.4.2 Layout Example

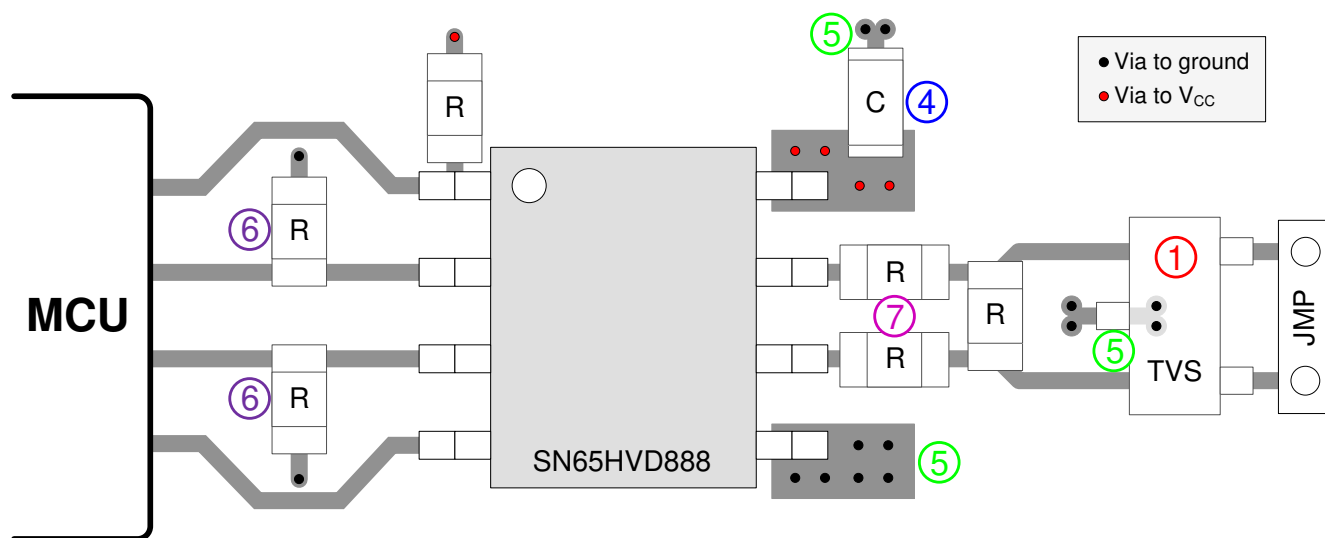


Figure 8-11. SN65HVD888 Layout Example

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Third-Party Products Disclaimer

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### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2018) to Revision D (September 2025)	Page
• Changed all instances of legacy terminology to controller and peripheral where mentioned.....	1
• Removed the 1K resistor in R Output of <a href="#">Figure 7-3</a> .....	13

Changes from Revision B (June 2017) to Revision C (January 2018)	Page
• Changed the Device Information table to the <i>Package Information</i> table.....	1
• Changed 3.3 V <sub>ISO</sub> To: 5V <sub>ISO</sub> in <a href="#">Figure 8-9</a> .....	21



<b>Changes from Revision A (September 2015) to Revision B (June 2017)</b>	<b>Page</b>
• Changed text From: "characterized from –40°C to 85°C" To: "characterized from –40°C to 125°C" in the <i>Description</i> .....	1
• Changed the T <sub>A</sub> MAX value From: 85°C To: 125°C in the <i>Recommended Operating Conditions</i> table.....	5
• Changed I <sub>CC</sub> to show values for the temperature ranges of –40°C to 85°C and –40°C to 125°C in the <i>Electrical Characteristics</i> table.....	6

<b>Changes from Revision * (July 2013) to Revision A (September 2015)</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed JEDEC Standard 22, Test Method A114 (HBM) from ±4 to ±8 kV.....	4
• Changed JEDEC Standard 22, Test Method A115 (Machine Model) from ±100 to ±200 V.....	4
• Changed the "D and $\overline{RE}$ Inputs" circuit and the "DE Input" circuit of <a href="#">Figure 7-3</a> .....	13

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65HVD888D</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888D.A	Active	Production	null (null)	75   TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65HVD888D	HVD888
SN65HVD888D.B	Active	Production	null (null)	75   TUBE	-	NIPDAU	Level-1-260C-UNLIM	See SN65HVD888D	HVD888
<a href="#">SN65HVD888DR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888DR.A	Active	Production	null (null)	2500   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65HVD888DR	HVD888
SN65HVD888DR.B	Active	Production	null (null)	2500   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN65HVD888DR	HVD888

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD888DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD888DR	SOIC	D	8	2500	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD888D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD888D.A	D	SOIC	8	75	507	8	3940	4.32
SN65HVD888D.B	D	SOIC	8	75	507	8	3940	4.32

**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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