TEXAS INSTRUMENTS
SN65HVD3080E, SN65HVD3083E, SN65HVD3086E
SLLS771F – NOVEMBER 2006 – REVISED MARCH 2023

SN65HVD308xE Low-Power RS-485 Full-Duplex Drivers and Receivers

1 Features

- Low quiescent power
  - 375 µA (Typical) Enabled mode
  - 2 nA (Typical) Shutdown mode
- Small MSOP package
- 1/8 Unit-Load—Up to 256 nodes per bus
- 16 kV Bus-pin ESD protection, 6 kV all pins
- Failsafe receiver (bus open, short, idle)
- TIA/EIA-485A Standard compliant
- RS-422 Compatible
- Power-up, power-down glitch-free operation

2 Applications

- Motion controllers
- Point-of-sale (POS) terminals
- Rack-to-rack communications
- Industrial networks
- Power inverters
- Battery-powered applications
- Building automation

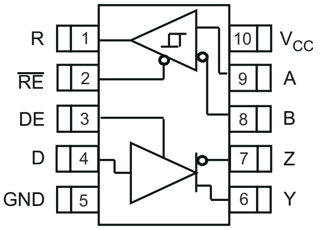
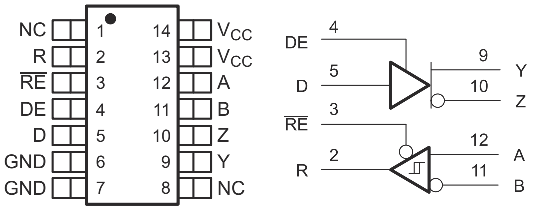


Figure 2-1. DGS Package (Top View)



NC - No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

Figure 2-2. D Package (Top View)

3 Description

Each of these devices is a balanced driver and receiver designed for full-duplex RS-485 or RS-422 data bus networks. Powered by a 5-V supply, they are fully compliant with the TIA/EIA-485A standard.

With controlled bus output transition times, the devices are suitable for signaling rates from 200 kbps to 20 Mbps.

The devices are designed to operate with a low supply current, less than 1 mA (typical), exclusive of the load. When in the inactive shutdown mode, the supply current drops to a few nanoamps, making these devices ideal for power-sensitive applications.

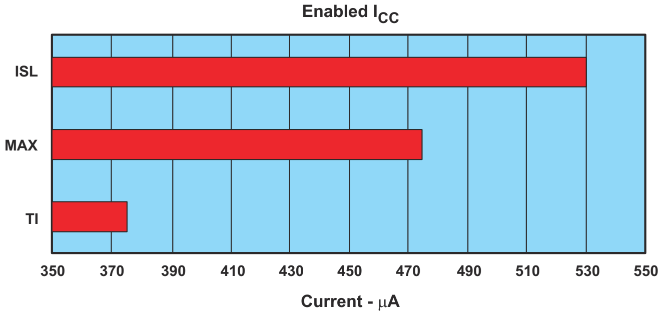
The wide common-mode range and high ESD protection levels of these devices make them suitable for demanding applications such as motion controllers, electrical inverters, industrial networks, and cabled chassis interconnects where noise tolerance is essential.

These devices are characterized for operation over the temperature range -40°C to 85°C

Device Information

PART NUMBER	SIGNALING RATE	PACKAGE[1]
SN65HVD3080E	200 kbps	DGS, DGSR 10-pin MSOP[2]
SN65HVD3083E	1 Mbps	
SN65HVD3086E	20 Mbps	D 14-pin SOIC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The R suffix indicated tape and reel.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2012) to Revision F (March 2023)	Page
• Deleted the Ordering Information table	1
• Added the Device Information table	1
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics*	7

Changes from Revision D (January 2011) to Revision E (November 2012)	Page
• Added Power-Up, Power-Down Glitch-Free Operation to *Features*	1
• Changed ENABLE in DRIVER FUNCTION TABLE from L to L or OPEN	11
• Changed ENABLE in RECEIVER FUNCTION TABLE from H to H or OPEN	11
• Added *Application Information* section	13

Changes from Revision C (December 2009) to Revision D (January 2011)	Page
• Added Differential input voltage dynamic to RECOMMENDED OPERATING CONDITIONS	4
• Added Figure 7-1	11

Changes from Revision B (March 2007) to Revision C ()	Page
• Added D package	1
• Added D package information to Power Dissipation Ratings	3
• Changed Electrostatic Discharge Protection	3
• Changed Supply Current information	4
• Changed Receiver Switching Characteristics	6
• Changed Figure 6-5	8
• Changed Figure 6-6	8

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		UNIT
V_{CC}	Supply voltage range(2)	–0.3 V to 7 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See Figure 6-10 (A, B, Y, Z)	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	-0.3 V to V_{CC}+0.3 V
P_D	Continuous total power dissipation	See the dissipation rating table
T_J	Junction temperature	170°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 Power Dissipation Ratings

PACKAGE	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A < 25°C	T_A = 85°C
10-pin MSOP (DGS)	463 mW	3.71 mW/°C	241 mW
14-pin SOIC (D)	765 mW	6.1 mW/°C	400 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Electrostatic Discharge Protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Human Body Model(1)	A,B,Y,Z, and GND		16		kV
	All pins		6		kV
Charged Device Mode(2)	All pins		1.5		kV
Machine Model(3)	All pins		400		V

(1) Tested in accordance JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and V_{CC}.

(2) Tested in accordance JEDEC Standard 22, Test Method C101.

(3) Tested in accordance JEDEC Standard 22, Test Method A115.

5.4 Supply Current

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D and DE at $V_{CC,}$ No load	Receiver enabled, Driver enabled		375	750	µA
		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled, Driver disabled		300	680	µA
		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled, Driver enabled		240	600	µA
		$\overline{RE}$ and D at V_{CC}, DE at 0 V, No load	Receiver disabled, Driver disabled		2	1000	nA

5.5 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7[1]		12	
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage		–12		12	V
		Dynamic, See Figure 7-1				V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			10	
T_J	Junction temperature				150	°C
T_A	Ambient still-air temperature		–40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.6 Thermal Information

THERMAL METRIC[1]		D (SOIC)	DGS (VSSOP)	UNIT
		14 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	22.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	44.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.2	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.9	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Driver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage	No load, $I_O = 0$	3	4.3	V_{CC}	V
		$R_L = 54\ \Omega$, See Figure 6-1	1.5	2.3		
		$V_{test} = –7$ V to 12 V, See Figure 6-2	1.5			
		$R_L = 100\ \Omega$, See Figure 6-1	2			
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage	$R_L = 54\ \Omega$, See Figure 6-1 and Figure 6-2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 6-3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Common-mode output voltage (Dominant)		-0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			0.5		
$I_{Z(Y)}$ or $I_{Z(Z)}$	High-impedance state output current	$V_{CC} = 0$ V, $V_{(Z)}$ or $V_{(Y)} = 12$ V Other input at 0 V			1	μA
		$V_{CC} = 0$ V, $V_{(Z)}$ or $V_{(Y)} = -7$ V Other input at 0 V	-1			
		$V_{CC} = 5$ V, $V_{(Z)}$ or $V_{(Y)} = 12$ V Other input at 0 V			1	
		$V_{CC} = 5$ V, $V_{(Z)}$ or $V_{(Y)} = -7$ V Other input at 0 V	-1			
I_I	Input current	D, DE	-100		100	μA
I_{OS}	Short-circuit output current	$–7\ V \le V_O \le 12$ V	-250		250	mA

5.8 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	HVD3080E	$R_L = 54\ \Omega$, $C_L = 50$ pF, See Figure 6-4		0.7	1.3	μs
		HVD3083E			150	500	ns
		HVD3086E			12	20	ns
t_r, t_f	Differential output signal rise time Differential output signal fall time	HVD3080E		0.5	0.9	1.5	μs
		HVD3083E			200	300	ns
		HVD3086E			7	15	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$)	HVD3080E			20	200	ns
		HVD3083E			5	50	ns
		HVD3086E			1.4	5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD3080E	$R_L = 110\ \Omega$, $\overline{RE}$ at 0 V, See Figure 6-5		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD3080E	$R_L = 110\ \Omega$, $\overline{RE}$ at 0 V, See Figure 6-6		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZH}, t_{PZL}	Propagation delay time, standby-to-high-level output (See Figure 6-5) Propagation delay time, standby-to-low-level output (See Figure 6-6)		$R_L = 110\ \Omega$, $\overline{RE}$ at 3 V		3.5	7	μs

5.9 Receiver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)](#)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –10 mA		-0.08	–0.01	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 10 mA	–0.2	-0.1		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				30		mV
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –10 mA, See Figure 6-7 and Figure 6-8	4	4.6		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OH} = 10 mA, See Figure 6-7 and Figure 6-8		0.15	0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	–1		1	μA
I_I	Bus input current	Other input at 0V	V_A or V_B = 12 V		0.04	0.11	mA
			V_A or V_B = 12 V, V_{CC} = 0 V		0.06	0.13	
			V_A or V_B = -7 V	–0.1	–0.04		
			V_A or V_B = -7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current		V_{IH} = 2 V	–60	-30		μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V	-60	-30		μA
C_{ID}	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V		7		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

5.10 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 6-8			75	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output				79	100	
$t_{sk(p)}$	Pulse skew (|t_{PHL} – t_{PLH}|)				4	10	
t_r	Output signal rise time				1.5	3	
t_f	Output signal fall time				1.8	3	
t_{PZH}, t_{PZL}	Output enable time		DE at V_{CC}, See Figure 6-9		10	50	ns
		From standby	DE at GND, See Figure 6-9		1.7	3.5	μs
t_{PHZ}, t_{PLZ}	Output disable time	DE at GND or V_{CC}, See Figure 6-9			7	50	ns

5.11 Typical Characteristics

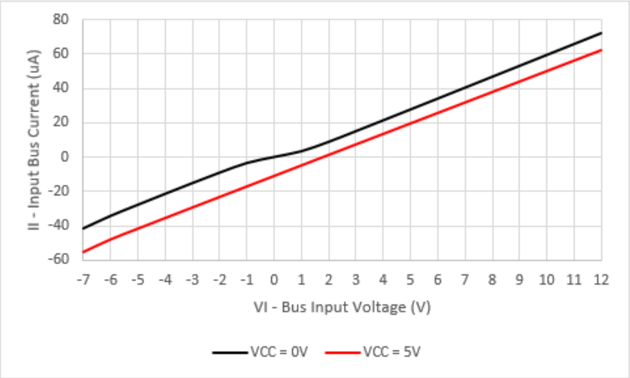


Figure 5-1. Input Bias Current vs BUS Input Voltage

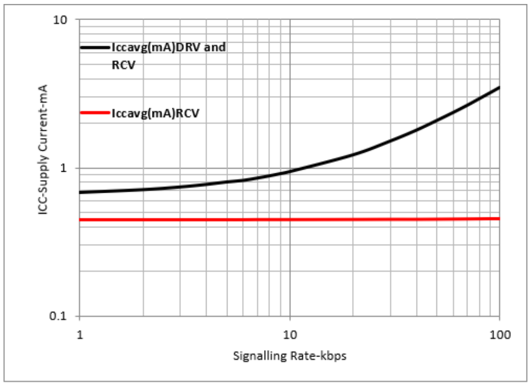


Figure 5-2. HVD3080E Supply Current vs Signaling Rate

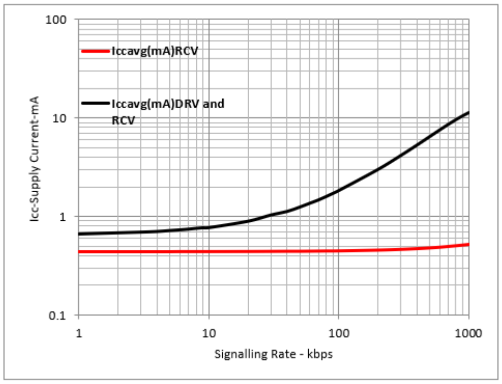


Figure 5-3. HVD3083E Supply Current vs Signaling Rate

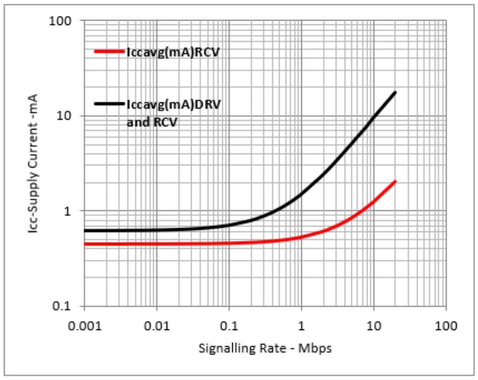


Figure 5-4. HVD3086E Supply Current vs Signaling Rate

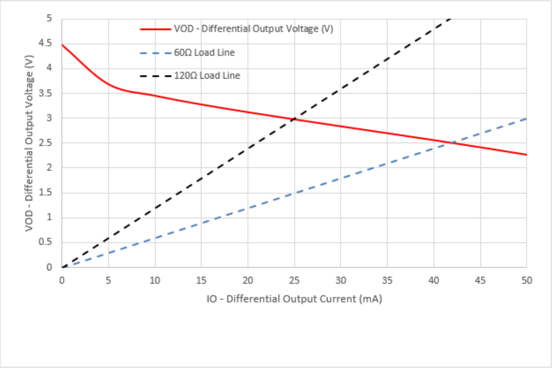


Figure 5-5. Differential Output Voltage vs Differential Output Current

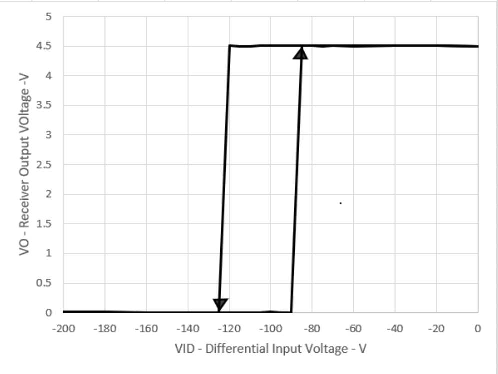


Figure 5-6. Receiver Output Voltage vs Differential Input Voltage

6 Parameter Measurement Information

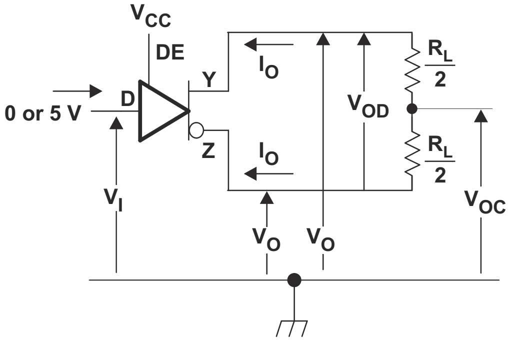


Figure 6-1. Driver V_{OD} Test Circuit and Current Definitions

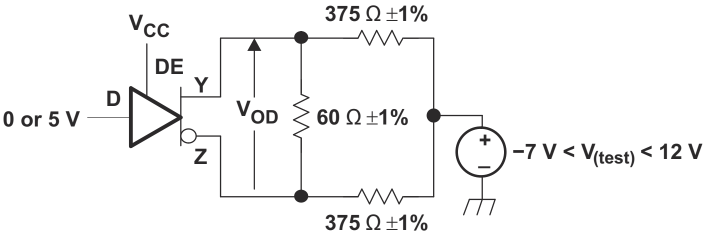


Figure 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit

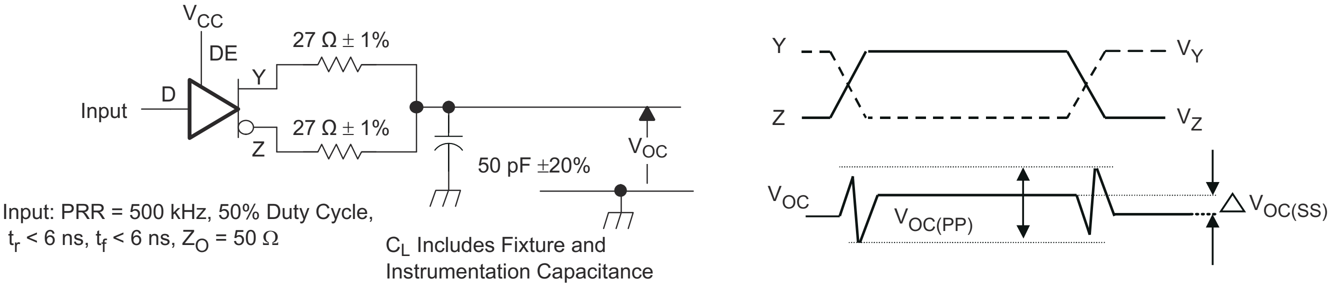


Figure 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

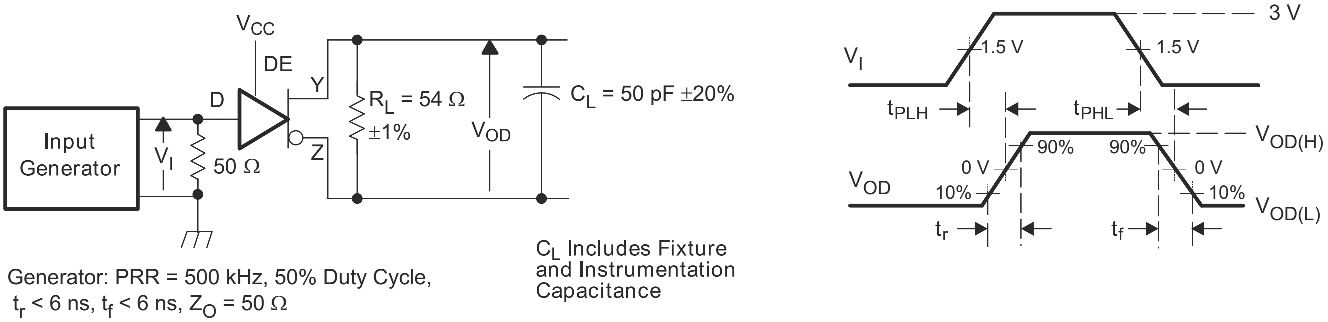
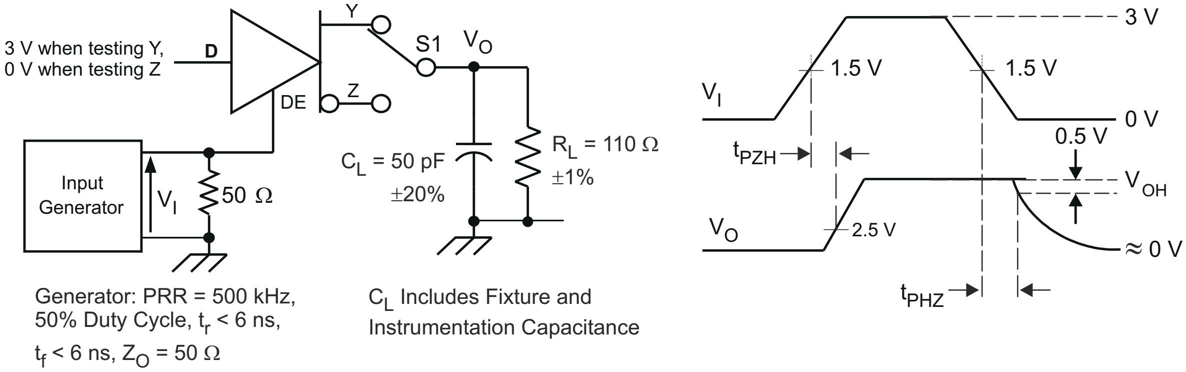


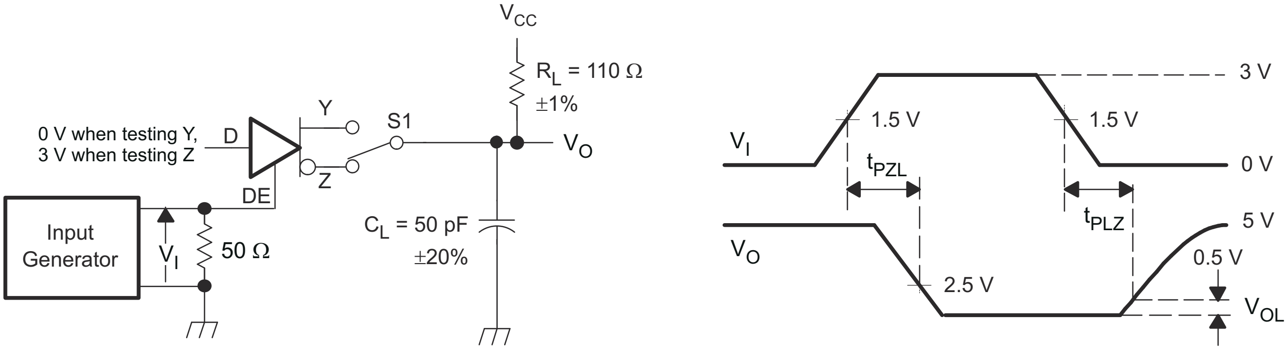
Figure 6-4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$

C_L Includes Fixture and Instrumentation Capacitance

Figure 6-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$

C_L Includes Fixture and Instrumentation Capacitance

Figure 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

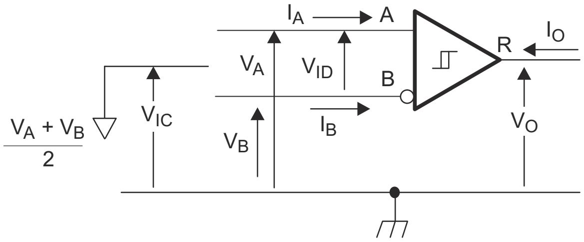
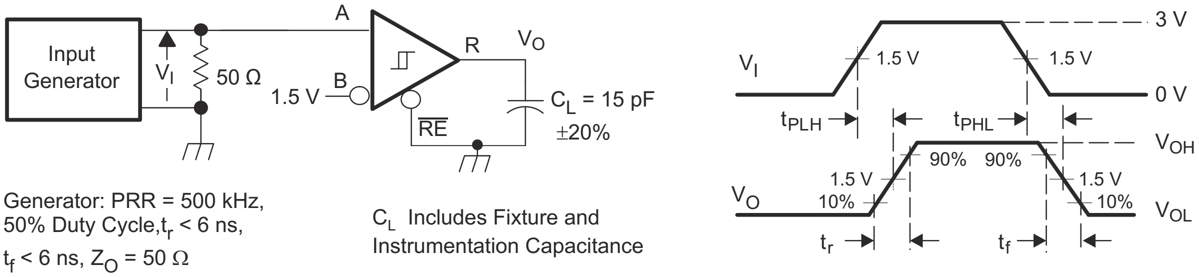


Figure 6-7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_O = 50\ \Omega$

C_L Includes Fixture and Instrumentation Capacitance

Figure 6-8. Receiver Switching Test Circuit and Voltage Waveforms

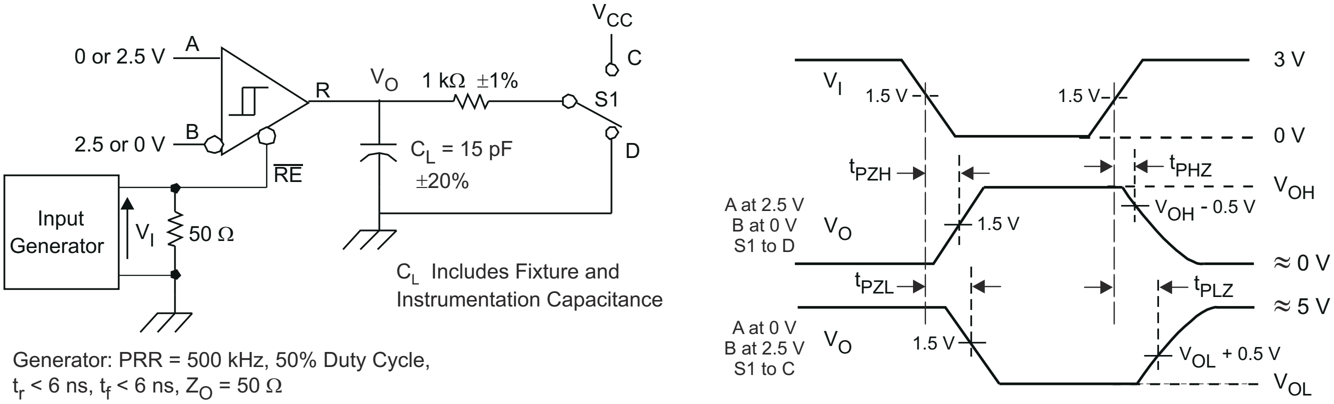
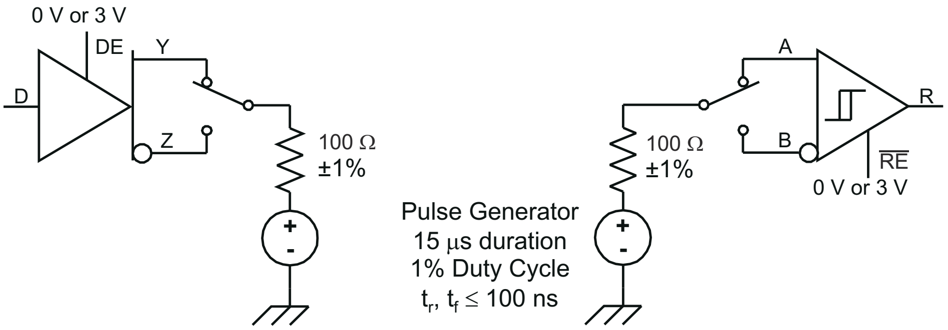


Figure 6-9. Receiver Enable and Disable Test Circuit and Voltage Waveforms



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 6-10. Transient Overvoltage Test Circuit

7 Device Information

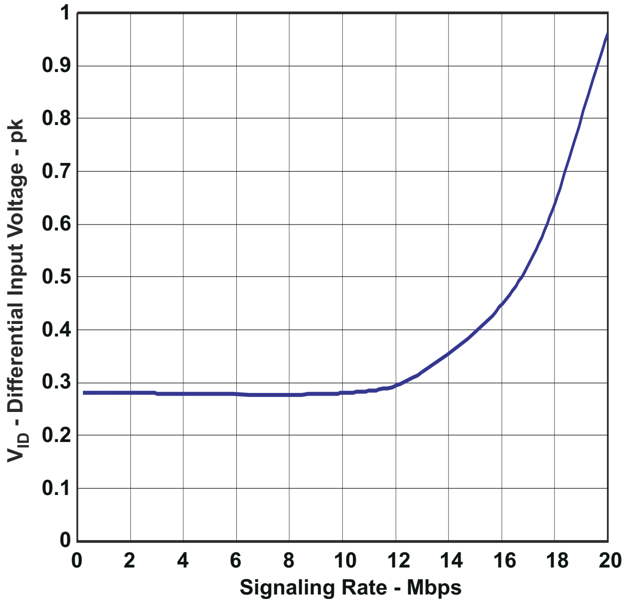


Figure 7-1. Recommended Minimum Differential Input Voltage vs Signaling Rate

7.1 Function Tables

DRIVER

INPUT[1]	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or OPEN	Z	Z
Open	H	H	L

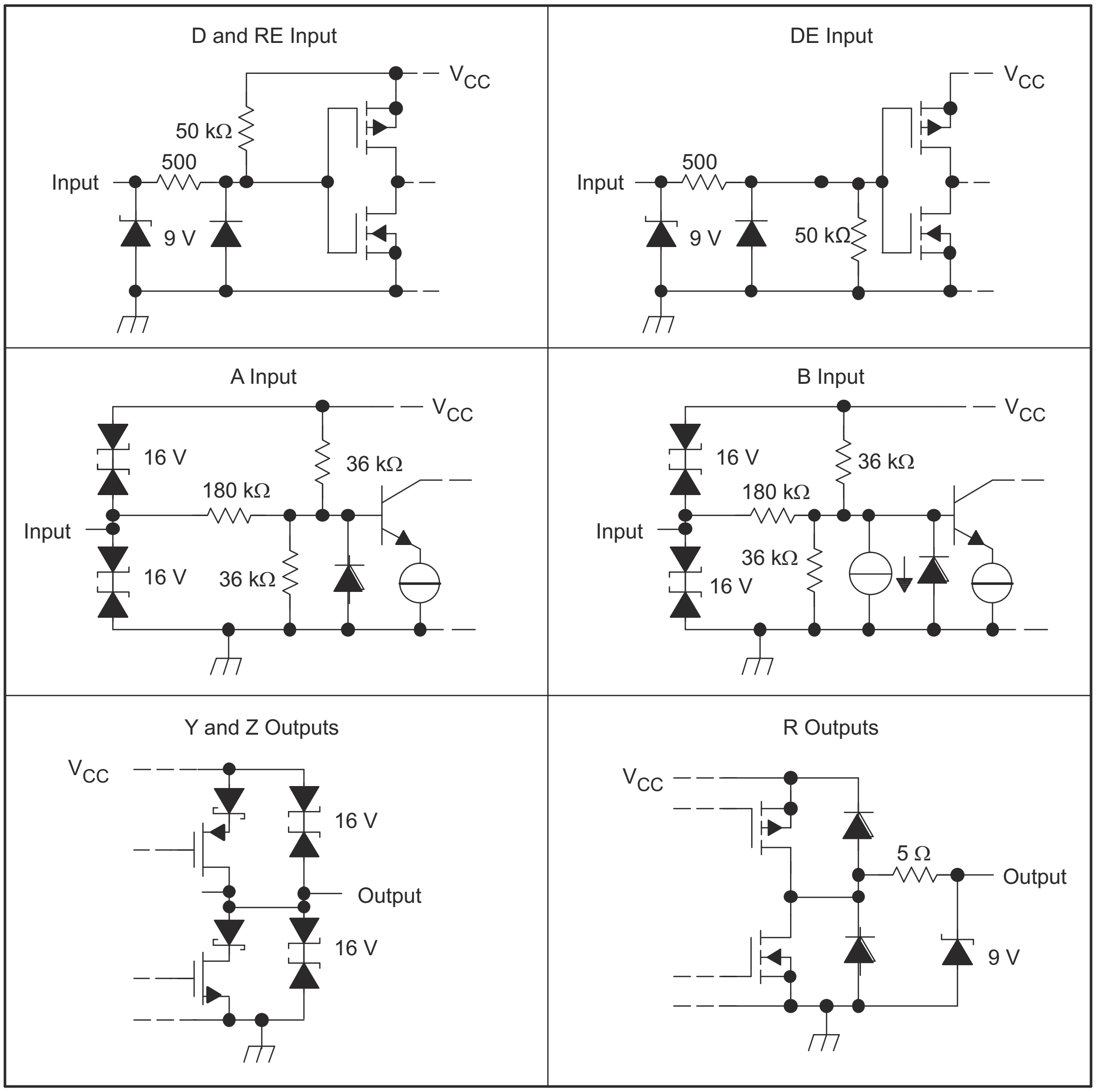
(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

RECEIVER

DIFFERENTIAL INPUTS[1] $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
-0.2 V < V_{ID} < -0.01 V	L	?
-0.01 V ≤ V_{ID}	L	H
X	H or OPEN	Z
Open Circuit	L	H
BUS Idle	L	H
Short Circuit	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

7.2 Equivalent Input and Output Schematic Diagrams



8 Application Information

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD3080EDGS	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 85	BTT
SN65HVD3080EDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTT
SN65HVD3080EDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTT
SN65HVD3083EDGS	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 85	BTU
SN65HVD3083EDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTU
SN65HVD3083EDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTU
SN65HVD3086ED	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HVD3086E
SN65HVD3086EDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTF
SN65HVD3086EDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BTF
SN65HVD3086EDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD3086E
SN65HVD3086EDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD3086E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

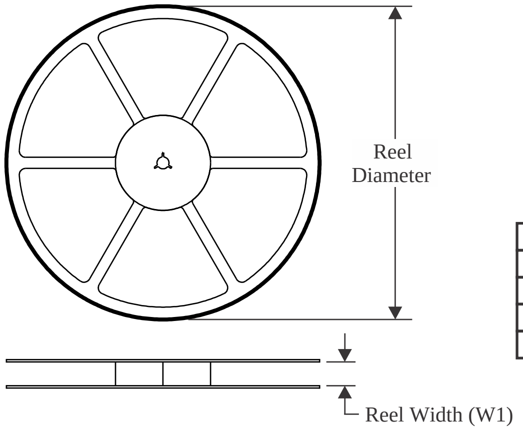
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

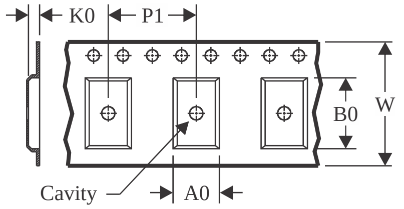
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

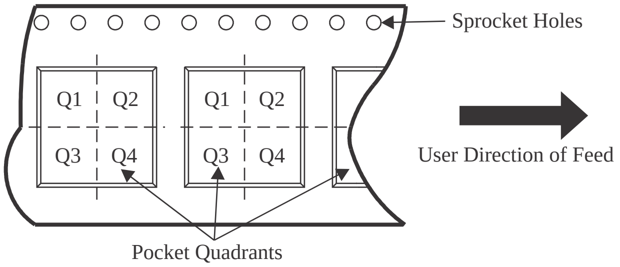


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

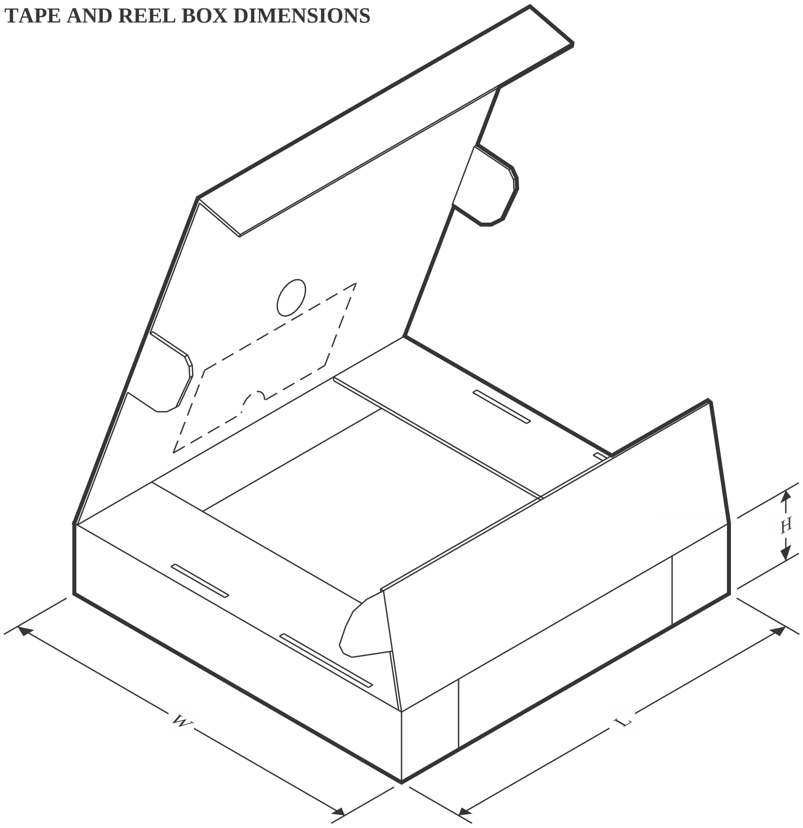
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
SN65HVD3086EDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

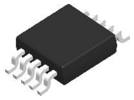
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3086EDR	SOIC	D	14	2500	356.0	356.0	35.0

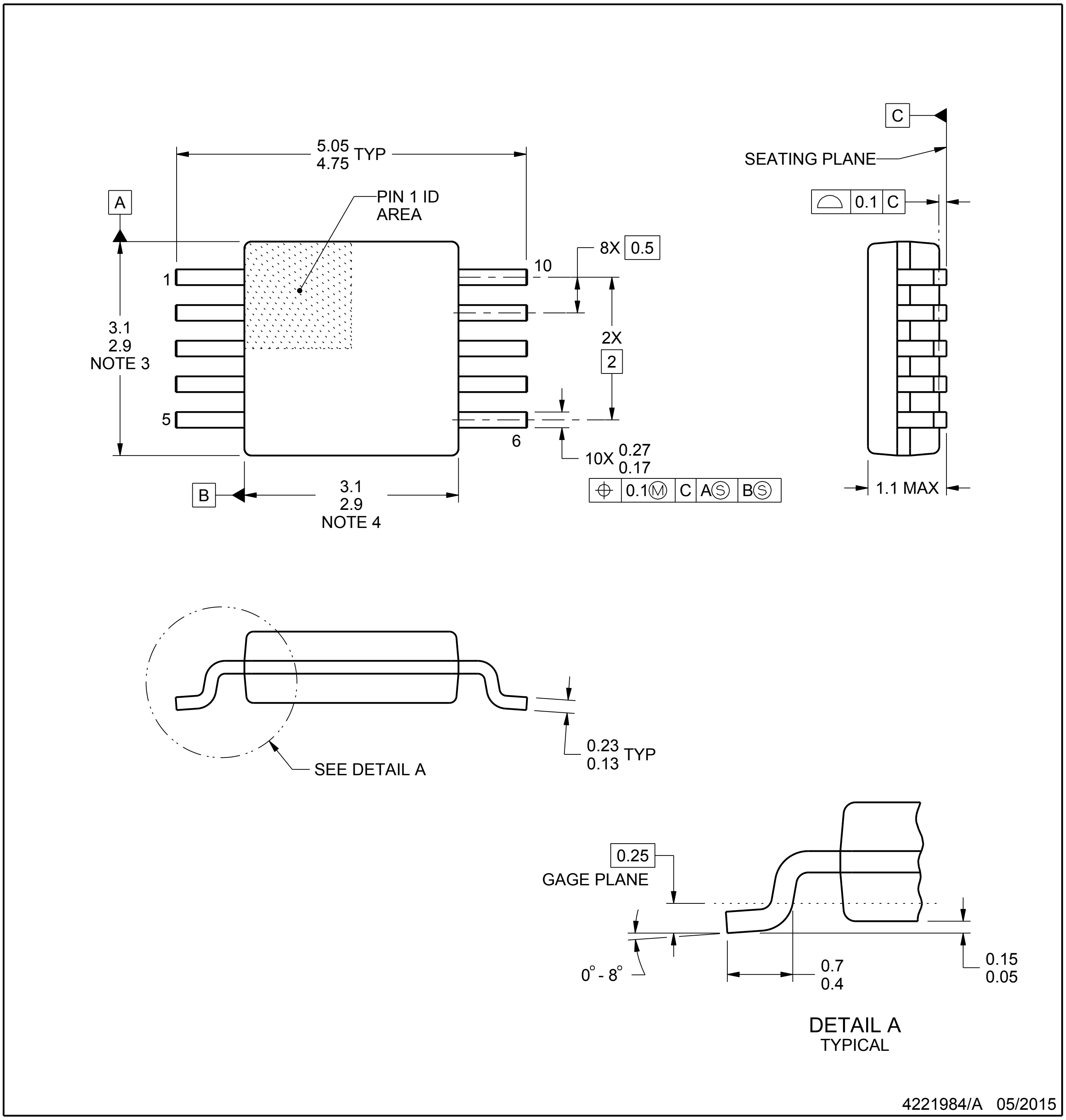
PACKAGE OUTLINE



DGS0010A

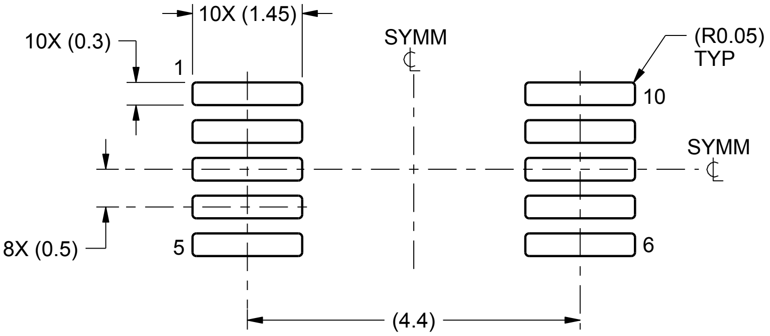
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

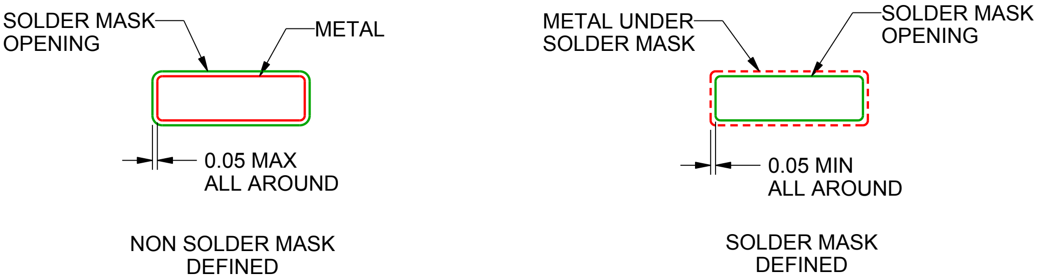


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

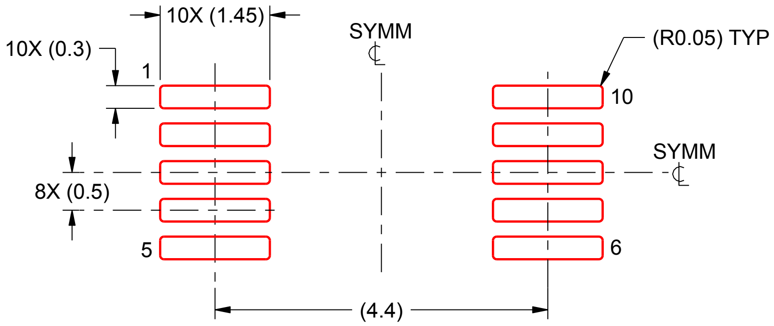


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

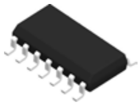


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

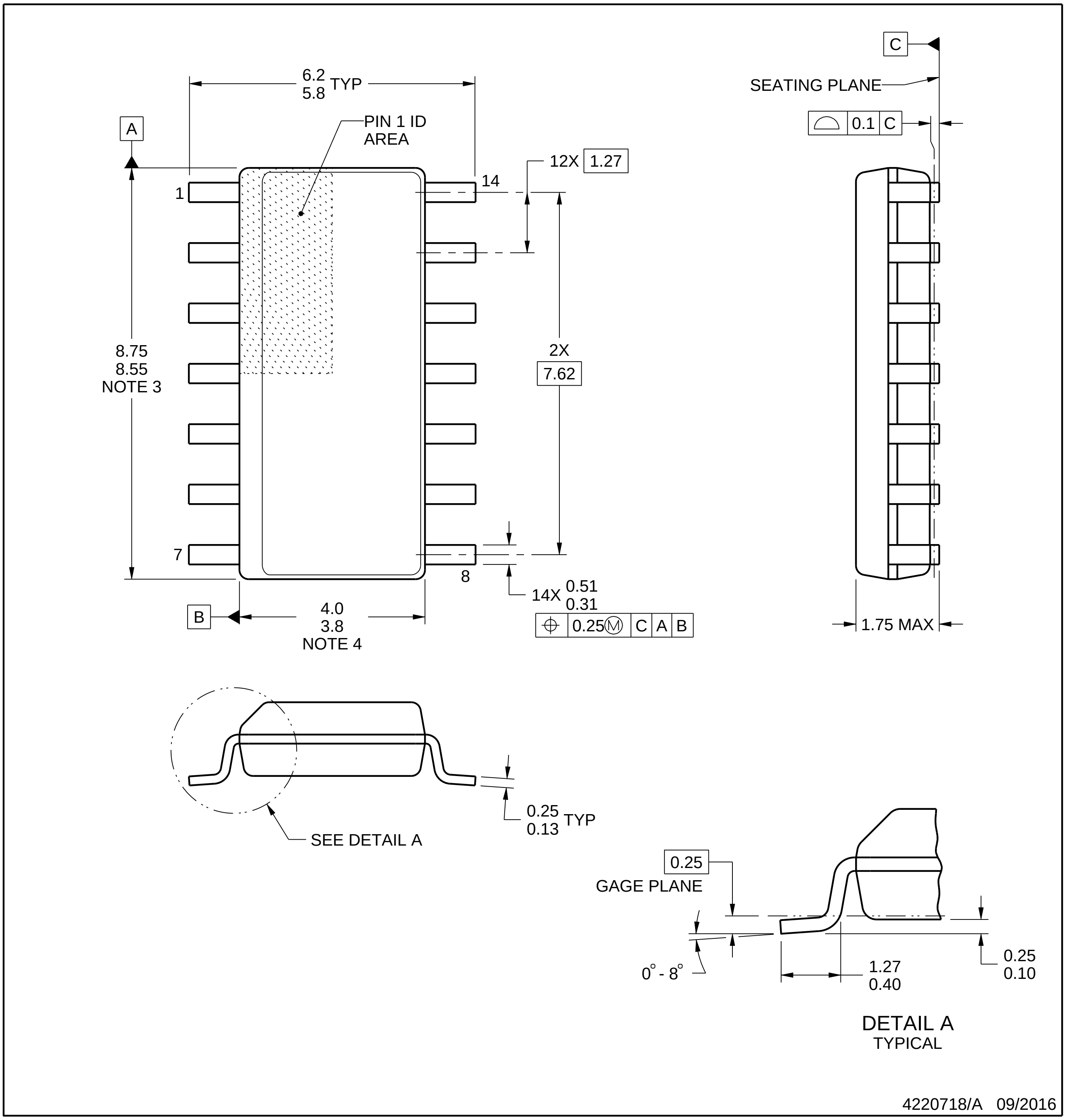
PACKAGE OUTLINE



D0014A

SOIC - 1.75 mm max height

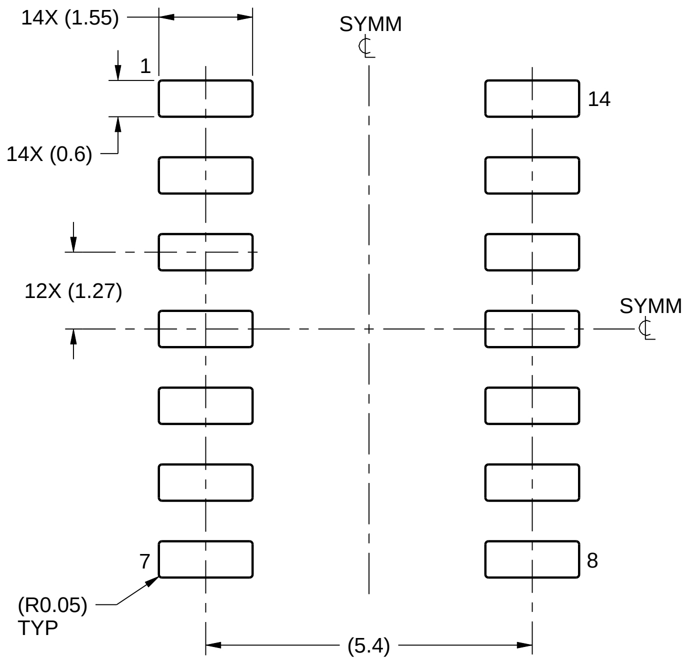
SMALL OUTLINE INTEGRATED CIRCUIT



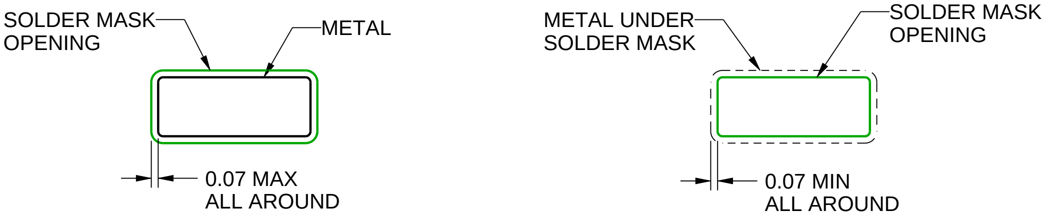
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

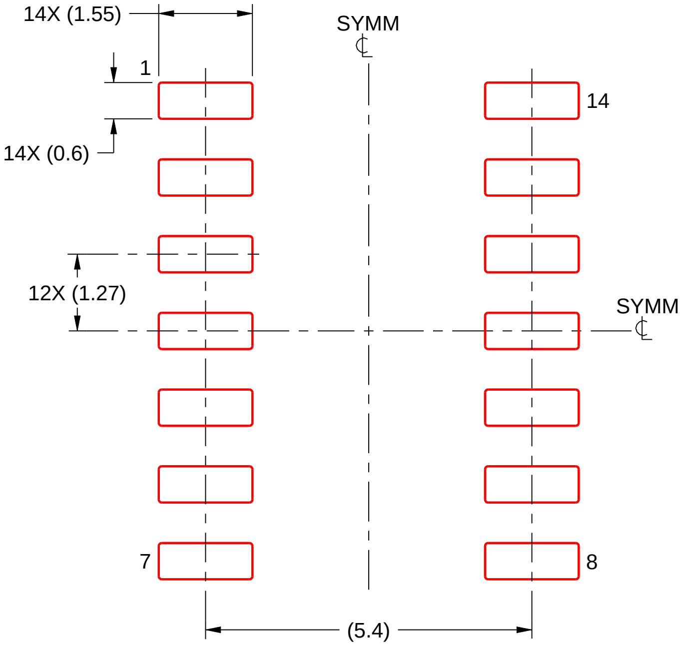
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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