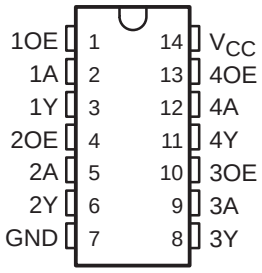
- **State-of-the-Art BiCMOS Design Significantly Reduces $I_{CCZ}$**
- **3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883 Method 3015**
- **High-Impedance State During Power Up and Power Down**
- **Package Options Include Plastic Small-Outline (D) and Standard Plastic 300-mil DIPs (N)**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

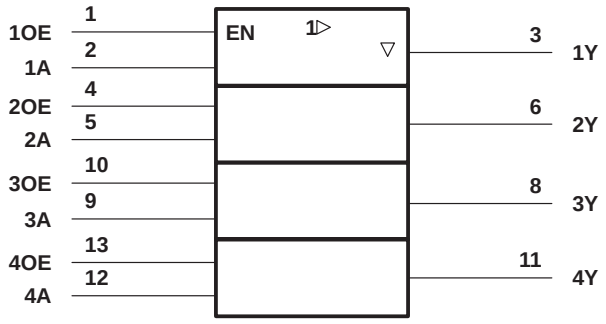
The SN64BCT126A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN64BCT126A is characterized for operation from – 40°C to 85°C and 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

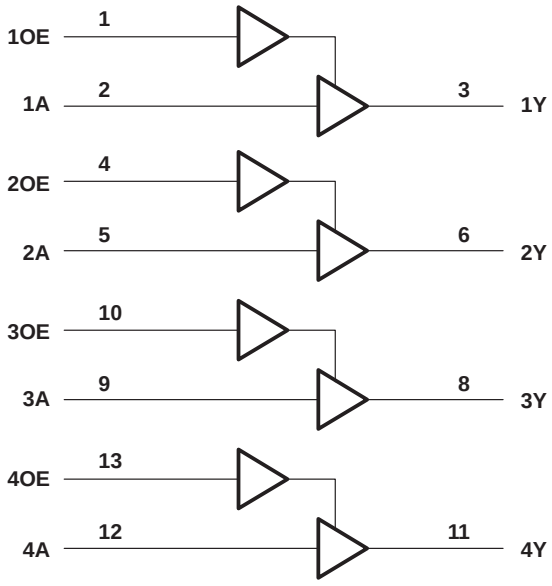
| INPUTS | | OUTPUT |
|---|---|---|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ . . . . . –0.5 V to $V_{CC}$
Current into any output in the low state, $I_O$ . . . . . 128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 127°C/W
N package . . . . . 78°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative voltage rating may be exceeded if the input clamp current rating is observed.
2. The package thermal impedance is calculated in acordane with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

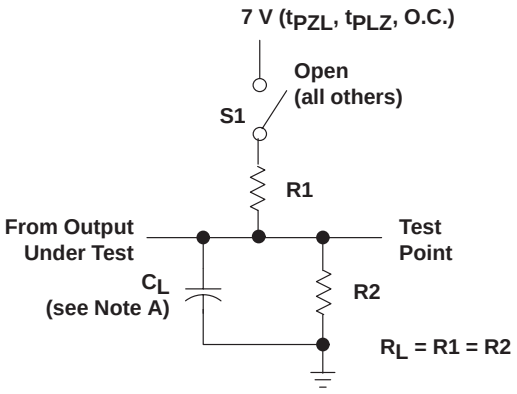
| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = –15 mA | | 2 | 3.1 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = 64 mA | | | 0.42 | 0.55 | V |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | µA |
| $I_{OZ}$ | $V_{CC}$ = 0 to 1.3 V (power up) | $V_O$ = 2.7 V or 0.5 V, | OE at 2 V | | | ±50 | µA |
| | $V_{CC}$ = 1.3 V to 0 (power down) | | | | | ±50 | |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 25 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | | –20 | µA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | –100 | | –225 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V | | | | 35 | 51 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V | | | | 21 | 33 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V | | | | 5 | 10 | mA |
| $C_i$ | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 4 | | pF |
| $C_o$ | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 9 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

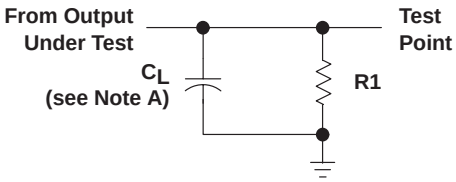
## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$ = –40°C to 85°C | | $T_A$ = 0°C to 70°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.5 | 3.6 | 4.9 | 1.5 | 6.3 | 1.5 | 6.3 | ns |
| $t_{PHL}$ | | | 2.7 | 5.3 | 6.9 | 2.7 | 7.7 | 2.7 | 7.4 | |
| $t_{PZH}$ | OE | Y | 2.6 | 4.8 | 6.4 | 2.6 | 7.9 | 2.6 | 7.9 | ns |
| $t_{PZL}$ | | | 3.7 | 6.4 | 8.3 | 3.7 | 10.5 | 3.7 | 10 | |
| $t_{PHZ}$ | OE | Y | 3.2 | 6.6 | 8.2 | 3.2 | 10 | 3.2 | 10 | ns |
| $t_{PLZ}$ | | | 3.4 | 6.5 | 8 | 3.4 | 12.3 | 3.4 | 10.7 | |

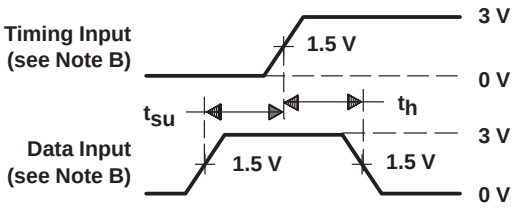
## PARAMETER MEASUREMENT INFORMATION



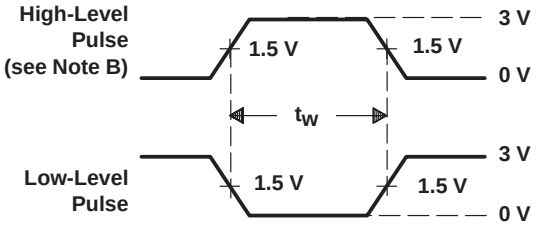

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



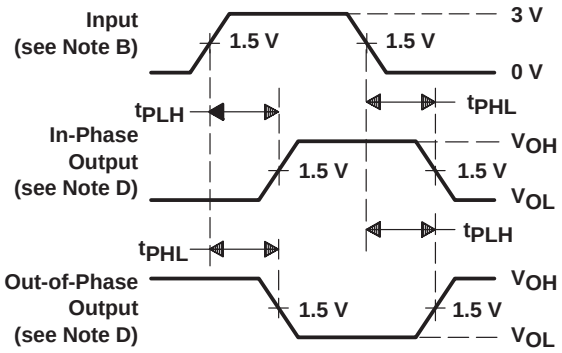

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



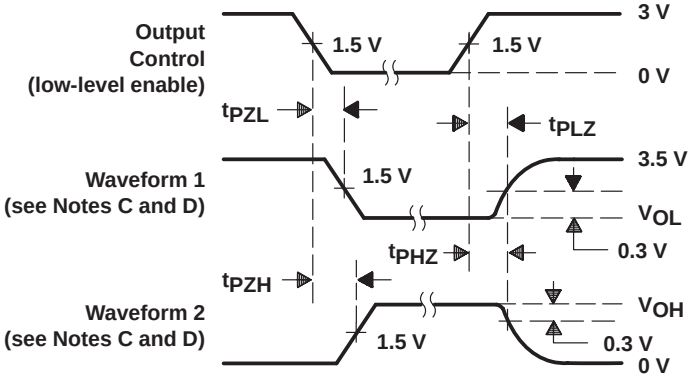

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN64BCT126AD | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 6BCT126A |
| SN64BCT126AD.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 6BCT126A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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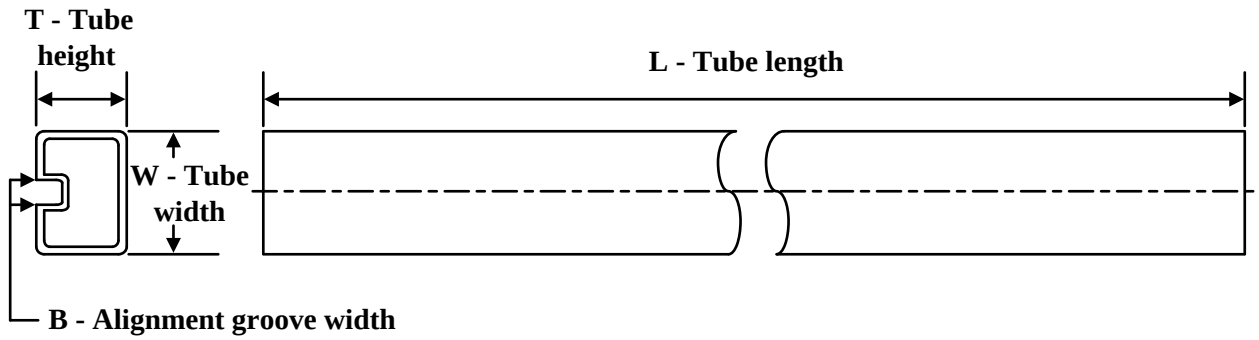
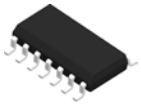
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN64BCT126AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN64BCT126AD.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

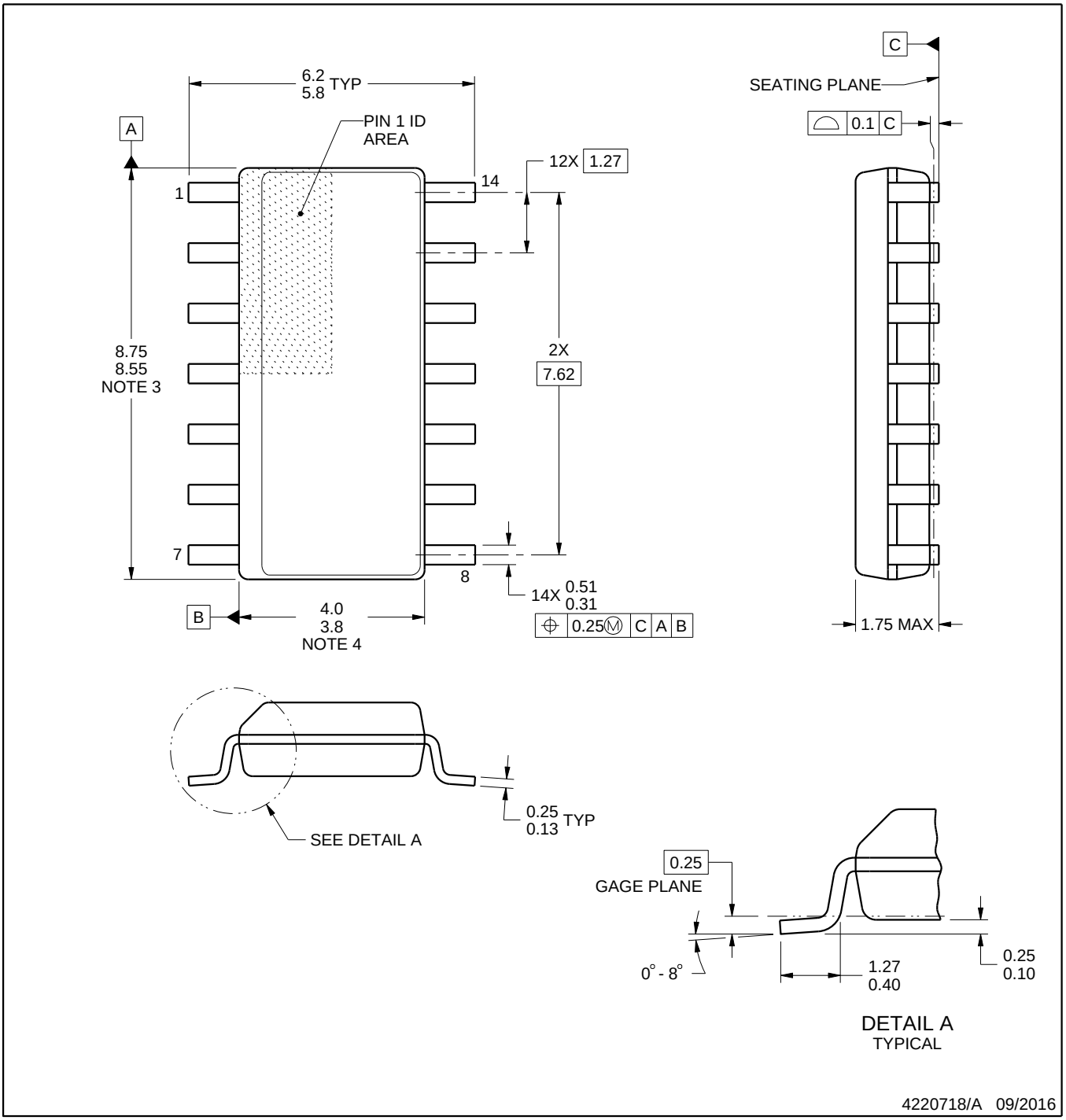


# PACKAGE OUTLINE

## D0014A

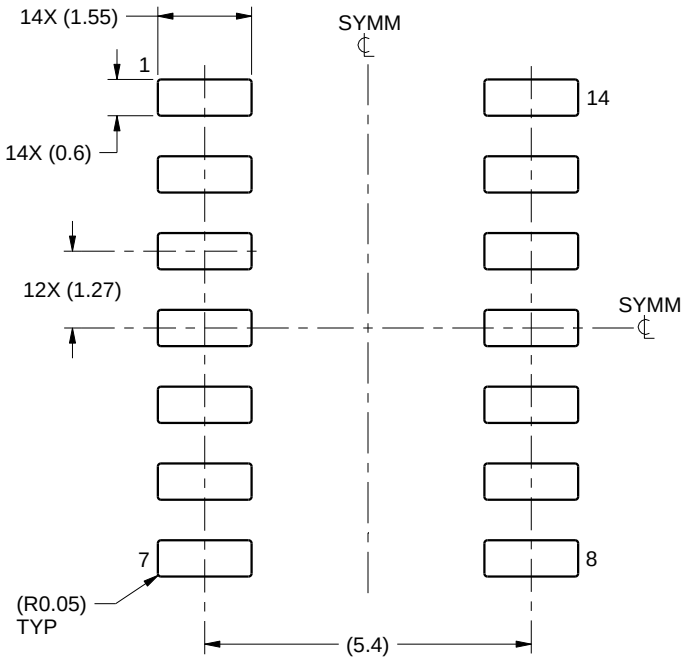
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

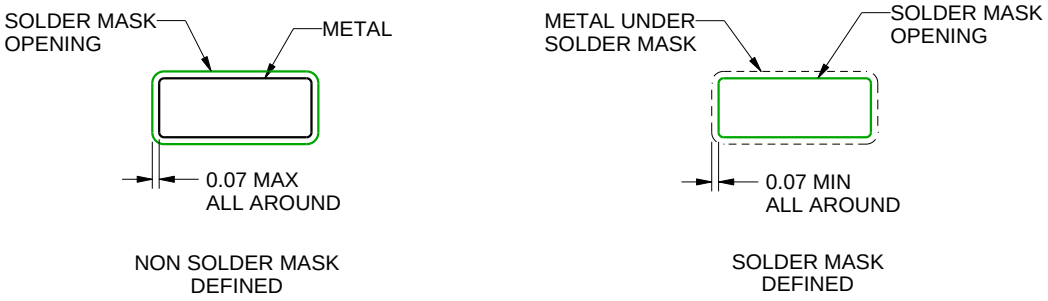



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

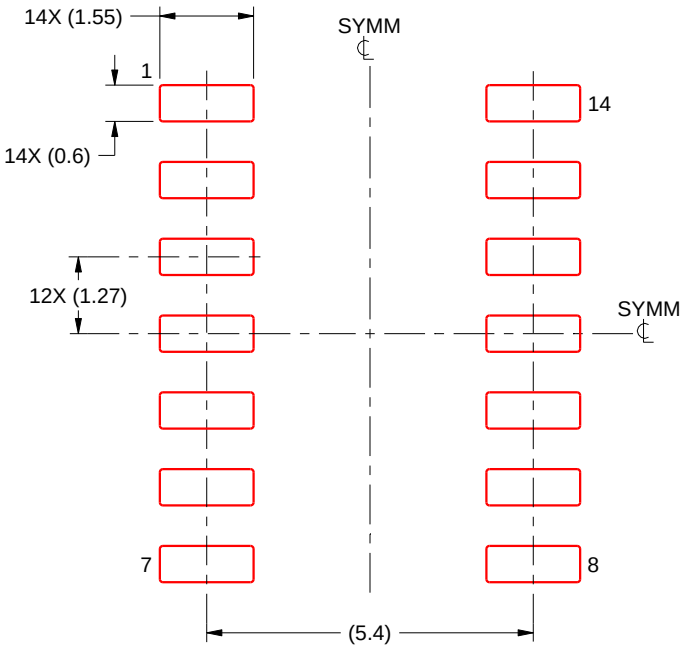
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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