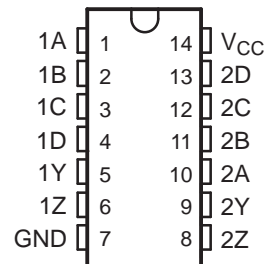


## RAD-TOLERANT CLASS V, DUAL DIFFERENTIAL LINE DRIVER

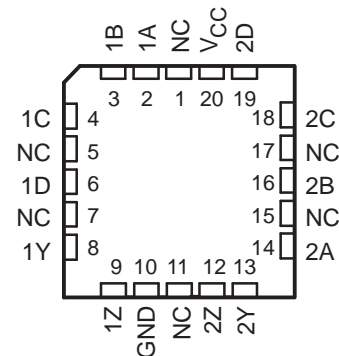
### FEATURES

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830
- Rad-Tolerant: >40 KRad(Si) TID
- QML-V Qualified, SMD 5962-79008

SN55183 . . . J OR W PACKAGE  
(TOP VIEW)



SN55183 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

### DESCRIPTION

The SN55183 dual differential line driver is designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The device can be used as a TTL expander/phase splitter, because the output stages are similar to TTL totem-pole outputs.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### PACKAGING/ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	J package	5962-7900801VCA	5962-7900801VCA
	W package	5962-7900801VDA	5962-7900801VDA

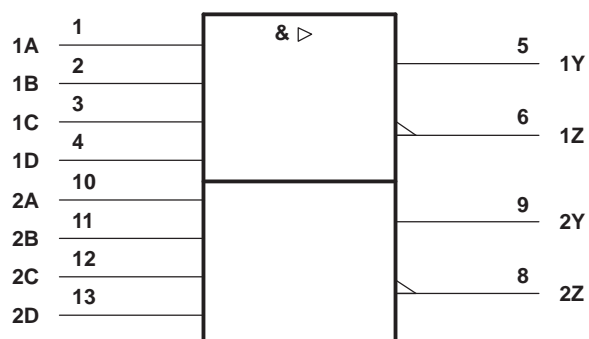
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



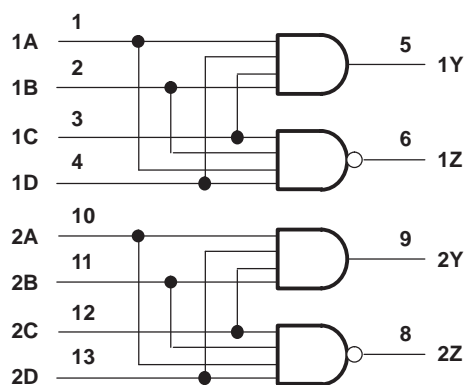
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Logic Symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the J and W packages.

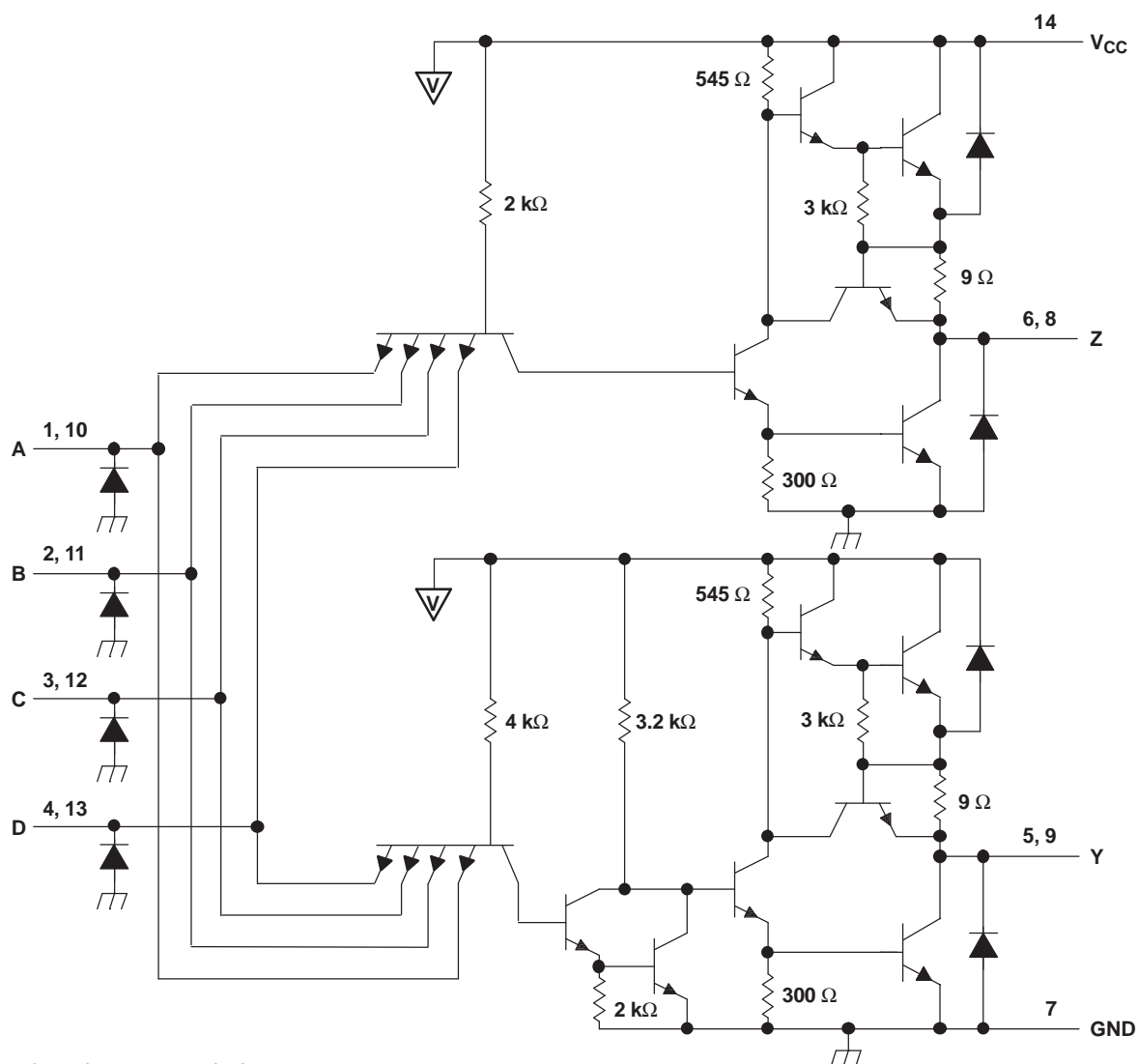
## Logic Diagram (Positive Logic)



**Positive logic:**  $y = ABCD$ ,  $Z = \overline{ABCD}$

Pin numbers shown are for the J and W packages.

## Schematic (Each Driver)



Resistor values shown are nominal.  
Pin numbers shown are for the J and W packages.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		7	V
V <sub>I</sub>	Input voltage		5.5	V
	Duration of output short circuit <sup>(3)</sup>		1	s
	Continuous total power dissipation	See Dissipation Ratings Table		
T <sub>stg</sub>	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package		300 °C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Not more than one output should be shorted to ground at any one time.

## DISSIPATION RATINGS

PACKAGE <sup>(1)</sup>	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

(1) SN55183 chips are alloy mounted.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–40	mA
$I_{OL}$	Low-level output current			40	mA
$T_A$	Operating free-air temperature	–55		125	°C

## ELECTRICAL CHARACTERISTICS

over recommended ranges of  $V_{CC}$  and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	Y (AND) outputs	$V_{IH} = 2\text{ V}$	$I_{OH} = -0.8\text{ mA}$	2.4			V
				$I_{OH} = -40\text{ mA}$	1.8	3.3		
$V_{OL}$	Low-level output voltage	Y (AND) outputs	$V_{IL} = 0.8\text{ V}$	$I_{OL} = 32\text{ mA}$		0.2		V
				$I_{OL} = 40\text{ mA}$		0.22	0.4	
$V_{OH}$	High-level output voltage	Z (NAND) outputs	$V_{IL} = 0.8\text{ V}$	$I_{OH} = -0.8\text{ mA}$	2.4			V
				$I_{OH} = -40\text{ mA}$	1.8	3.3		
$V_{OL}$	Low-level output voltage	Z (NAND) outputs	$V_{IH} = 2\text{ V}$	$I_{OL} = 32\text{ mA}$		0.2		V
				$I_{OL} = 40\text{ mA}$		0.22	0.4	
$I_{IH}$	High-level input current		$V_{IH} = 2.4\text{ V}$				120	$\mu\text{A}$
$I_I$	Input current at maximum input voltage		$V_{IH} = 5.5\text{ V}$				2	mA
$I_{IL}$	Low-level input current		$V_{IL} = 0.4\text{ V}$				-4.8	mA
$I_{OS}$	Short-circuit output current <sup>(2)</sup>		$V_{CC} = 5\text{ V}, T_A = 125^\circ\text{C}^{(3)}$		-40	-100	-120	mA
$I_{CC}$	Supply current (average per driver)		$V_{CC} = 5\text{ V},$ All inputs at 5 V, No load			10	18	mA

(1) All typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

(2) Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

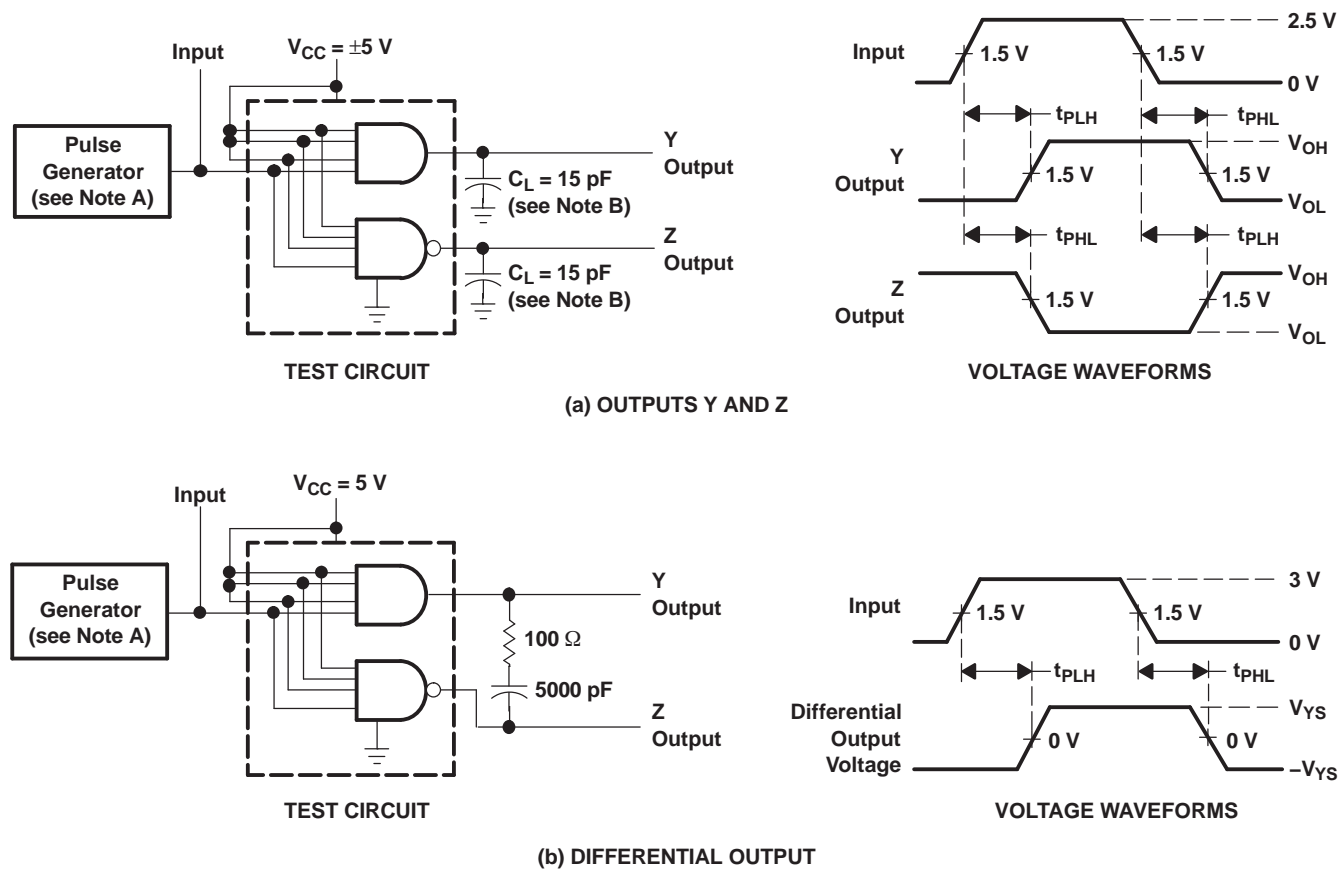
(3)  $T_A = 125^\circ\text{C}$  is applicable to SN55183 only.

## SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level Y output	AND gates	$C_L = 15\text{ pF},$ See Figure 1(a)		8	12	ns
$t_{PHL}$	Propagation delay time, high- to low-level Y output	AND gates	$C_L = 15\text{ pF},$ See Figure 1(a)		12	18	ns
$t_{PLH}$	Propagation delay time, low- to high-level Z output	NAND gates	$C_L = 15\text{ pF},$ See Figure 1(a)		6	12	ns
$t_{PHL}$	Propagation delay time, high- to low-level Z output	NAND gates	$C_L = 15\text{ pF},$ See Figure 1(a)		6	8	ns
$t_{PLH}$	Propagation delay time, low- to high-level differential output	Y output with respect to Z output, $R_L = 100\ \Omega$ in series with 5000 pF, See Figure 1(b)			9	16	ns
$t_{PHL}$	Propagation delay time, high- to low-level differential output	Y output with respect to Z output, $R_L = 100\ \Omega$ in series with 5000 pF, See Figure 1(b)			8	16	ns

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics:  $Z_O = 50\ \Omega$ ,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ ,  $t_w = 0.5\ \mu\text{s}$ ,  $\text{PRR} \leq 1\ \text{MHz}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Waveforms are monitored on an oscilloscope with  $r_i \geq 1\ \text{M}\Omega$ .

**Figure 1. Test Circuits and Voltage Waveforms**

# **TYPICAL CHARACTERISTICS<sup>(1)</sup>**

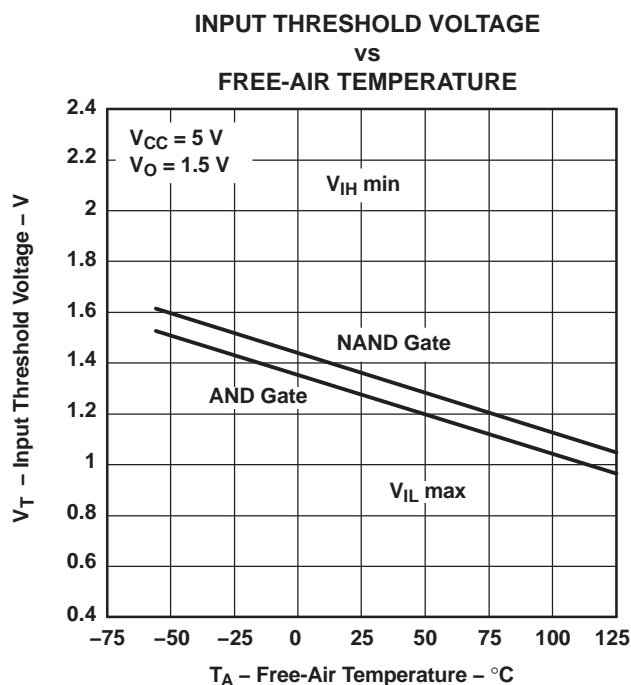


Figure 2.

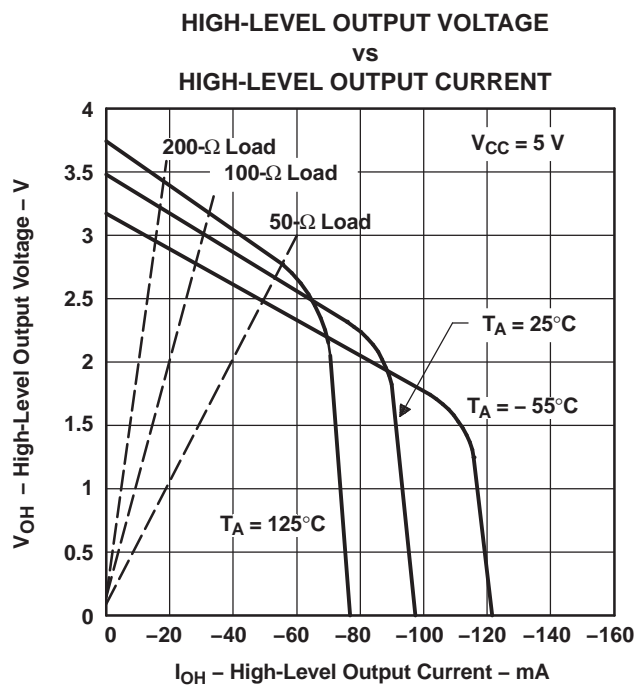


Figure 3.

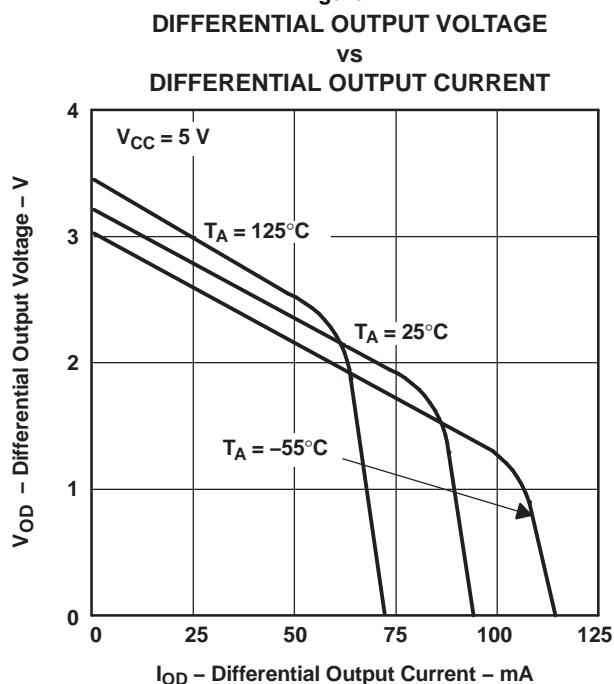


Figure 4.

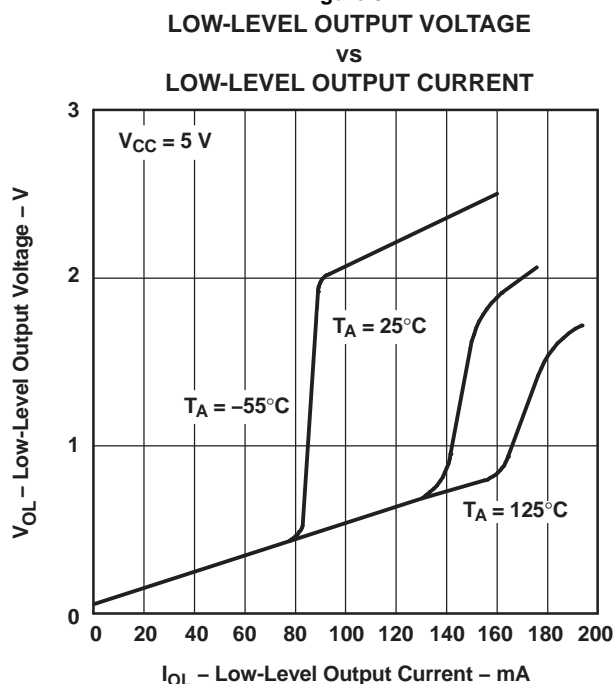


Figure 5.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

# TYPICAL CHARACTERISTICS<sup>(2)</sup> (continued)

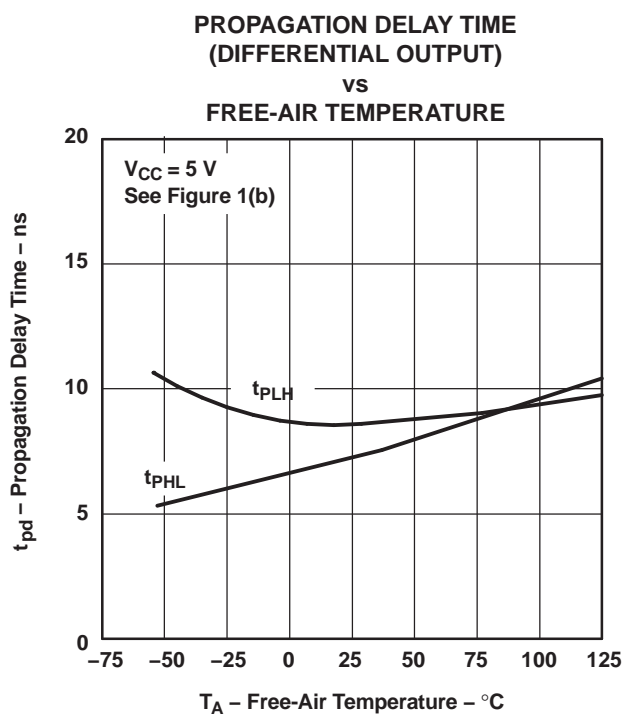


Figure 6.

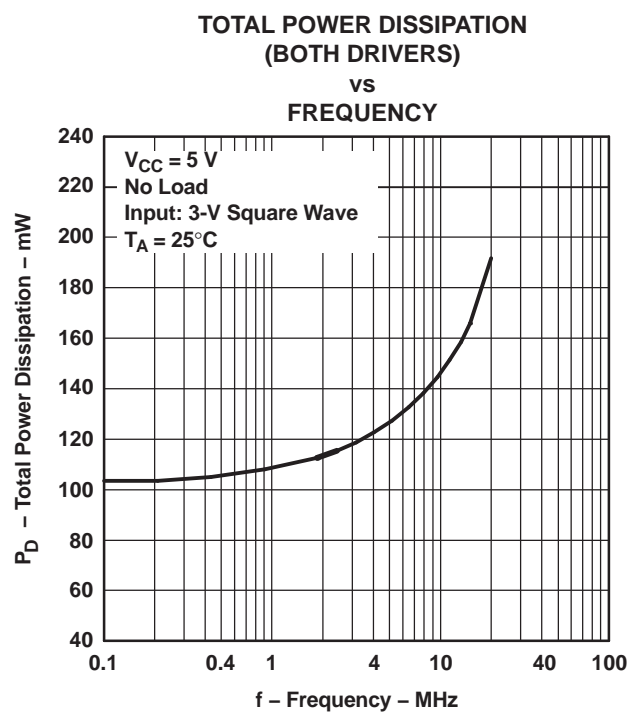
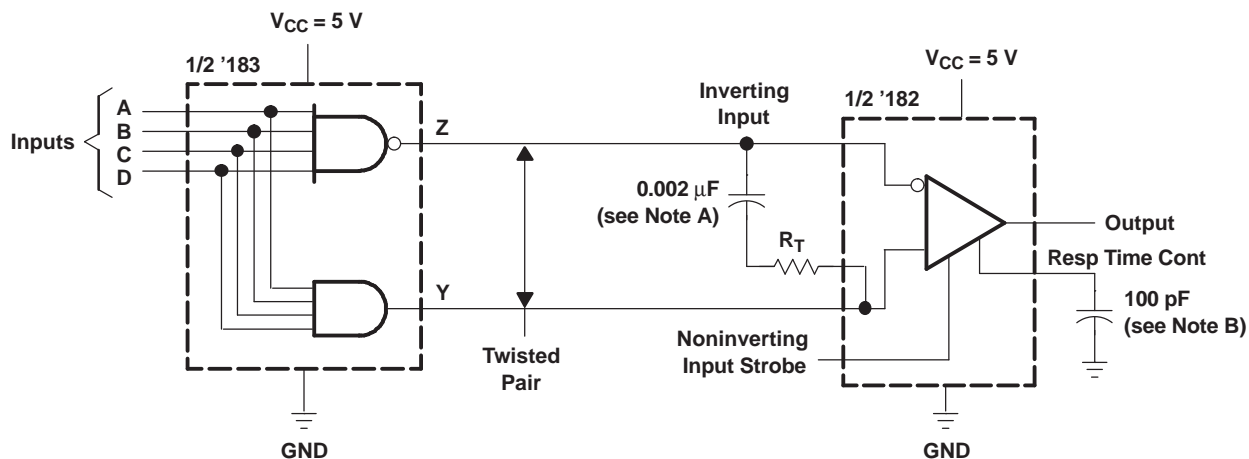


Figure 7.



## APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let  $f = 5 \text{ MHz}$   
 $C = 0.002 \mu\text{F}$

$$Z_{(\text{circuit})} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(\text{circuit})} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

**Figure 8. Transmission of Digital Data Over Twisted-Pair Line**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-7900901VCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7900901VC A SNV55183J
5962-7900901VCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7900901VC A SNV55183J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN55183-SP :**

- Catalog : [SN55183](#)

NOTE: Qualified Version Definitions:

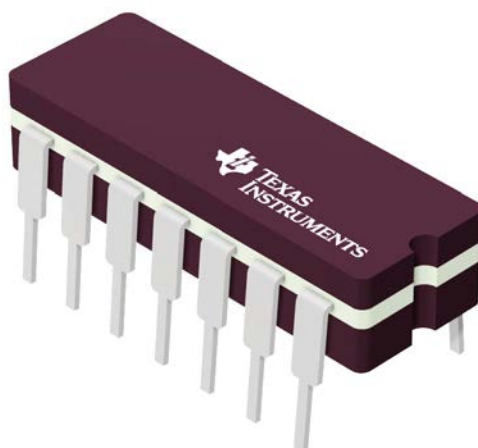
- Catalog - TI's standard catalog product

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



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# EXAMPLE BOARD LAYOUT

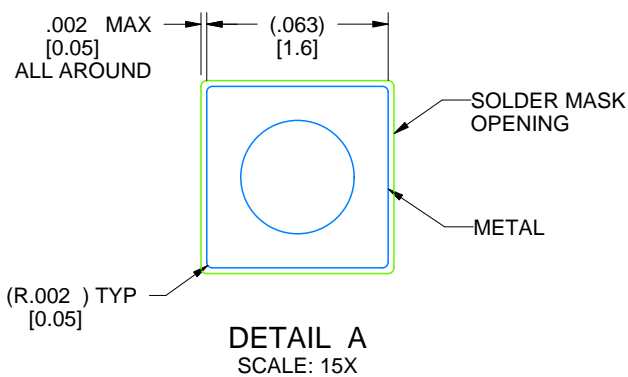
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

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