SN54SC1G125-SEP Radiation Tolerant, Single Bus Buffer Gate with 3-State Output

1 Features

- VID TBD-01XE
- Radiation - Total Ionizing Dose (TID):
  - TID characterized up to 50 krad(Si)
  - TID performance assurance up to 30 krad(Si)
  - Radiation Lot Acceptance Testing (RLAT) for every wafer lot up to 30 krad(Si)
- Radiation - Single-Event Effects (SEE):
  - Single Event Latch-Up (SEL) immune up to 50 MeV-cm^2/mg at 125°C
  - Single Event Transient (SET) characterized up to LET = 50 MeV-cm^2/mg
- Wide operating range of 1.2V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Up to 150Mbps with 5V or 3.3V V_{CC}
- Latch-up performance exceeds 100mA per JESD 78
- Space enhanced plastic:
  - Supports Defense and Aerospace Applications
  - Controlled baseline
  - Au bondwire and NiPdAu lead finish
  - Meets NASA ASTM E595 outgassing specification
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Product traceability

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED

3 Description

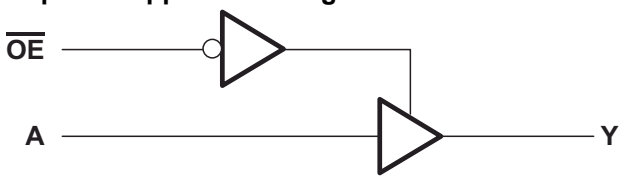
The SN54SC1G125-SEP is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input pin is at a logic high level. When ($\overline{OE}$) is at a logic low level, true data is passed from the A input to the Y output.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN54SC1G125-SEP	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.65mm

(1) For all available packages, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

Simplified Application Diagram



ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

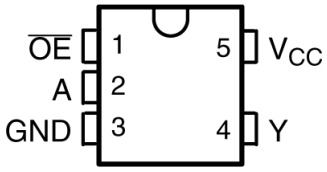


Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	(High or low state)	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 3.0V		-16	
				-24	
		V_{CC} = 4.5V		-32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3.0V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.2V to 5.0V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.8V ± 0.15V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V_{cc} = 2.5V ± 0.2V		20	ns/V
Δt/Δv	Input transition rise or fall rate (1G04, 1G06, 1G07, 1G34)	V_{cc} = 3.3V ± 0.3V		10	ns/V

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate (1G34)	V_{cc} = 5.0V ± 0.5V		10	ns/V
Δt/Δv	Input transition rise or fall rate (1G04, 1G06, 1G07)	V_{cc} = 5.0V ± 0.5V		5	ns/V
T_A	Operating free-air temperature		-55	125	°C
V_{IH}	High-level input voltage	V_{CC} = 1.1V	0.75		V
V_{IH}	High-level input voltage	V_{CC} = 1.32V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	0.975		V
V_{IH}	High-level input voltage	V_{CC} = 1.65V	1.075		V
V_{IH}	High-level input voltage	V_{CC} = 1.95V	1.2675		V
V_{IH}	High-level input voltage	V_{CC} = 2.3V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 2.7V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 3.0V	2		V
V_{IH}	High-level input voltage	V_{CC} = 3.6V	2		V
V_{IH}	High-level input voltage	V_{CC} = 4.5V	3.15		V
V_{IH}	High-level input voltage	V_{CC} = 5.5V	3.85		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V		0.3	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.32V		0.42	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5V		0.525	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V		0.5775	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.95V		0.6825	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.3V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.7V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.0V		0.8	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.6V		0.8	V
V_{IL}	Low-Level input voltage	V_{CC} = 4.5V		1.35	V
V_{IL}	Low-Level input voltage	V_{CC} = 5.5V		1.65	V

ADVANCE INFORMATION

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-55°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100 µA	1.1V to 5.5V	V_{CC} - 0.1			V
V_{OH}	I_{OH}= –4 mA	1.65V	1.2			V
V_{OH}	I_{OH}= –8 mA	2.3V	1.9			V
V_{OH}	I_{OH}= –12 mA	2.7V	2.2			V
V_{OH}	I_{OH}= –16 mA	3V	2.4			V
V_{OH}	I_{OH}= –24 mA	3V	2.3			V
V_{OH}	I_{OH}= –32 mA	4.5V	3.8			V
V_{OL}	I_{OL}= 100 µA	1.1V to 5.5V			0.15	V
V_{OL}	I_{OL}= 4 mA	1.65V			0.45	V
V_{OL}	I_{OL}= 8 mA	2.3V			0.3	V
V_{OL}	I_{OL}= 12 mA	2.7V			0.4	V
V_{OL}	I_{OL}= 16 mA	3V			0.4	V
V_{OL}	I_{OL}= 24 mA	3V			0.55	V
V_{OL}	I_{OL}= 32 mA	4.5V			0.55	V
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 5.5V		±1	±5	µA
I_{off}	V_I or V_O = V_{CC}	V_{CC} = 0V		±1	±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 1.1V to 5.5V		1	10	µA
ΔI_{CC}	One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND	3.0V to 5.5V			500	µA
C_I	V_I = V_{CC} or GND	3.3V		3.5		pF
C_O	V_O = V_{CC} or GND	3.3V				pF

ADVANCE INFORMATION

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF	1.2V ± 0.1V		27	41.5	ns
t_{pd}	A	Y	C_L = 15 pF	1.5V ± 0.12V		8	9.1	ns
t_{pd}	A	Y	C_L = 15 pF	1.8V ± 0.15V		6	6.9	ns
t_{pd}	A	Y	C_L = 15 pF	2.5V ± 0.2V		3.9	4.6	ns
t_{pd}	A	Y	C_L = 15 pF	3.3V ± 0.3V		2.8	3.7	ns
t_{pd}	A	Y	C_L = 15 pF	5.0V ± 0.5V		2	3.4	ns
t_{pd}	A	Y	C_L = 30 pF	1.8V ± 0.15V	2.8	6	9.3	ns
t_{pd}	A	Y	C_L = 30 pF	2.5V ± 0.2V	1.2	4	5.8	ns
t_{pd}	A	Y	C_L = 50 pF	3.3V ± 0.3V	1	3.4	4.9	ns
t_{pd}	A	Y	C_L = 50 pF	5.0V ± 0.5V	1	2.6	4	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	1.2V ± 0.1V		30	44	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	1.5V ± 0.12V		8	9.5	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	1.8V ± 0.15V		6	7.4	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	2.5V ± 0.2V		3	4.3	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	3.3V ± 0.3V		2	3.2	ns
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	5.0V ± 0.5V		1.5	2.2	ns
t_{en}	$\overline{OE}$	Y	C_L = 30 pF	1.8V ± 0.15V	3.1	7.3	10.4	ns
t_{en}	$\overline{OE}$	Y	C_L = 30 pF	2.5V ± 0.2V	1.5	4.1	6.9	ns
t_{en}	$\overline{OE}$	Y	C_L = 50 pF	3.3V ± 0.3V	1	3.3	5.8	ns
t_{en}	$\overline{OE}$	Y	C_L = 50 pF	5.0V ± 0.5V	1	2.6	5	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	1.2V ± 0.1V		23	30	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	1.5V ± 0.12V		8	10.8	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	1.8V ± 0.15V		7	8.5	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	2.5V ± 0.2V		4	5.1	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	3.3V ± 0.3V		4	4.4	ns
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	5.0V ± 0.5V		2.5	3.4	ns
t_{dis}	$\overline{OE}$	Y	C_L = 30 pF	1.8V ± 0.15V	1.3	8	9.4	ns
t_{dis}	$\overline{OE}$	Y	C_L = 30 pF	2.5V ± 0.2V	1	4	5.5	ns
t_{dis}	$\overline{OE}$	Y	C_L = 50 pF	3.3V ± 0.3V	1	4	5	ns
t_{dis}	$\overline{OE}$	Y	C_L = 50 pF	5.0V ± 0.5V	1	3	4.2	ns
C_{pd}		outputs enabled	f = 10 MHz	1.8V		18		pf
C_{pd}		outputs disabled	f = 10 MHz	1.8V		2		pf
C_{pd}		outputs enabled	f = 10 MHz	2.5V		18		pf
C_{pd}		outputs disabled	f = 10 MHz	2.5V		2		pf
C_{pd}		outputs enabled	f = 10 MHz	3.3V		19		pf
C_{pd}		outputs disabled	f = 10 MHz	3.3V		2		pf
C_{pd}		outputs enabled	f = 10 MHz	5V		21		pf
C_{pd}		outputs disabled	f = 10 MHz	5V		4		pf

ADVANCE INFORMATION

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

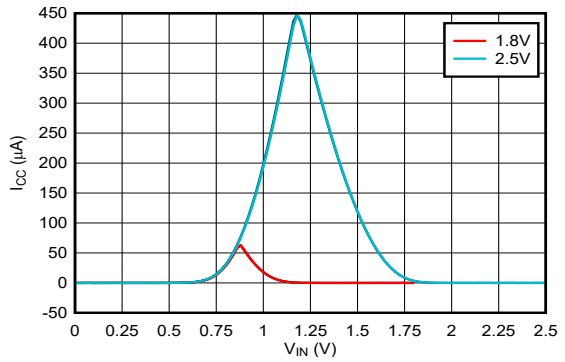


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

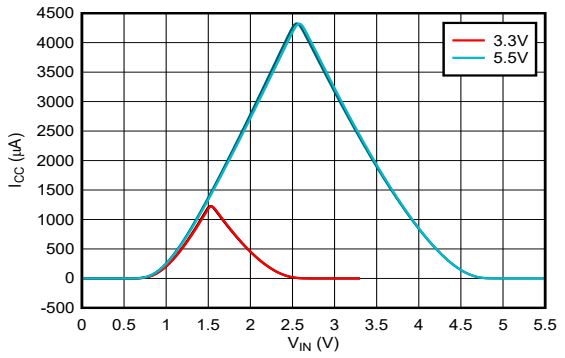


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.5V Supply

ADVANCE INFORMATION

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

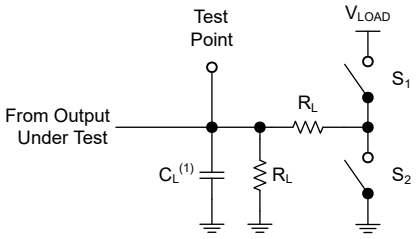
The outputs are measured individually with one input transition per measurement.

Table 6-1. 3-State Outputs

TEST	S1	S2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PLZ}, t_{PZL}	CLOSED	OPEN
t_{PHZ}, t_{PZH}	OPEN	CLOSED

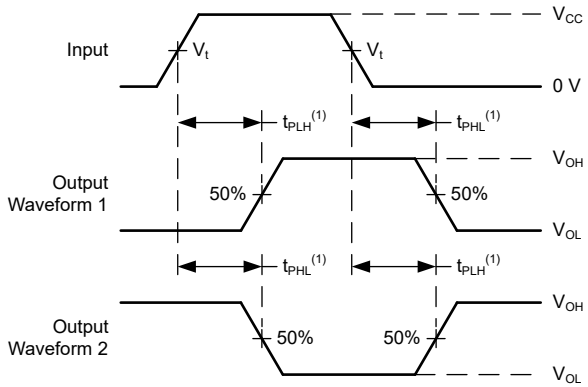
Table 6-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.8V ± 0.15V	V_{CC}/2	1kΩ	15pF/30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	15pF/30pF	0.15V	2×V_{CC}
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V	6V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V	6V



(1) C_L includes probe and test-fixture capacitance.

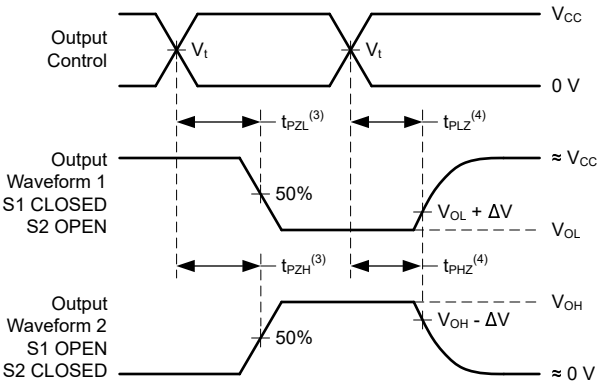
Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays

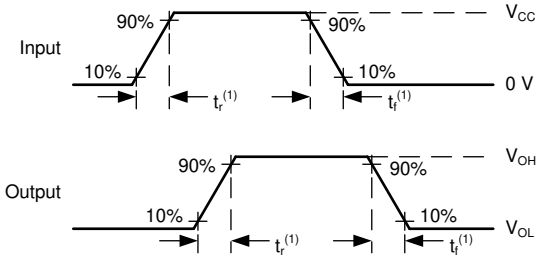
ADVANCE INFORMATION



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The SN54SC1G125-SEP device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

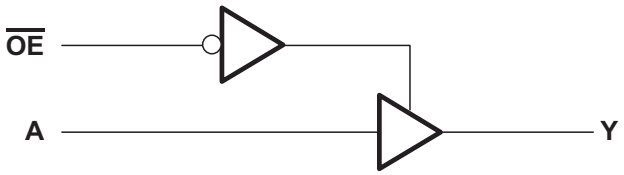


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

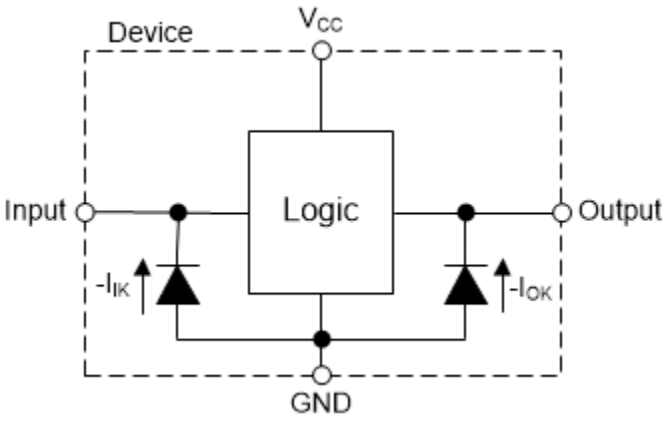


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS(1)		OUTPUT(2)
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN54SC1G125-SEP is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V. Figure 8-1 shows this type of translation.

8.2 Typical Application

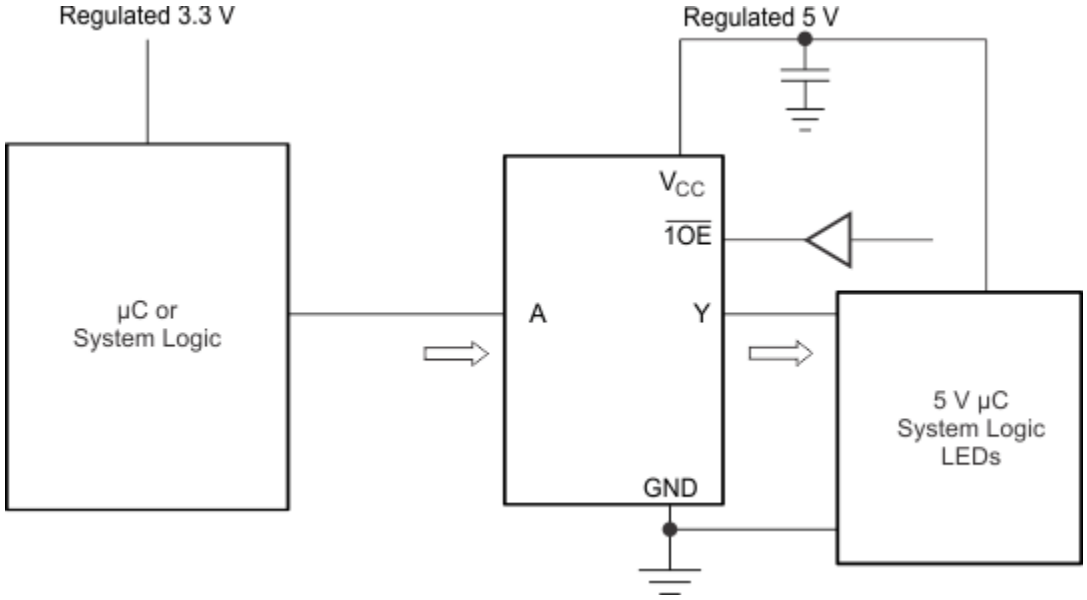

Figure 8-1. Typical Application Schematic

8.3 Design Requirements

8.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN54SC1G125-SEP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN54SC1G125-SEP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN54SC1G125-SEP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN54SC1G125-SEP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

ADVANCE INFORMATION

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN54SC1G125-SEP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN54SC1G125-SEP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

ADVANCE INFORMATION

8.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN54SC1G125-SEP to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.5 Application Curves

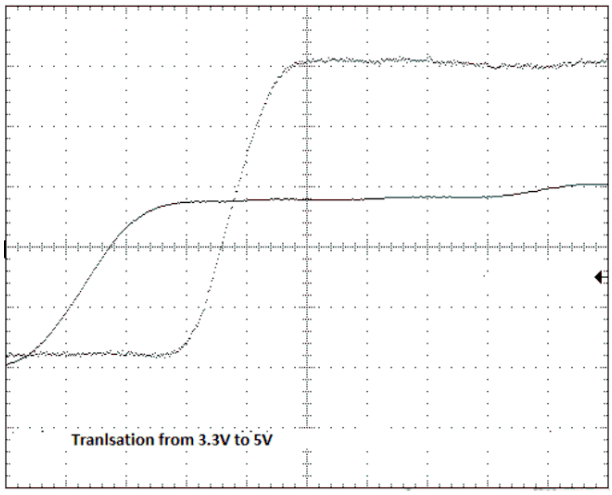

Figure 8-2. Translation from 3.3 V to 5 V

ADVANCE INFORMATION

8.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN54SC1G125-SEP, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.7 Layout

8.7.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.7.2 Layout Example

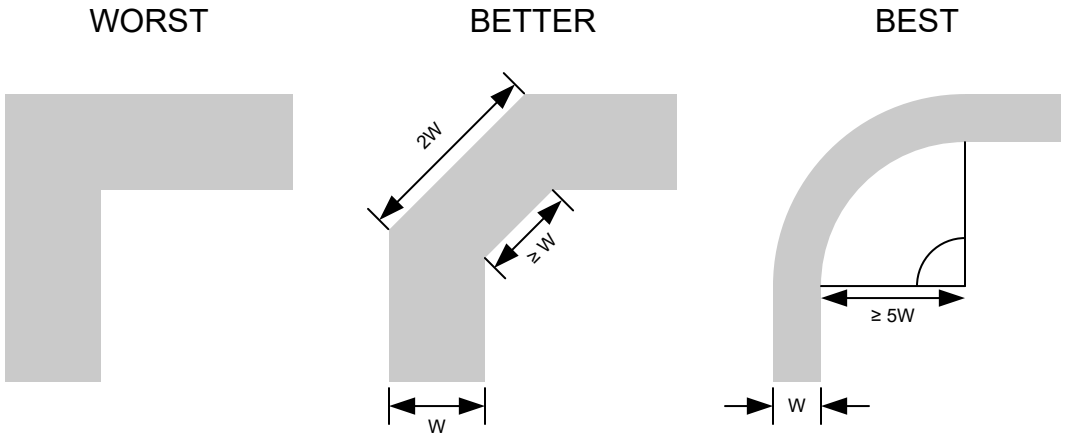

Figure 8-3. Example Trace Corners for Improved Signal Integrity

ADVANCE INFORMATION

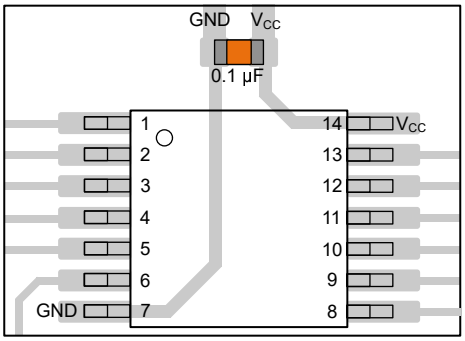

Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

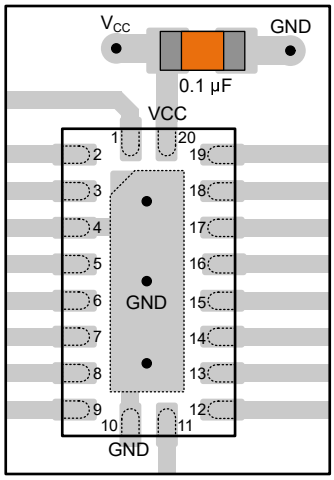

Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

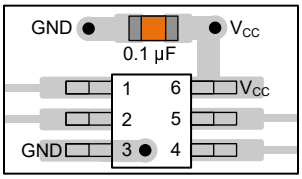

Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

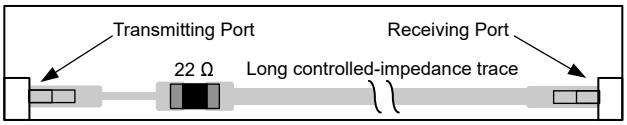

Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

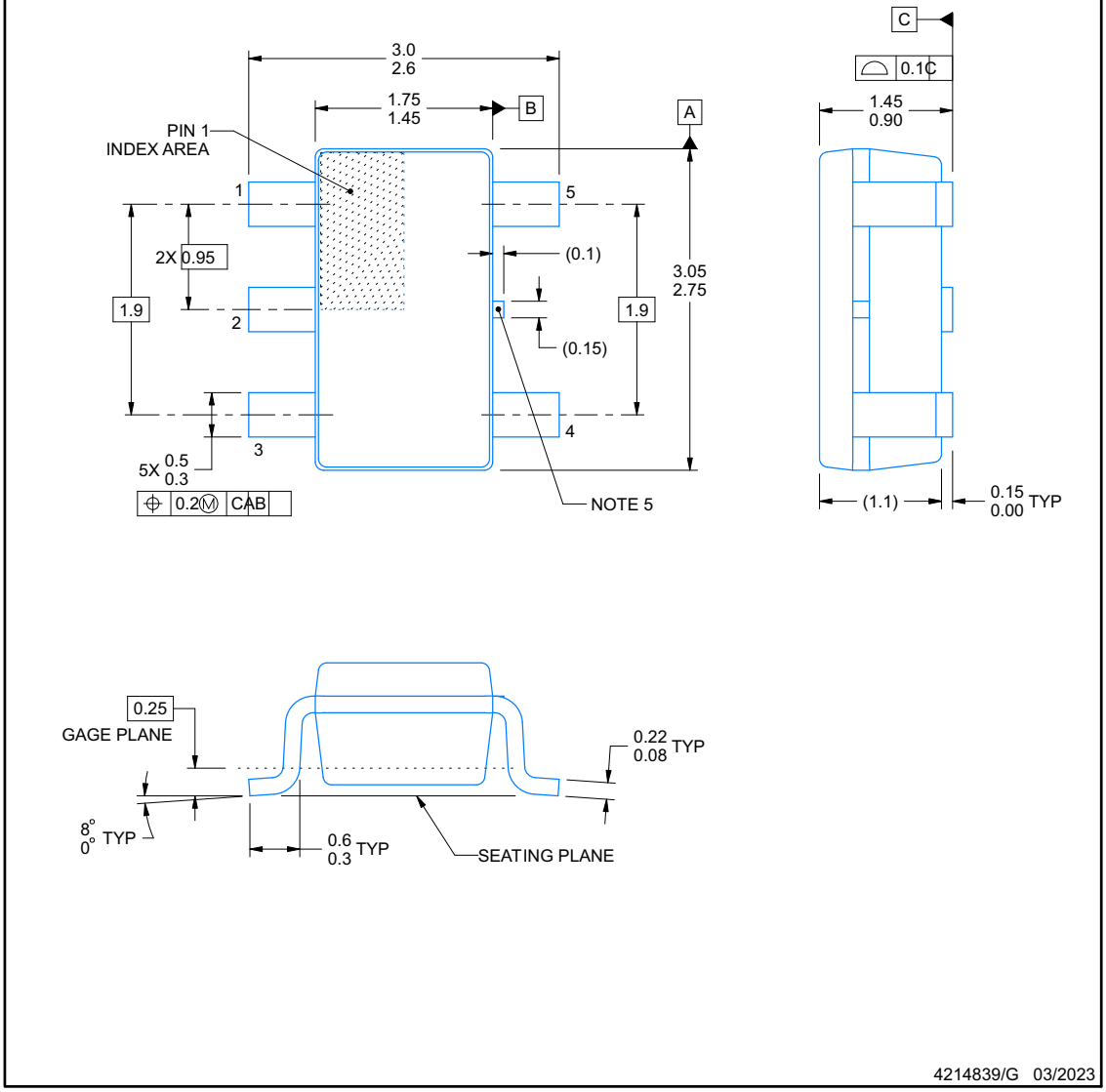
ADVANCE INFORMATION

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



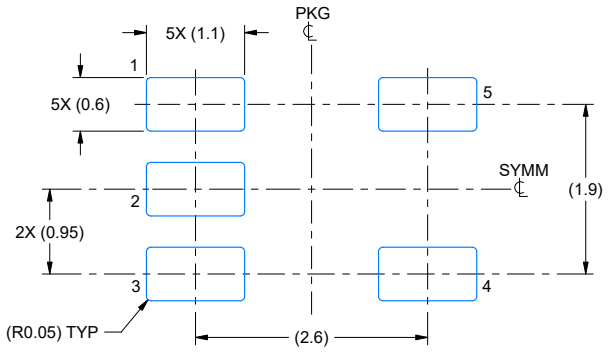
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

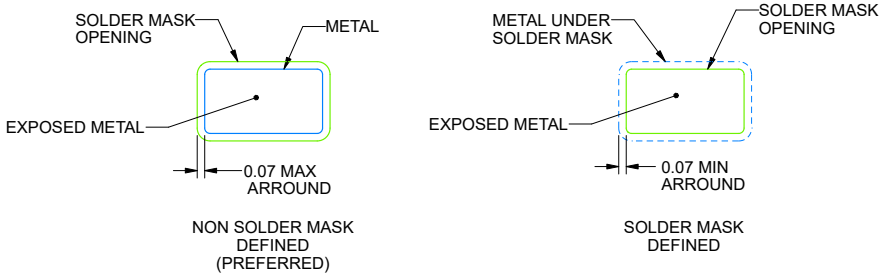
EXAMPLE BOARD LAYOUT

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

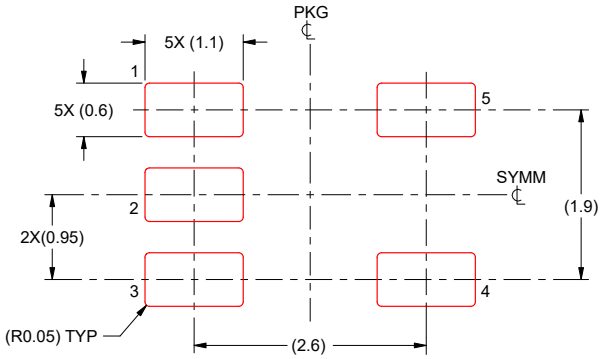
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
P54SC1G125MDBVTSEP	Active	Preproduction	SOT-23 (DBV) | 5	250 | SMALL T&R	-	Call TI	Call TI	-	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

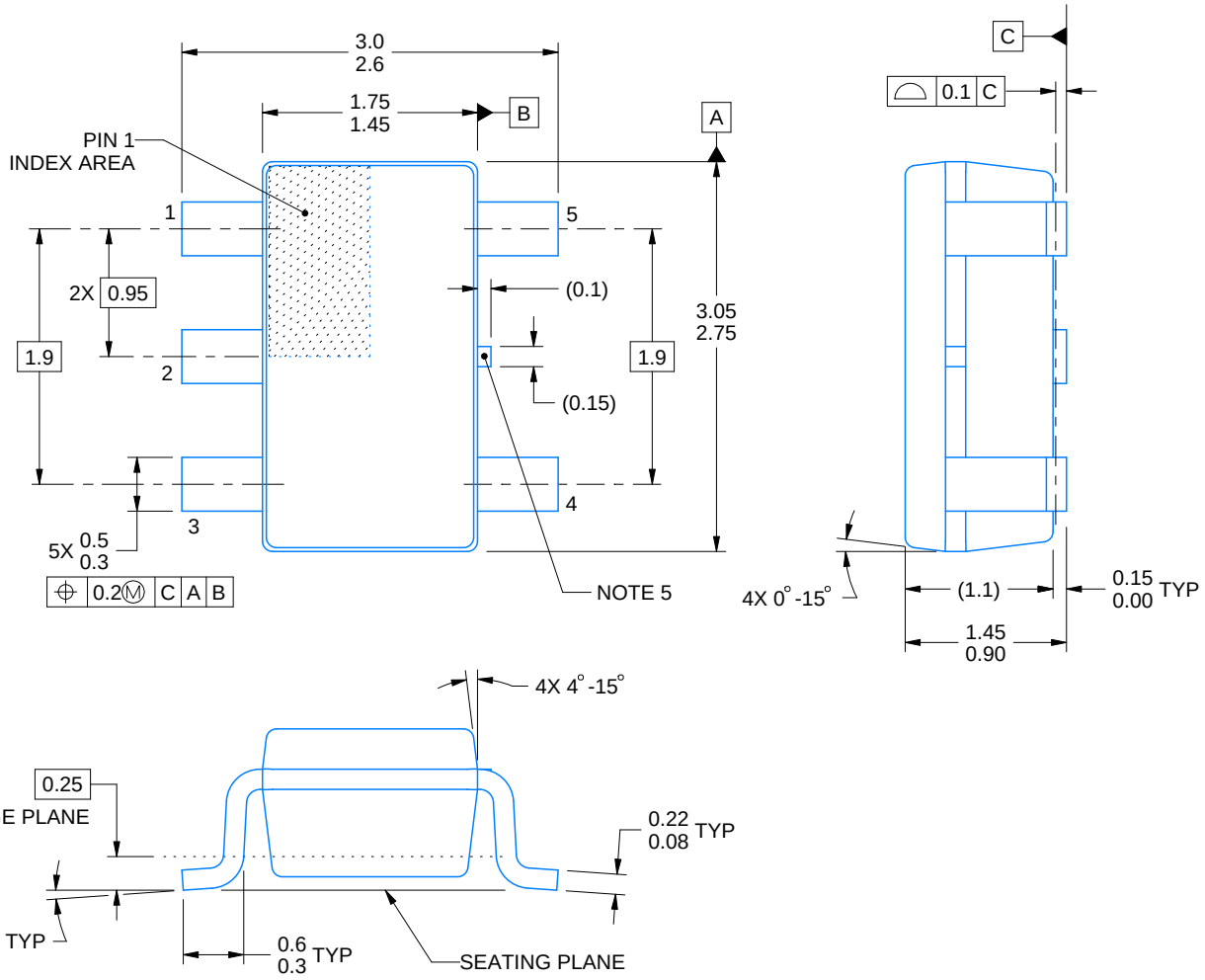
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

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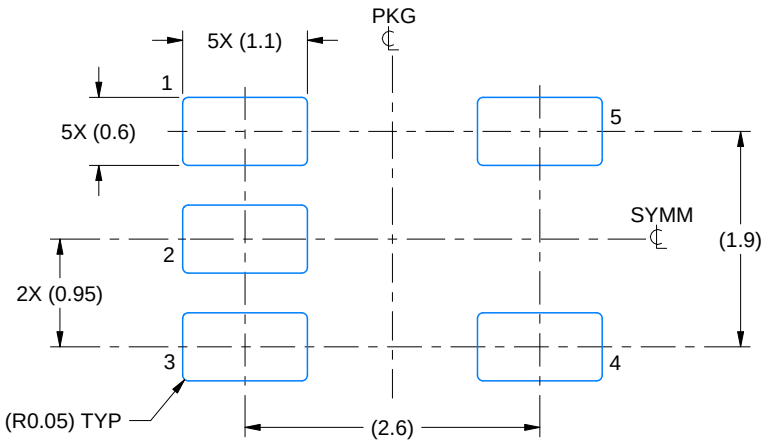
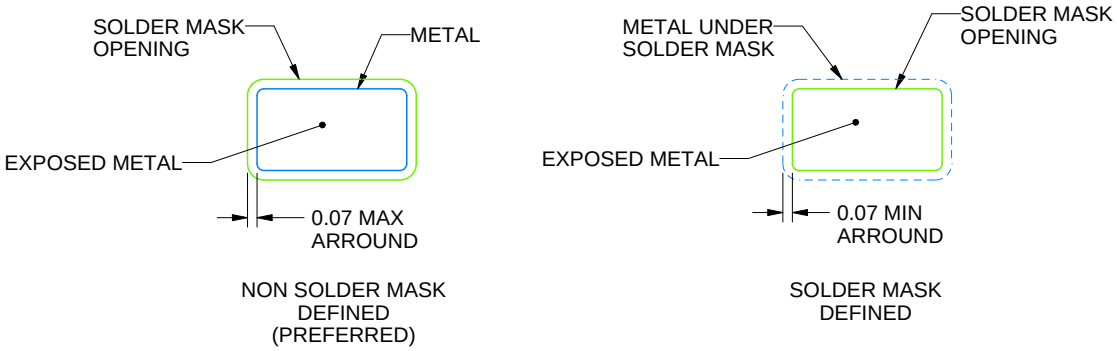


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

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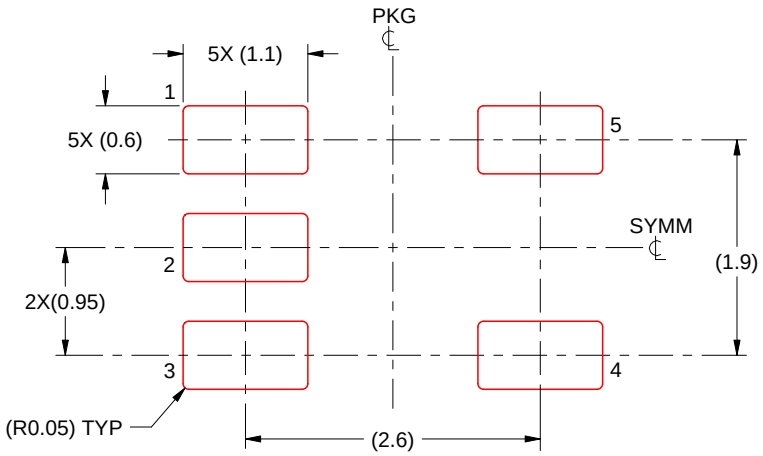

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025