

SN54SC1G08-SEP Radiation Tolerant, Single 2-Input Positive-AND Gate

1 Features

- VID TBD-01XE
- Radiation - Total Ionizing Dose (TID):
 - TID characterized up to 50krad(Si)
 - TID performance assurance up to 30krad(Si)
 - Radiation Lot Acceptance Testing (RLAT) for every wafer lot up to 30krad(Si)
- Radiation - Single-Event Effects (SEE):
 - Single Event Latch-Up (SEL) immune up to 50MeV-cm²/mg at 125°C
 - Single Event Transient (SET) characterized up to LET = 50MeV-cm²/mg
- Wide operating range of 1.2V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Up to 150Mbps with 5V or 3.3V V_{CC}
- Latch-up performance exceeds 100mA per JESD 78
- Space enhanced plastic:
 - Supports Defense and Aerospace Applications
 - Controlled baseline
 - Au bondwire and NiPdAu lead finish
 - Meets NASA ASTM E595 outgassing specification
 - One fabrication, assembly, and test site
 - Extended product life cycle
 - Product traceability

2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)

3 Description

The SN54SC1G08-SEP device performs the Boolean function or $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN54SC1G08-SEP	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.65mm

- (1) For all available packages, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



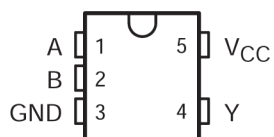
Logic Diagram



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4 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 4-1. DBV Package 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DBV		
A	1	I	Data Input
B	2	I	Data Input
GND	3	-	Ground
Y	4	O	Data Output
V _{CC}	5	-	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT	
V _{CC}	Supply voltage range		-0.5	6.5	V	
V _I	Input voltage range ⁽²⁾		-0.5	6.5	V	
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0V			-50	mA
I _{OK}	Output clamp current	V _O < 0V			-50	mA
I _O	Continuous output current				±50	mA
I _O	Continuous output current through V _{CC} or GND				±100	mA
T _J	Junction temperature		-65	150	°C	
T _{stg}	Storage temperature		-65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.1	5.5	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage	(High or low state)	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V		-4	mA
		V _{CC} = 2.3V		-8	
		V _{CC} = 3.0V		-16	
				-24	
		V _{CC} = 4.5V		-32	
I _{OL}	Low-level output current	V _{CC} = 1.65V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 3.0V		16	
				24	
		V _{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.2V to 5.0V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8V ± 0.15V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.5V ± 0.2V		20	ns/V
Δt/Δv	Input transition rise or fall rate (1G04, 1G06, 1G07, 1G34)	V _{CC} = 3.3V ± 0.3V		10	ns/V

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate (1G34)	$V_{CC} = 5.0V \pm 0.5V$		10	ns/V
$\Delta t/\Delta v$	Input transition rise or fall rate (1G04, 1G06, 1G07)	$V_{CC} = 5.0V \pm 0.5V$		5	ns/V
T_A	Operating free-air temperature		-55	125	°C
V_{IH}	High-level input voltage	$V_{CC} = 1.1V$	0.75		V
V_{IH}	High-level input voltage	$V_{CC} = 1.32V$	0.78		V
V_{IH}	High-level input voltage	$V_{CC} = 1.5V$	0.975		V
V_{IH}	High-level input voltage	$V_{CC} = 1.65V$	1.075		V
V_{IH}	High-level input voltage	$V_{CC} = 1.95V$	1.2675		V
V_{IH}	High-level input voltage	$V_{CC} = 2.3V$	1.7		V
V_{IH}	High-level input voltage	$V_{CC} = 2.7V$	1.7		V
V_{IH}	High-level input voltage	$V_{CC} = 3.0V$	2		V
V_{IH}	High-level input voltage	$V_{CC} = 3.6V$	2		V
V_{IH}	High-level input voltage	$V_{CC} = 4.5V$	3.15		V
V_{IH}	High-level input voltage	$V_{CC} = 5.5V$	3.85		V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.1V$		0.3	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.32V$		0.42	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.5V$		0.525	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.65V$		0.5775	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.95V$		0.6825	V
V_{IL}	Low-Level input voltage	$V_{CC} = 2.3V$		0.7	V
V_{IL}	Low-Level input voltage	$V_{CC} = 2.7V$		0.7	V
V_{IL}	Low-Level input voltage	$V_{CC} = 3.0V$		0.8	V
V_{IL}	Low-Level input voltage	$V_{CC} = 3.6V$		0.8	V
V_{IL}	Low-Level input voltage	$V_{CC} = 4.5V$		1.35	V
V_{IL}	Low-Level input voltage	$V_{CC} = 5.5V$		1.65	V

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-55°C to 125°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100µA	1.1V to 5.5V	V _{CC} - 0.1			V
V _{OH}	I _{OH} = -4mA	1.65V	1.2			V
V _{OH}	I _{OH} = -8mA	2.3V	1.9			V
V _{OH}	I _{OH} = -12mA	2.7V	2.2			V
V _{OH}	I _{OH} = -16mA	3V	2.4			V
V _{OH}	I _{OH} = -24mA	3V	2.3			V
V _{OH}	I _{OH} = -32mA	4.5V	3.8			V
V _{OL}	I _{OL} = 100µA	1.1V to 5.5V	0.15			V
V _{OL}	I _{OL} = 4mA	1.65V	0.45			V
V _{OL}	I _{OL} = 8mA	2.3V	0.3			V
V _{OL}	I _{OL} = 12mA	2.7V	0.4			V
V _{OL}	I _{OL} = 16mA	3V	0.4			V
V _{OL}	I _{OL} = 24mA	3V	0.55			V
V _{OL}	I _{OL} = 32mA	4.5V	0.55			V
I _I	V _I = V _{CC} or GND	V _{CC} = 0V to 5.5V	±1 ±5			µA
I _{off}	V _I or V _O = V _{CC}	V _{CC} = 0V	±1 ±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	V _{CC} = 1.1V to 5.5V	1 10			µA
ΔI _{CC}	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND	3.0V to 5.5V	500			µA
C _I	V _I = V _{CC} or GND	3.3V	3.5			pF
C _O	V _O = V _{CC} or GND	3.3V				pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See ###Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
t _{pd}	A or B	Y	C _L = 15pF	1.2V ± 0.1V		32.5	47	ns
t _{pd}	A or B	Y	C _L = 15pF	1.5V ± 0.12V		6	11	ns
t _{pd}	A or B	Y	C _L = 15pF	1.8V ± 0.15V		5.5	8	ns
t _{pd}	A or B	Y	C _L = 15pF	2.5V ± 0.2V		4	4.8	ns
t _{pd}	A or B	Y	C _L = 15pF	3.3V ± 0.3V		3	3.7	ns
t _{pd}	A or B	Y	C _L = 15pF	5.0V ± 0.5V		2	3.4	ns
t _{pd}	A or B	Y	C _L = 30pF	1.8V ± 0.15V	2.4	6	11	ns
t _{pd}	A or B	Y	C _L = 30pF	2.5V ± 0.2V	1.1	4.3	7.5	ns
t _{pd}	A or B	Y	C _L = 50pF	3.3V ± 0.3V	1	3.8	6.5	ns
t _{pd}	A or B	Y	C _L = 50pF	5.0V ± 0.5V	1	2.9	5	ns
C _{pd}			f = 10MHz	1.8V		21		pf
C _{pd}			f = 10MHz	2.5V		24		pf
C _{pd}			f = 10MHz	3.3V		26		pf
C _{pd}			f = 10MHz	5V		31		pf

5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

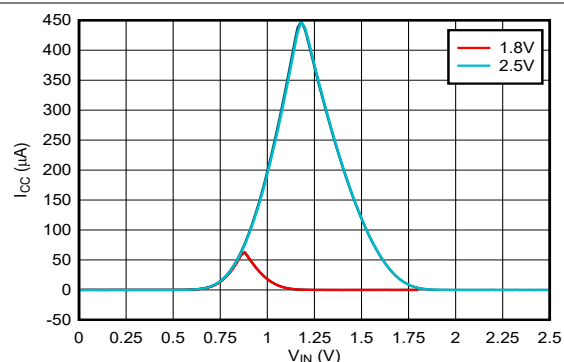


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

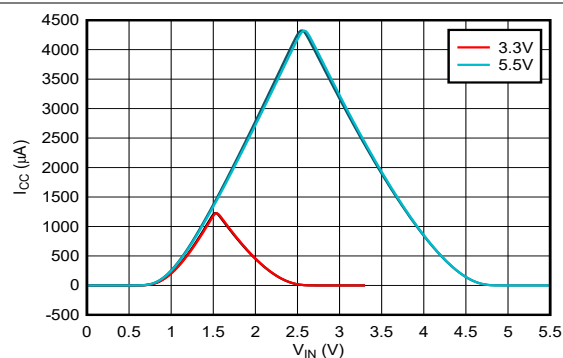


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.5V Supply

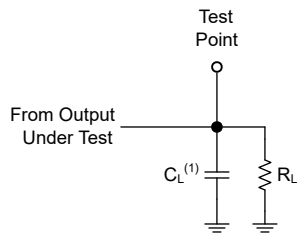
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f \leq 2.5\text{ns}$.

The outputs are measured individually with one input transition per measurement.

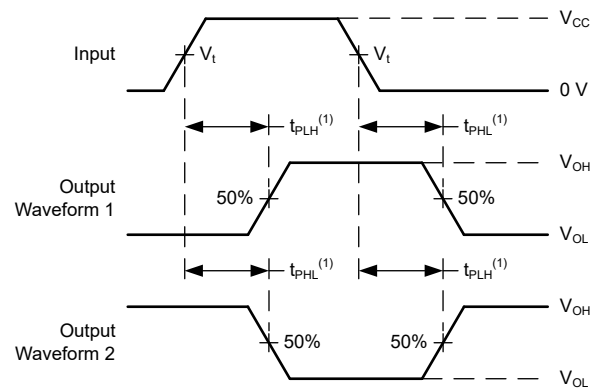
Table 6-1. Push-Pull Outputs

V_{CC}	V_t	R_L	C_L	ΔV
$1.2\text{V} \pm 0.1\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V
$1.5\text{V} \pm 0.12\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V
$1.8\text{V} \pm 0.15\text{V}$	$V_{CC}/2$	$1\text{k}\Omega$	$15\text{pF}/30\text{pF}$	0.15V
$2.5\text{V} \pm 0.2\text{V}$	$V_{CC}/2$	500Ω	$15\text{pF}/30\text{pF}$	0.15V
$3.3\text{V} \pm 0.3\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V
$5.0\text{V} \pm 0.5\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V



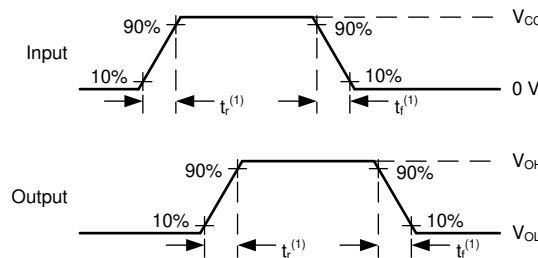
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN54SC1G08-SEP device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Side)

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

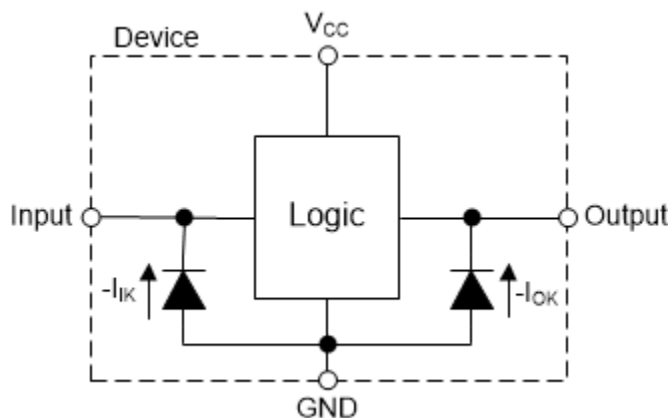


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Function Table lists the functional modes for SN54SC1G08-SEP.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
A	B	Y
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A common application for AND gates is their use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN54SC1G08-SEP to verify that the processor has turned on can protect it from any harmful signals.

8.2 Typical Application

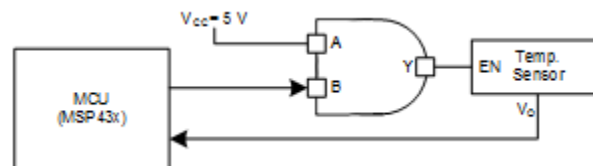


Figure 8-1. Power Sequencing Application

8.3 Design Requirements

The SN54SC1G08-SEP device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN54SC1G08-SEP allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0V or V_{CC} as possible for optimal operation.

8.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics of the device as described in the [Electrical Characteristics](#) section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN54SC1G08-SEP plus the maximum static supply current, I_{CC} , listed in the [Electrical Characteristics](#), and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the [Absolute Maximum Ratings](#) is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN54SC1G08-SEP plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#), and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the [Absolute Maximum Ratings](#) is not exceeded.

The SN54SC1G08-SEP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN54SC1G08-SEP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the [Electrical Characteristics](#) table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the [Absolute Maximum Ratings](#), is an additional limitation to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [Absolute Maximum Ratings](#).

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN54SC1G08-SEP (as specified in the [Electrical Characteristics](#)), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN54SC1G08-SEP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the [Recommended Operating Conditions](#) table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the [Feature Description](#) section for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#).

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the [Feature Description](#) section for additional information regarding the outputs for this device.

8.4 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed ± 50 mA.
- Frequency selection criterion:
 - The effects of frequency upon the device's power consumption should be studied in [CMOS Power Consumption and CPD Calculation, SCAA035](#).
 - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Layout](#) section.

8.5 Application Curves

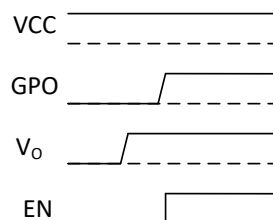


Figure 8-2. Typical Application Timing Diagram

8.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN54SC1G08-SEP, a 0.1 μ F bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel.

8.7 Layout

8.7.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.7.2 Layout Example

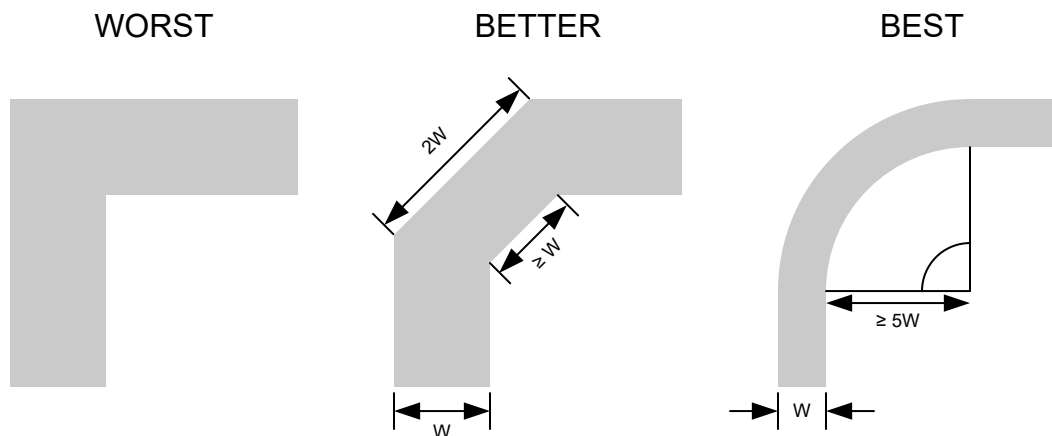


Figure 8-3. Example Trace Corners for Improved Signal Integrity

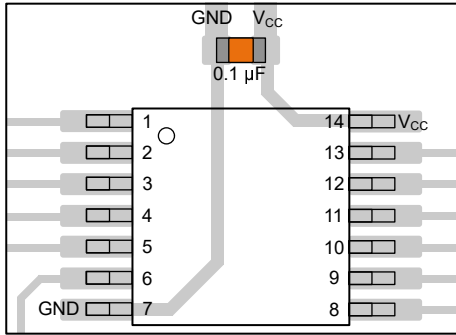


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

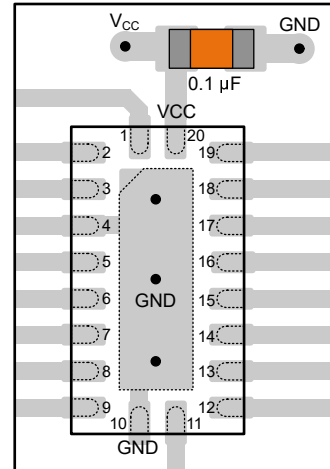


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

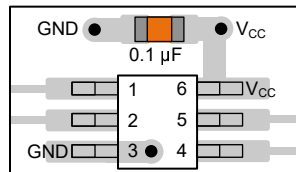


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

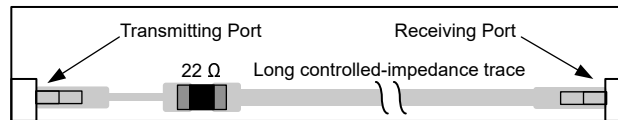


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Advance Information Release

11 Mechanical, Packaging, and Orderable Information

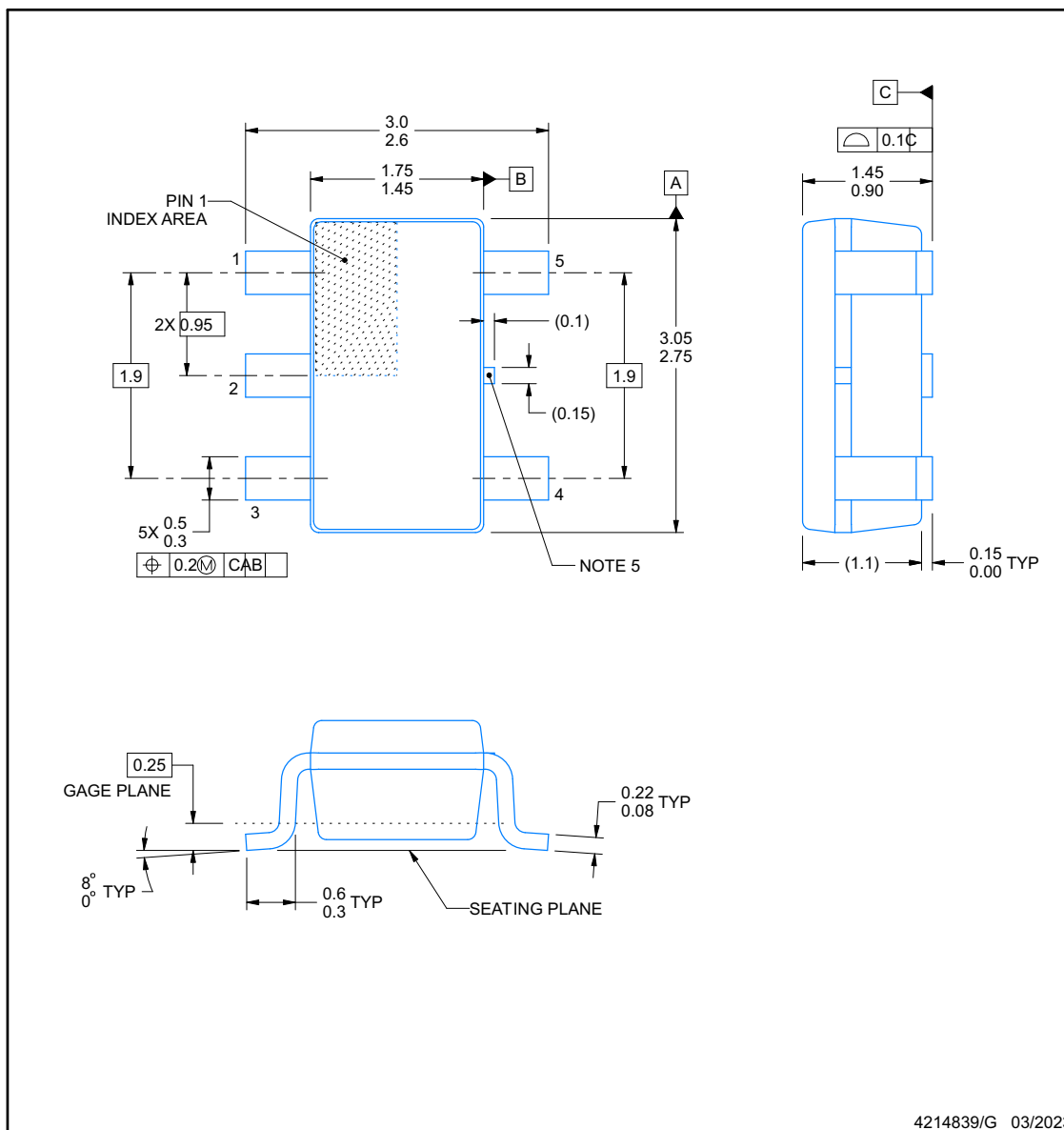
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ADVANCE INFORMATION

NOTES:

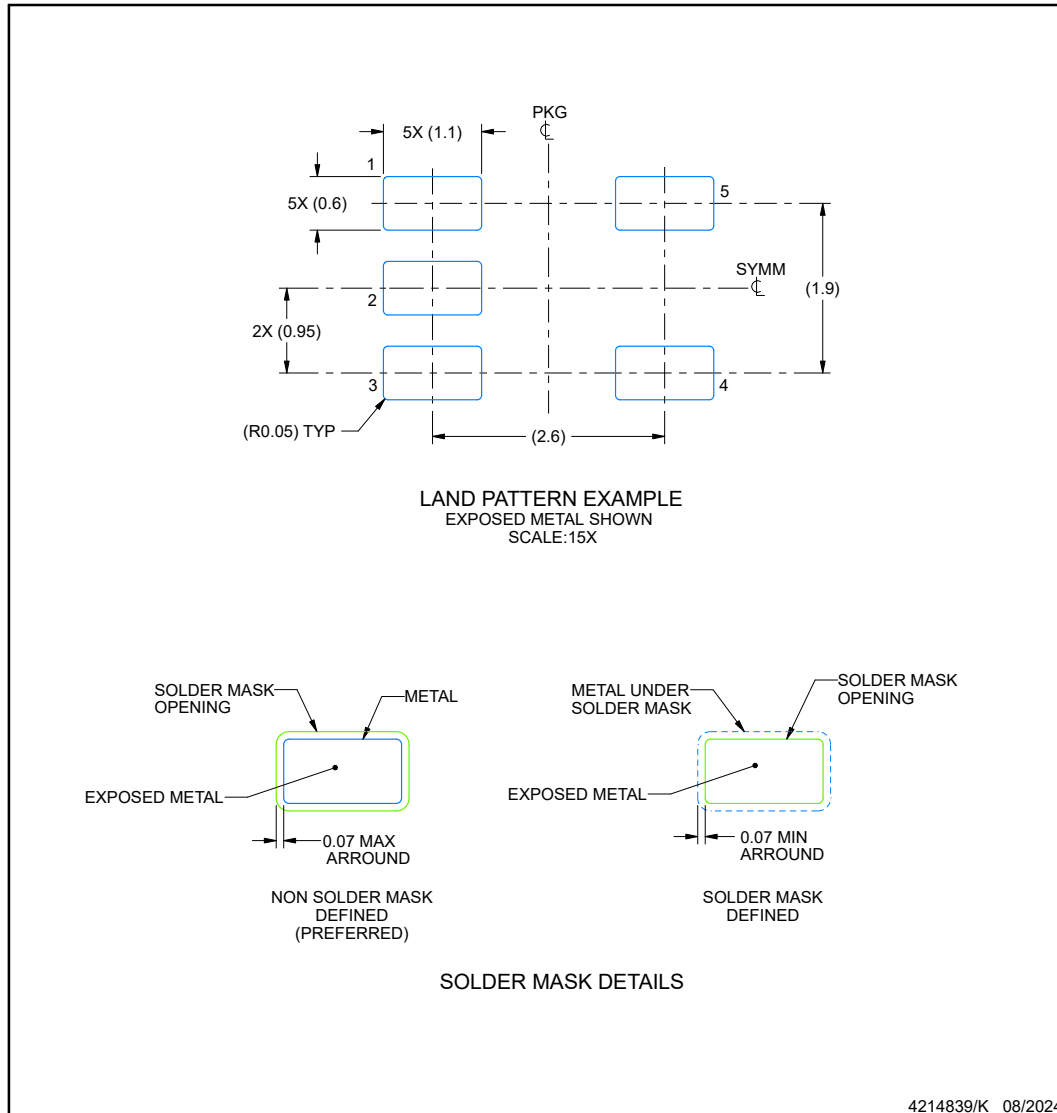
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PN54SC1G08MDBVTSEP	Active	Preproduction	SOT-23 (DBV) 5	250 SMALL T&R	-	Call TI	Call TI	-	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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