SNx4LVC74A Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

1 Features

- Operate from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 5.2ns at 3.3V
- Typical V_{OLP} (output ground bounce) <0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) >2V at V_{CC} = 3.3V, T_A = 25°C
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 1000V charged-device model (C101)

2 Applications

- Servers
- Medical, Healthcare, and Fitness
- Telecom Infrastructures
- TVs, Set-Top Boxes, and Audio
- Test and Measurement
- Industrial Transport
- Wireless Infrastructure
- Enterprise Switching
- Motor Drives
- Factory Automation and Control

3 Description

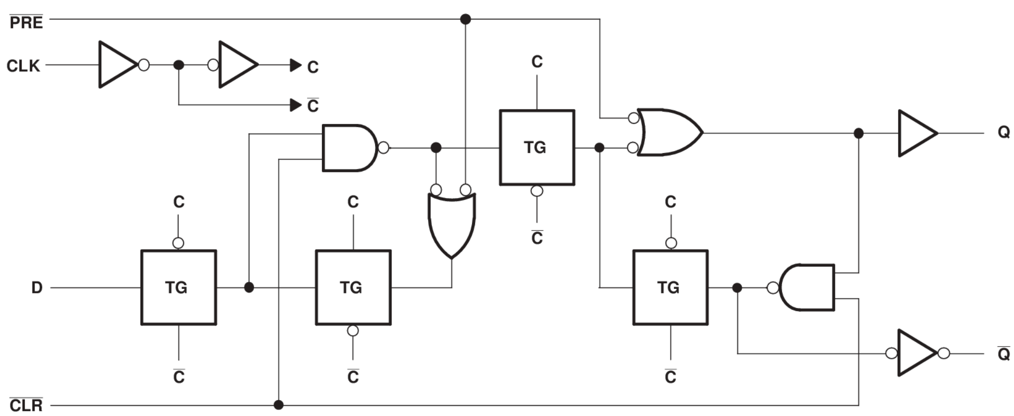
The SNx4LVC74A devices integrate two positive-edge triggered D-type flip-flops in one convenient device.

The SN54LVC74A is designed for 2.7V to 3.6V V_{CC} operation, and the SN74LVC74A is designed for 1.65V to 3.6V V_{CC} operation.

Device Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4LVC74A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm x 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm x 7.8mm	10.20mm × 5.30mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm
	J (CDIP, 14)	19.55mm x 7.9mm	19.56 mm × 6.67 mm
	W (CFP, 14)	9.21mm x 9 mm	9.21 mm × 5.97 mm
	FK (LCCC, 20)	8.9mm x 8.9mm	8.89 mm × 8.89 mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Flip-Flop (Positive Logic)

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4 Pin Configuration and Functions

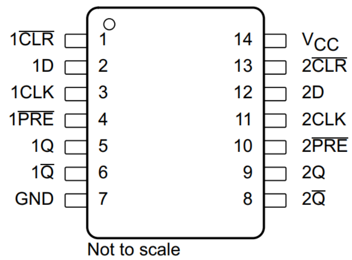


Figure 4-1. D, DB, J, PW, NS, or W Package 14-Pin SOIC, SSOP, CDIP, TSSOP, SO, or CFP (Top View)

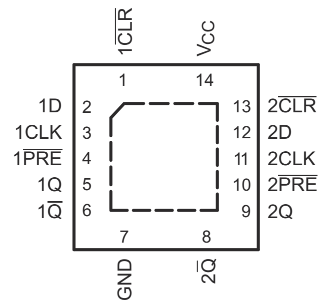


Figure 4-2. BQA or RGY Package 14-Pin WQFN or VQFN With Exposed Thermal Pad (Top View)

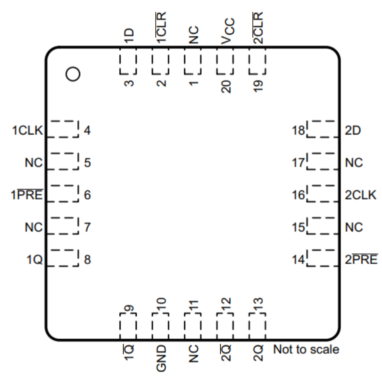


Figure 4-3. FK Package 20-Pin LCCC (Top View)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, CFP, PDIP, SO, SOIC, SSOP, TSSOP, VQFN	LCCC		
1CLK	3	4	I	Channel 1 clock input
1 $\overline{CLR}$	1	2	I	Channel 1 clear input. Pull low to set Q output low.
1D	2	3	I	Channel 1 data input
1 $\overline{PRE}$	4	6	I	Channel 1 preset input. Pull low to set Q output high.
1Q	5	8	O	Channel 1 output
1 $\overline{Q}$	6	9	O	Channel 1 inverted output
2CLK	11	16	I	Channel 2 clock input
2 $\overline{CLR}$	13	19	I	Channel 2 clear input. Pull low to set Q output low.
2D	12	18	I	Channel 2 data input
2 $\overline{PRE}$	10	14	I	Channel 2 preset input. Pull low to set Q output high.
2Q	9	13	O	Channel 2 output
2 $\overline{Q}$	8	12	O	Channel 2 Inverted output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	20	—	Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I [(2)]		–0.5	6.5	V
Output voltage, V_O [(2)] [(3)]		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions* .

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see[(1)]

				MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	SN54LVC74A	2	3.6	V
			SN74LVC74A	1.65	3.6	
		Data retention only		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	SN74LVC74A	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	SN74LVC74A	1.7		
		V_{CC} = 2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V	SN74LVC74A		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	SN74LVC74A		0.7	
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V	SN74LVC74A		–4	mA
		V_{CC} = 2.3 V	SN74LVC74A		–8	
		V_{CC} = 2.7 V			–12	
		V_{CC} = 3 V			–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V	SN74LVC74A		4	mA
		V_{CC} = 2.3 V	SN74LVC74A		8	
		V_{CC} = 2.7 V			12	
		V_{CC} = 3 V			24	
Δt/Δv	Input transition rise or fall rate				10	ns/V

5.3 Recommended Operating Conditions (continued)

see[(1)]

			MIN	MAX	UNIT
T_A	Operating free-air temperature	SN54LVC74A	–55	125	°C
		SN74LVC74A	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information: SN74LVC74A

THERMAL METRIC[(1)]		SN74LVC74A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	96.8	54.8	59.2	48.1	50.3	52.2	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	70.9	48	54.6	49.1	63.4	30.8	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	16.6	20.3	24.1	17.9	6.2	2.4	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	70.9	47.7	54.1	48.8	62.8	30.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	50.1	—	—	—	—	12.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA	V_{CC} = 1.65 V to 3.6 V and T_A = –55°C to 125°C (SN54LVC74A only)	V_{CC} – 0.2			V
			V_{CC} = 2.7 V to 3.6 V and T_A = –40°C to 125°C (SN74LVC74A only)	V_{CC} – 0.2			
		I_{OH} = –4 mA, V_{CC} = 1.65 V, and T_A = –40°C to 125°C (SN74LVC74A only)		1.2			
		I_{OH} = –8 mA, V_{CC} = 2.3 V, and T_A = –40°C to 125°C (SN74LVC74A only)		1.7			
		I_{OH} = –12 mA	V_{CC} = 2.7 V	2.2			
			V_{CC} = 3 V	2.4			
		I_{OH} = –24 mA, V_{CC} = 3 V		2.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	V_{CC} = 1.65 V to 3.6 V, and T_A = –40°C to 125°C (SN74LVC74A only)			0.2	V
			V_{CC} = 2.7 V to 3.6 V and T_A = –55°C to 125°C (SN54LVC74A only)			0.2	
		I_{OL} = 4 mA, V_{CC} = 1.65 V, and T_A = –40°C to 125°C (SN74LVC74A only)				0.45	
		I_{OL} = 8 mA, V_{CC} = 2.3 V, and T_A = –40°C to 125°C (SN74LVC74A only)				0.7	
		I_{OL} = 12 mA, V_{CC} = 2.7 V				0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V				0.55	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 3.6 V				±5	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 3.6 V				10	µA
$ΔI_{CC}$	Change in supply current	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, and V_{CC} = 2.7 V to 3.6 V				500	µA

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	$V_I = V_{CC}$ or GND, V_{CC} = 3.3 V, T_A = 25°C		5		pF

5.6 Timing Requirements: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

				MIN	MAX	UNIT
f_{clock}	Clock frequency	V_{CC} = 2.7 V			83	MHz
		V_{CC} = 3.3 V ± 0.3 V			100	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low		3.3		ns
		CLK high or low		3.3		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 2.7 V	3.4		ns
			V_{CC} = 3.3 V ± 0.3 V	3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	V_{CC} = 2.7 V	2.2		
			V_{CC} = 3.3 V ± 0.3 V	2		
t_h	Hold time, data after CLK↑			1		ns

5.7 Timing Requirements: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

				MIN	MAX	UNIT
f_{clock}	Clock frequency	V_{CC} = 1.8 V or 2.5 V			83	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 1.8 V ± 0.15 V	4.1		ns
			V_{CC} = 2.5 V ± 0.2 V	3.3		
		CLK high or low	V_{CC} = 1.8 V ± 0.15 V	4.1		
			V_{CC} = 2.5 V ± 0.2 V	3.3		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 1.8 V ± 0.15 V	3.6		ns
			V_{CC} = 2.5 V ± 0.2 V	2.3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	V_{CC} = 1.8 V ± 0.15 V	2.7		
			V_{CC} = 2.5 V ± 0.2 V	1.9		
t_h	Hold time, data after CLK↑	V_{CC} = 1.8 V or 2.5 V		1		ns

5.8 Timing Requirements: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

					MIN	MAX	UNIT
f_{clock}	Clock frequency	T_A = –40°C to 125°C	V_{CC} = 2.7 V			83	MHz
			V_{CC} = 3.3 V ± 0.3 V			100	
		T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V				150	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 2.7 V or 3.3 V		3.3		ns
		CLK high or low	V_{CC} = 2.7 V or 3.3 V		3.3		
t_{su}	Setup time before CLK↑	Data	T_A = –40°C to 125°C	V_{CC} = 2.7 V	3.4		ns
				V_{CC} = 3.3 V ± 0.3 V	3		
			T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	T_A = –40°C to 125°C	V_{CC} = 2.7 V	2.2		
				V_{CC} = 3.3 V ± 0.3 V	2		
			T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		2		
t_h	Hold time, data after CLK↑	V_{CC} = 2.7 V or 3.3 V			1		ns

5.9 Switching Characteristics: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—	V_{CC} = 2.7 V	83		MHz
				V_{CC} = 3.3 V ± 0.3 V	100		
t_{pd}	Propagation (delay) time	CLK	Q or $\overline{Q}$	V_{CC} = 2.7 V		6	ns
				V_{CC} = 2.7 V	1	5.2	
		$\overline{PRE}$ or $\overline{CLR}$		V_{CC} = 3.3 V ± 0.3 V		6.4	
				V_{CC} = 3.3 V ± 0.3 V	1	5.4	

5.10 Switching Characteristics: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—		83		MHz
t_{pd}	Propagation (delay) time	CLK $\overline{PRE}$	Q or $\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	1	7.1	ns
				V_{CC} = 2.5 V ± 0.2 V	1	4.4	
		or $\overline{CLR}$		V_{CC} = 1.8 V ± 0.15 V	1	6.9	
				V_{CC} = 2.5 V ± 0.2 V	1	4.6	

5.11 Switching Characteristics: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—	T_A = –40°C to 125°C	V_{CC} = 2.7 V	83		MHz
					V_{CC} = 3.3 V ± 0.3 V	100		
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		150		
t_{pd}	Propagation (delay) time	CLK	Q or $\overline{Q}$	T_A = –40°C to 125°C	V_{CC} = 2.7 V	1	6	ns
					V_{CC} = 3.3 V ± 0.3 V		5.2	
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		1	5.2	
		$\overline{PRE}$ or $\overline{CLR}$		T_A = –40°C to 125°C	V_{CC} = 2.7 V	1	6.4	
					V_{CC} = 3.3 V ± 0.3 V		5.4	
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		1	5.4	
$t_{sk(o)}$	Skew (time), output	—	—	T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V			1	ns

5.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	V_{CC} = 1.8 V	24	pF
			V_{CC} = 2.5 V	24	
			V_{CC} = 3.3 V	26	

5.13 Typical Characteristics

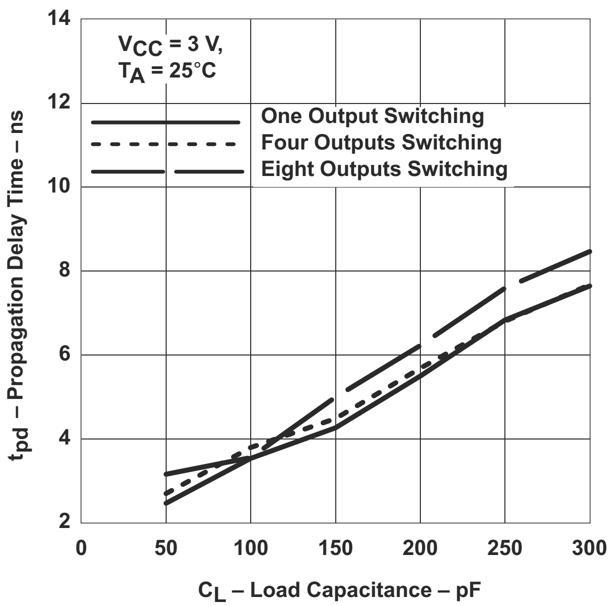


Figure 5-1. Propagation Delay (Low-to-High Transition) vs Load Capacitance

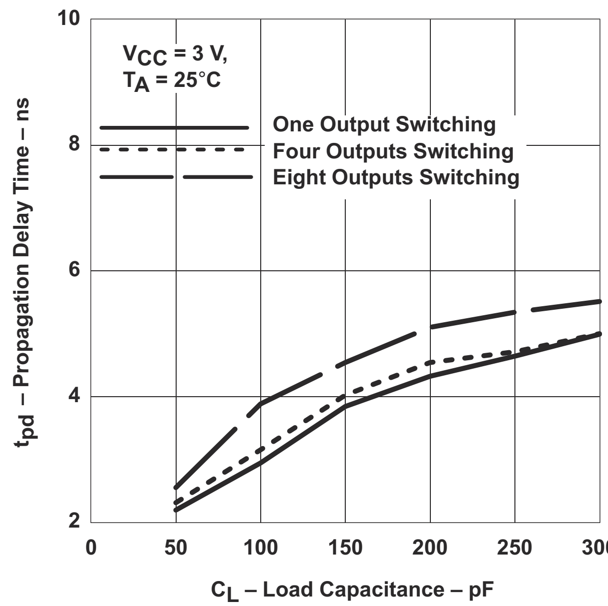


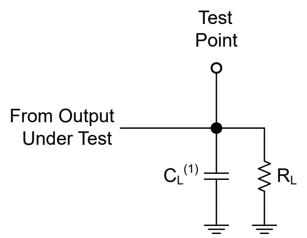
Figure 5-2. Figure 2. Propagation Delay (High-to-Low Transition) vs Load Capacitance

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

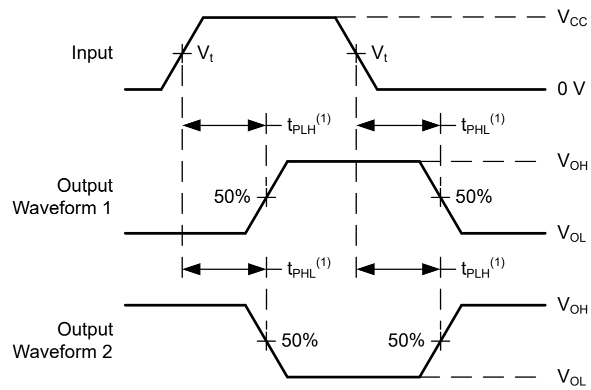
The outputs are measured individually with one input transition per measurement.

V_{CC}	V_t	R_L	C_L	ΔV
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



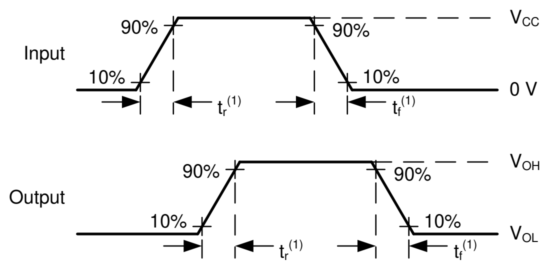
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

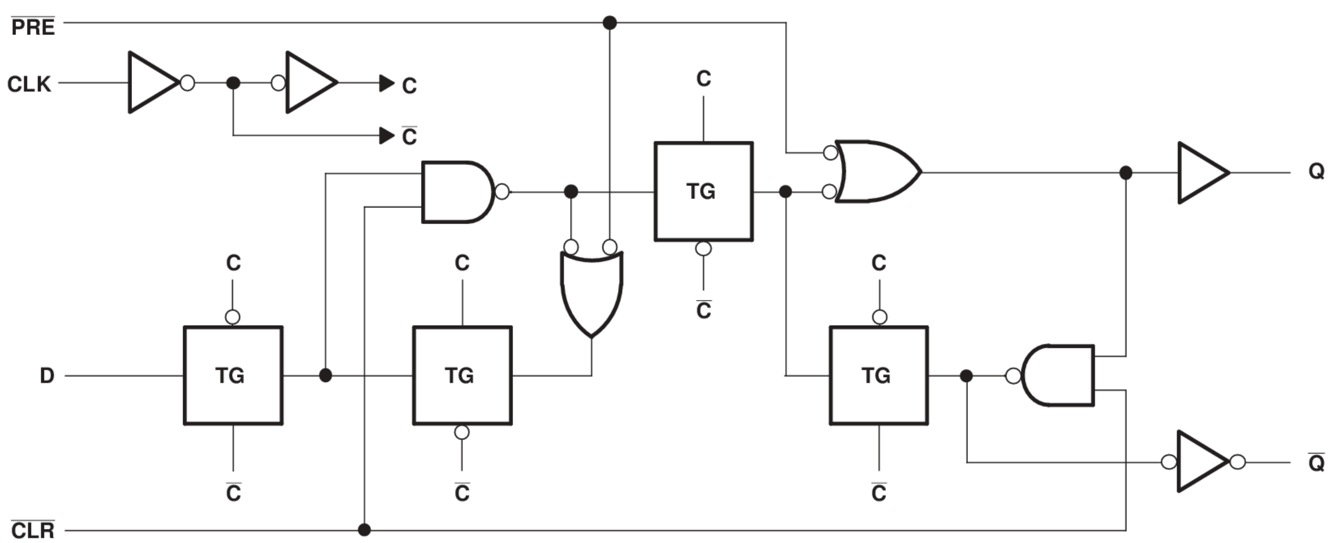
The SNx4LVC74A devices feature two independent positive-edge triggered D flip-flops. Integrated preset ($\overline{\text{PRE}}$) and clear ($\overline{\text{CLR}}$) functions allow for easy setup and control during operation.

The SN54LVC74A device is specified from –55°C to 125°C, and the SN74LVC74A device is specified from –40°C to 125°C.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

7.2 Functional Block Diagram



7.3 Feature Description

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

7.4 Device Functional Modes

Table 7-1 describes the SNx4LVC74A functionality and interactions between the $\overline{\text{PRE}}$, $\overline{\text{CLR}}$, CLK, and D inputs.

Table 7-1. Function Table

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L

Table 7-1. Function Table (continued)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A common application for the SN74LVC74A is a frequency divider. By connecting the $\overline{Q}$ output to the D input, the Q output toggles states on each positive edge of the incoming clock signal. Because it takes two positive edges, or two clock pulses, to complete one complete pulse on the output (one pulse to toggle from low to high, another to toggle from high to low), the incoming clock frequency is effectively divided by two.

8.2 Typical Application

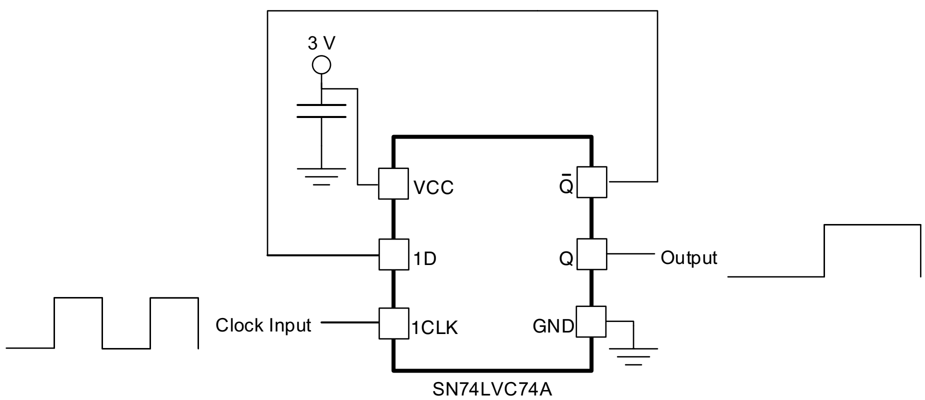


Figure 8-1. Frequency Divider

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specification, see (Δt/ΔV) in *Recommended Operating Conditions*.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Recommended maximum output conditions:

- Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
- Outputs must not be pulled above V_{CC}.

8.2.3 Application Curves

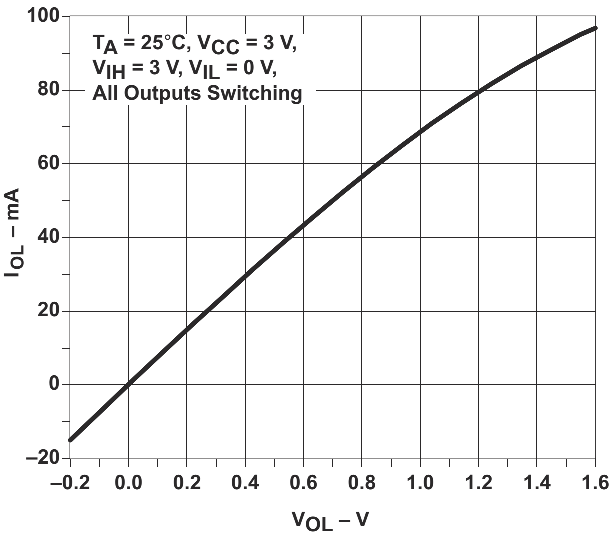


Figure 8-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

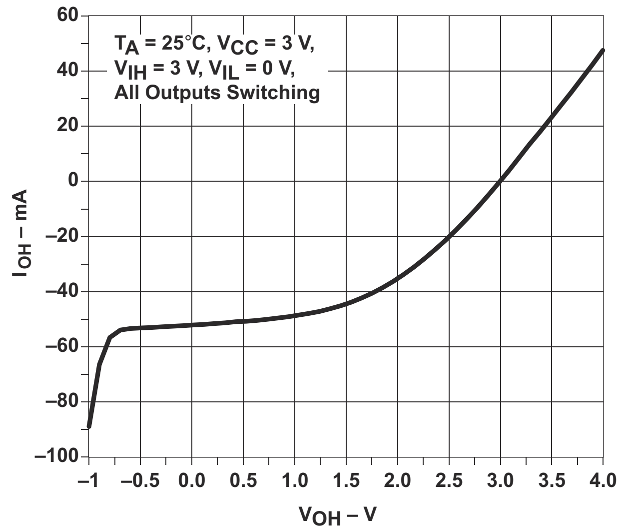


Figure 8-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

8.3 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions* .

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

8.4 Layout

8.4.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

8.4.2 Layout Example

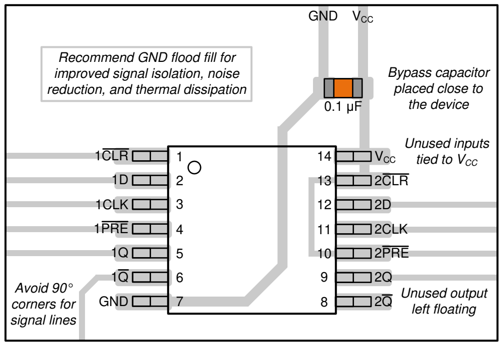


Figure 8-4. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision V (May 2024) to Revision W (December 2024) — **Page**

- Updated RθJA values: D = 93.7 to 127.8, DB = 107.3 to 140.4, NS = 90.3 to 123.8, PW = 121.7 to 150.8, RGY = 54.9 to 92.1; Updated D, DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.......... 5

Changes from Revision U (January 2017) to Revision V (May 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.......... 1
- Added BQA package to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table.......... 1
- Added package size to *Device Information* table.......... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9761601Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9761601Q2A SNJ54LVC 74AFK
5962-9761601QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ
5962-9761601QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW
5962-9761601VDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601VD A SNV54LVC74AW
SN74LVC74ABQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ABQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74AD.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBR.B	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADBRG4	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ADT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR.B	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74ANSR1G4.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC74ANSR1G4.B	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A
SN74LVC74APW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWG4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74APWTG4	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A
SN74LVC74ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYRG4.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SN74LVC74ARGYRG4.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A
SNJ54LVC74AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601Q2A SNJ54LVC 74AFK
SNJ54LVC74AJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QCA SNJ54LVC74AJ
SNJ54LVC74AW	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9761601QDA SNJ54LVC74AW

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A :

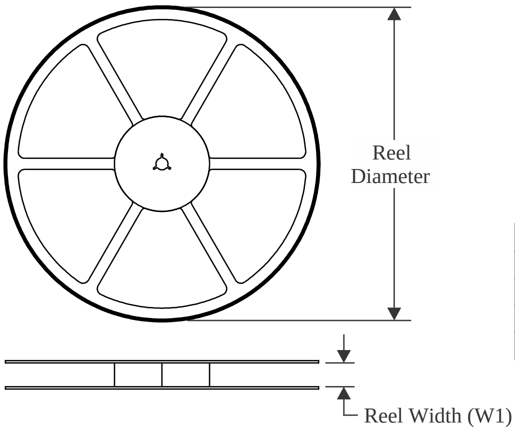
- Catalog : SN74LVC74A, SN54LVC74A
- Automotive : SN74LVC74A-Q1, SN74LVC74A-Q1
- Enhanced Product : SN74LVC74A-EP, SN74LVC74A-EP
- Military : SN54LVC74A
- Space : SN54LVC74A-SP

NOTE: Qualified Version Definitions:

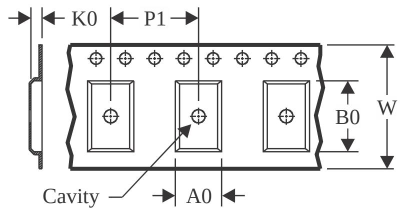
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

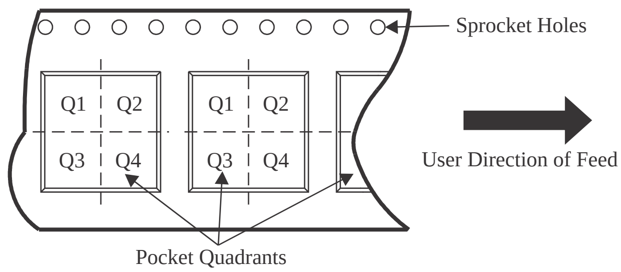


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

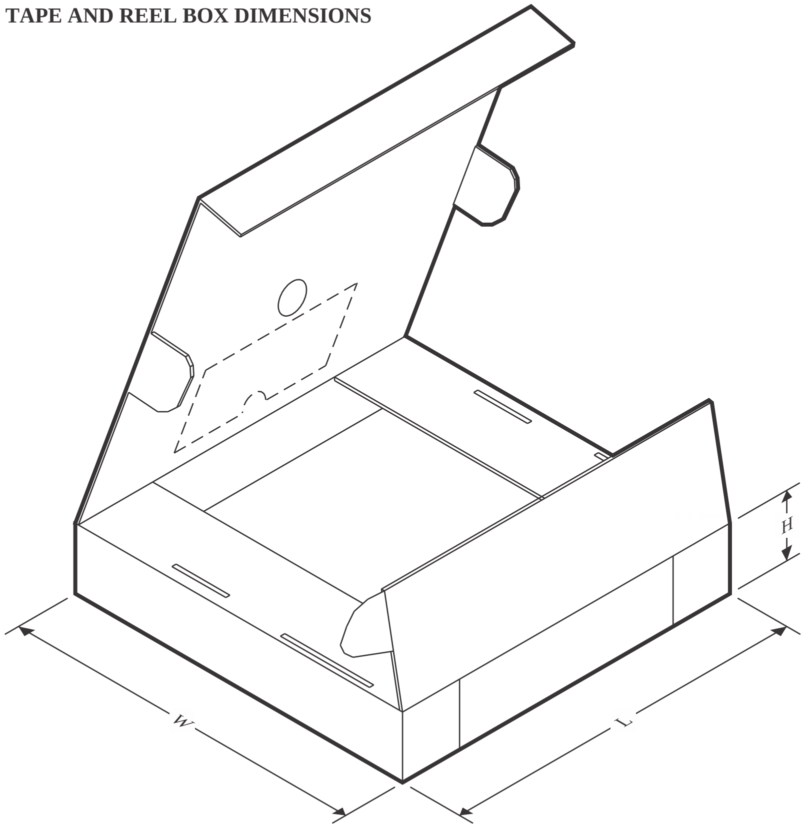
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC74ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

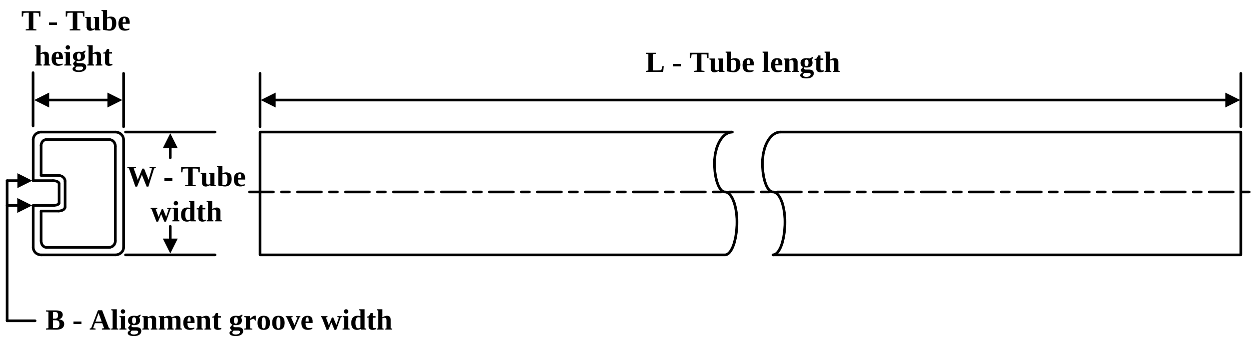
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

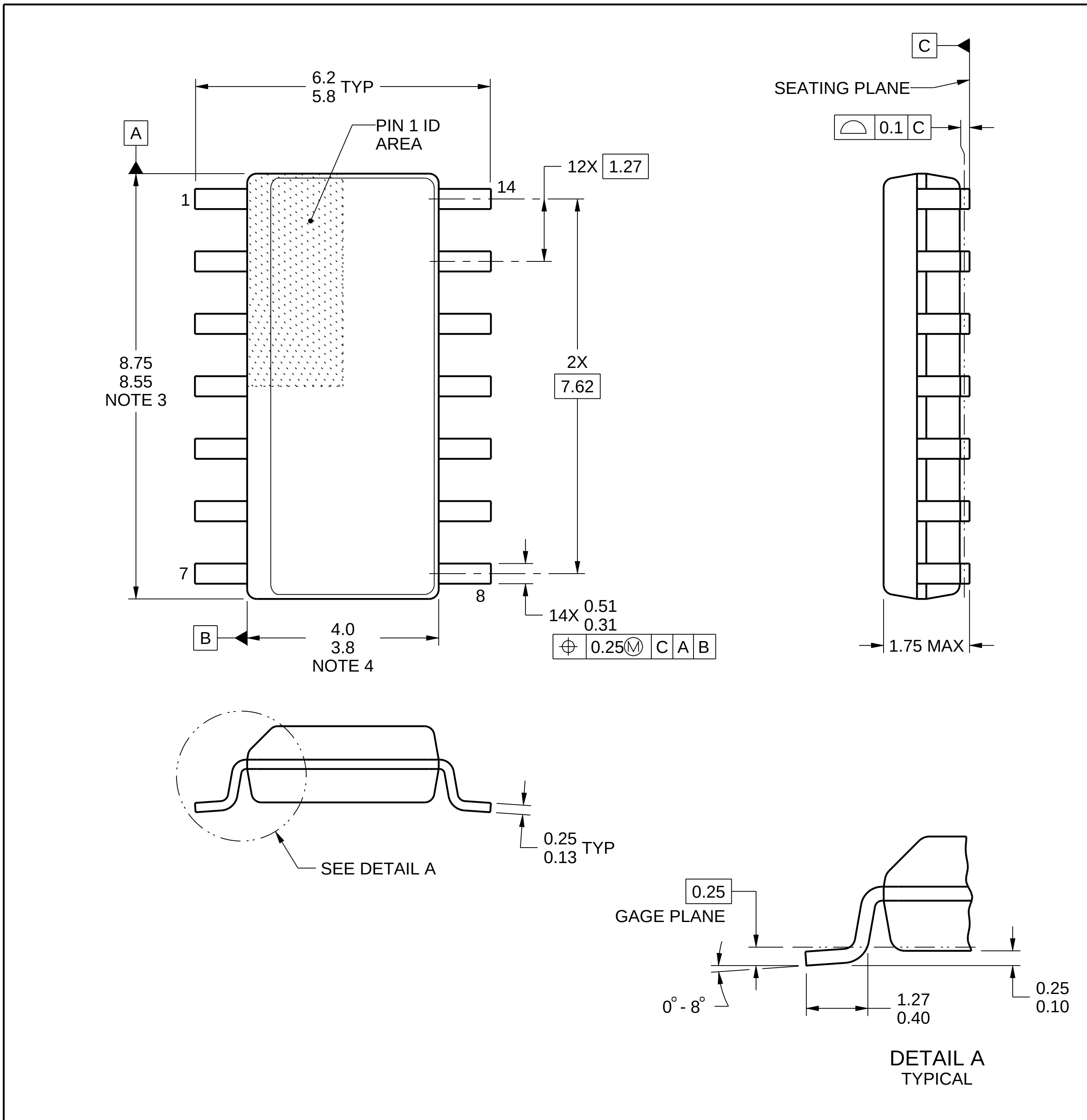
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC74ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC74ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC74ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC74ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC74ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LVC74APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC74APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC74APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC74APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC74ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

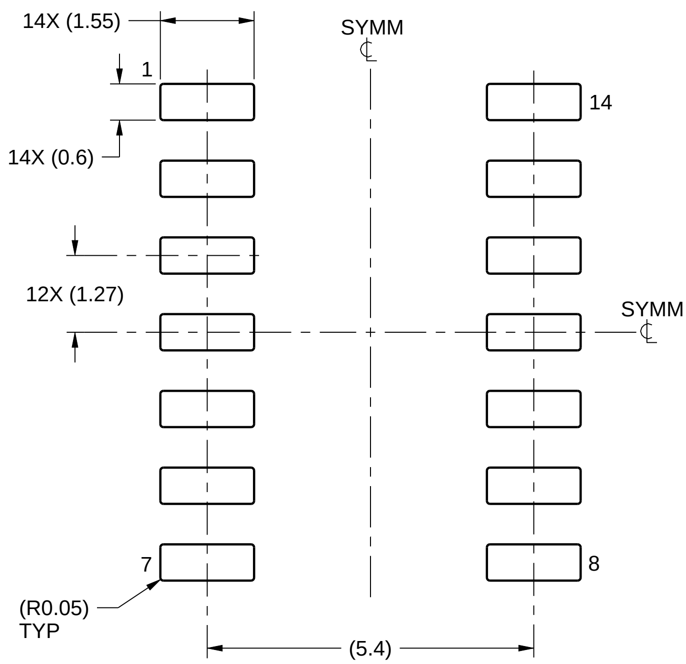
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761601VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC74AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC74AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC74APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC74APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC74APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA



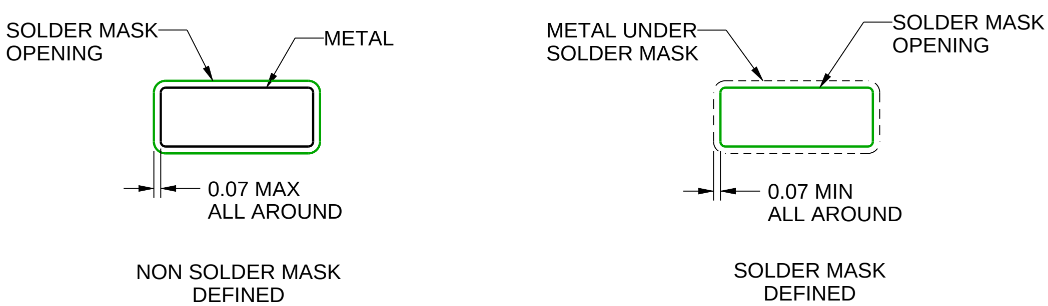
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

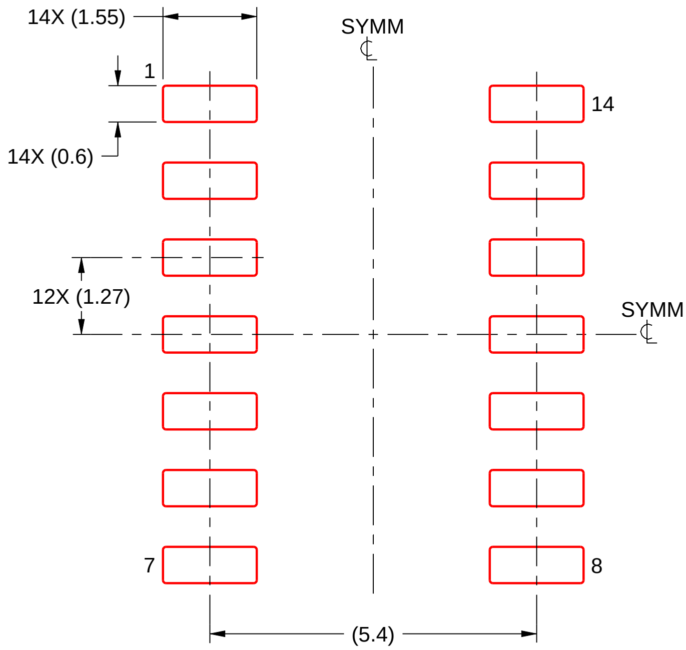


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



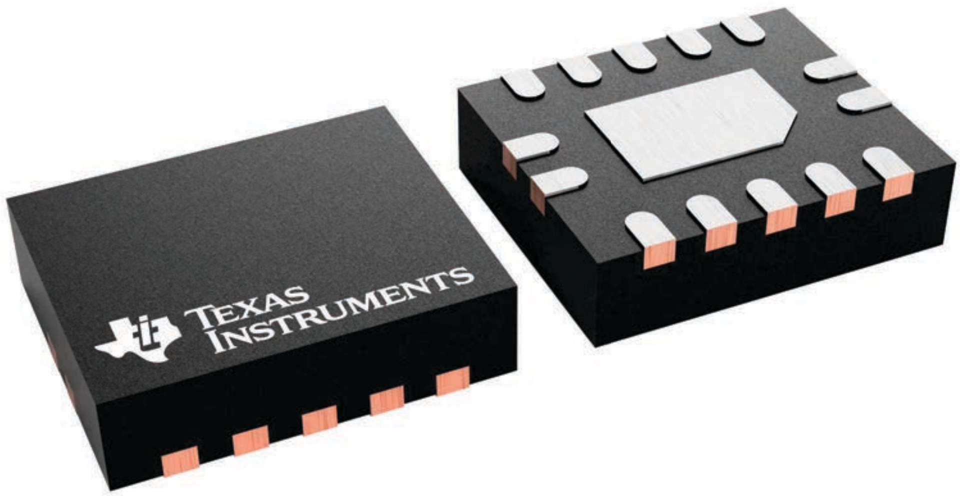
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

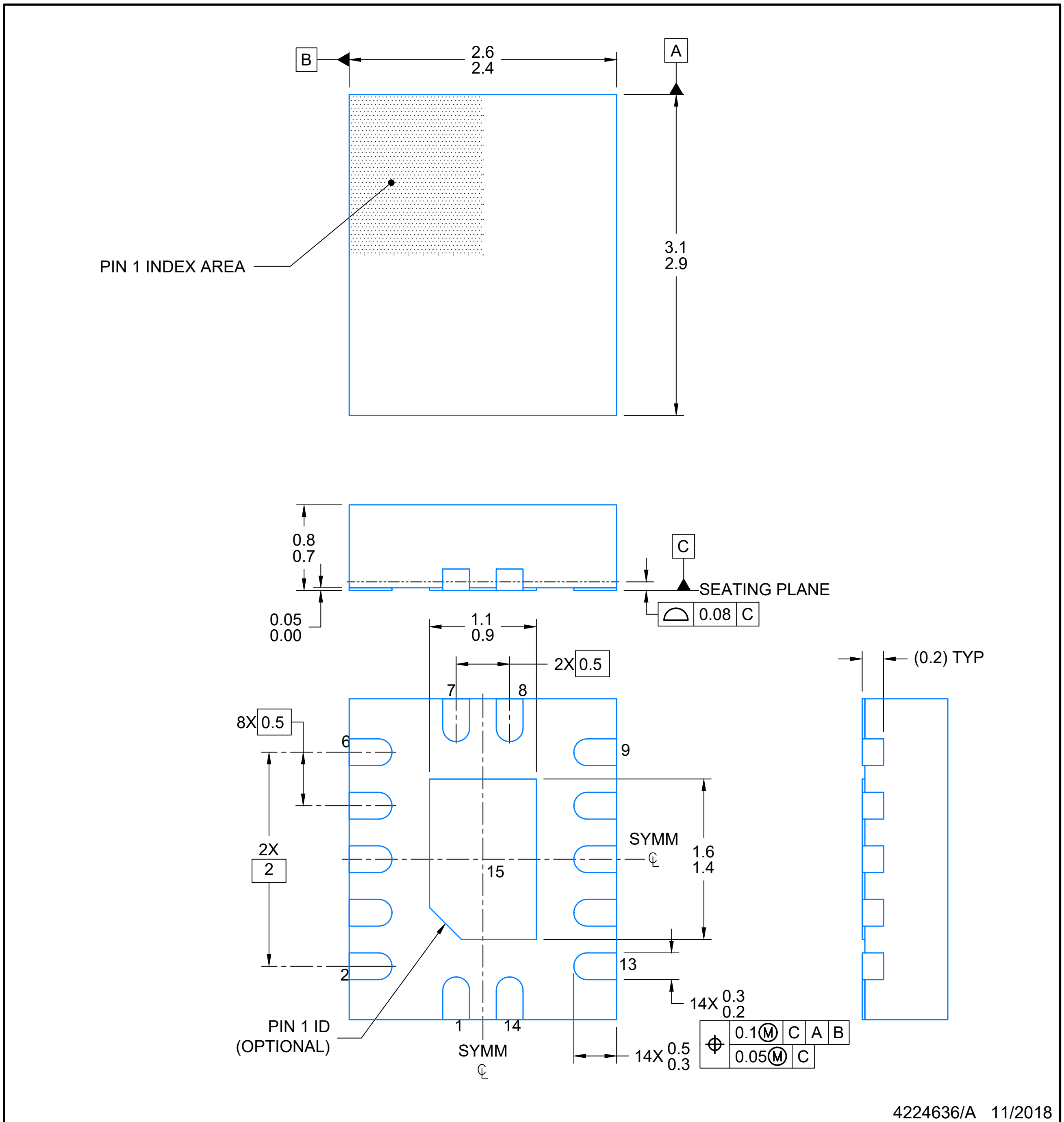
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

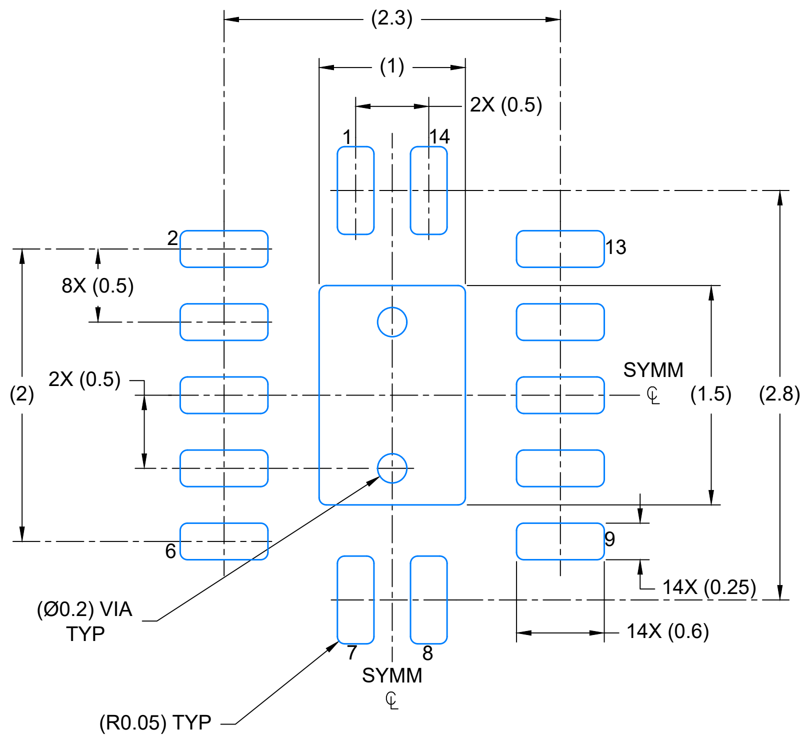


4227145/A

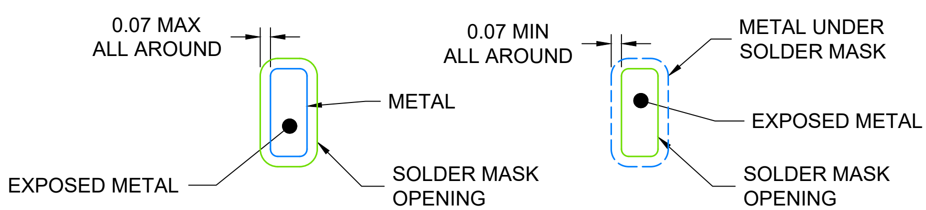


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



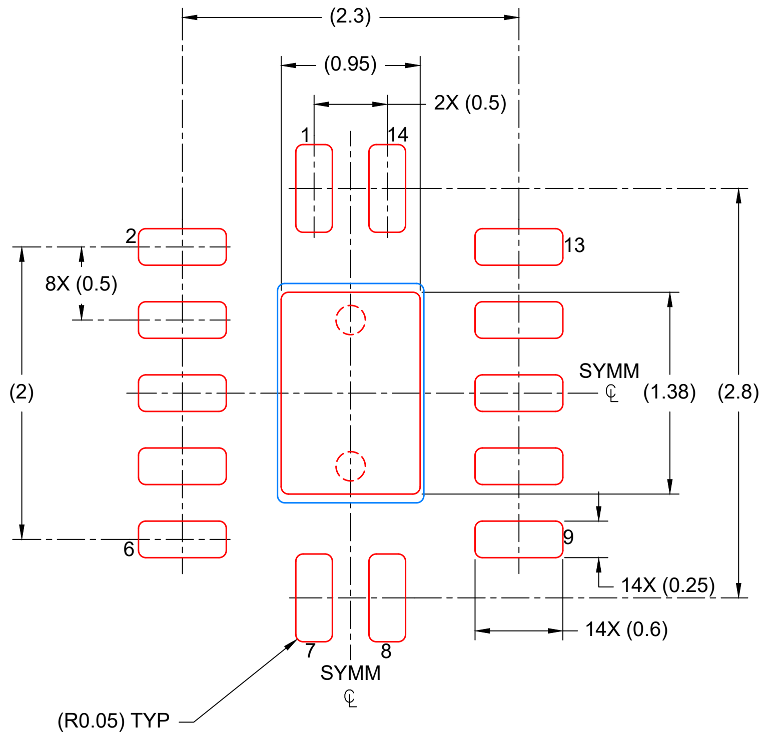
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

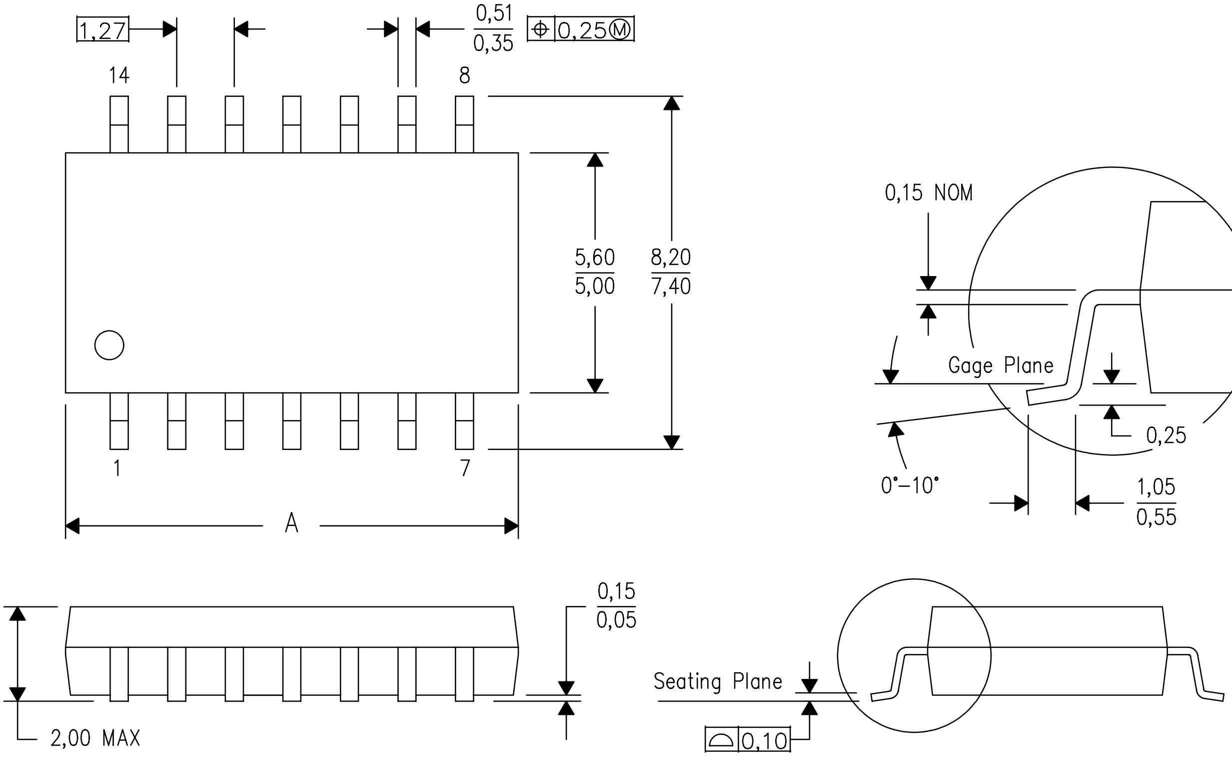
4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

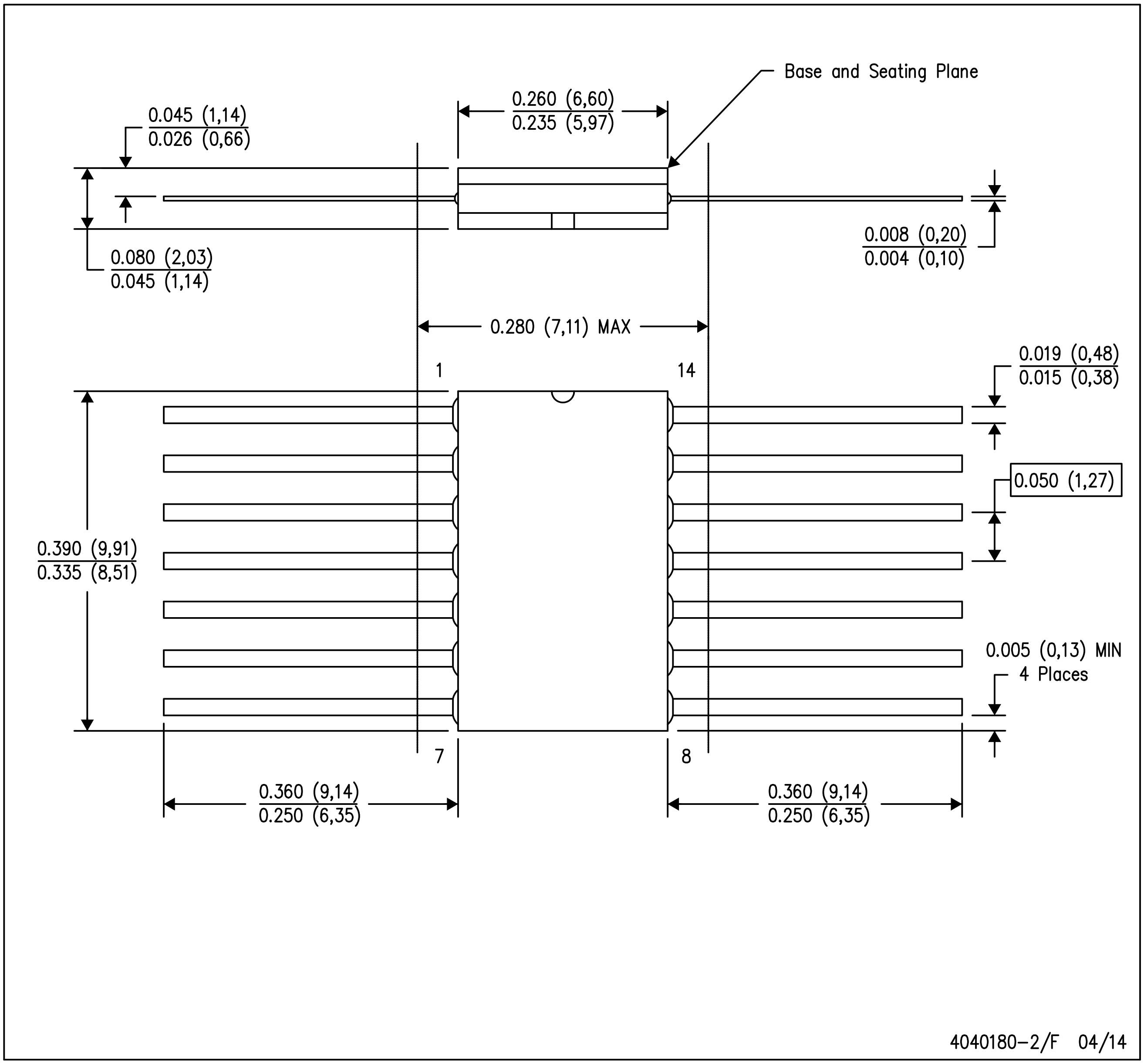


PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

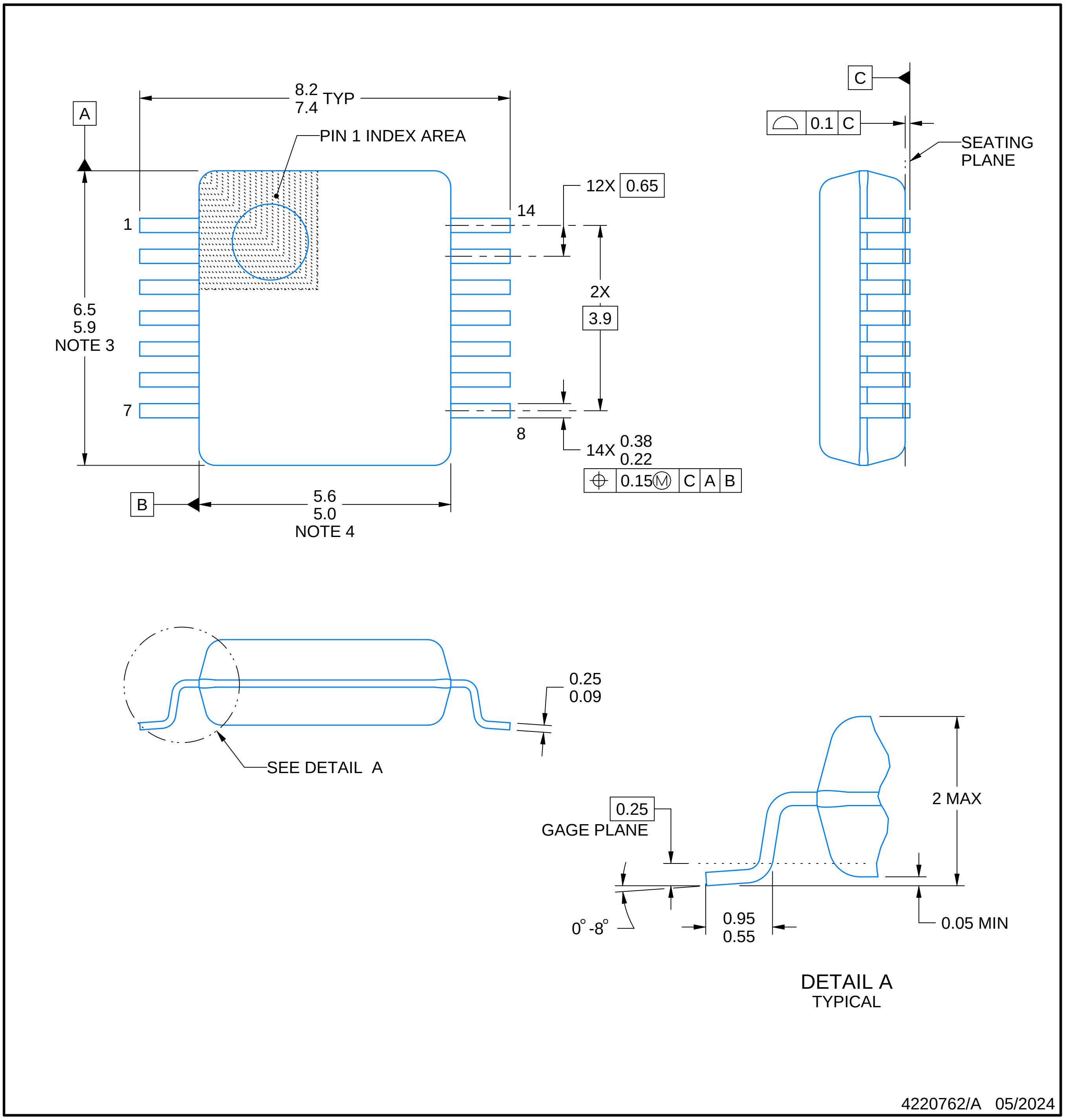
4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



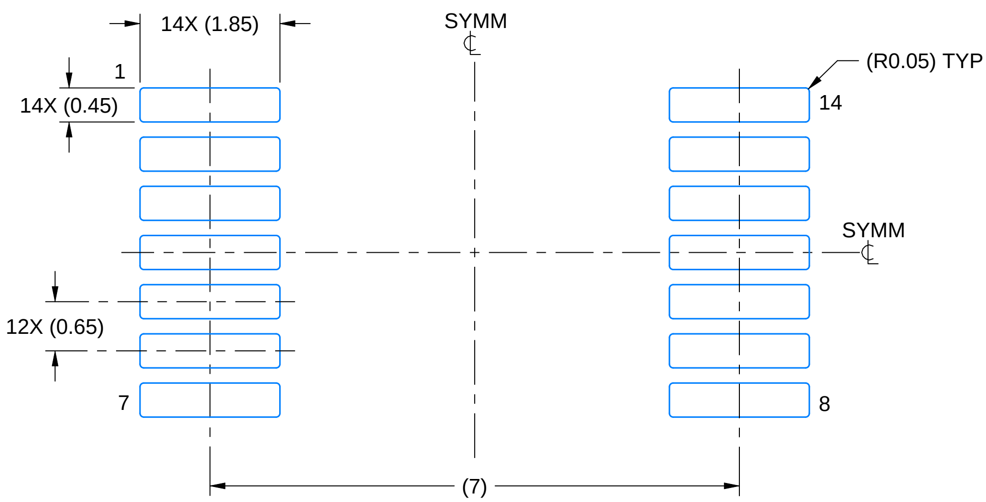
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14



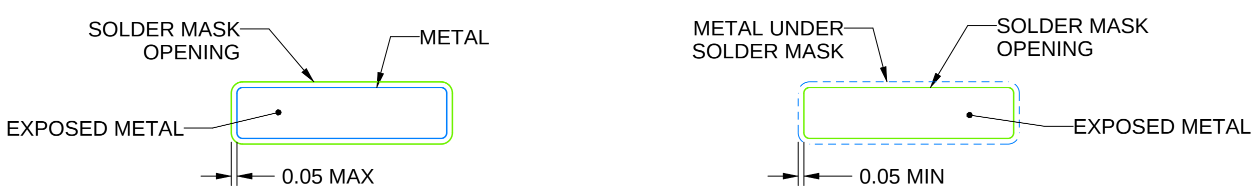
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

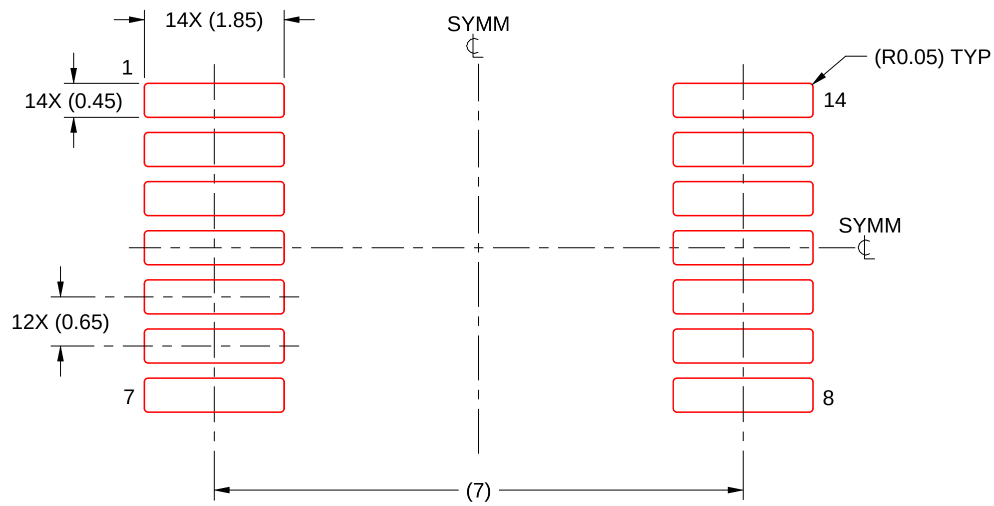
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

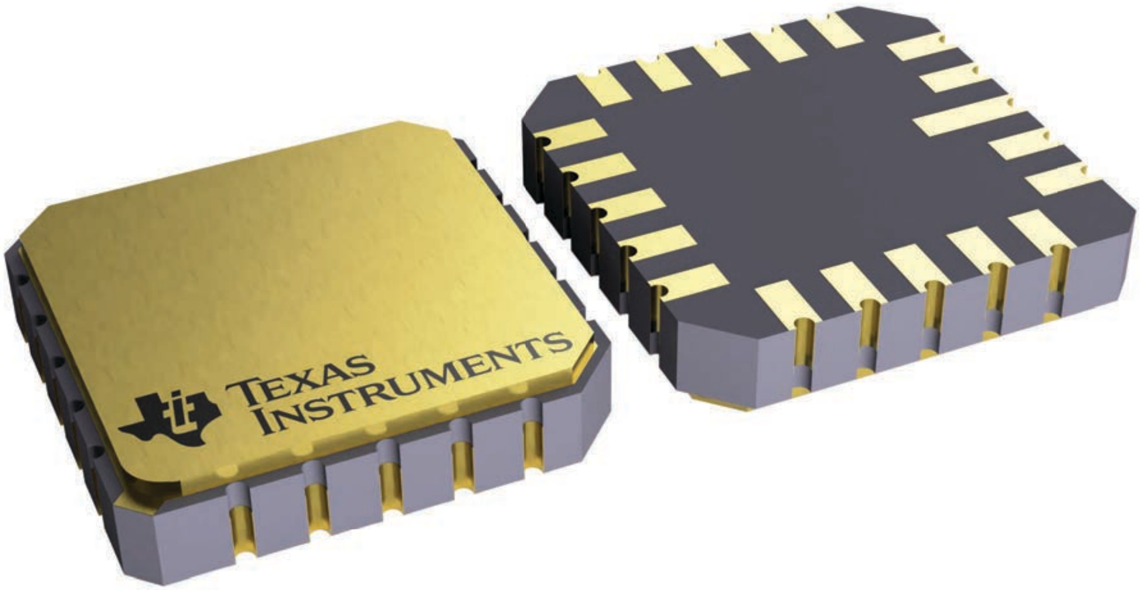
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

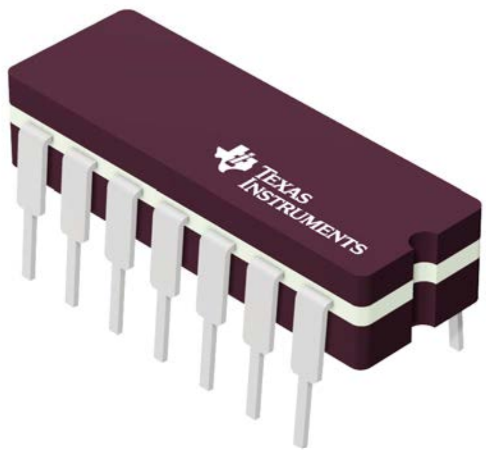
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370\A\

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

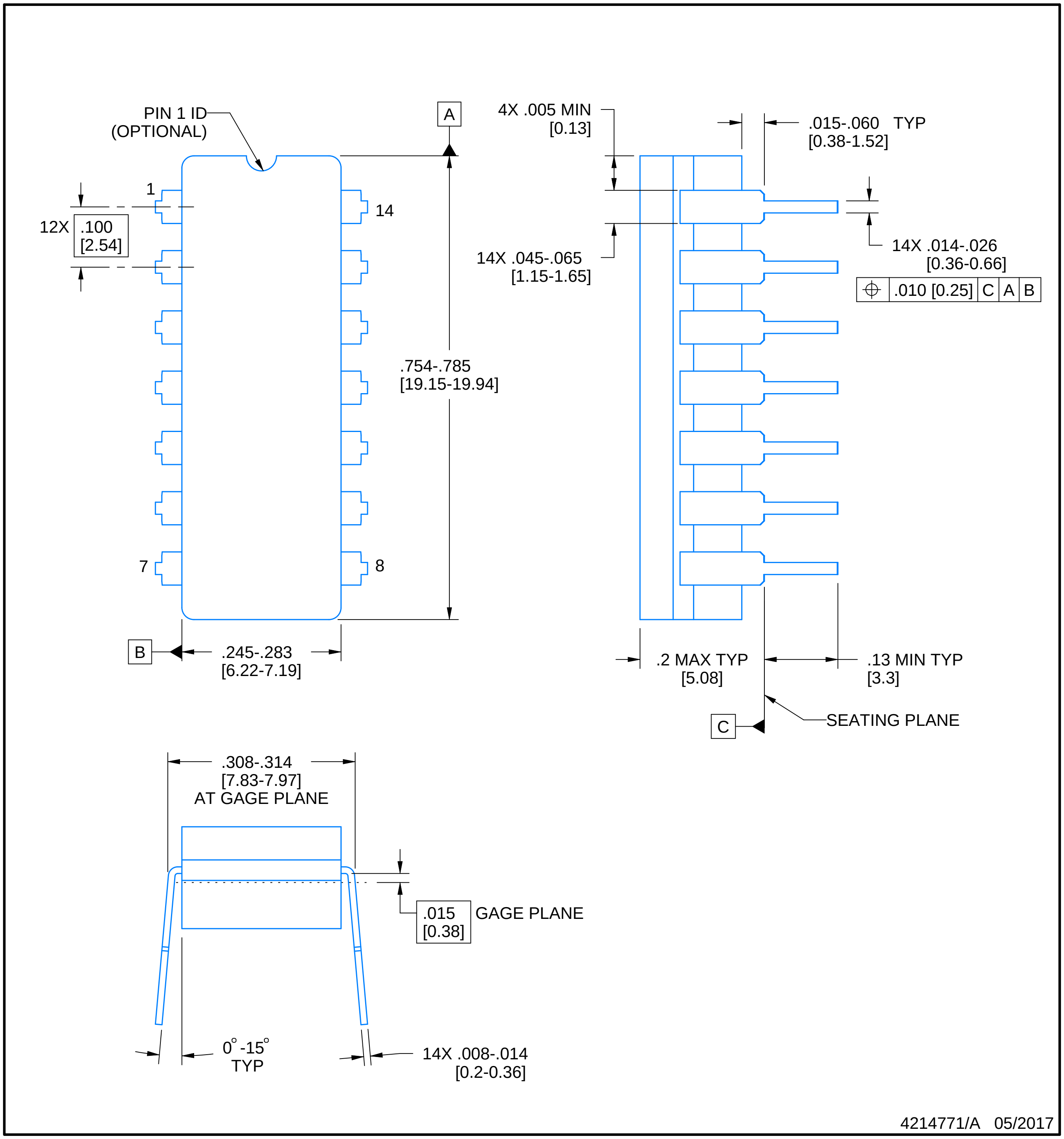
4040083-5/G

J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

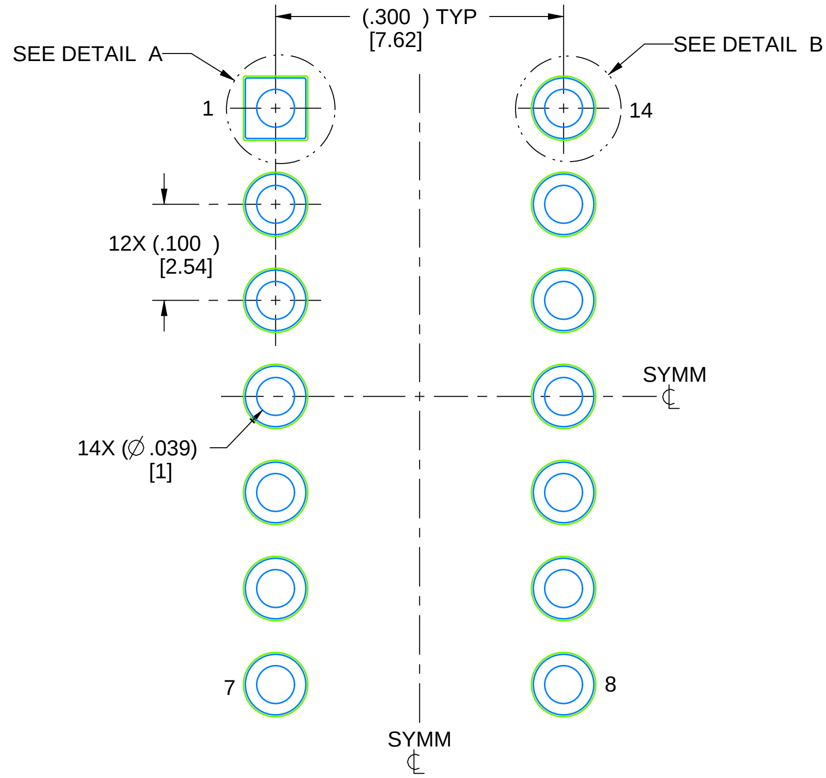
CERAMIC DUAL IN LINE PACKAGE



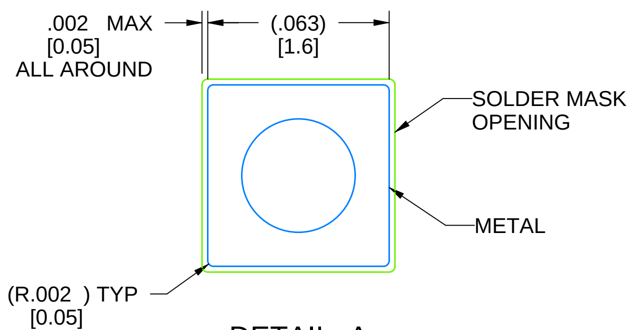
4214771/A 05/2017

NOTES:

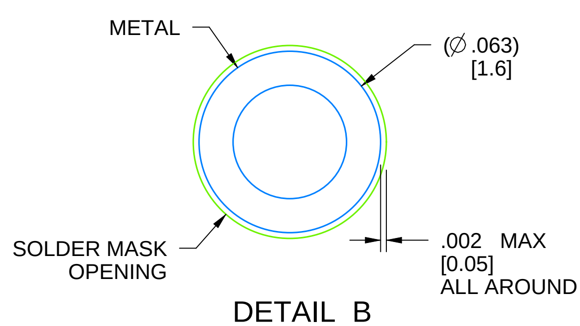
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

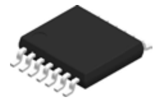


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

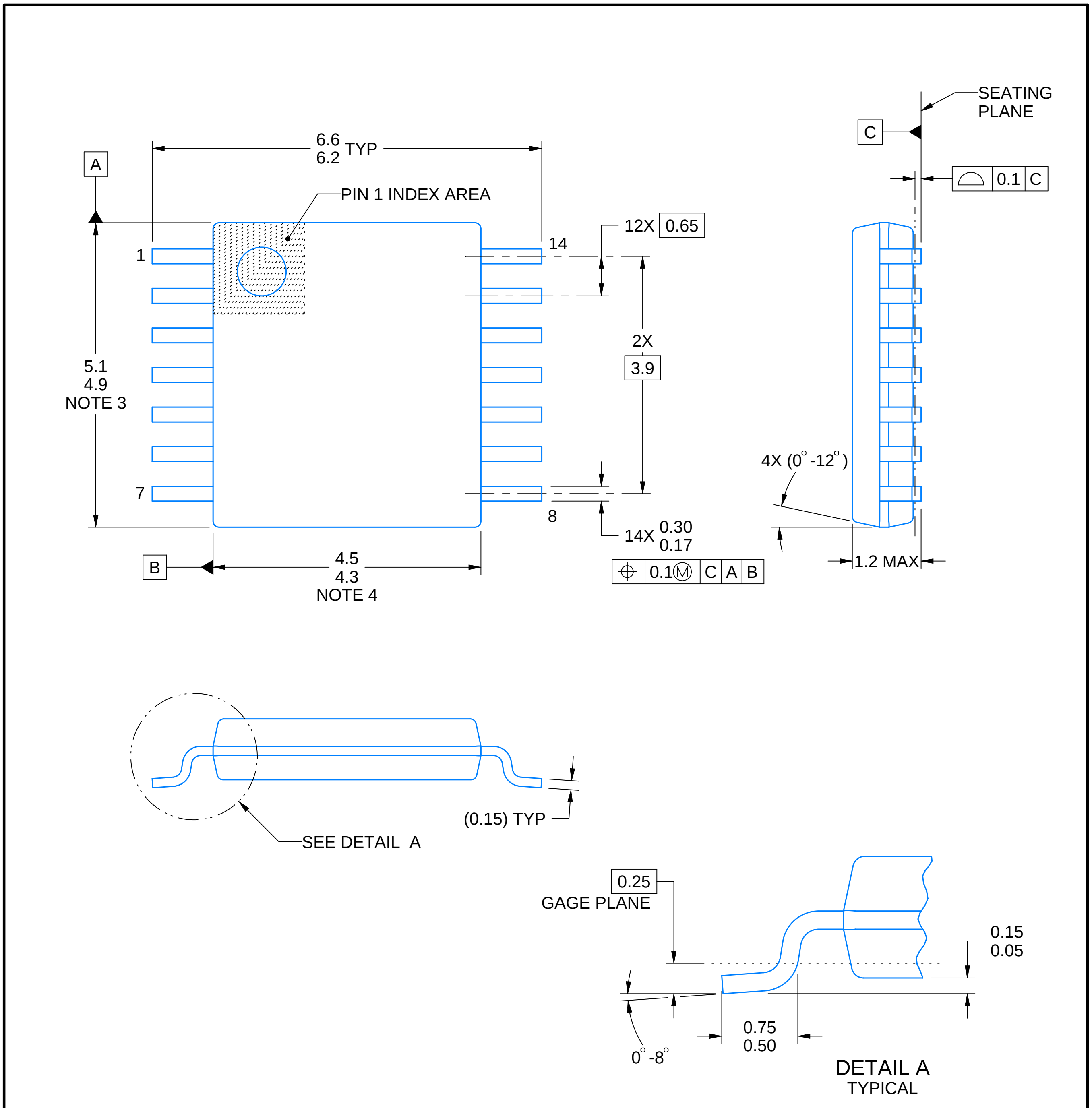
4214771/A 05/2017



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

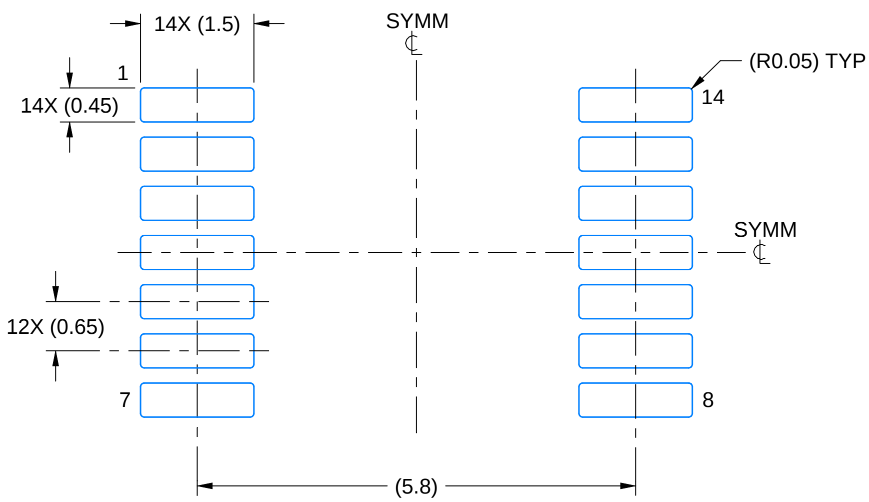
SMALL OUTLINE PACKAGE



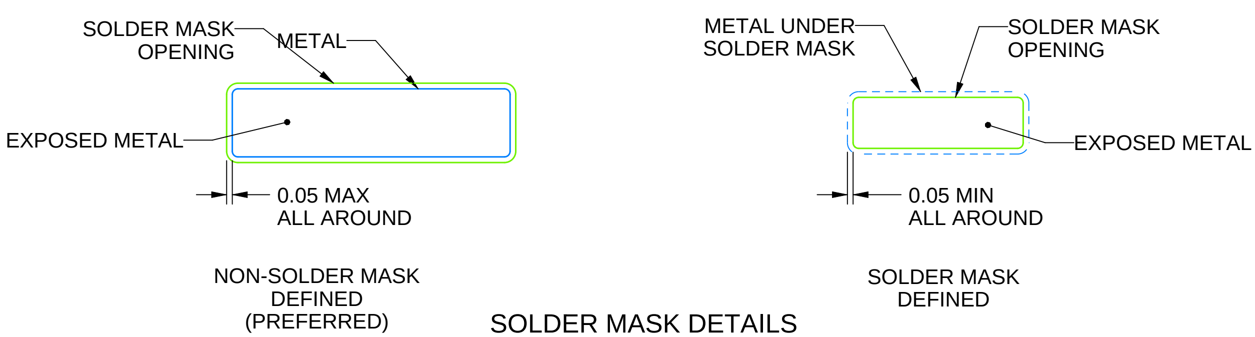
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

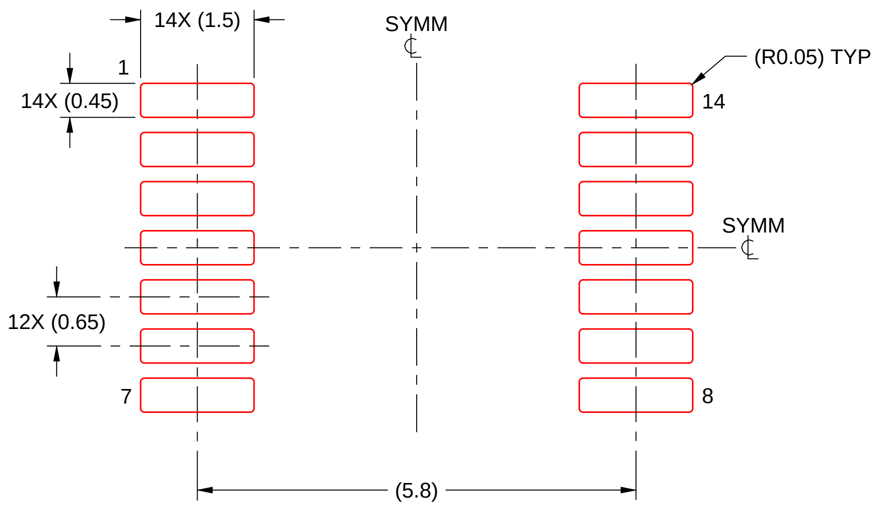


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

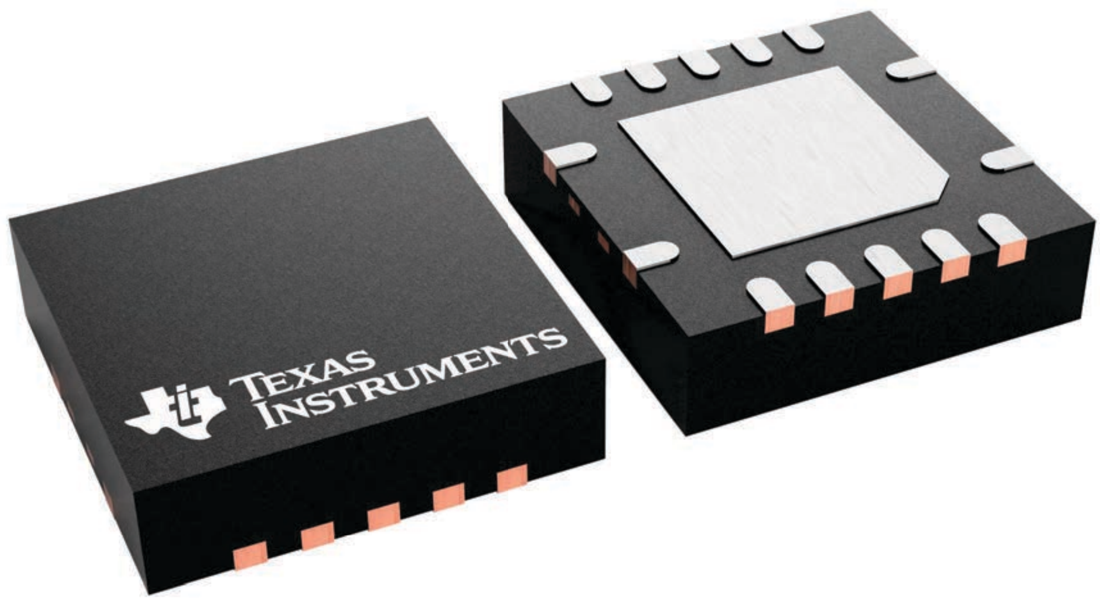
RGY 14

VQFN - 1 mm max height

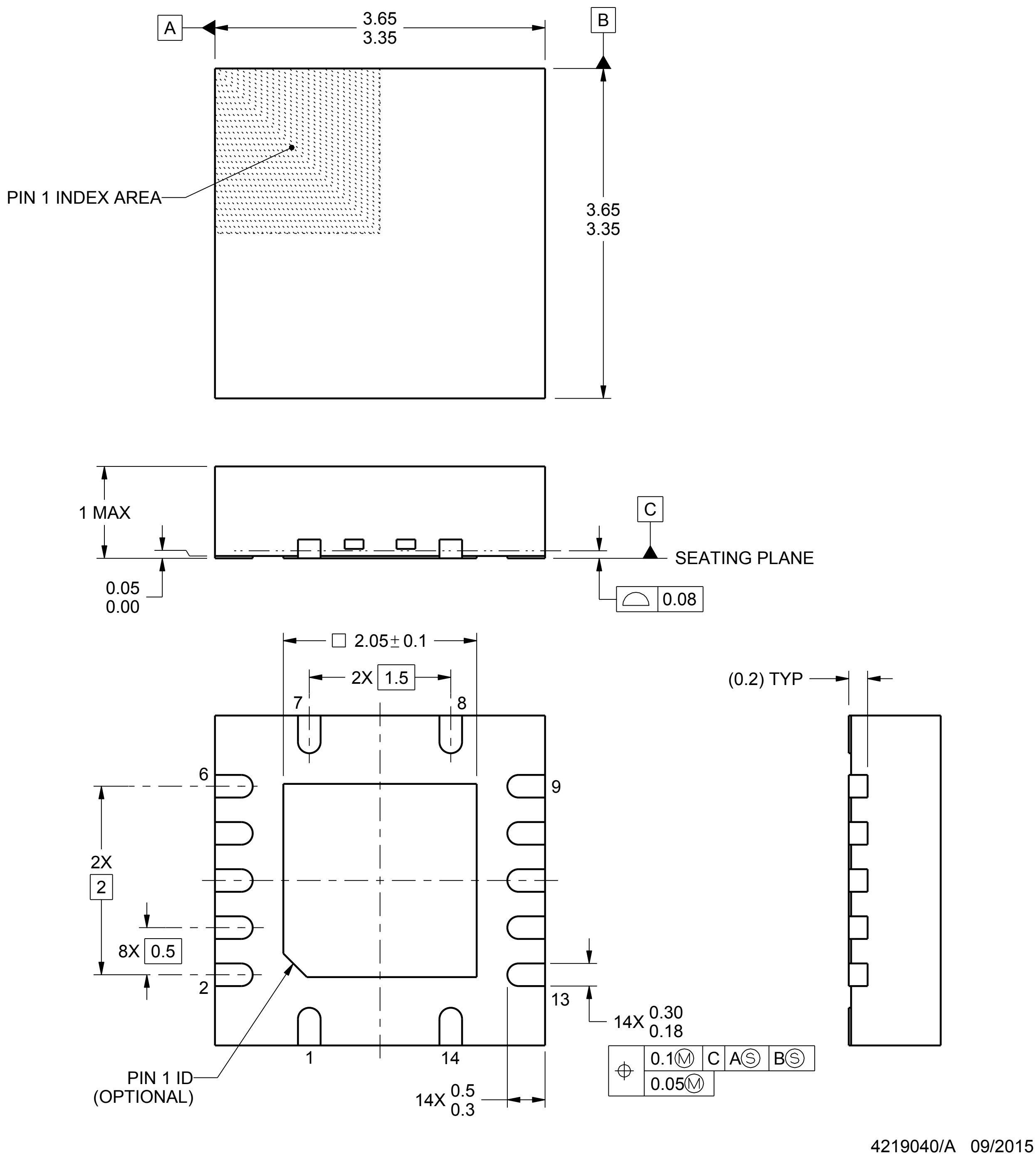
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

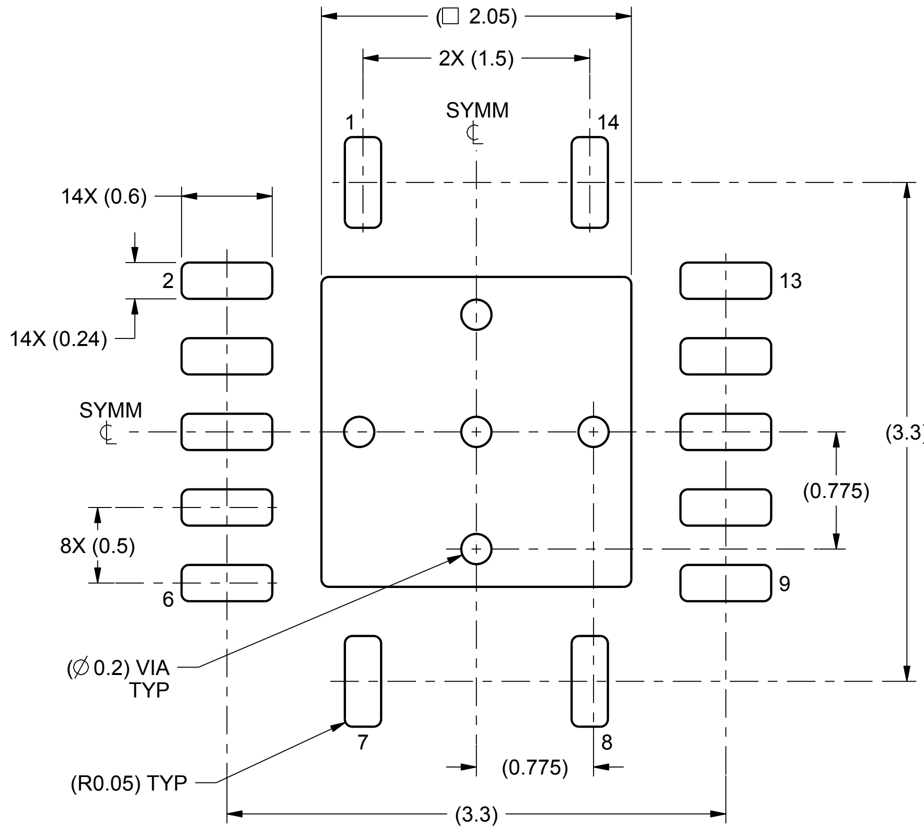


4231541/A

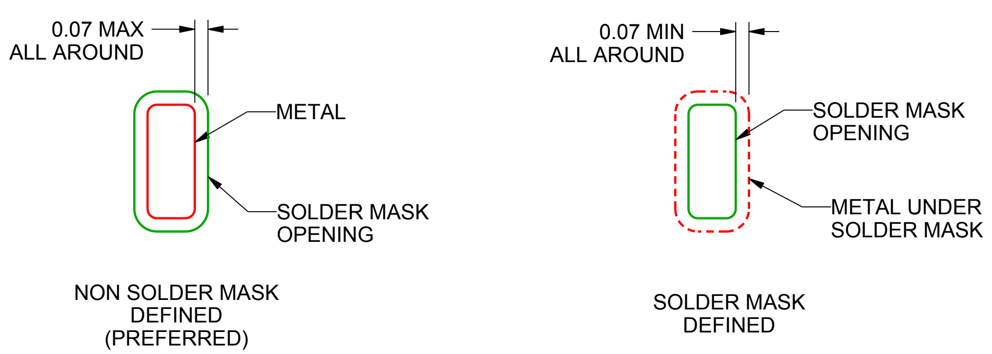


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

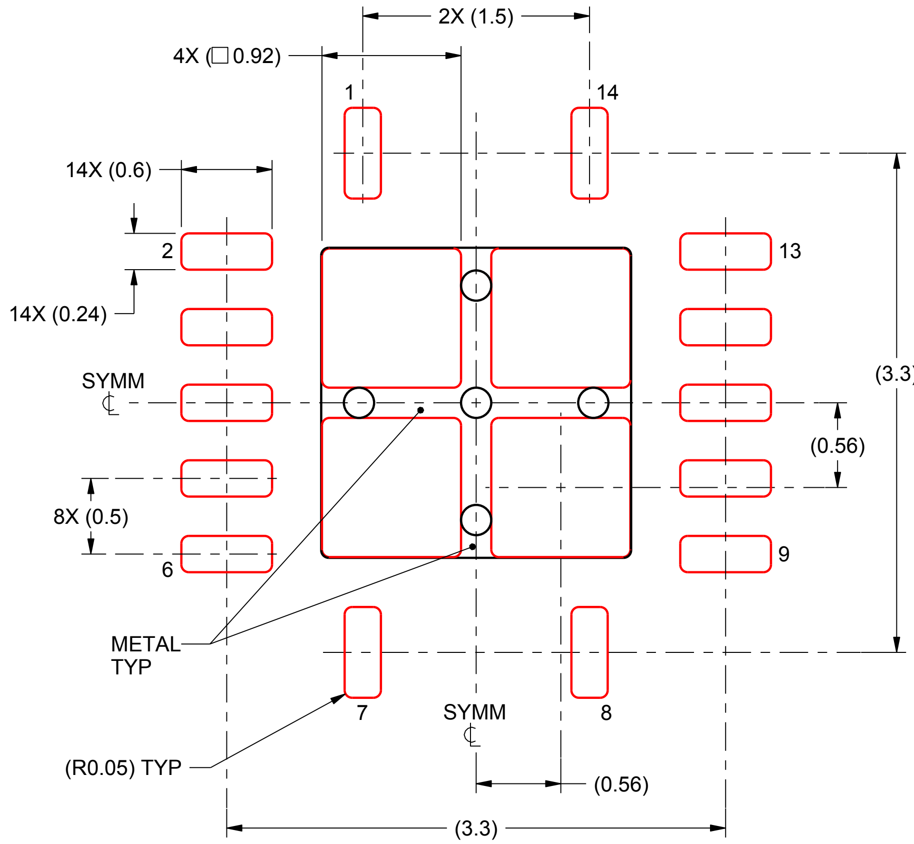


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265