

SNx4HC03 Quadruple 2-Input NAND Gates with Open-Drain Outputs

1 Features

- Wide Operating Voltage Range: 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Maximum I_{CC}
- Typical $t_{pd} = 8$ ns at 5 V
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A

2 Applications

- NAND OD

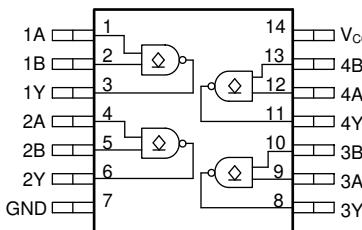
3 Description

This device contains four independent 2-input NAND Gates with open-drain outputs. Each gate performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ in positive logic.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|---------------------------|
| SN74HC03N | PDIP (14) | 19.30 mm \times 6.40 mm |
| SN74HC03NS | SO (14) | 10.20 mm \times 5.30 mm |
| SN74HC03D | SOIC (14) | 8.70 mm \times 3.90 mm |
| SN74HC03PW | TSSOP (14) | 5.00 mm \times 4.40 mm |
| SN54HC03J | CDIP (14) | 21.30 mm \times 7.60 mm |
| SN54HC03FK | LCCC (20) | 8.9 mm \times 8.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional pinout of the SN74HC03



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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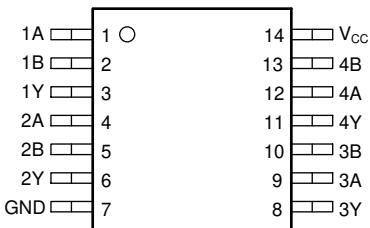
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4 Revision History

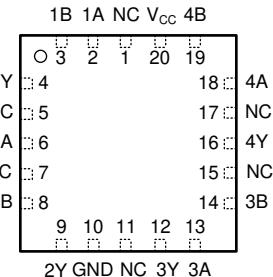
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (November 2003) to Revision F (April 2021) | Page |
|--|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Updated to new TIS format | 1 |
| • Increased D (86 to 133.6), NS (76 to 122.6), and PW (113 to 151.7); decreased N (80 to 66) °C/W..... | 4 |

Pin Configuration and Functions



**Figure 5-1. D, N, NS, PW, or J Package
14-Pin SOIC, PDIP, SO, TSSOP, or CDIP
Top View**



**Figure 5-2. FK Package
20-Pin LCCC
Top View**

Pin Functions

| PIN | | I/O | DESCRIPTION | |
|-----------------|-----------------------|------------------------|-------------|--------------------------|
| NAME | D, N, NS, PW, or J | | | |
| 1A | 1 | 2 | Input | Channel 1, Input A |
| 1B | 2 | 3 | Input | Channel 1, Input B |
| 1Y | 3 | 4 | Output | Channel 1, Output Y |
| 2A | 4 | 6 | Input | Channel 2, Input A |
| 2B | 5 | 8 | Input | Channel 2, Input B |
| 2Y | 6 | 9 | Output | Channel 2, Output Y |
| GND | 7 | 10 | — | Ground |
| 3Y | 8 | 12 | Output | Channel 3, Output Y |
| 3A | 9 | 13 | Input | Channel 3, Input A |
| 3B | 10 | 14 | Input | Channel 3, Input B |
| 4Y | 11 | 16 | Output | Channel 4, Output Y |
| 4A | 12 | 18 | Input | Channel 4, Input A |
| 4B | 13 | 19 | Input | Channel 4, Input B |
| V _{cc} | 14 | 20 | — | Positive Supply |
| NC | | 1, 5, 7, 11, 15, 17 | — | Not internally connected |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|---|--|------|-----|------|
| V _{CC} | Supply voltage | | -0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 | mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 | mA |
| | Continuous current through V _{CC} or GND | | | ±50 | mA |
| T _J | Junction temperature ⁽³⁾ | | | 150 | °C |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-----------------|-------------------------------------|-------------------------|------|-----------------|-----|------|
| V _{CC} | Supply voltage | | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | | V |
| | | V _{CC} = 4.5 V | 3.15 | | | |
| | | V _{CC} = 6 V | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | | V |
| | | V _{CC} = 4.5 V | | 1.35 | | |
| | | V _{CC} = 6 V | | 1.8 | | |
| V _I | Input voltage | | 0 | V _{CC} | | V |
| V _O | Output voltage | | 0 | V _{CC} | | V |
| Δt/Δv | Input transition rise and fall rate | V _{CC} = 2 V | | 1000 | | ns |
| | | V _{CC} = 4.5 V | | 500 | | |
| | | V _{CC} = 6 V | | 400 | | |
| T _A | Operating free-air temperature | SN54HC03 | -55 | 125 | | °C |
| | | SN74HC03 | -40 | 85 | | |

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74HC03 | | | | UNIT |
|-------------------------------|--|----------|----------|----------|------------|------|
| | | D (SOIC) | N (PDIP) | NS (SOP) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 133.6 | 66.0 | 122.6 | 151.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 89 | 53.7 | 81.8 | 79.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 89.5 | 45.7 | 83.8 | 94.7 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 45.5 | 33.3 | 45.4 | 25.2 | °C/W |

| THERMAL METRIC ⁽¹⁾ | | SN74HC03 | | | | UNIT |
|-------------------------------|--|----------|----------|----------|------------|------|
| | | D (SOIC) | N (PDIP) | NS (SOP) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| Ψ_{JB} | Junction-to-board characterization parameter | 89.1 | 45.5 | 83.4 | 94.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

5.4 Electrical Characteristics - 74

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

| PARAMETER | | TEST CONDITIONS | | V _{CC} | Operating free-air temperature (T _A) | | | UNIT | |
|-----------------|--------------------------|---|----------------------------------|--------------------------|--|-----------|------|-----------------|--|
| | | | | | 25°C | | | | |
| | | | | | MIN | TYP | MAX | | |
| I _{OH} | Output voltage | V _I = V _{IH} or V _{IL} | V _O = V _{CC} | 6 V | | 0.01 | 0.5 | 5 μ A | |
| V _{OL} | Low-level output voltage | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μ A | 2 V | | 0.002 | 0.1 | 0.1 | |
| | | | | 4.5 V | | 0.001 | 0.1 | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | 0.1 | |
| | | | | I _{OL} = 4 mA | 4.5 V | 0.17 | 0.26 | 0.33 | |
| | | | | I _{OL} = 5.2 mA | 6 V | 0.15 | 0.26 | 0.33 | |
| I _I | Input leakage current | V _I = V _{CC} or 0 | | 6 V | | \pm 0.1 | | \pm 1 μ A | |
| I _{CC} | Supply current | V _I = V _{CC} or 0 | I _O = 0 | 6 V | | 2 | | 20 μ A | |
| C _i | Input capacitance | | | 2 V to 6 V | | 3 | 10 | 10 pF | |

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

5.5 Electrical Characteristics - 54

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | V _{CC} | Operating free-air temperature (T _A) | | | | | | UNIT | |
|-----------------|--------------------------|---|----------------------------------|--------------------------|--|-----------|------|---------------|---------|-----|-----------------|------------|
| | | | | | 25°C | | | –40°C to 85°C | | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| I _{OH} | Output voltage | V _I = V _{IH} or V _{IL} | V _O = V _{CC} | 6 V | | 0.01 | 0.5 | | 5 | | 10 μ A | |
| V _{OL} | Low-level output voltage | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μ A | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | |
| | | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | | I _{OL} = 4 mA | 4.5 V | 0.17 | 0.26 | | 0.33 | | 0.4 | |
| | | | | I _{OL} = 5.2 mA | 6 V | 0.15 | 0.26 | | 0.33 | | 0.4 | |
| I _I | Input leakage current | V _I = V _{CC} or 0 | | 6 V | | \pm 0.1 | | | \pm 1 | | \pm 1 μ A | |
| I _{CC} | Supply current | V _I = V _{CC} or 0 | I _O = 0 | 6 V | | 2 | | 20 | | 40 | | 40 μ A |
| C _i | Input capacitance | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | 10 pF |

5.6 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

| PARAMETER | | FROM | TO | V_{CC} | Operating free-air temperature (T_A) | | | | | | UNIT | |
|-----------|--------------------------------|--------|----|----------|--|-----|-----|---------------|-----|-----|------|--|
| | | | | | 25°C | | | -40°C to 85°C | | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| t_{phl} | Propagation delay, low-to-high | A or B | Y | 2 V | 60 | 105 | | 131 | | 155 | ns | |
| | | | | 4.5 V | 13 | 25 | | 31 | | 36 | | |
| | | | | 6 V | 10 | 23 | | 27 | | 31 | | |
| t_{phl} | Propagation delay, high-to-low | A or B | Y | 2 V | 50 | 100 | | 125 | | 150 | ns | |
| | | | | 4.5 V | 10 | 20 | | 25 | | 30 | | |
| | | | | 6 V | 8 | 17 | | 21 | | 25 | | |
| t_t | Transition-time | | Y | 2 V | 38 | 75 | | 95 | | 110 | ns | |
| | | | | 4.5 V | 8 | 15 | | 19 | | 22 | | |
| | | | | 6 V | 6 | 13 | | 16 | | 19 | | |

5.7 Switching Characteristics - 74

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM | TO | V_{CC} | Operating free-air temperature (T_A) | | | | | | UNIT | |
|-----------|--------------------------------|--------|----|----------|--|-----|-----|---------------|-----|-----|------|--|
| | | | | | 25°C | | | -40°C to 85°C | | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| t_{phl} | Propagation delay, low-to-high | A or B | Y | 2 V | 60 | 105 | | 131 | | 155 | ns | |
| | | | | 4.5 V | 13 | 25 | | 31 | | 36 | | |
| | | | | 6 V | 10 | 23 | | 27 | | 31 | | |
| t_{phl} | Propagation delay, high-to-low | A or B | Y | 2 V | 50 | 100 | | 125 | | 150 | ns | |
| | | | | 4.5 V | 10 | 20 | | 25 | | 30 | | |
| | | | | 6 V | 8 | 17 | | 21 | | 25 | | |
| t_t | Transition-time | | Y | 2 V | 38 | 75 | | 95 | | 110 | ns | |
| | | | | 4.5 V | 8 | 15 | | 19 | | 22 | | |
| | | | | 6 V | 6 | 13 | | 16 | | 19 | | |

5.8 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|--|------------|-----|-----|-----|------|
| C_{pd} | Power dissipation capacitance per gate | No load | | 2 V to 6 V | | 20 | | pF |

5.9 Typical Characteristics

$T_A = 25^\circ\text{C}$

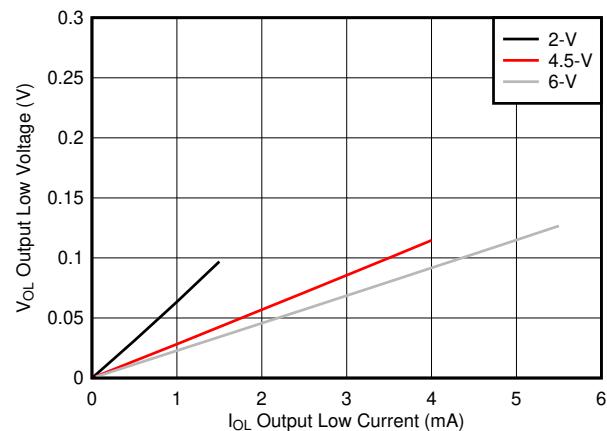
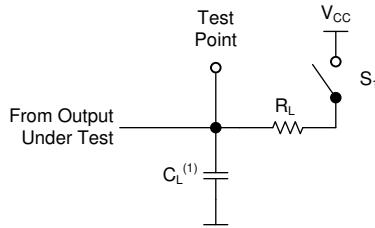


Figure 5-1. Typical output voltage in the low state (V_{OL})

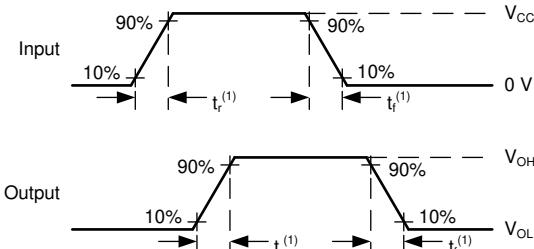
6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f < 6$ ns.
- The outputs are measured one at a time, with one input transition per measurement.



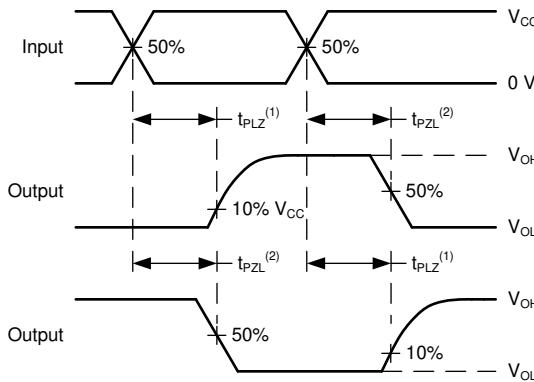
A. $C_L = 50$ pF and includes probe and jig capacitance.

Figure 6-1. Load Circuit



A. t_t is the greater of t_r and t_f .

Figure 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

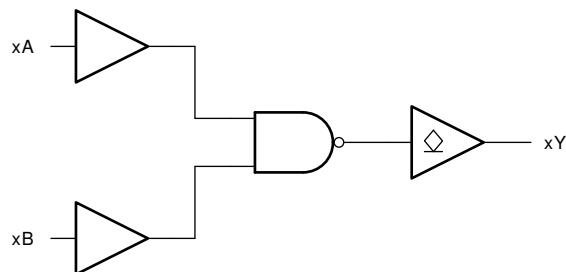
Figure 6-3. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Overview

This device contains four independent 2-input NAND gates with open-drain outputs. Each gate performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from V_{CC} . When the output is not actively pulling the line low, it will go into a high impedance state. This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pull-up resistor.

The current drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The SN74HC03 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Switching Characteristics - 74](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics - 74](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics - 74](#), using ohm's law ($R = V / I$).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

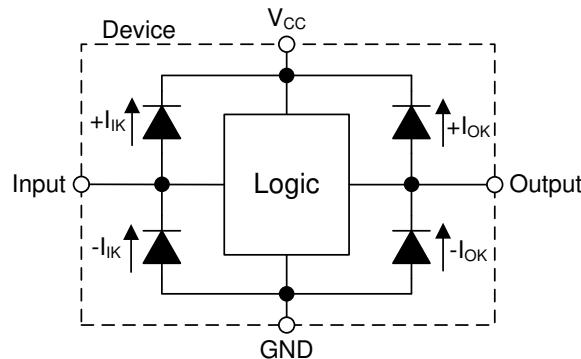


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | Z |
| X | L | Z |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, one 2-input open-drain NAND gate is used as shown in [Figure 8-1](#). The other three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

This device is used to directly control an LED. The LED is on when the inputs are both high, and off any other time.

8.2 Typical Application

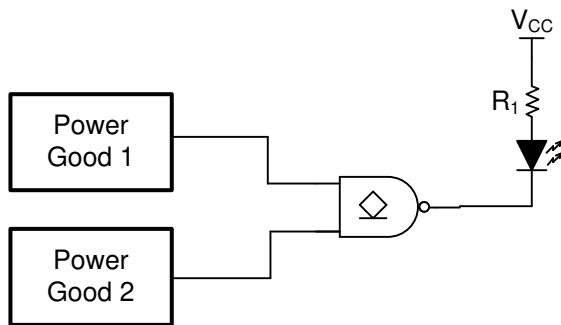


Figure 8-1. Typical application schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics - 74](#).

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HC03 plus the maximum supply current, I_{CC} , listed in [Electrical Characteristics - 74](#). The logic device can only sink as much current as is provided by the external pull-up resistor or other supply source. Be sure not to exceed the maximum total current through GND listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\max)$ listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is

used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC03, as specified in the [Electrical Characteristics - 74](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HC03 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to the [Section 7.3](#) for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics -74](#). The plot in the [Typical Characteristics](#) provides a typical relationship between output voltage and current for this device.

Open-drain outputs can be directly connected together to produce a wired-AND. This is possible because the outputs cannot source current, and thus can never be in bus-contention.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [Section 7.3](#) for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in [Section 10](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC03 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

8.2.3 Application Curves

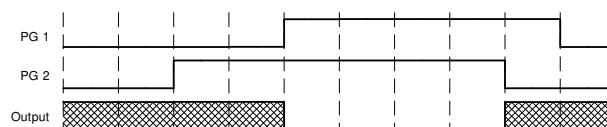


Figure 8-2. Typical application timing diagram

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 10-1*.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10.2 Layout Example

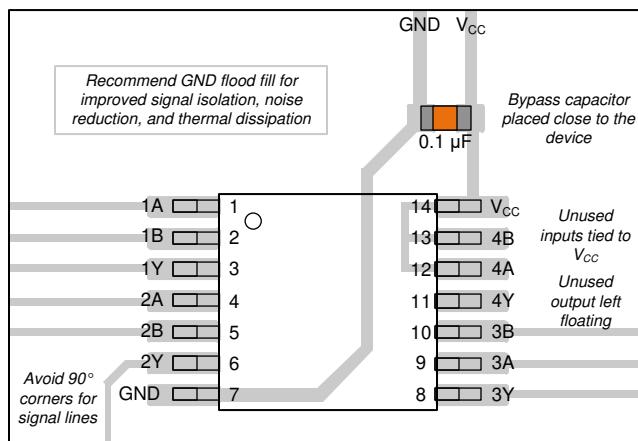


Figure 10-1. Example layout for the SN74HC03

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11-1. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54HC03 | Click here |
| SN74HC03 | Click here |

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------------|
| 5962-87647012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87647012A SNJ54HC 03FK |
| 5962-8764701CA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8764701CA SNJ54HC03J |
| SN54HC03J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC03J |
| SN54HC03J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC03J |
| SN74HC03D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | HC03 |
| SN74HC03DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03DR1G4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03DR1G4.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03DT | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | HC03 |
| SN74HC03N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC03N |
| SN74HC03N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC03N |
| SN74HC03NE4 | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC03N |
| SN74HC03NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03NSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03PW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -40 to 85 | HC03 |
| SN74HC03PWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03PWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03PWRG4 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SN74HC03PWRG4.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC03 |
| SNJ54HC03FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87647012A SNJ54HC 03FK |
| SNJ54HC03FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87647012A SNJ54HC 03FK |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------|
| SNJ54HC03J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8764701CA SNJ54HC03J |
| SNJ54HC03J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8764701CA SNJ54HC03J |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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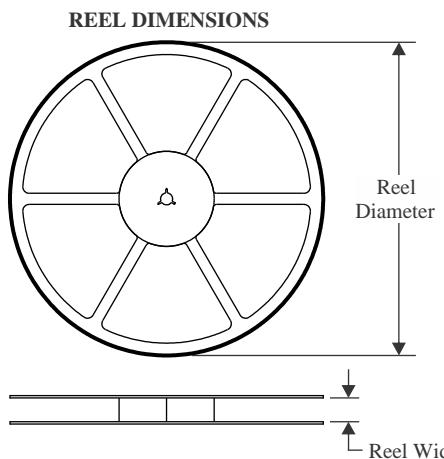
OTHER QUALIFIED VERSIONS OF SN54HC03, SN74HC03 :

- Catalog : [SN74HC03](#)

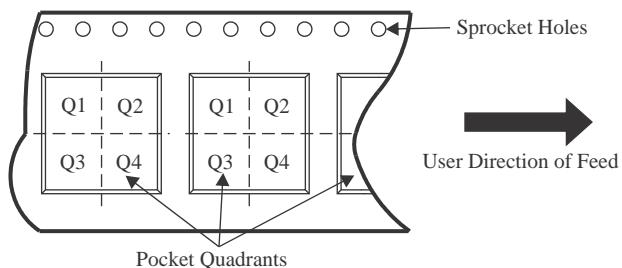
- Military : [SN54HC03](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

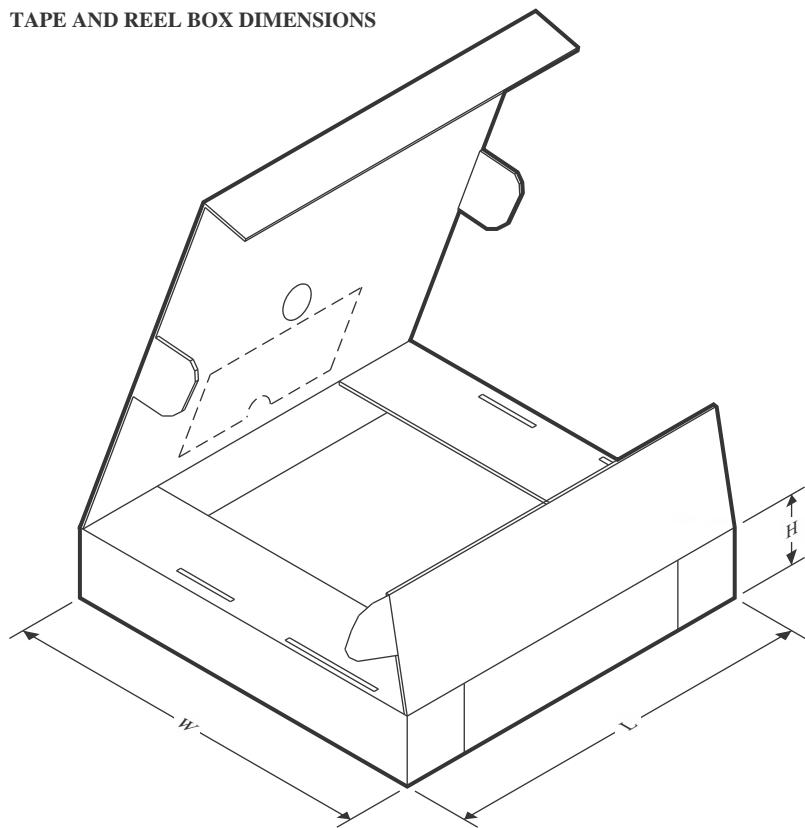
TAPE AND REEL INFORMATION


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


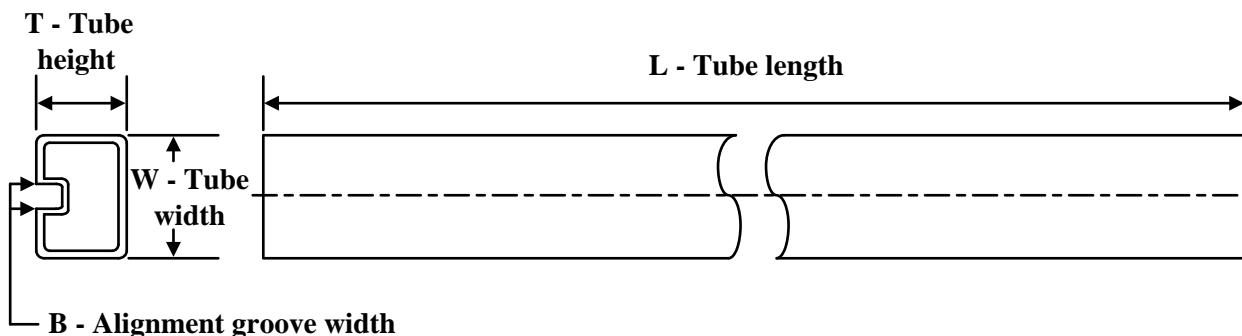
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC03DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC03DR1G4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC03NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HC03PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC03PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC03DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC03DR1G4 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC03NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC03PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC03PWRG4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

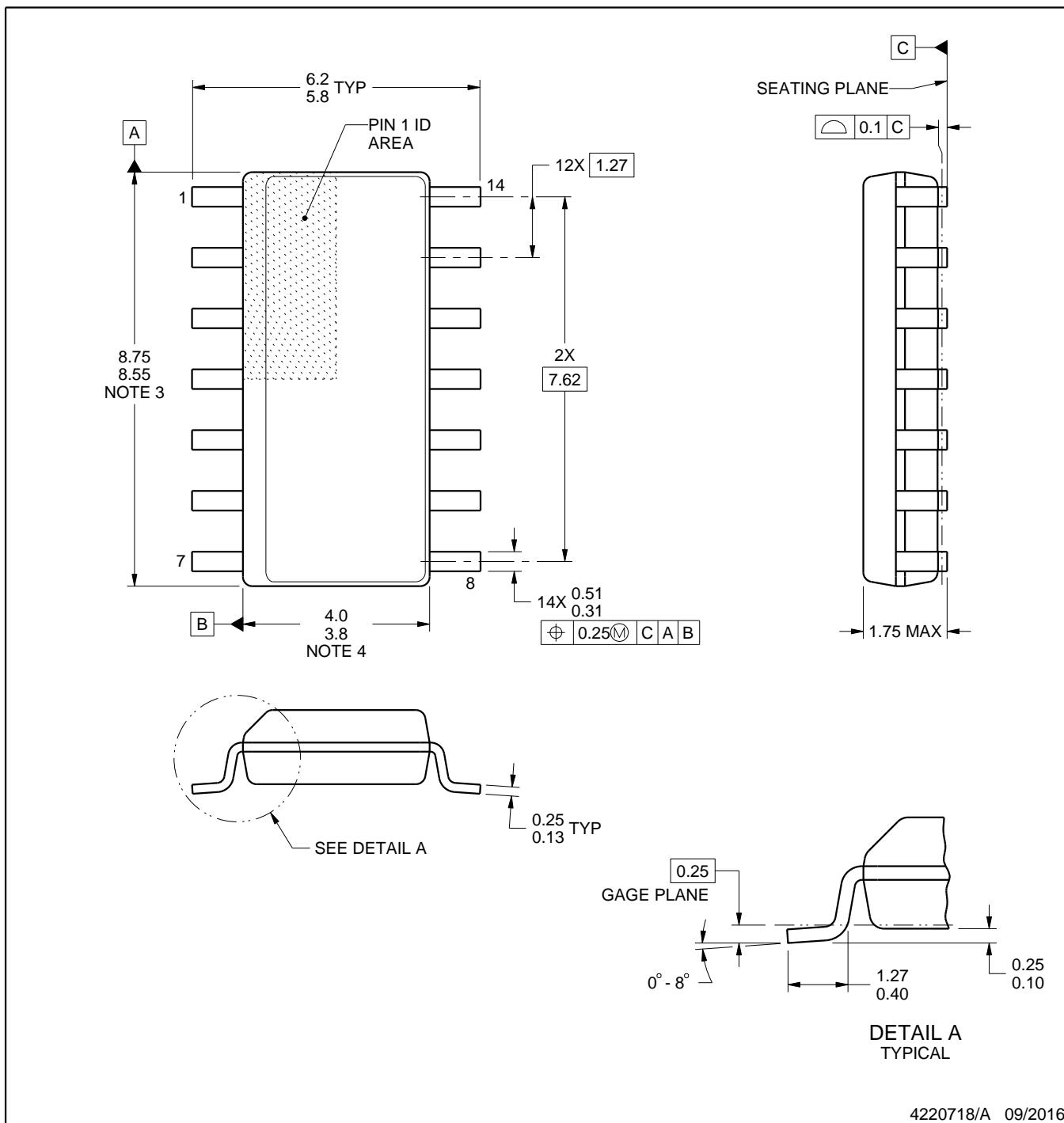
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μ m) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| 5962-87647012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74HC03N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC03N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC03NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC03FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC03FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

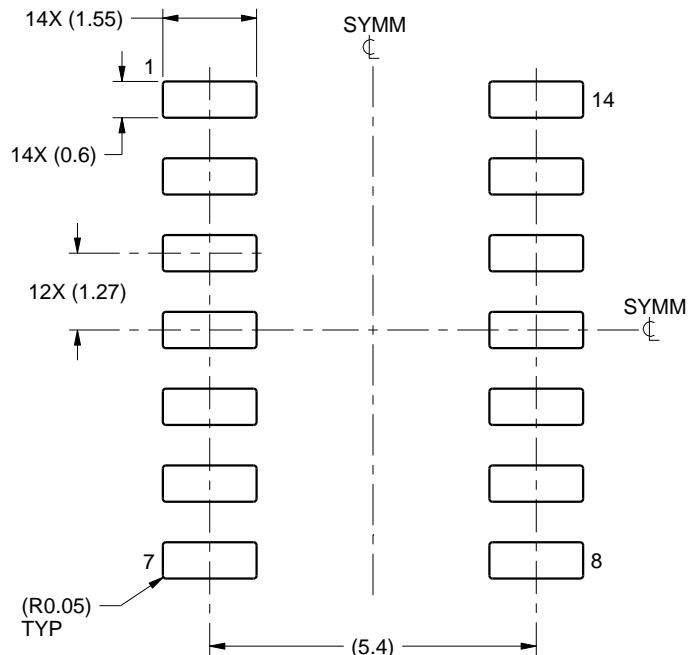
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

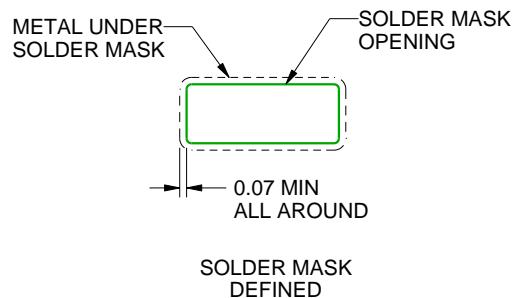
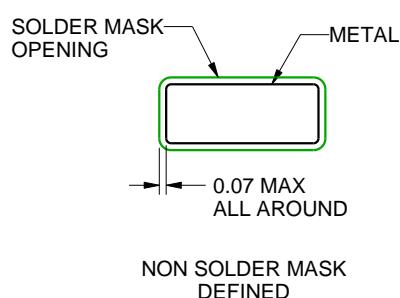
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

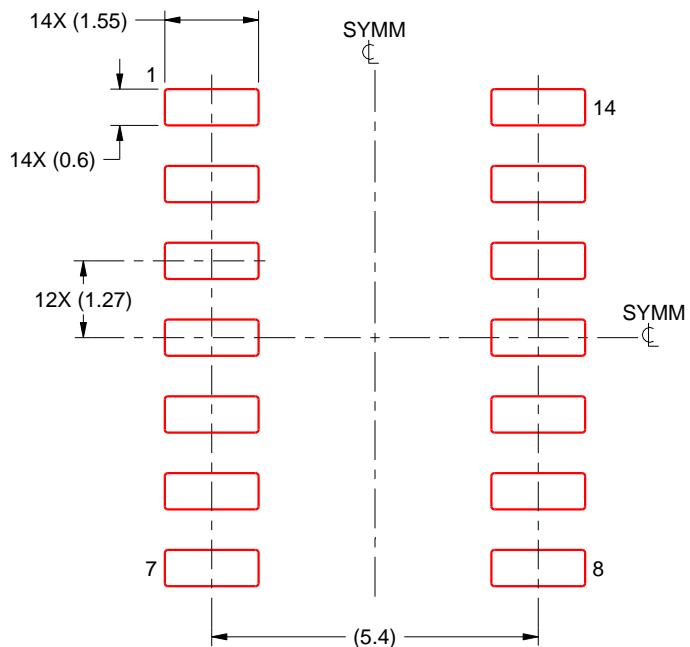
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

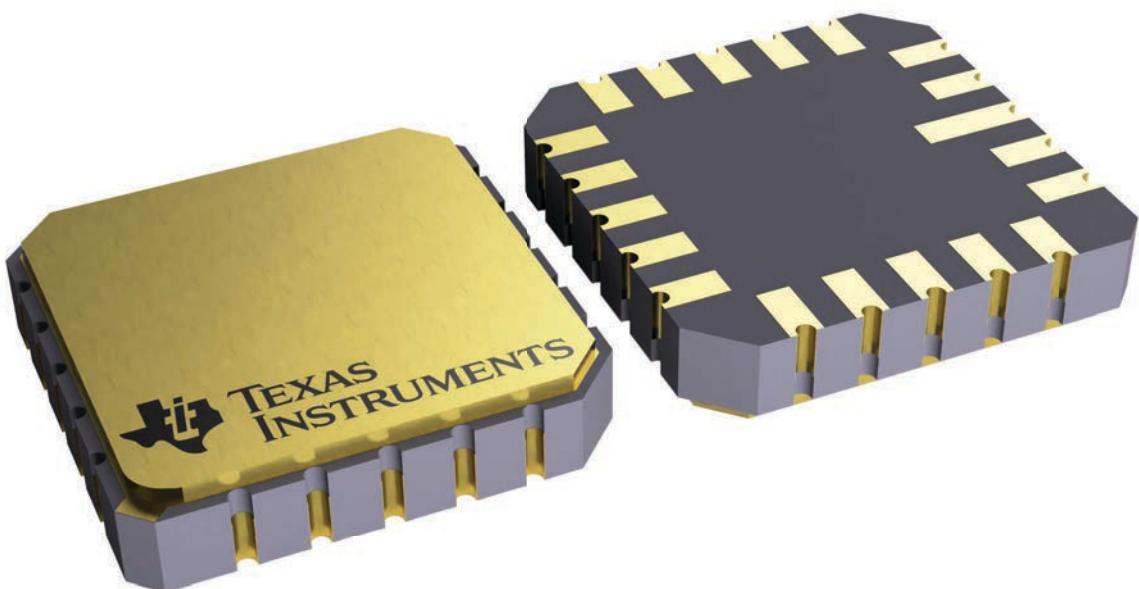
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



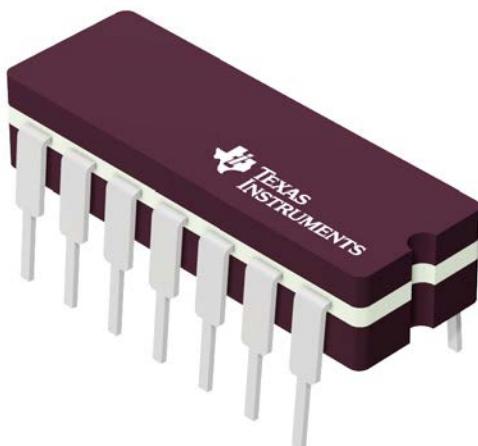
4229370VA\

GENERIC PACKAGE VIEW

J 14

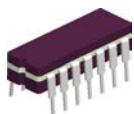
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

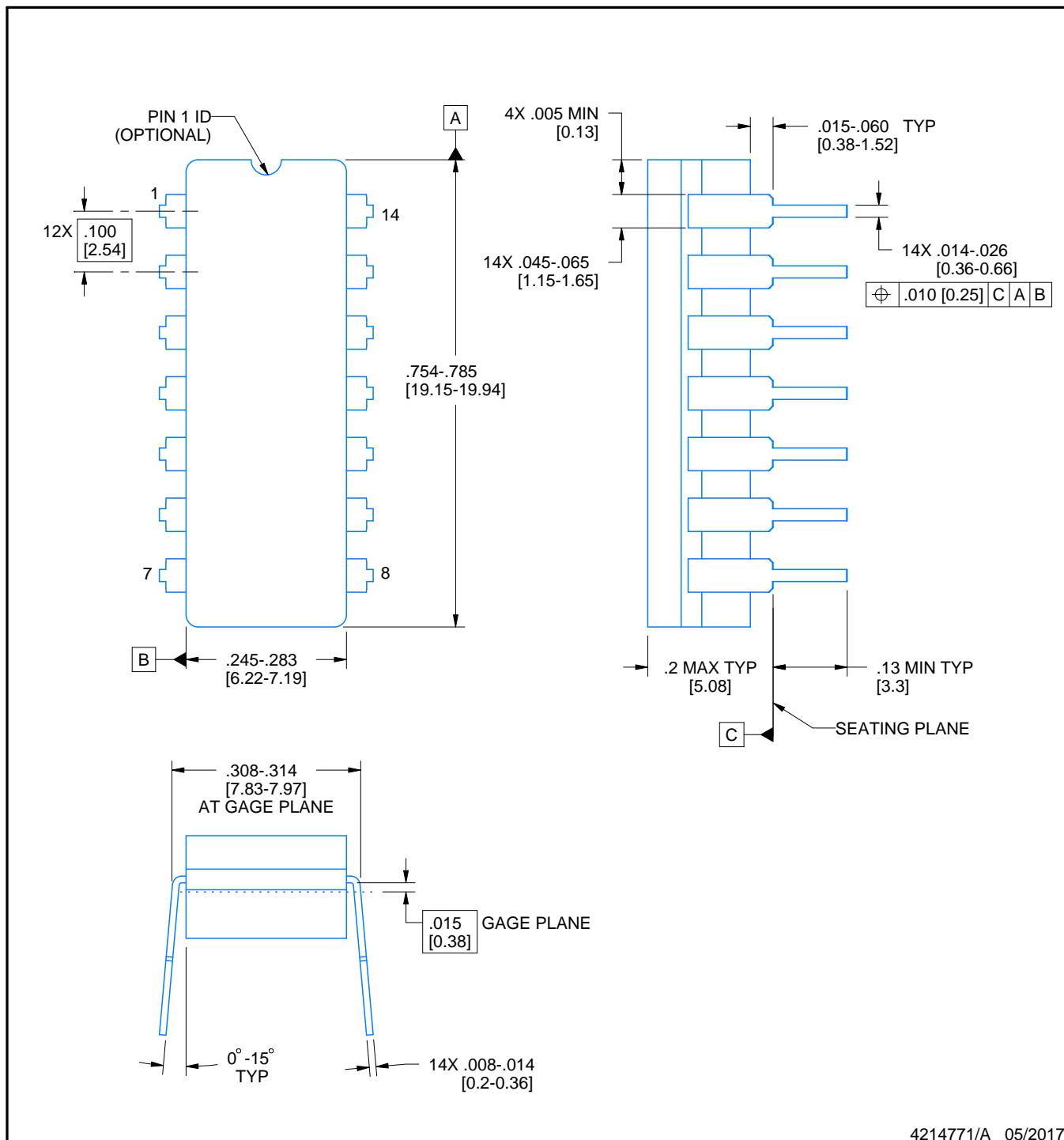


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

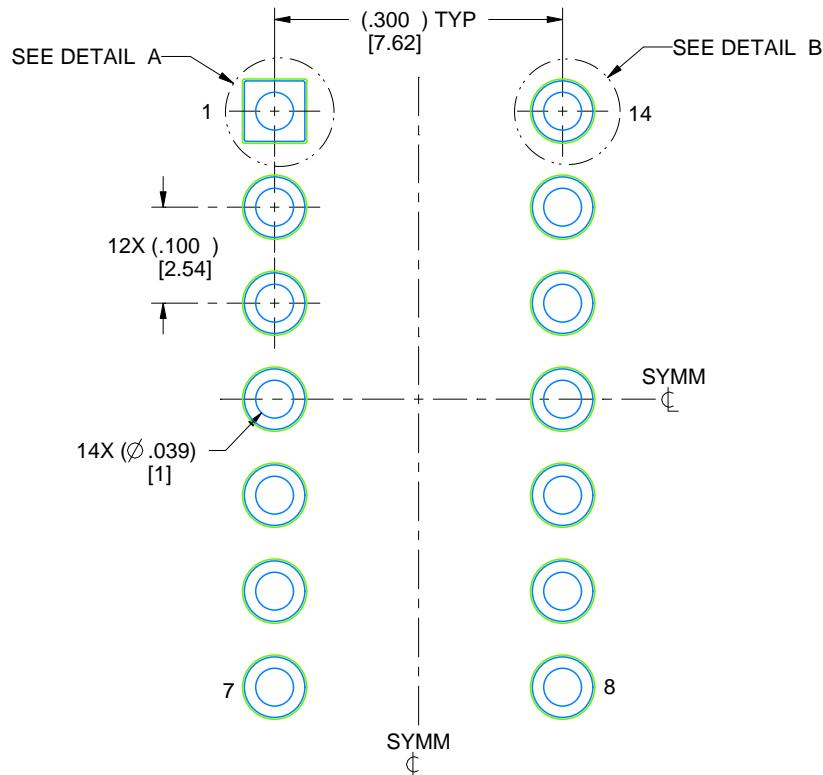
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

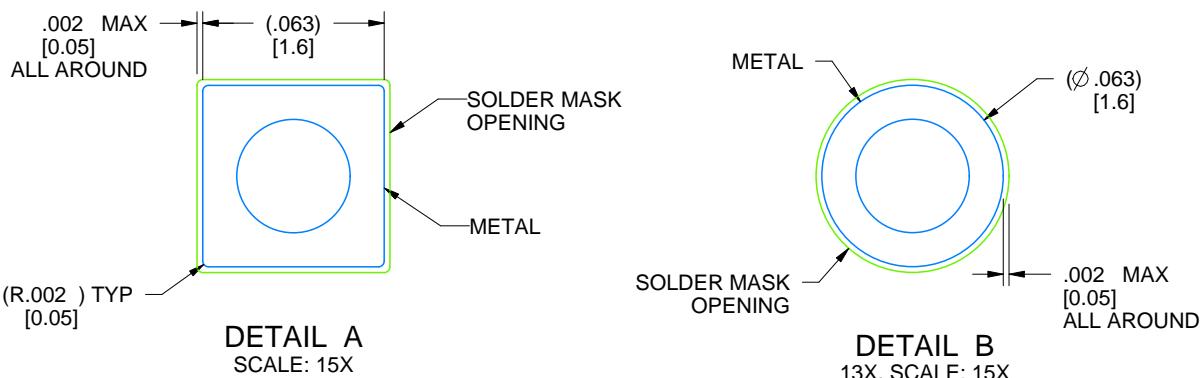
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

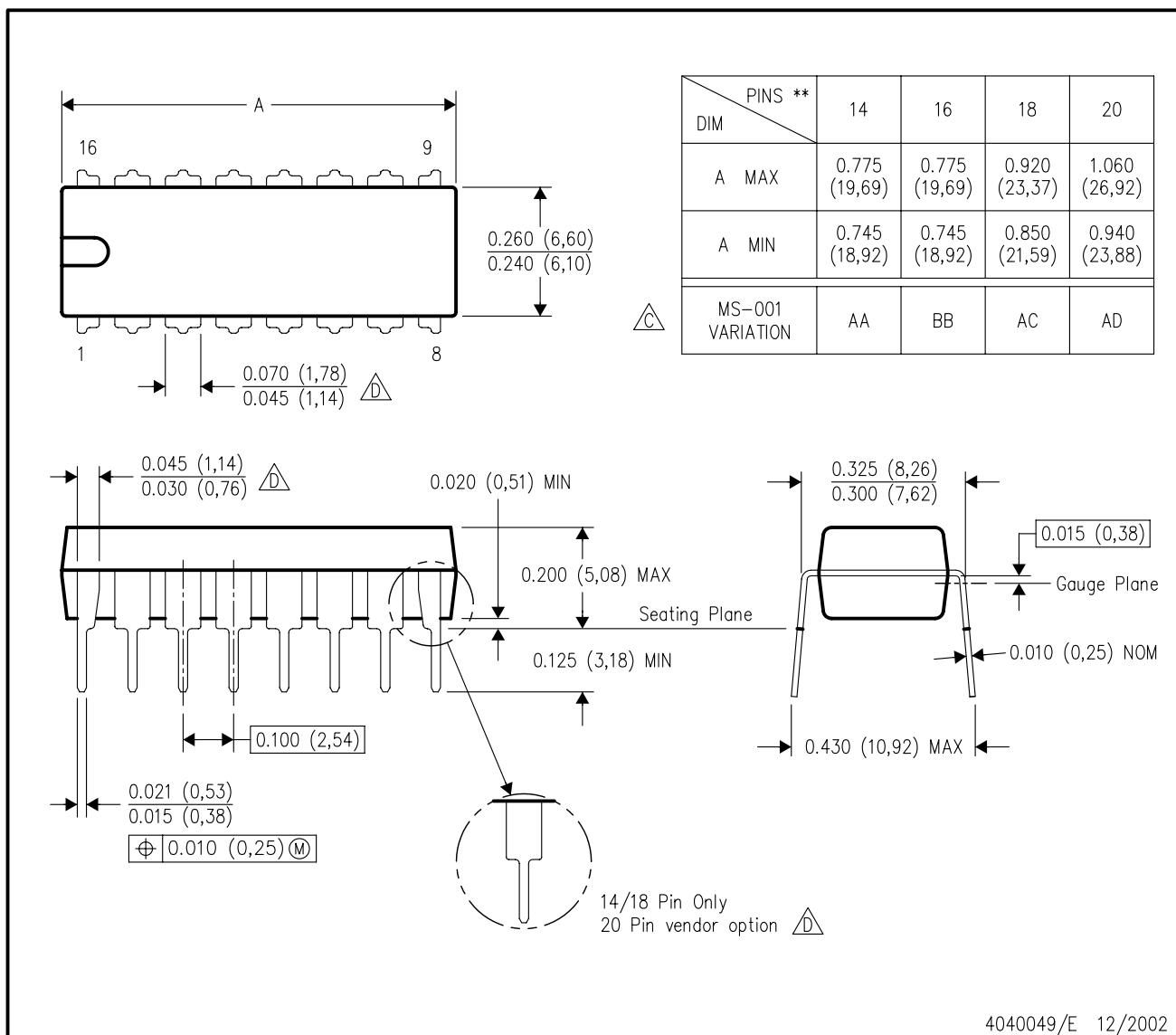


4214771/A 05/2017

N (R-PDIP-T**)

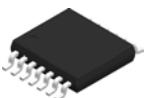
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



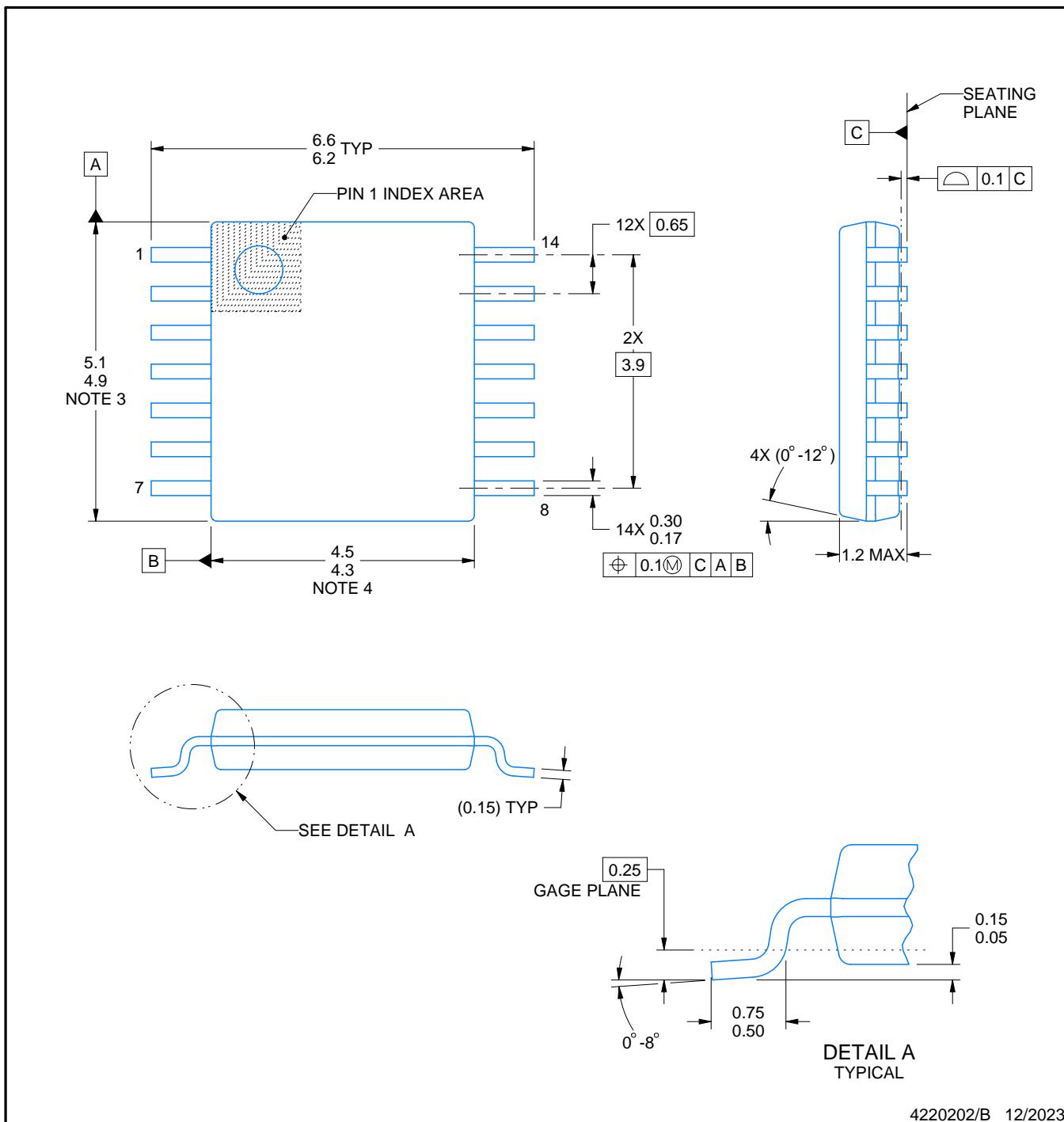
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

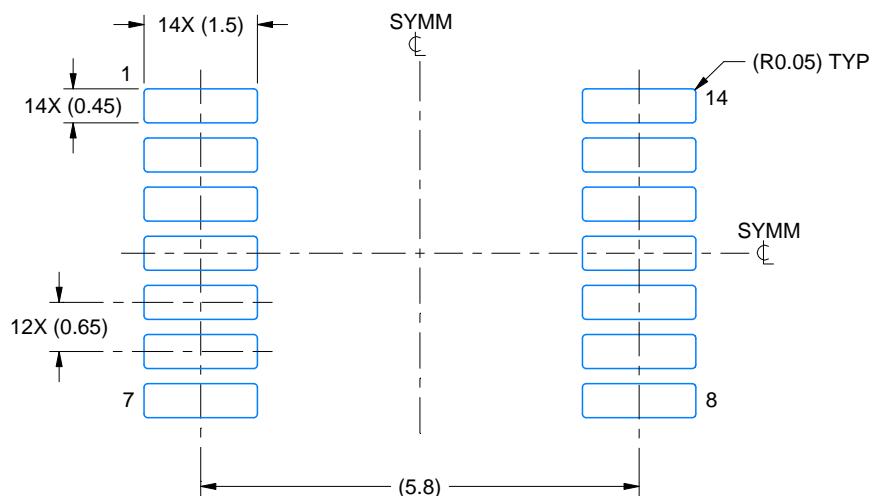
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

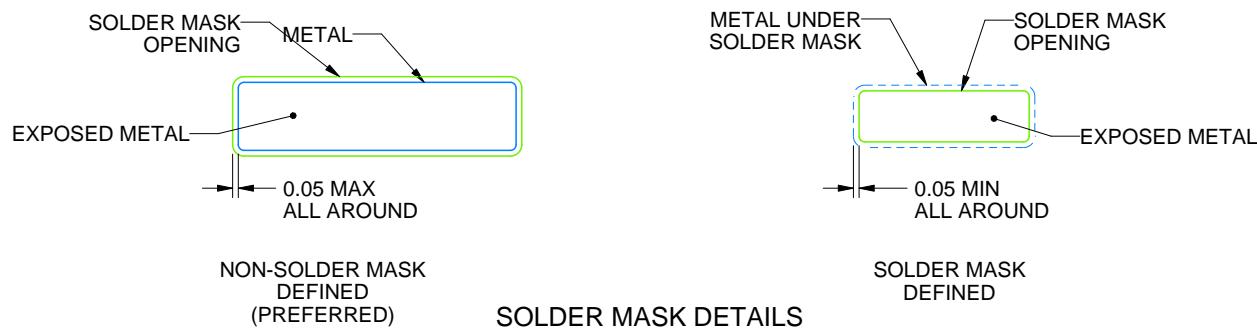
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

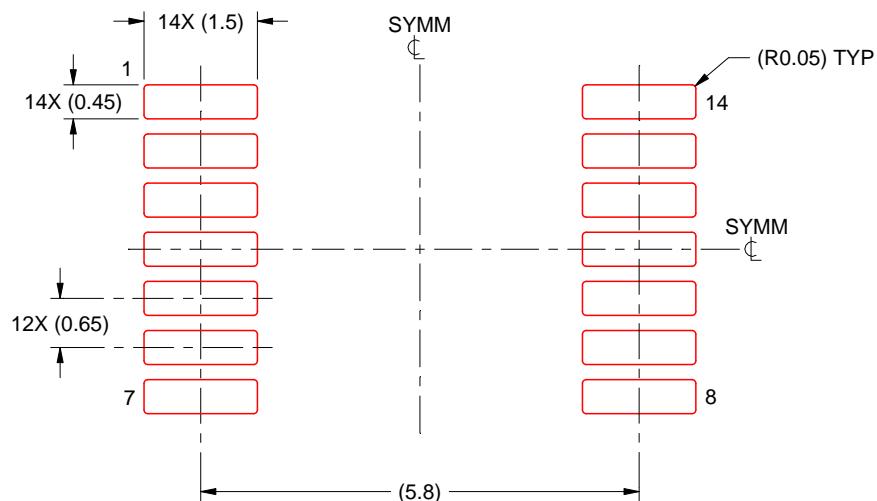
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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