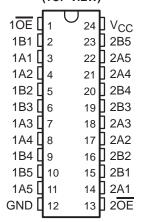
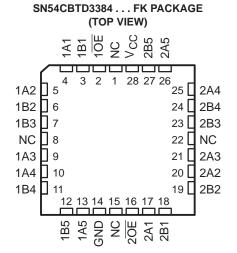
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

SN54CBTD3384 . . . JT OR W PACKAGE SN74CBTD3384 . . . DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



Designed to Be Used in Level-Shifting Applications



NC - No internal connection

description/ordering information

The 'CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

These devices are organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

TA	PACKAGI	<u>≡</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	COIC DW	Tube	SN74CBTD3384DW	CDTD2204
	SOIC - DW	Tape and reel	SN74CBTD3384DWR	CBTD3384
	SSOP – DB	Tape and reel	SN74CBTD3384DBR	CC384
-40°C to 85°C	SSOP (QSOP) – DBQ Tape and		SN74CBTD3384DBQR	CBTD3384
	T000D DW	Tube	SN74CBTD3384PW	00004
	TSSOP – PW	Tape and reel	SN74CBTD3384PWR	CC384
	TVSOP – DGV	Tape and reel	SN74CBTD3384DGVR	CC384
	CDIP – JT	Tube	SNJ54CBTD3384JT	SNJ54CBTD3384JT
-55°C to 125°C	CFP – W	Tube	SNJ54CBTD3384W	SNJ54CBTD3384W
	LCCC - FK	Tube	SNJ54CBTD3384FK	SNJ54CBTD3384FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



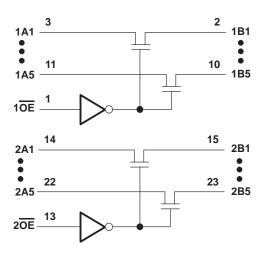
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FUNCTION TABLE (each 5-bit bus switch)

INP	UTS	INPUTS/OUTPUTS				
1OE	2OE	1B1-1B5	2B1-2B5			
L	L L 1A1–		2A1-2A5			
L	Н	1A1-1A5	Z			
Н	L	Z	2A1-2A5			
Н	Н	Z	Z			

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)	
Package thermal impedance, θ _{JA} (see Note 2): DB package	
DBQ package	61°C/W
DGV package	
DW package	46°C/W
PW package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 3)

		SN54CBT	SN54CBTD3384		SN74CBTD3384		
		MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V	
VIH	High-level control input voltage	2		2		V	
VIL	Low-level control input voltage		0.8		0.8	V	
TA	Operating free-air temperature	-55	125	-40	85	°C	

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER					SN5	4CBTD3	384	SN7	4CBTD3	384			
			TEST CONDITIONS				MAX	MIN	TYP†	MAX	UNIT		
٧ıK		$V_{CC} = 4.5 \text{ V},$	V _{CC} = 4.5 V, I _I = -18 mA				-1.2			-1.2	V		
Vон		See Figure 2	See Figure 2										
II		V _{CC} = 5.5 V,	/ _{CC} = 5.5 V, V _I = 5.5 V or GND				±1			±1	μА		
ICC		V _{CC} = 5.5 V,	$V_{CC} = 5.5 \text{ V}, I_{O} = 0, V_{I} = V_{CC} \text{ or GND}$				1.5			1.5	mA		
ΔI _{CC} ‡	Control inputs		CC = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				2.5			2.5	mA		
Ci	Control inputs	V _I = 3 V or 0				3			3		рF		
C _{io(OFI}	F)	$V_0 = 3 \text{ V or } 0,$	OE = VCC			3.5			3.5		pF		
			V 0	I _I = 64 mA		5			5	7			
ron§		$V_{CC} = 4.5 \text{ V}$ $V_{I} = 0$		I _I = 30 mA		5			5	7	Ω		
			V _I = 2.4 V,	I _I = 15 mA		35			35	50			

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	SN54CBT	D3384	SN74CBT	D3384	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
$t_{pd}\P$	A or B	B or A		0.25		0.25	ns
^t en	ŌE	A or B	2.2	9.7	2.3	7	ns
^t dis	ŌE	A or B	1.5	8.6	1.7	5.3	ns

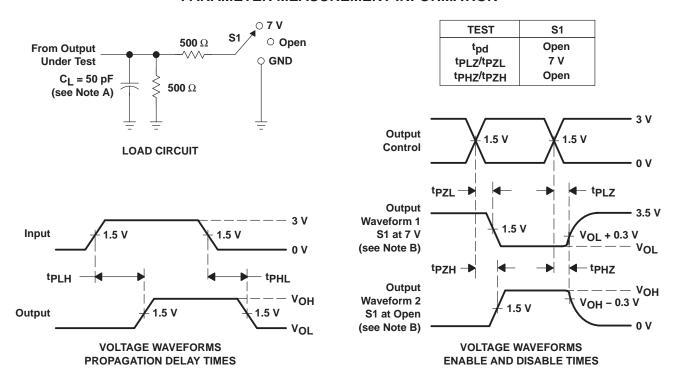
The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



[‡]This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



OUTPUT VOLTAGE HIGH

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH SUPPLY VOLTAGE T_A = 85°C 3.75 **100** μ**A** 3.5 6 mA V_{OH} - Output Voltage High - V 12 mA 3.25 24 mA 3 2.75 2.5 2.25 2 1.75 1.5 5.25 4.5 4.75 5 5.5 5.75 V_{CC} - Supply Voltage - V

SUPPLY VOLTAGE $T_A = 25^{\circ}C$ 3.75 100 μ A 3.5 V_{OH} - Output Voltage High - V 6 mA 3.25 12 mA 24 mA 3 2.75 2.5 2.25 2 1.75 1.5 L 4.5 4.75 5.5 5.25 5.75 V_{CC} - Supply Voltage - V

OUTPUT VOLTAGE HIGH SUPPLY VOLTAGE $T_A = 0^{\circ}C$ 3.75 3.5 **100** μ**A** V_{OH} - Output Voltage High - V 3.25 6 mA 12 mA 3 24 mA 2.75 2.5 2.25 2 1.75 1.5 4.5 4.75 5.25 5.5 5.75 V_{CC} - Supply Voltage - V

Figure 2. V_{OH} Values

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9752701Q3A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9752701Q3A SNJ54CBTD 3384FK
SN74CBTD3384DBQR	Obsolete	Production	SSOP (DBQ) 24	-	-	Call TI	Call TI	-40 to 85	CBTD3384
SN74CBTD3384DBR	NRND	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384
SN74CBTD3384DBR.A	NRND	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384
SN74CBTD3384DGVR	Obsolete	Production	TVSOP (DGV) 24	-	-	Call TI	Call TI	-40 to 85	CC384
SN74CBTD3384DW	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-40 to 85	CBTD3384
SN74CBTD3384DWR	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-40 to 85	CBTD3384
SN74CBTD3384PW	Obsolete	Production	TSSOP (PW) 24	-	-	Call TI	Call TI	-40 to 85	CC384
SNJ54CBTD3384FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9752701Q3A SNJ54CBTD 3384FK
SNJ54CBTD3384FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9752701Q3A SNJ54CBTD 3384FK

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54CBTD3384, SN74CBTD3384:

Catalog: SN74CBTD3384

Military: SN54CBTD3384

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTD3384DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	SN74CBTD3384DBR	SSOP	DB	24	2000	353.0	353.0	32.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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