# SNx4AHC374 Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

## 1 Features

- Operating range 2V to 5.5V $V_{CC}$
- 3-state outputs drive bus lines directly
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.
- ESD protection exceeds JESD 22
  - 2000V human-body model
  - 200V machine model
  - 1500V charged-device model

## 2 Applications

- Printers
- Network Switches
- Tests and Measurements
- Wireless Infrastructure
- Motor Controls
- Server Motherboards

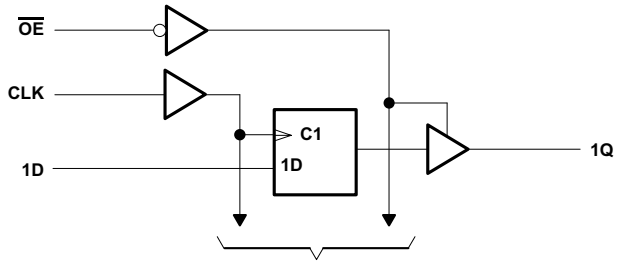
## 3 Description

The SNx4AHC374 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SNx4AHC374 | DB (SSOP, 20) | 7.2mm × 7.8mm | 7.2mm x 5.30mm |
| | DGV (TVSOP, 20) | 5.00mm x 6.4mm | 5.00mm x 4.40mm |
| | DW (SOIC, 20) | 12.80mm × 10.3mm | 12.8mm x 7.5mm |
| | N (PDIP, 20) | 24.33mm x 9.4mm | 24.33mm x 6.35mm |
| | PW (TSSOP, 20) | 6.50mm × 6.4mm | 6.50mm × 4.40mm |
| | J (CDIP, 20) | 24.2mm x 7.62mm | 24.2mm x 6.92mm |
| | W (CFP, 20) | 13.09mm x 8.13mm | 13.09mm x 6.92mm |
| | FK (LCCC, 20) | 8.89mm x 8.89mm | 8.89mm x 8.89mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Simplified Schematic**

# Table of Contents

## 4 Pin Configuration and Functions

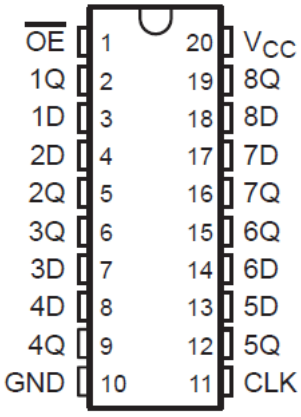



**Figure 4-1. SN54AHC374 J or W Package; SN74AHC374 DB, DGV, DW, N, or PW ; 20-Pin CDIP, CFP, SSOP, TVSOP, SOIC, PDIP, or TSSOP**

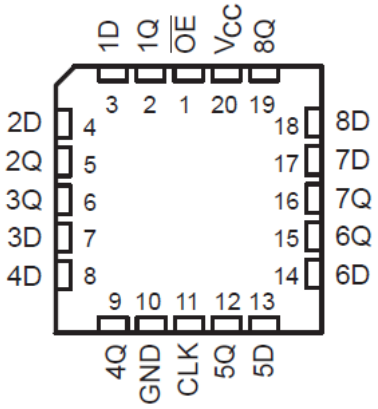



**Figure 4-2. SN54AHC374 FK Package, 20-Pin LCCC**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE}$ | I | Output Enable |
| 2 | 1Q | O | 1Q Output |
| 3 | 1D | I | 1D Input |
| 4 | 2D | I | 2D Input |
| 5 | 2Q | O | 2Q Output |
| 6 | 3Q | O | 3Q Output |
| 7 | 3D | I | 3D Input |
| 8 | 4D | I | 4D Input |
| 9 | 4Q | O | 4Q Output |
| 10 | GND | — | Ground |
| 11 | CLK | I | Clock Pin |
| 12 | 5Q | O | 5Q Output |
| 13 | 5D | I | 5D Input |
| 14 | 6D | I | 6D Input |
| 15 | 6Q | O | 6Q Output |
| 16 | 7Q | O | 7Q Output |
| 17 | 7D | I | 7D Input |
| 18 | 8D | I | 8D Input |
| 19 | 8Q | O | 8Q Output |
| 20 | $V_{CC}$ | — | Power Pin |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 1500 | |
| | | Machine Model (MM) | 200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 5.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 5.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 5.5 V | | 20 | | 20 | |

## 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AHC374 | | SN74AHC374 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC374 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DB | DGV | DW | N | NS | PW | |
| | | 20 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97.9 | 117.2 | 79.4 | 53.3 | 79.2 | 116.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 59.6 | 32.7 | 45.7 | 40.0 | 45.7 | 58.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.1 | 58.7 | 46.9 | 34.2 | 46.8 | 78.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.3 | 1.15 | 18.7 | 26.4 | 19.3 | 12.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.7 | 58.0 | 46.5 | 34.1 | 46.4 | 77.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC374 | | SN74AHC374 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = −4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = −8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1(1) | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_I = V_{IH}$ or $V_{IL}$<br>$V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | | ±2.5 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | | 40 | µA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 6 | | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.

## 5.6 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | | $T_A$ = 25°C | | SN54AHC374 | | SN74AHC374 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5.5 | | 5.5 | | 6.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 4.5 | | 4 | | 4 | | 4.5 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | 2.5 | | ns |

## 5.7 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | | $T_A$ = 25°C | | SN54AHC374 | | SN74AHC374 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 3 | | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 2 | | 2 | | 2 | | 2 | | ns |

## 5.8 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC374 | | SN74AHC374 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{MAX}$ | | | $C_L$ = 15 pF | 80[1] | 130[1] | | 70[1] | | 70 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 85 | | 50 | | 50 | | 50 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.1[1] | 12.7[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 8.1[1] | 12.7[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.1[1] | 11[1] | 1[1] | 13[1] | 1 | 13 | 1 | 14 | ns |
| $t_{PZL}$ | | | | | 7.1[1] | 11[1] | 1[1] | 13[1] | 1 | 13 | 1 | 14 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.5[1] | 10.5[1] | 1[1] | 12.5[1] | 1 | 12.5 | 1 | 13.5 | ns |
| $t_{PLZ}$ | | | | | 7.5[1] | 10.5[1] | 1[1] | 12.5[1] | 1 | 12.5 | 1 | 13.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 10.6 | 16.2 | 1 | 18.5 | 1 | 18.5 | 1 | 20 | ns |
| $t_{PHL}$ | | | | | 10.6 | 16.2 | 1 | 18.5 | 1 | 18.5 | 1 | 20 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.6 | 14.5 | 1 | 16.5 | 1 | 16.5 | 1 | 17.5 | ns |
| $t_{PZL}$ | | | | | 9.6 | 14.5 | 1 | 16.5 | 1 | 16.5 | 1 | 17.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.2 | 14 | 1 | 16 | 1 | 16 | 1 | 17 | ns |
| $t_{PLZ}$ | | | | | 10.2 | 14 | 1 | 16 | 1 | 16 | 1 | 17 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5[2] | | | | 1.5 | | 1.5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.9 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC374 | | SN74AHC374 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{MAX}$ | | | $C_L$ = 15 pF | 130[1] | 185[1] | | 110[1] | | 110 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 120 | | 75 | | 75 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.4[1] | 8.1[1] | 1[1] | 9.5[1] | 1 | 9.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.4[1] | 8.1[1] | 1[1] | 9.5[1] | 1 | 9.5 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.1[1] | 7.6[1] | 1[1] | 9[1] | 1 | 9 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.1[1] | 7.6[1] | 1[1] | 9[1] | 1 | 9 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.6[1] | 6.8[1] | 1[1] | 8[1] | 1 | 8 | 1 | 9 | ns |
| $t_{PLZ}$ | | | | | 4.6[1] | 6.8[1] | 1[1] | 8[1] | 1 | 8 | 1 | 9 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 6.9 | 10.1 | 1 | 11.5 | 1 | 11.5 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 6.9 | 10.1 | 1 | 11.5 | 1 | 11.5 | 1 | 12.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.6 | 9.6 | 1 | 11 | 1 | 11 | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 6.6 | 9.6 | 1 | 11 | 1 | 11 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | 1 | 11 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1[2] | | | | 1 | | 1.5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.10 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C[1]

| PARAMETER | | SN74AHC374 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 1 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.5 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

(1) Characteristics are for surface-mount packages only.

## 5.11 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 32 | pF |

## 5.12 Typical Characteristics

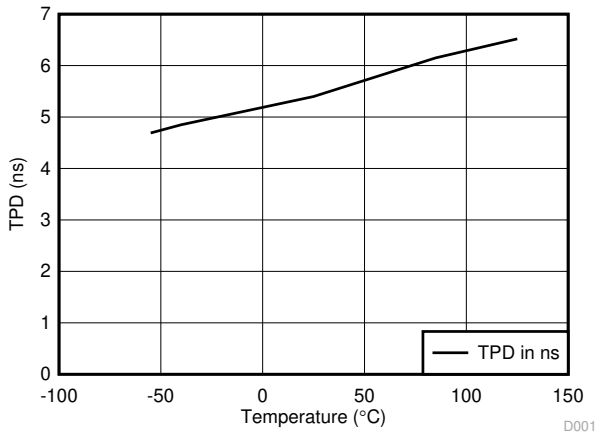



**Figure 5-1. TPD vs Temperature**

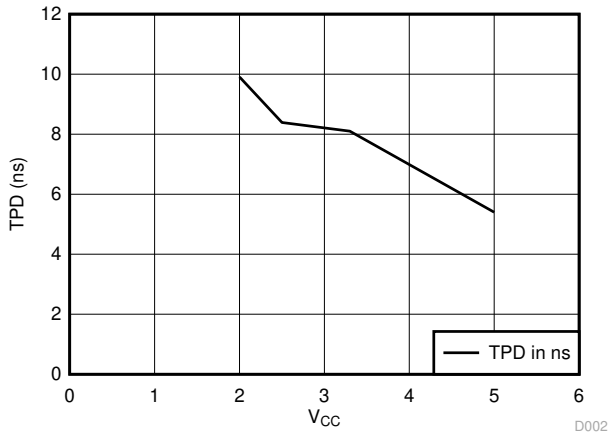
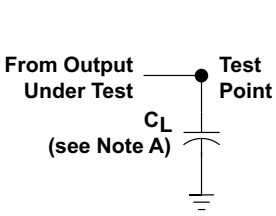
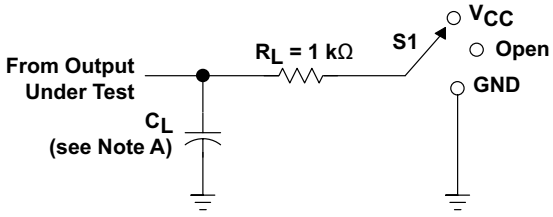



**Figure 5-2. TPD vs $V_{CC}$ at 25°C**

## 6 Parameter Measurement Information

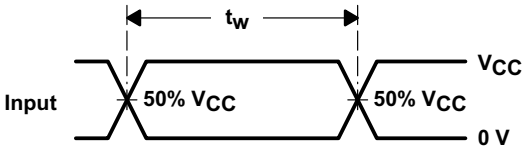



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

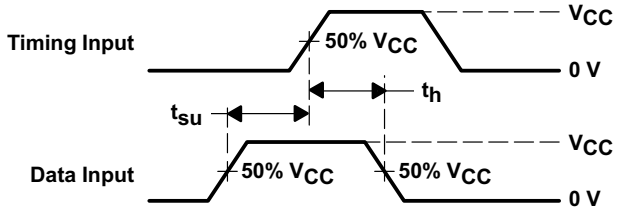



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

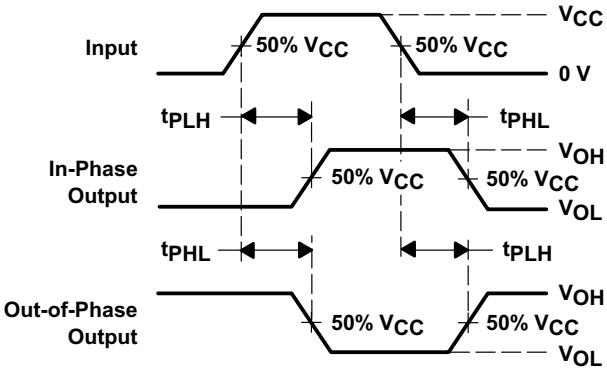
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



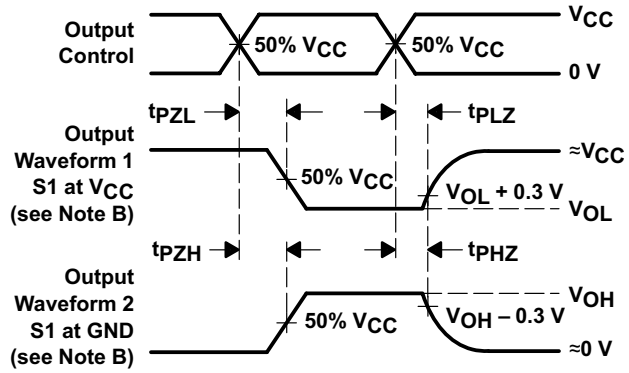

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

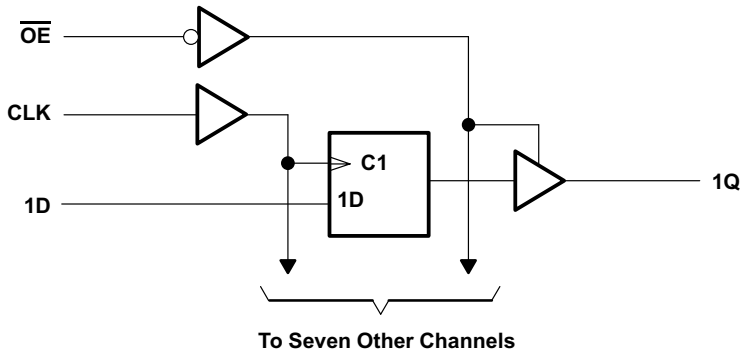
## 7.1 Overview

The SNx4AHC374 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing

## 7.4 Device Functional Modes

**Table 7-1. Function Table (Each Flip-Flop)**

| INPUTS | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

SNx4AHC374 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where putput ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid $V_{CC}$. This feature makes it Ideal for translating down to the $V_{CC}$ level. Figure 8-2 shows the reduction in ringing compared to higher drive parts such as AC.

## 8.2 Typical Application

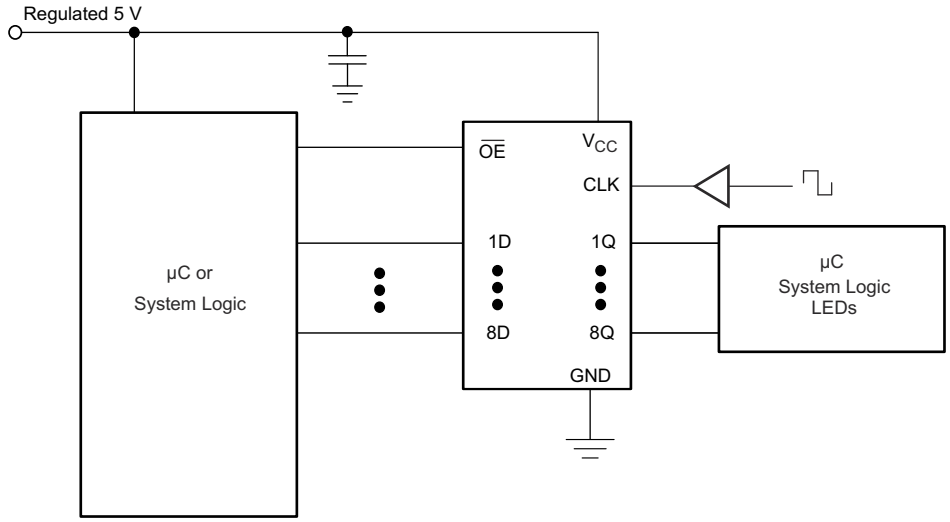



**Figure 8-1. Typical Application Schematic**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Section 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *Section 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 8.2.3 Application Curves

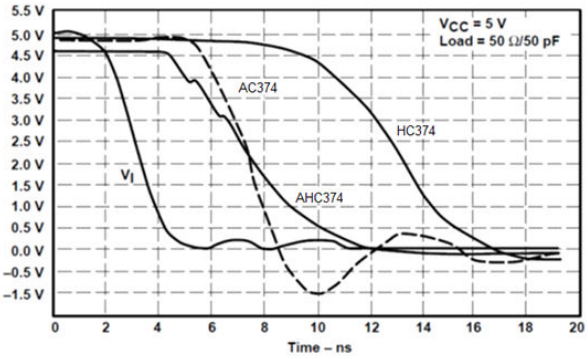



**Figure 8-2. Switching Characteristics Comparison**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

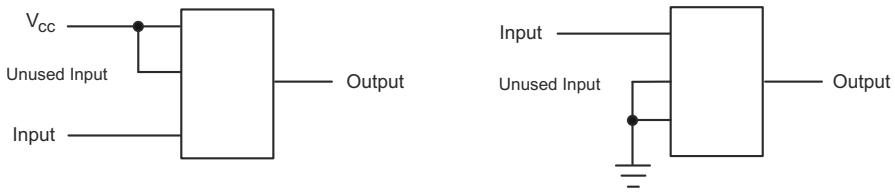



**Figure 8-3. Layout Diagram**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Links*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHC374 | Click here | Click here | Click here | Click here | Click here |
| SN74AHC374 | Click here | Click here | Click here | Click here | Click here |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

**Changes from Revision J (December 2014) to Revision K (July 2024)** — **Page**

- Added package size and military packages to *Device information* table.....1
- Updated thermal values for PW package from RθJA = 103.3 to 116.8, RθJC(top) = 37.8 to 58.5, RθJB = 54.3 to 78.7, ΨJT = 2.9 to 12.6, ΨJB =53.8 to 77.9, RθJC(bot) = N/A, all values in °C/W .....5

**Changes from Revision I (July 2003) to Revision J (December 2014)** — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.....1

- Deleted *Ordering Information* table.... 1
- Added Military Disclaimer to *Features* list.... 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. ....4

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9686401Q2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401Q2A SNJ54AHC374FK |
| 5962-9686401QRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QRA SNJ54AHC374J |
| 5962-9686401QSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QSA SNJ54AHC374W |
| SN74AHC374DBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA374 |
| SN74AHC374DBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA374 |
| SN74AHC374DGSR | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SN74AHC374DW | Obsolete | Production | SOIC (DW) \| 20 | - | - | Call TI | Call TI | -40 to 125 | AHC374 |
| SN74AHC374DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SN74AHC374DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SN74AHC374N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC374N |
| SN74AHC374N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC374N |
| SN74AHC374NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SN74AHC374NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SN74AHC374PW | Obsolete | Production | TSSOP (PW) \| 20 | - | - | Call TI | Call TI | -40 to 125 | HA374 |
| SN74AHC374PWR | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU \| NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA374 |
| SN74AHC374PWR.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA374 |
| SN74AHC374PWRG4 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA374 |
| SN74AHC374RKSR | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC374 |
| SNJ54AHC374FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401Q2A SNJ54AHC374FK |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54AHC374FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401Q2A SNJ54AHC 374FK |
| SNJ54AHC374J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QR A SNJ54AHC374J |
| SNJ54AHC374J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QR A SNJ54AHC374J |
| SNJ54AHC374W | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QS A SNJ54AHC374W |
| SNJ54AHC374W.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9686401QS A SNJ54AHC374W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN54AHC374, SN74AHC374 :**

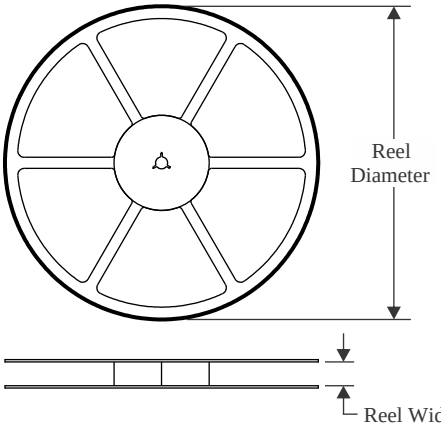
- Catalog : SN74AHC374
- Automotive : SN74AHC374-Q1, SN74AHC374-Q1
- Military : SN54AHC374

NOTE: Qualified Version Definitions:

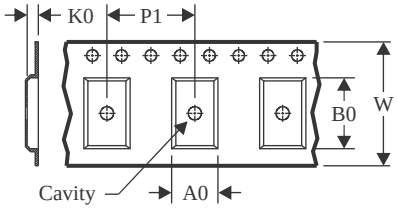
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

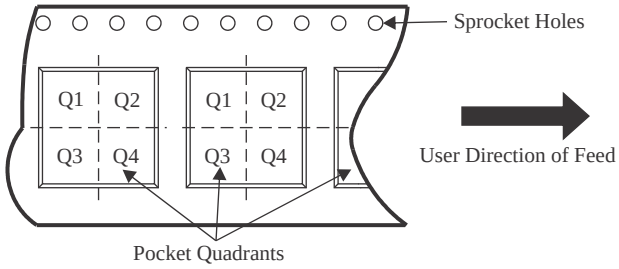



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

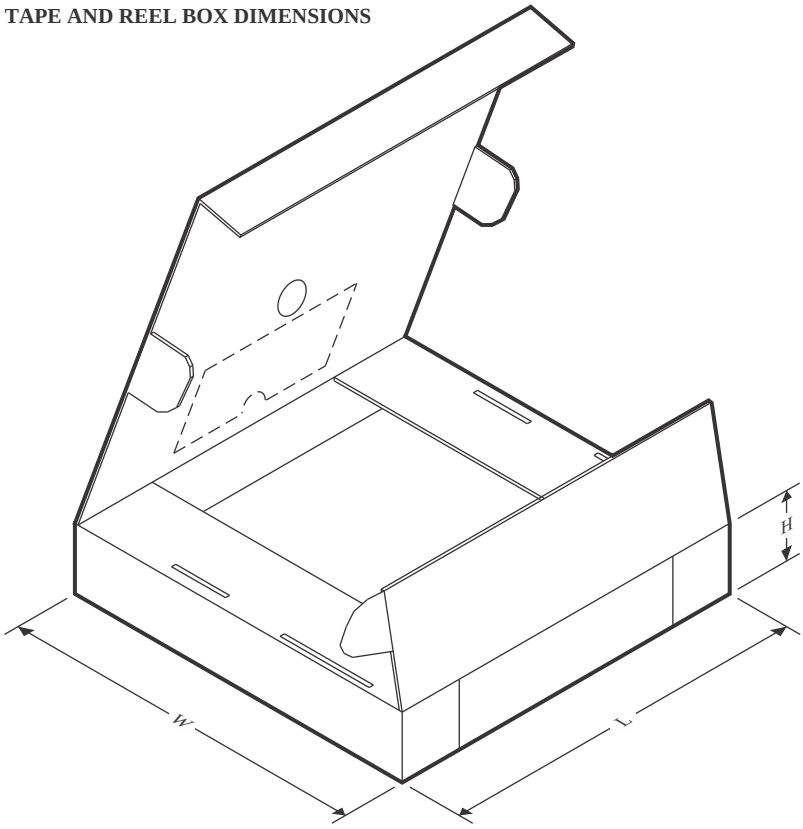
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC374DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC374DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74AHC374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC374NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC374PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC374RKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

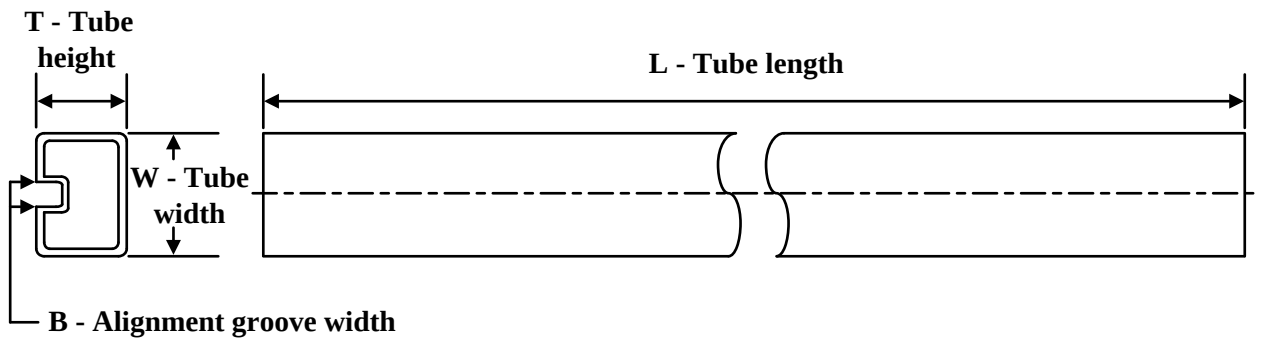
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC374DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC374DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74AHC374DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC374NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC374PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC374RKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

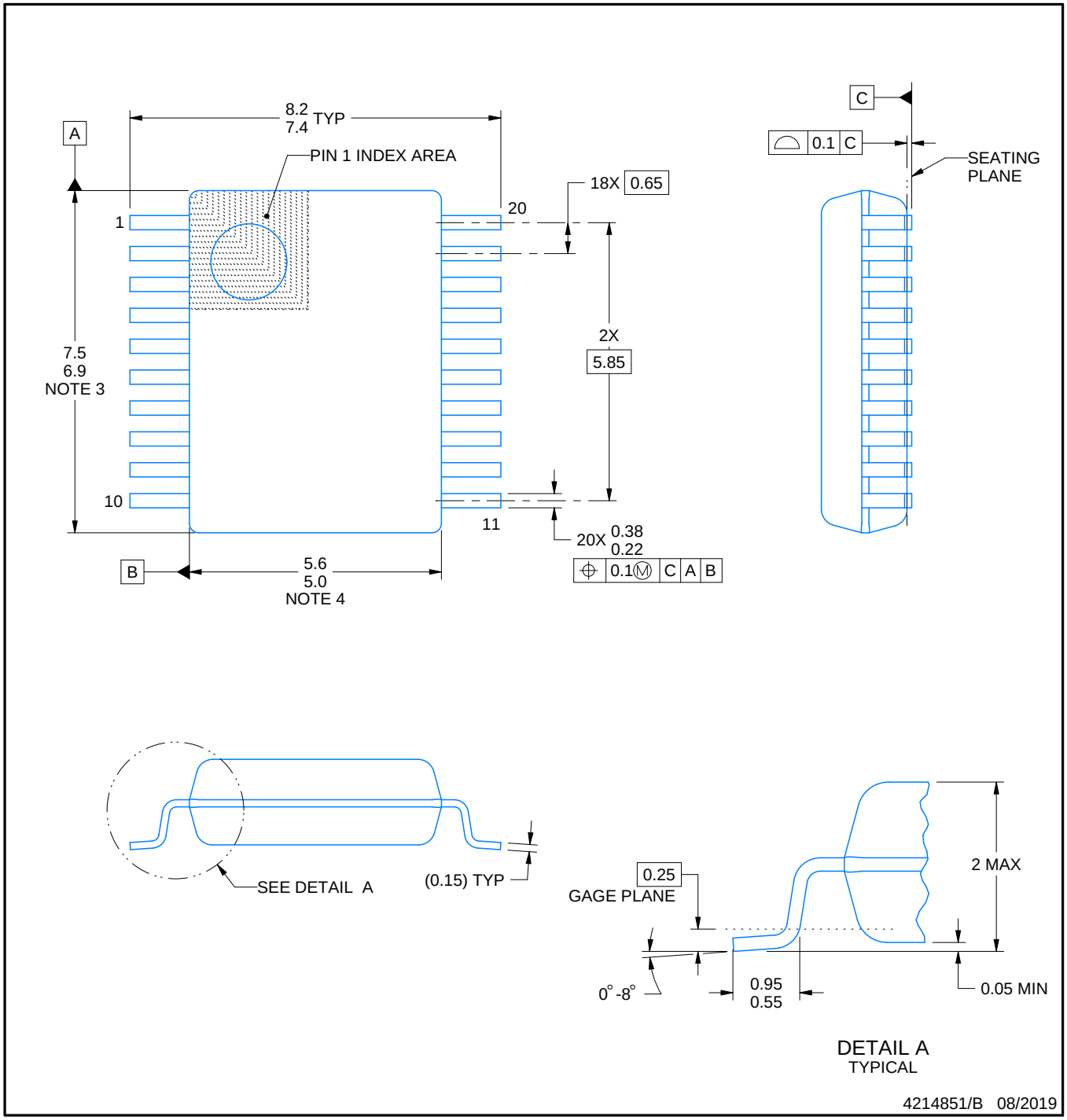
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9686401Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9686401QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC374N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC374N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC374FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC374FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC374W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AHC374W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

# PACKAGE OUTLINE

## DB0020A

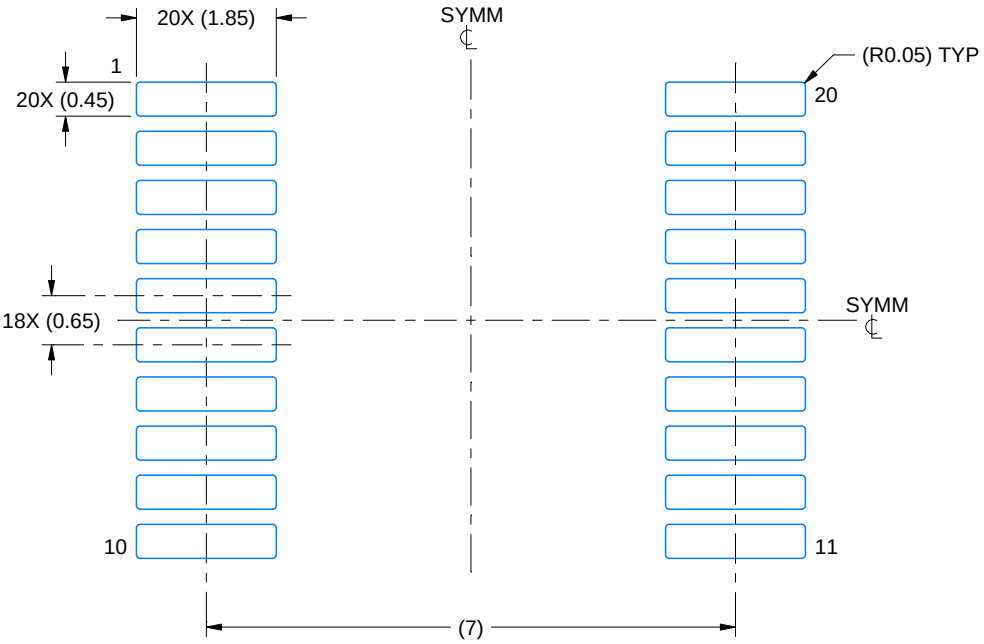
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

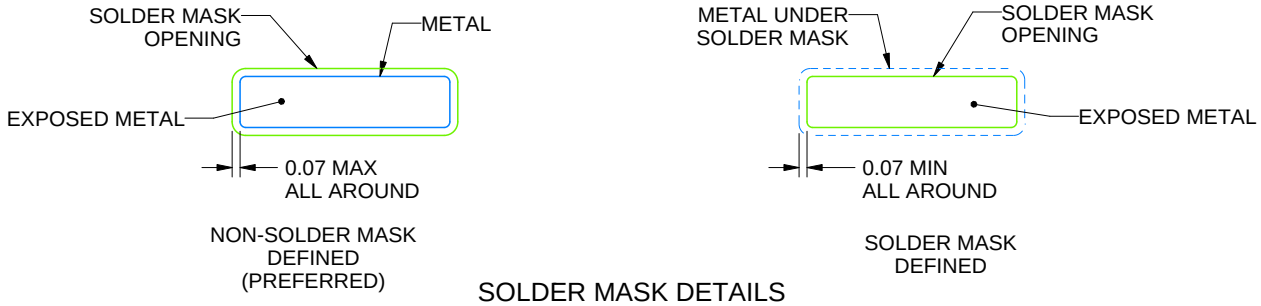



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

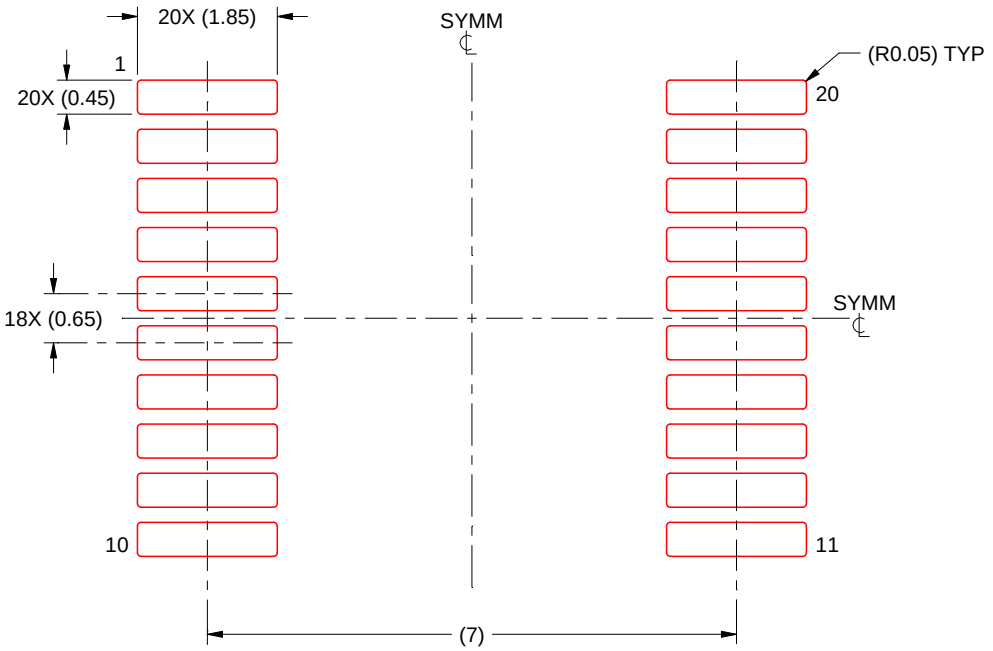
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

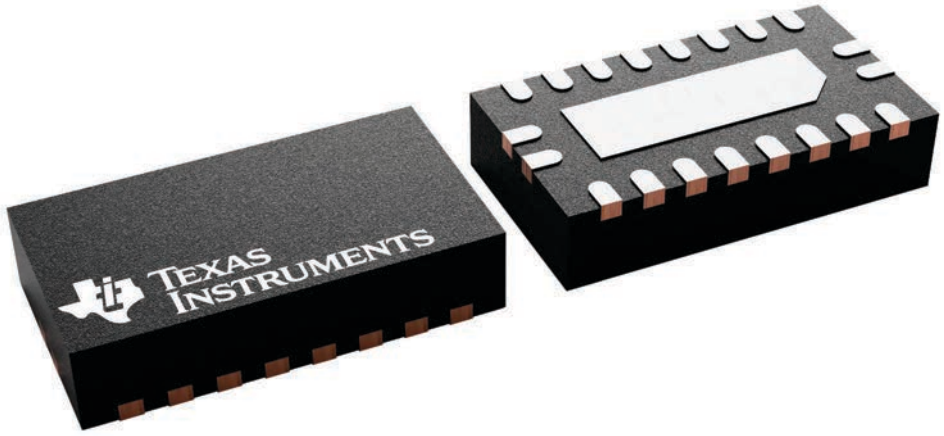
## RKS 20

## VQFN - 1 mm max height

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

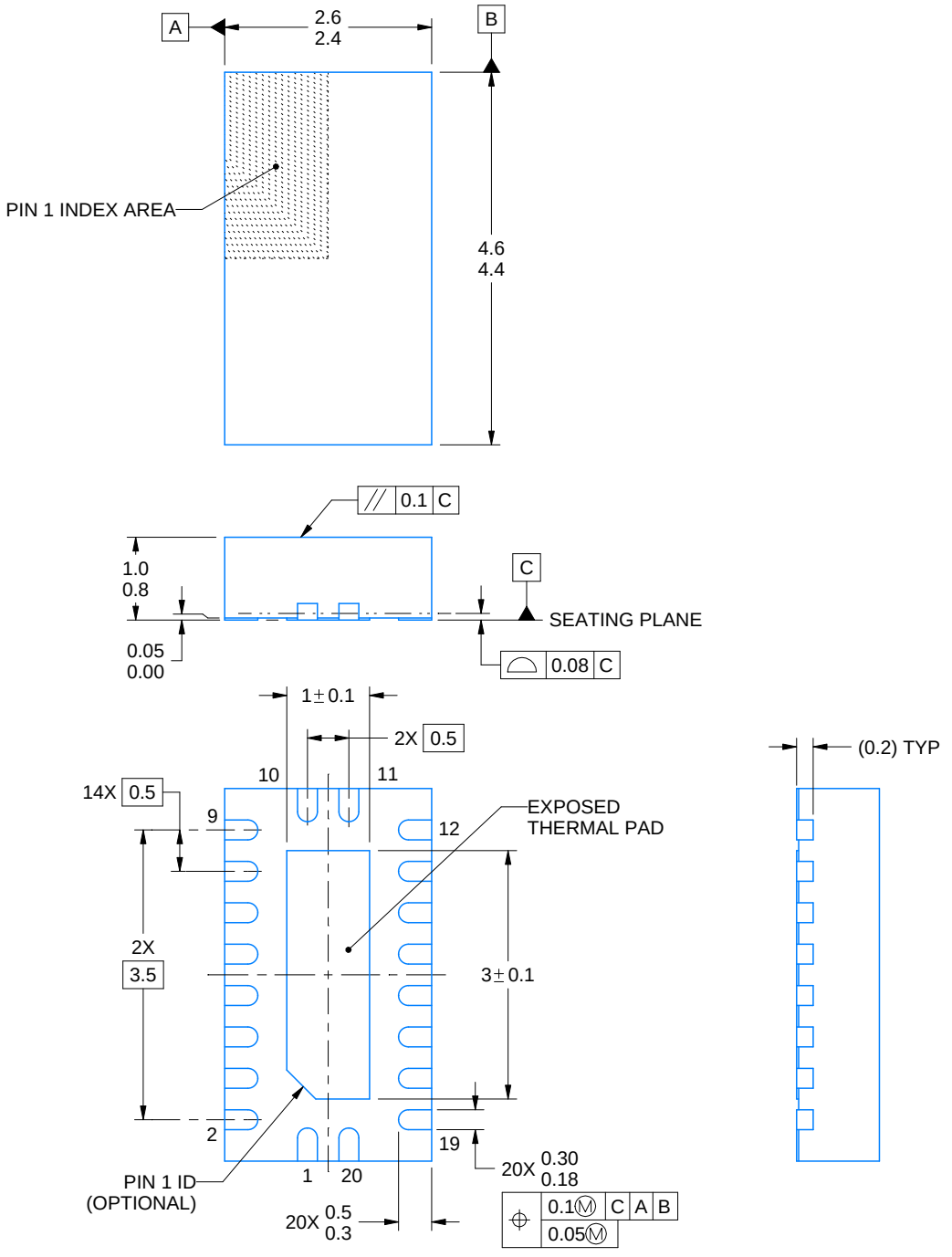


# PACKAGE OUTLINE

## RKS0020A

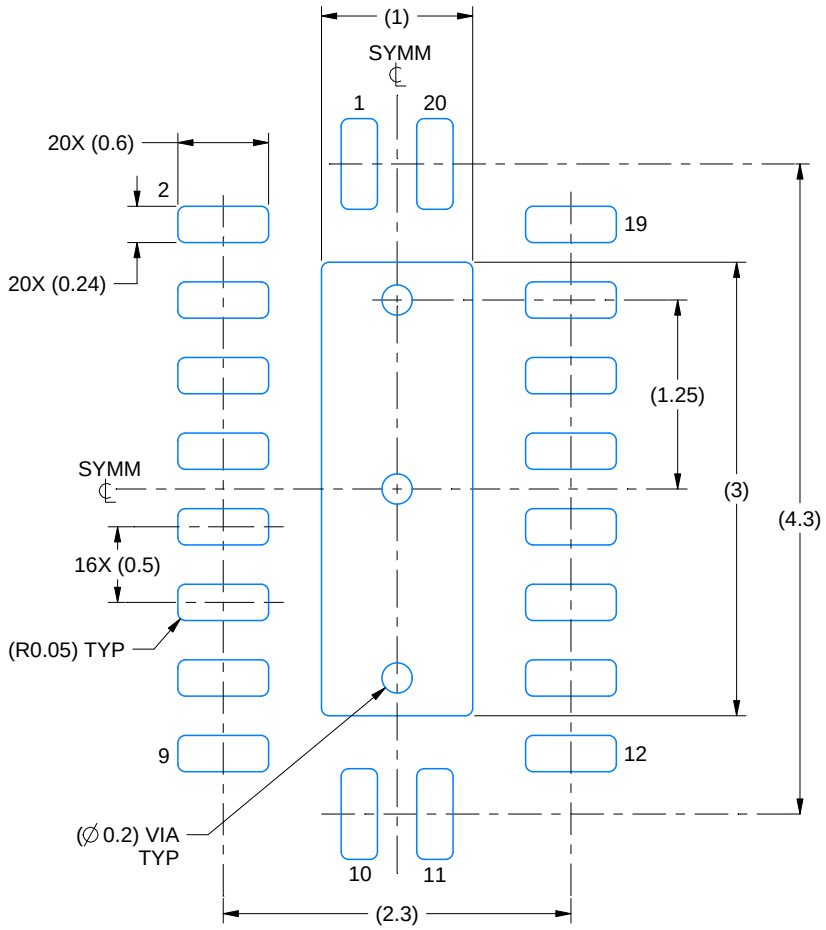
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

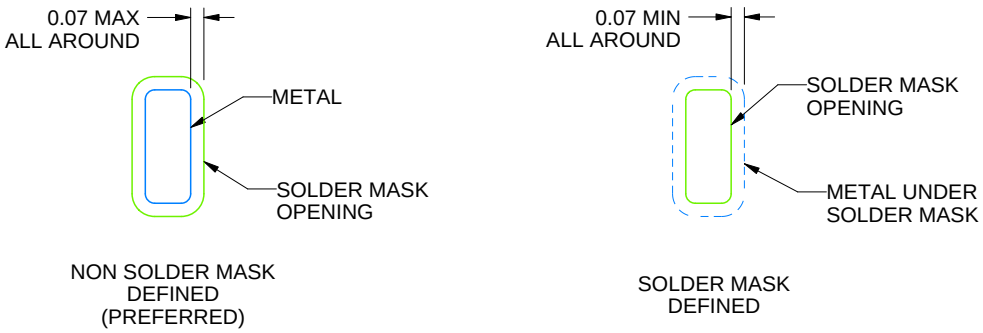



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

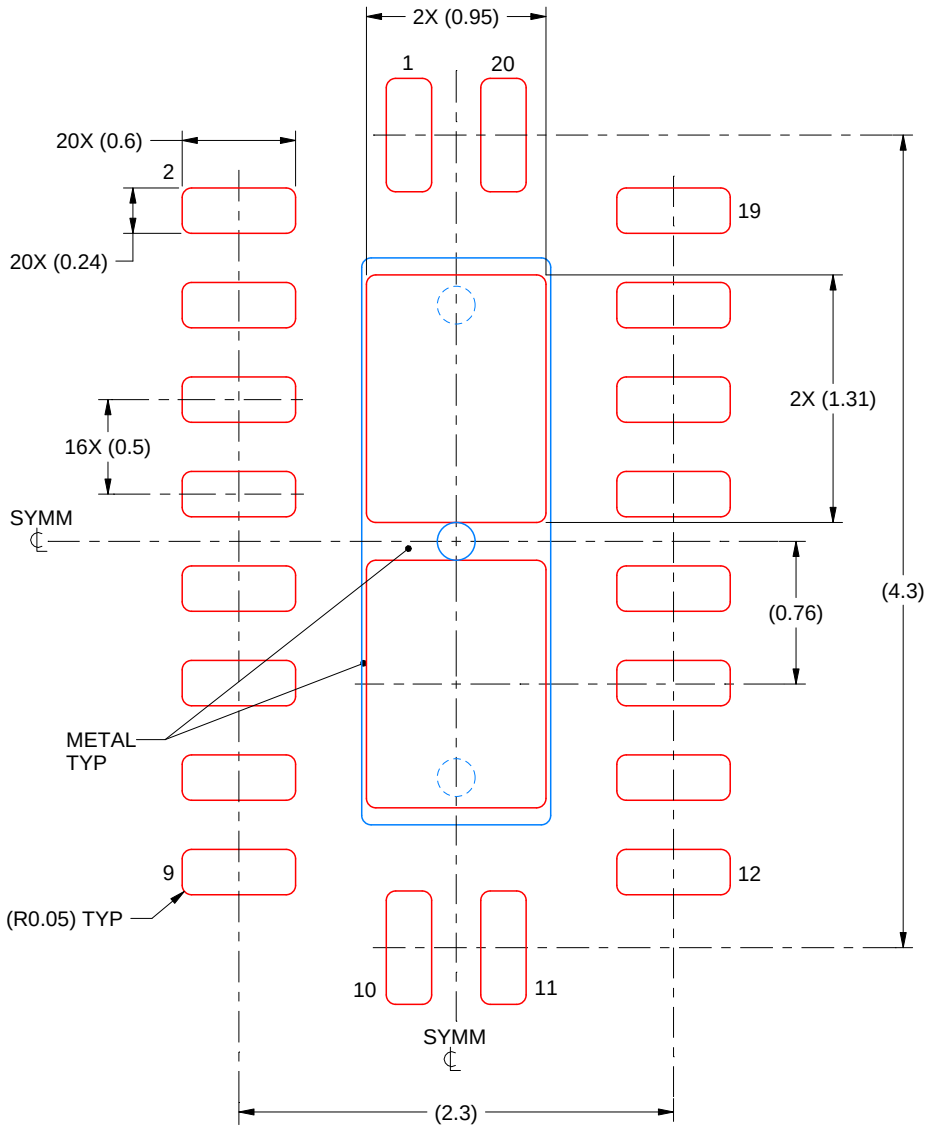



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

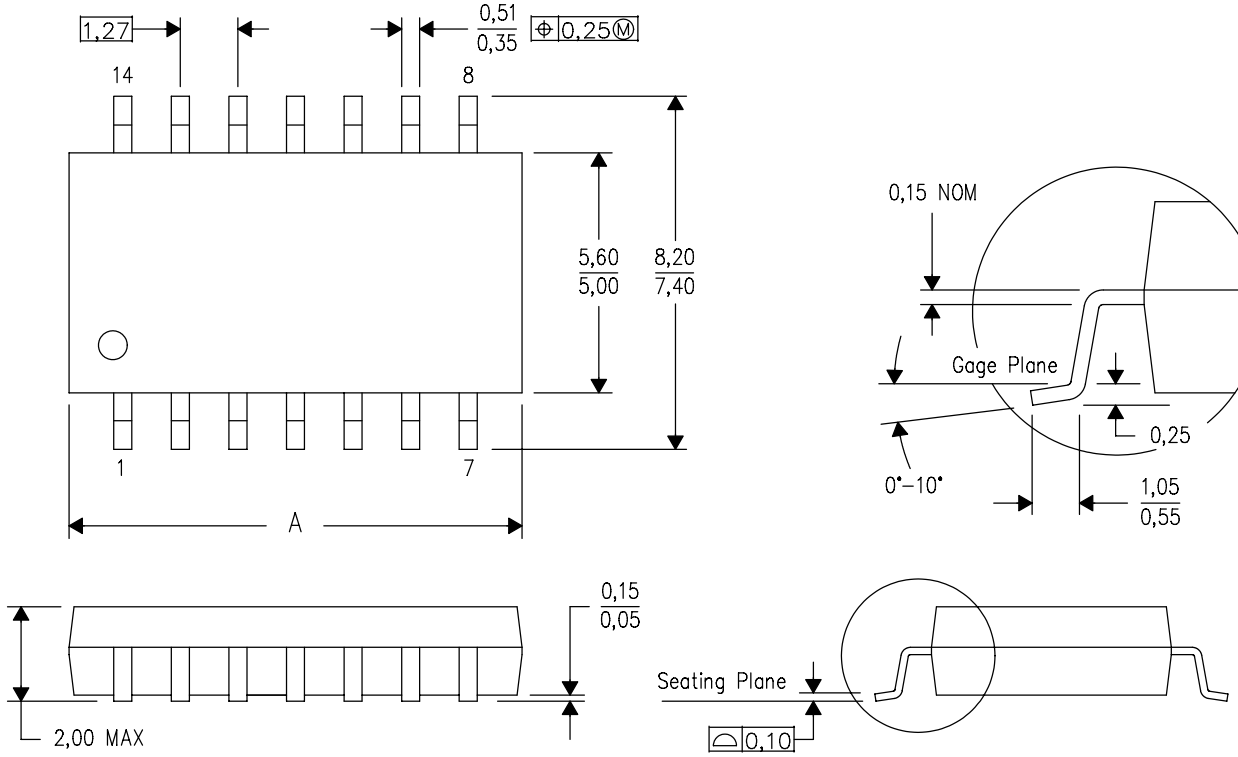
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

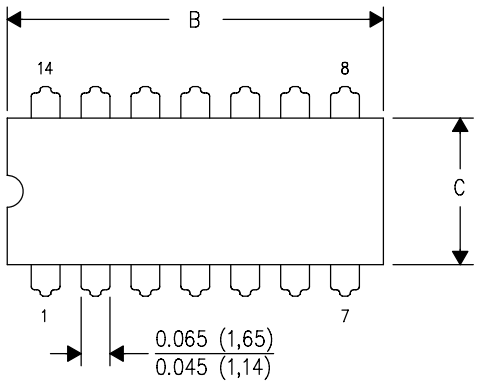
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

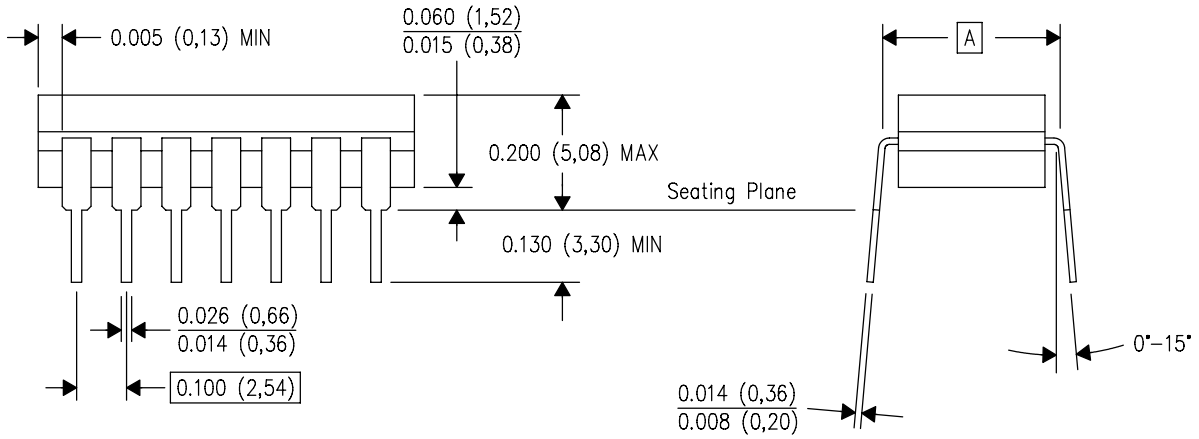
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

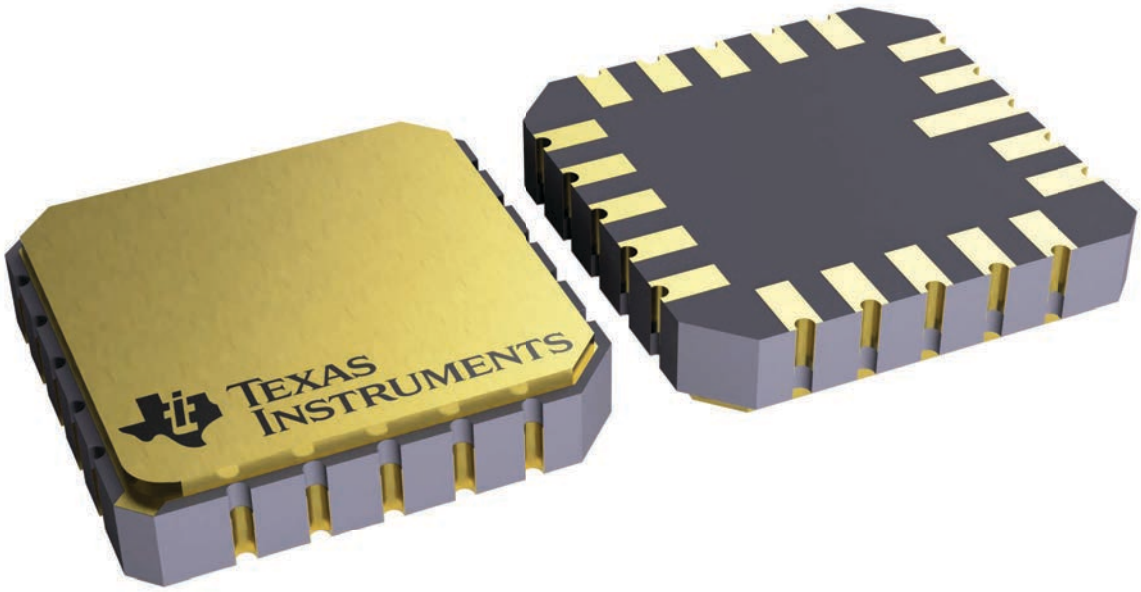
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

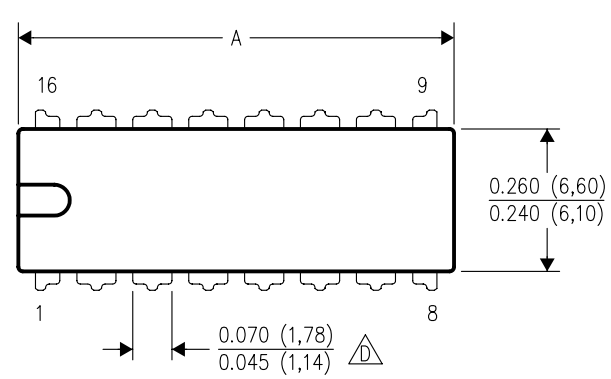



4229370VA\

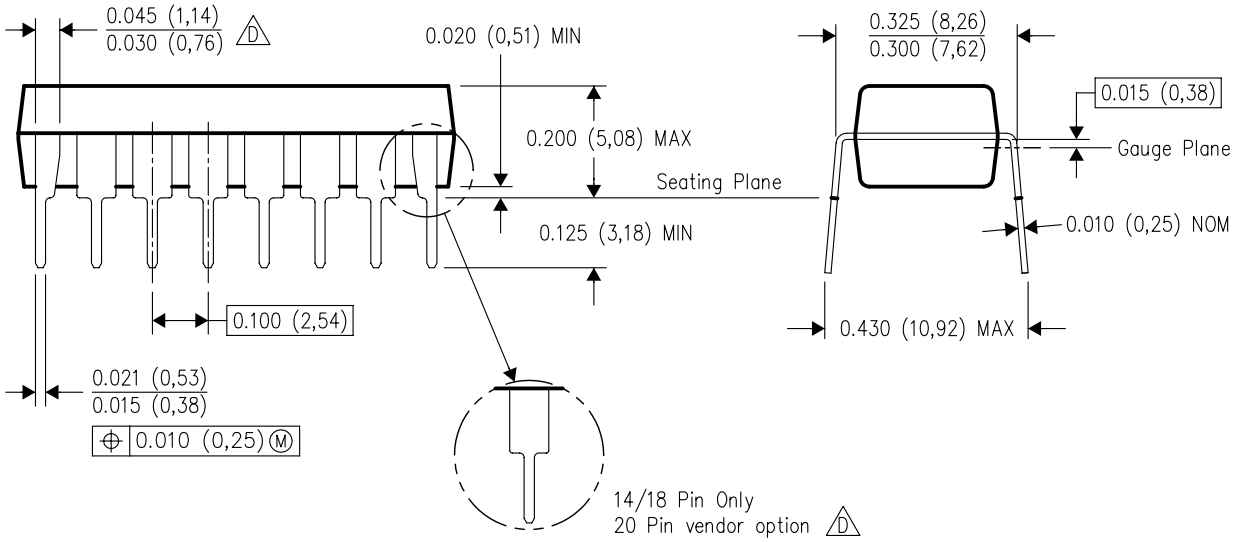
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

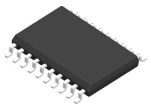



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

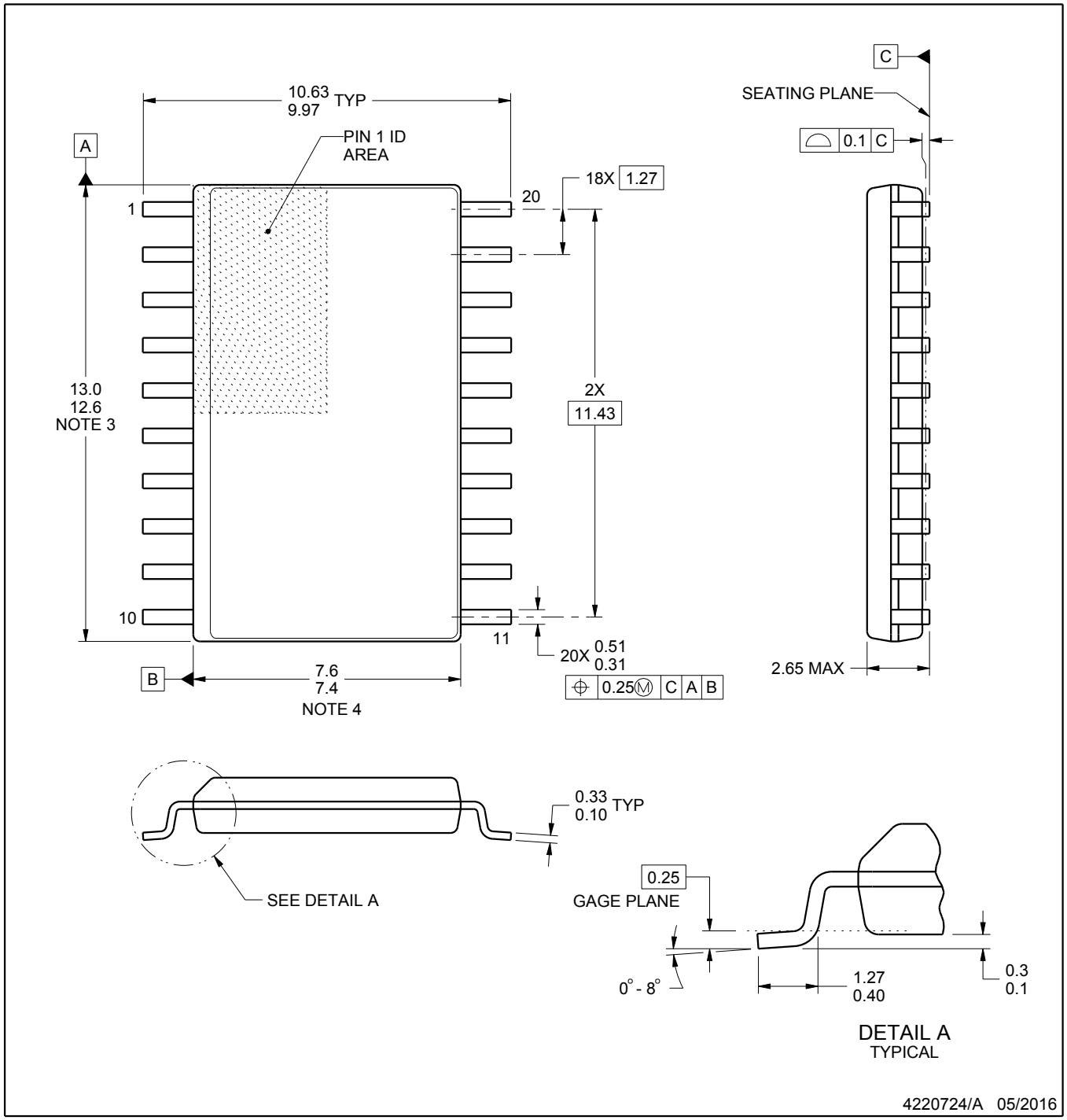


# PACKAGE OUTLINE

## DW0020A

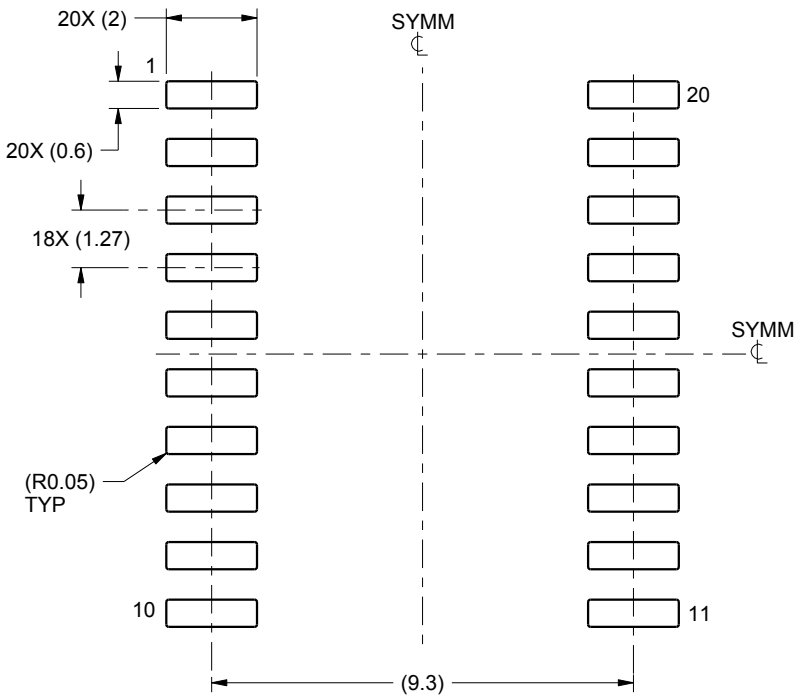
## SOIC - 2.65 mm max height

SOIC

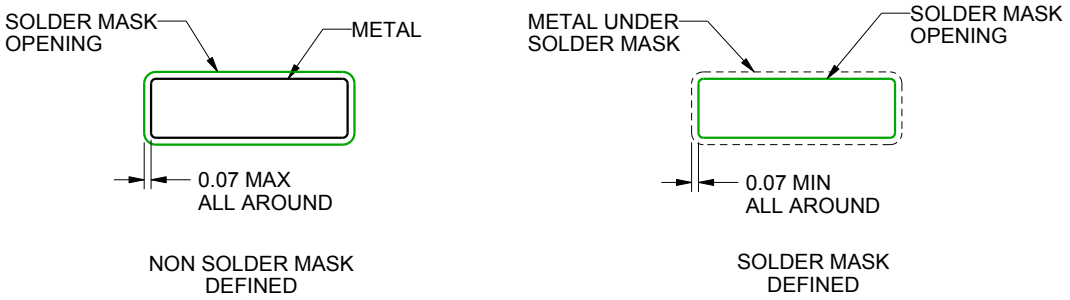



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

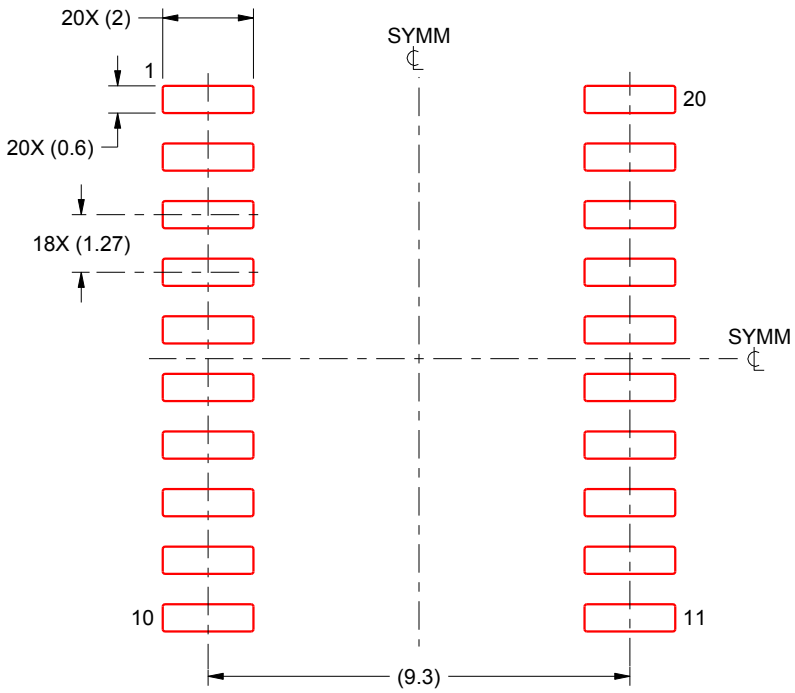



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



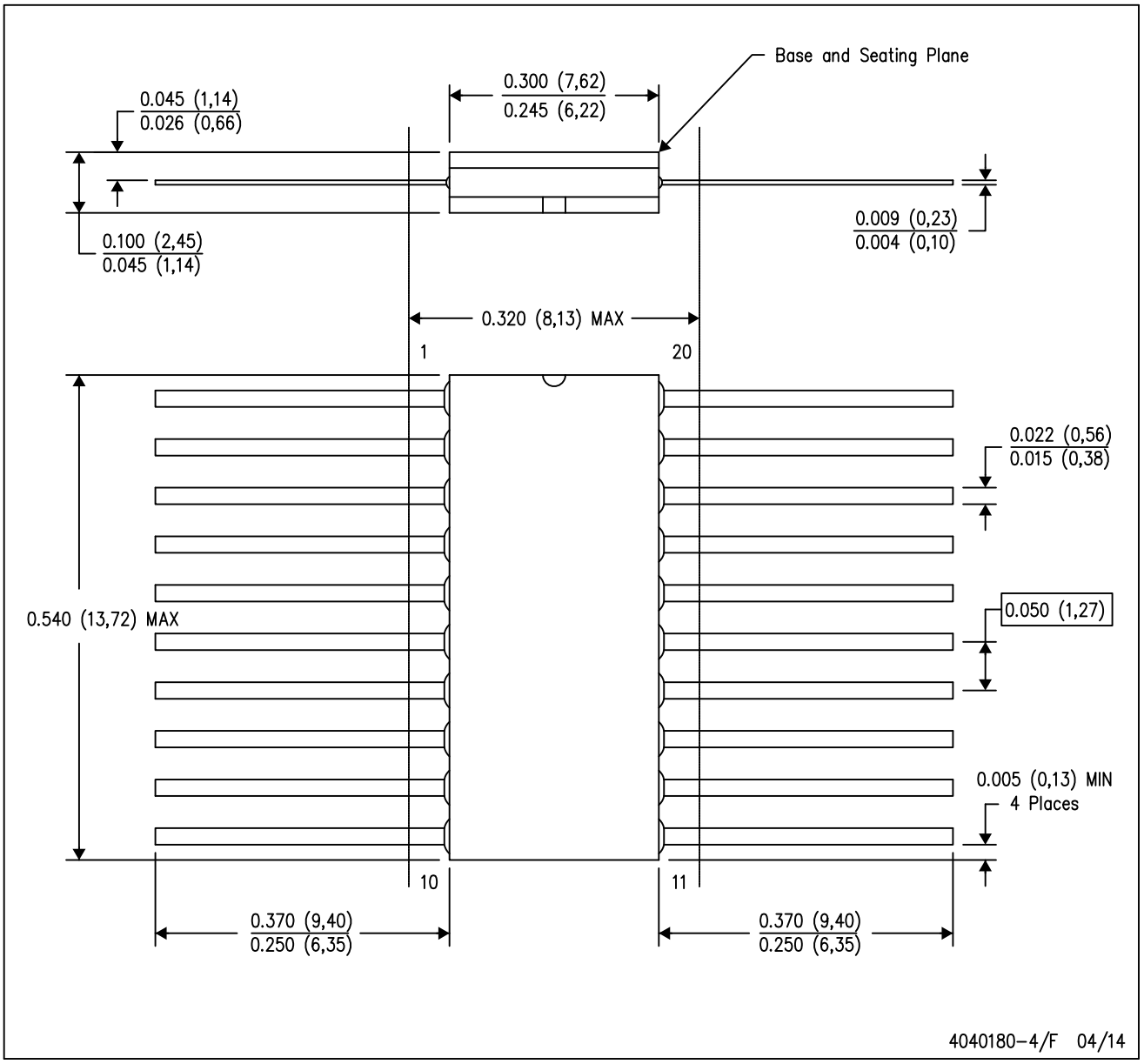

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



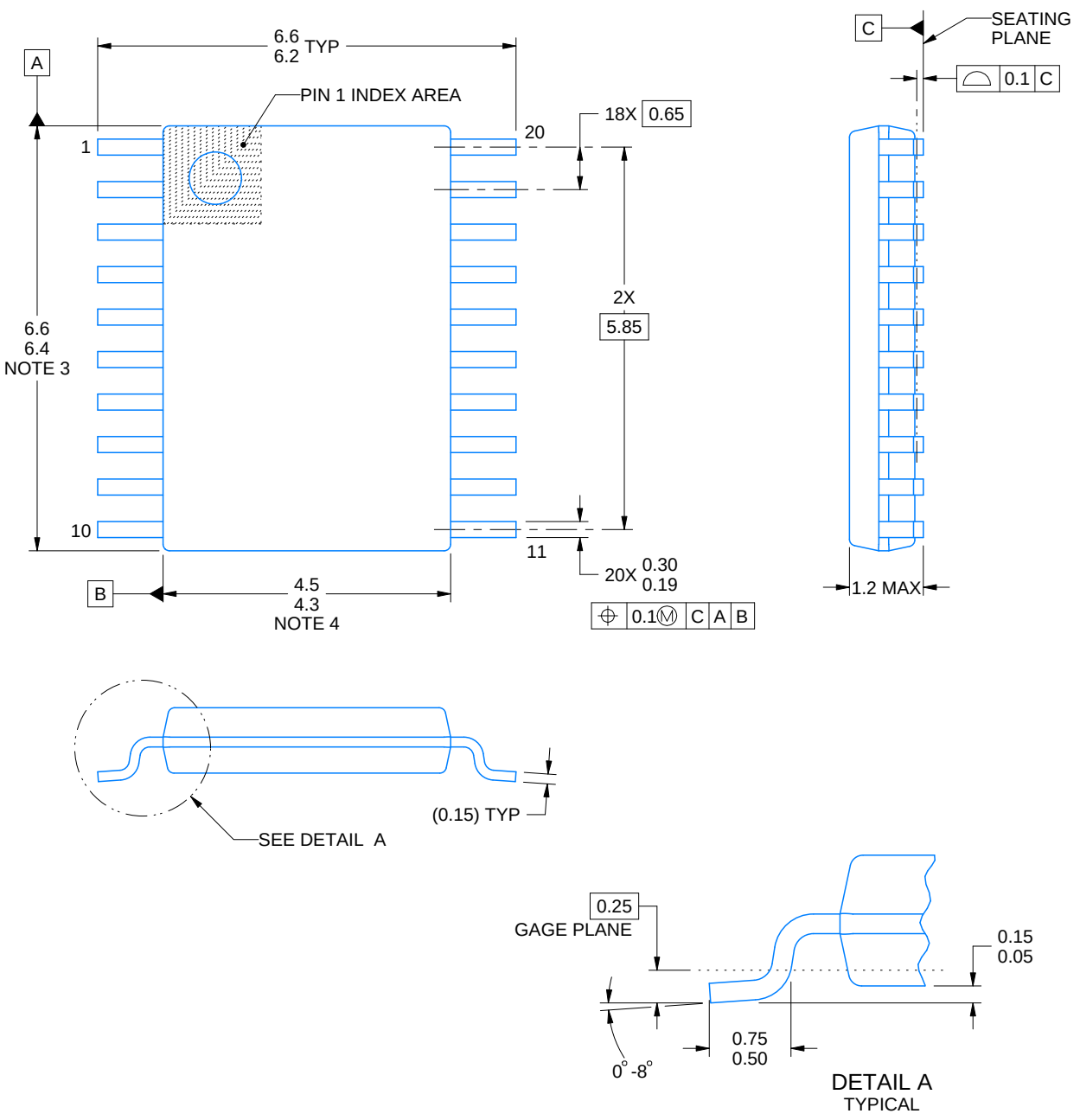

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

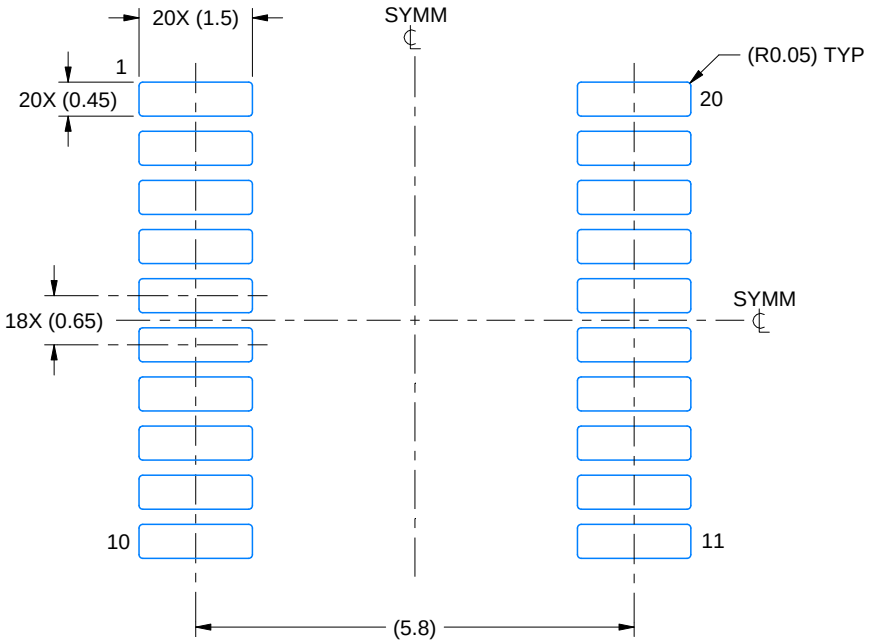
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



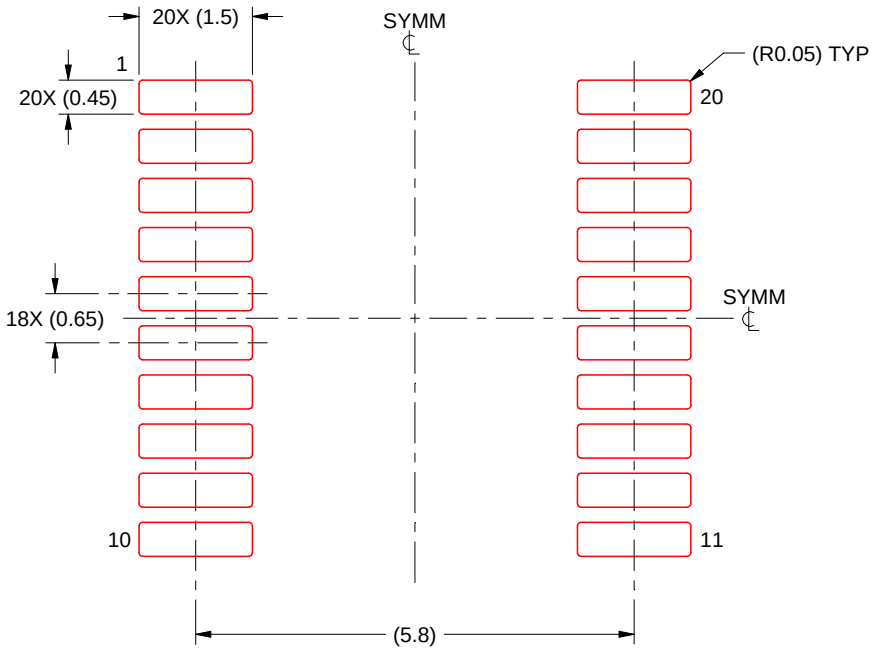

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

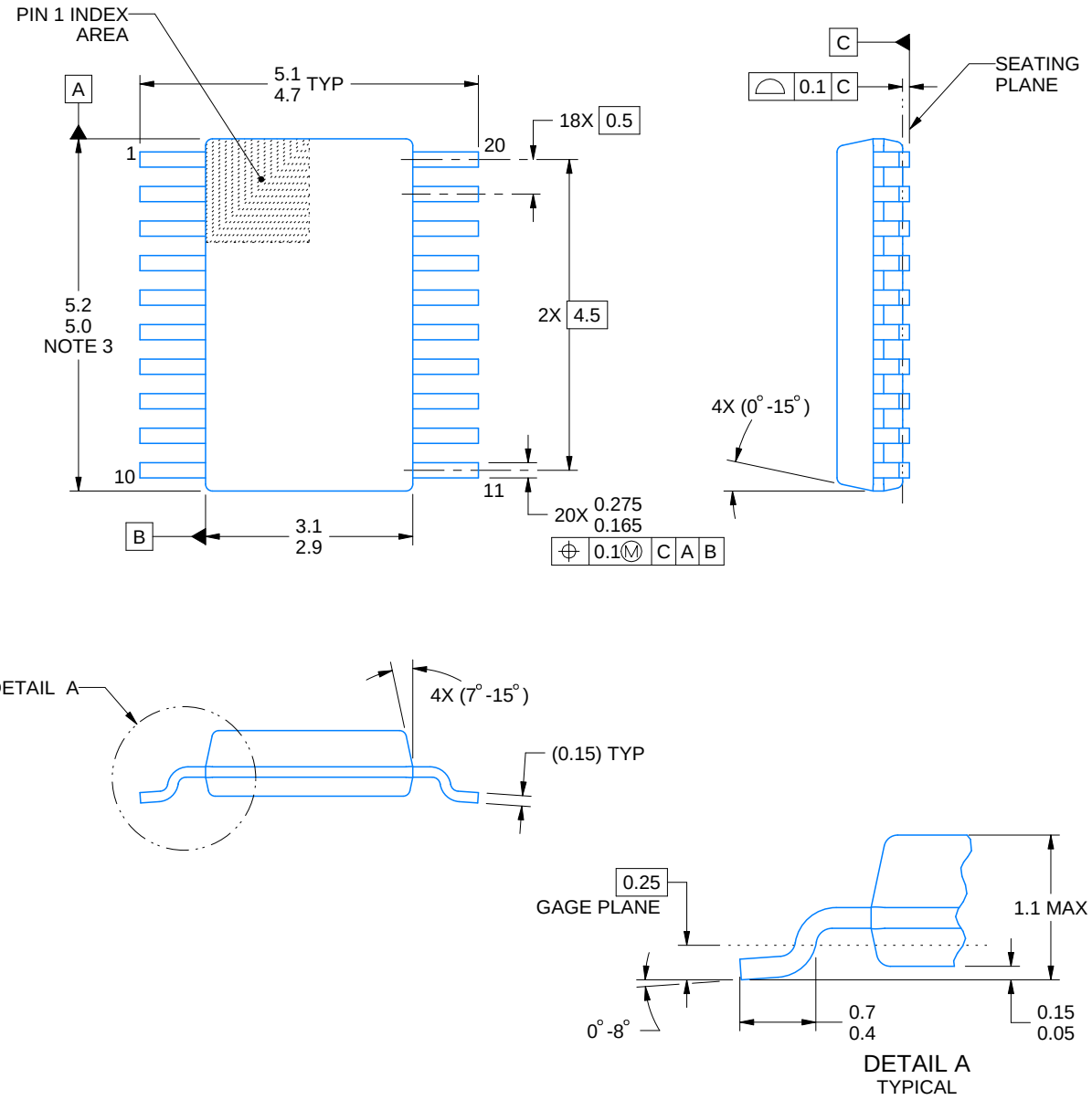
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0020A

## VSSOP - 1.1 mm max height

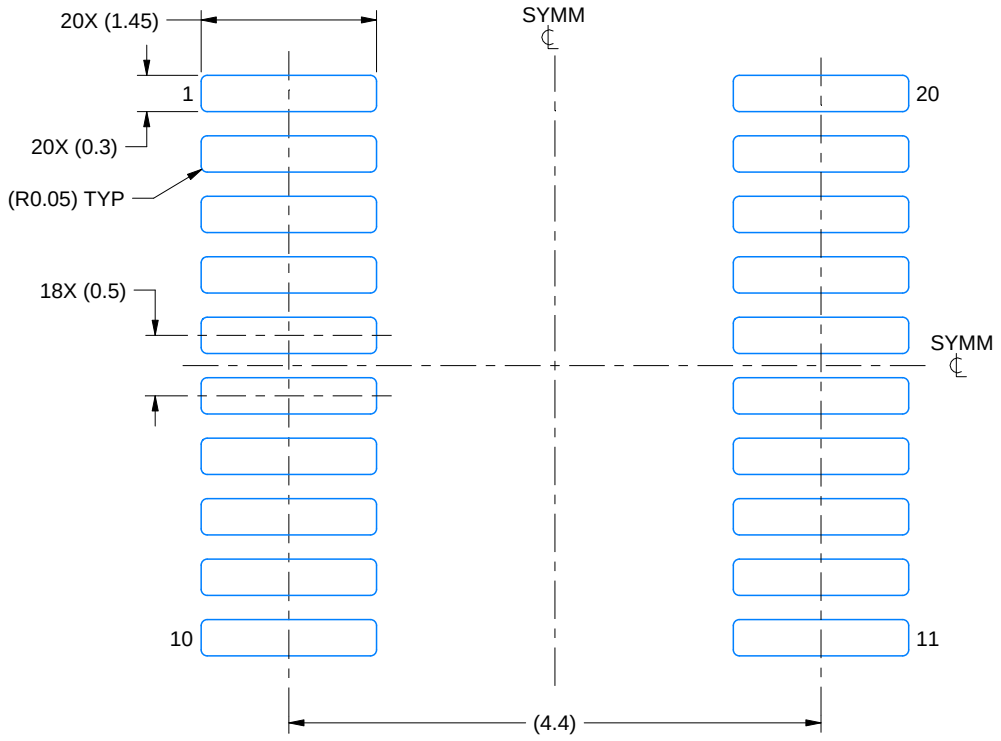
SMALL OUTLINE PACKAGE



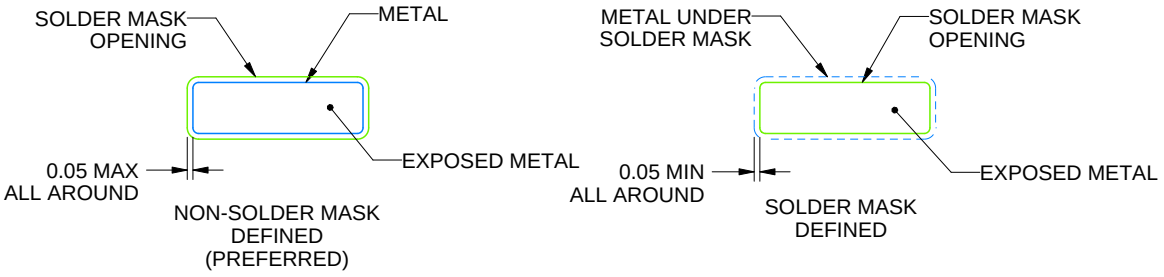

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE: 16X

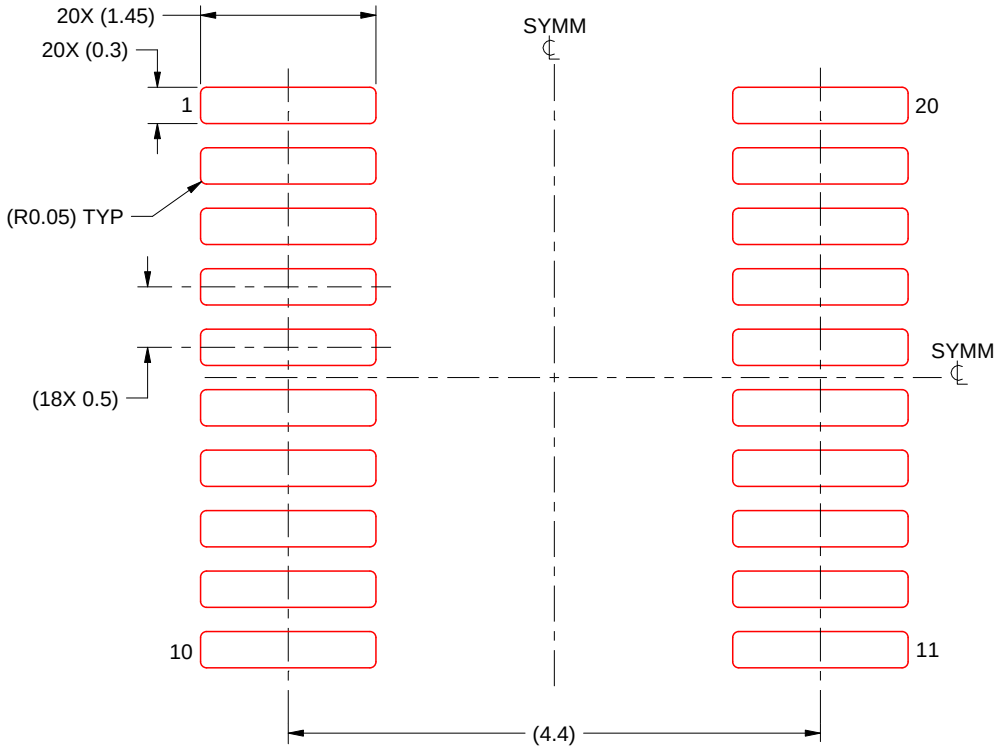



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265