

RES31A-Q1 Automotive, Matched, Thin-Film Resistor Dividers With 100kΩ Inputs

1 Features

- AEC-Q200 Qualified for automotive applications:
 - Temperature: -40°C to $+125^{\circ}\text{C}$
- Ratio = $R_{IN} : R_G$, $R_{IN} = 100\text{k}\Omega$ (nominal)
- Highly precise ratio tolerance: $\pm 0.05\%$ (maximum)
- Low drift:
 - $+2/-5\text{ppm}/^{\circ}\text{C}$ max $\text{TCR}_{\text{ratio}}$ for RES31A00-Q1 ($\pm 2\text{ppm}/^{\circ}\text{C}$ max $\text{TCR}_{\text{ratio}}$ from -40°C to $+105^{\circ}\text{C}$)
 - $\pm 2\text{ppm}/^{\circ}\text{C}$ max $\text{TCR}_{\text{ratio}}$ for other ratios
- **Functional safety-capable**
 - Documentation available to aid functional safety system design

2 Applications

- Precision voltage divider, precision level translation
- Amplifier gain and attenuation configuration
- Discrete difference and instrumentation amplifier implementations with high CMRR and gain accuracy
- Pinpoint comparator threshold setting

3 Description

The RES31A-Q1 is a matched pair of resistive dividers, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog CMOS process. The device has a nominal input resistance of $100\text{k}\Omega$, supporting higher divider voltages than the RES11A-Q1 but with a lower current draw than the RES21A-Q1, and is available in several nominal ratios to meet a wide array of system needs. Use the RES31A-Q1 in an inverse gain configuration by simply rotating the device placement by 180° . This feature supports layout reuse and increases flexibility for applications such

as discrete instrumentation or difference amplifier implementations.

The RES31A-Q1 series features high ratio-matching precision, with the measured ratio of each divider within 0.05% ($\pm 500\text{ppm}$) of the nominal. This precision is maintained over the temperature range.

The RES31A-Q1 is specified with a temperature range from -40°C to $+125^{\circ}\text{C}$. The device is offered in an 8-pin, SOT-23-THIN package, with a body size of $2.9\text{mm} \times 1.6\text{mm}$ (body size is a nominal value and does not include pins).

Package Information

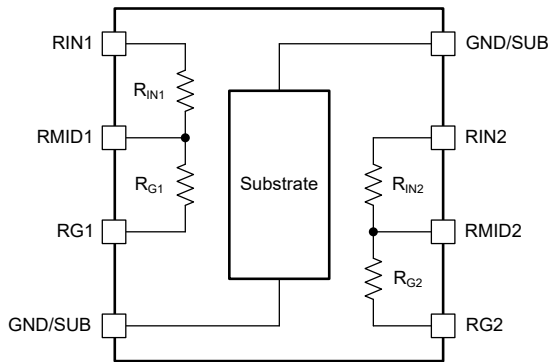
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
RES31A-Q1	DDF (SOT-23-THIN, 8)	$2.9\text{mm} \times 2.8\text{mm}$

- (1) For more information, see [Section 11](#).
 (2) The package size (length \times width) is a nominal value and includes pins, where applicable.

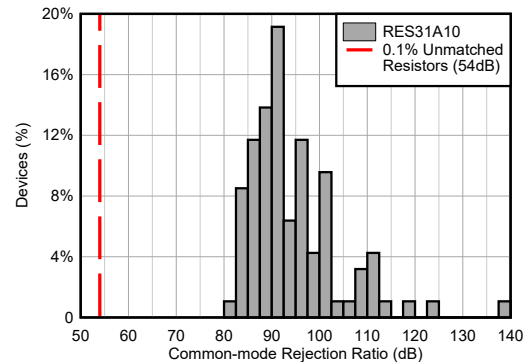
Device Information

PART NUMBER	NOMINAL RATIO
RES31A10-Q1	1:1
RES31A15-Q1 ⁽¹⁾	1:1.5
RES31A16-Q1 ⁽¹⁾	1:1.667
RES31A20-Q1	1:2
RES31A25-Q1	1:2.5
RES31A30-Q1	1:3
RES31A40-Q1	1:4
RES31A50-Q1	1:5
RES31A90-Q1 ⁽¹⁾	1:9
RES31A00-Q1	1:10

- (1) Preview information (not Advanced Information).



Functional Block Diagram



Excellent Ratio Matching for Best CMRR



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4 Pin Configuration and Functions

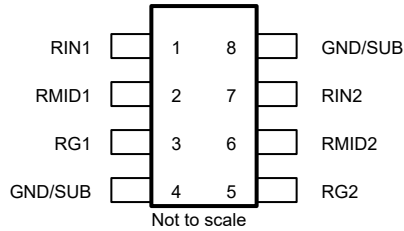


Figure 4-1. DDF Package, 8-Pin SOT-23-THN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND/SUB	4, 8	Ground	Substrate bias connection. Only bias one GND/SUB pin. Float the other GND/SUB pin to prevent current return paths from forming through the substrate. See also Section 7.4 .
RG1	3	Input	Gain resistor connection for divider 1
RG2	5	Input	Gain resistor connection for divider 2
RIN1	1	Input	Input resistor connection for divider 1
RIN2	7	Input	Input resistor connection for divider 2
RMID1	2	Output	Center tap of divider 1
RMID2	6	Output	Center tap of divider 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CM}	Maximum sustained common mode voltage (any pin to GND/SUB)	-85	85	V	
ΔV _{DMAX}	Maximum instantaneous overload voltage per divider (RINx pin to RGx pin) ⁽²⁾	RES31A10	-135	135	V
		RES31A15 ⁽³⁾	-135	135	
		RES31A16 ⁽³⁾	-135	135	
		RES31A20	-135	135	
		RES31A25	-135	135	
		RES31A30	-135	135	
		RES31A40	-135	135	
		RES31A50	-135	135	
		RES31A90 ⁽³⁾	-135	135	
RES31A00	-135	135			
T _A	Ambient temperature	-55	150	°C	
T _J	Junction temperature	-55	150	°C	
T _{stg}	Storage temperature	-55	175	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Maximum instantaneous voltage permitted under transient conditions. Avoid sustained operation at these voltage levels.
- (3) Preview only.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q200-002	±700	V

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
V _{RECMAX}	Maximum sustained divider voltage, dc (10 years at T _A = 25°C) ⁽¹⁾	RES31A10	-85		85	V
		RES31A15 ⁽²⁾	-85		85	
		RES31A16 ⁽²⁾	-85		85	
		RES31A20	-85		85	
		RES31A25	-85		85	
		RES31A30	-85		85	
		RES31A40	-85		85	
		RES31A50	-85		85	
		RES31A90 ⁽²⁾	-85		85	
		RES31A00	-85		85	
	Maximum sustained divider voltage, ac (≥50Hz, 10 years at T _A = 25°C) ⁽¹⁾	RES31A10	-85		85	V _{RMS}
		RES31A15 ⁽²⁾	-85		85	
		RES31A16 ⁽²⁾	-85		85	
		RES31A20	-85		85	
		RES31A25	-85		85	
		RES31A30	-85		85	
		RES31A40	-85		85	
		RES31A50	-85		85	
		RES31A90 ⁽²⁾	-85		85	
		RES31A00	-85		85	
T _A	Ambient temperature	-40		125	°C	

- (1) Assumes R_{θJA} = 156.2°C/W. Applies whether the specified voltage is applied across a *single* divider, or *both* dividers simultaneously. Adhere to the limitations in *Absolute Maximum Ratings*.
 (2) Preview only.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RES31A-Q1	UNIT
		DDF (SOT-23-THIN)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	156.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	77.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	73.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	73.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INITIAL RESISTANCE							
R_{INnom}	Nominal input resistance				100		k Ω
R_{Gnom}	Nominal gain resistance	RES31A10			100		k Ω
		RES31A15 ⁽¹⁾			150		
		RES31A16 ⁽¹⁾			166.67		
		RES31A20			200		
		RES31A25			250		
		RES31A30			300		
		RES31A40			400		
		RES31A50			500		
		RES31A90 ⁽¹⁾			900		
		RES31A00			1000		
G_{nom}	Nominal ratio (R_{Gx} / R_{INx})	RES31A10			1		V/V
		RES31A15 ⁽¹⁾			1.5		
		RES31A16 ⁽¹⁾			1.667		
		RES31A20			2		
		RES31A25			2.5		
		RES31A30			3		
		RES31A40			4		
		RES31A50			5		
		RES31A90 ⁽¹⁾			9		
		RES31A00			10		
t_{D1}	Ratio tolerance of divider 1 ^{(2) (3)}	$(R_{G1} / R_{IN1}) / G_{nom} - 1$	RES31A10	-500	± 43	500	ppm
			RES31A15 ⁽¹⁾	-500		500	
			RES31A16 ⁽¹⁾	-500		500	
			RES31A20	-500	± 48	500	
			RES31A25	-500	± 138	500	
			RES31A30	-500	± 100	500	
			RES31A40	-500	± 55	500	
			RES31A50	-500	± 112	500	
			RES31A90 ⁽¹⁾	-500		500	
t_{D2}	Ratio tolerance of divider 2 ^{(2) (3)}	$(R_{G2} / R_{IN2}) / G_{nom} - 1$	RES31A10	-500	± 77	500	ppm
			RES31A15 ⁽¹⁾	-500		500	
			RES31A16 ⁽¹⁾	-500		500	
			RES31A20	-500	± 75	500	
			RES31A25	-500	± 64	500	
			RES31A30	-500	± 98	500	
			RES31A40	-500	± 40	500	
			RES31A50	-500	± 121	500	
			RES31A90 ⁽¹⁾	-500		500	
RES31A00	-500	± 105	500				

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_M	Matching tolerance of dividers 1 and 2 ⁽³⁾	$t_{D2} - t_{D1}$	RES31A10	-1000	±68	1000	ppm
			RES31A15 ⁽¹⁾	-1000		1000	
			RES31A16 ⁽¹⁾	-1000		1000	
			RES31A20	-1000	±69	1000	
			RES31A25	-1000	±124	1000	
			RES31A30	-1000	±74	1000	
			RES31A40	-1000	±58	1000	
			RES31A50	-1000	±157	1000	
			RES31A90 ⁽¹⁾	-1000		1000	
	RES31A00	-1000	±99	1000			
t_{abs}	Absolute tolerance (per resistor) ⁽³⁾ ⁽⁴⁾	$(R_x / R_{x\text{nom}}) - 1$ ⁽⁵⁾		-12	±2	12	%
	Absolute tolerance span	$\text{MAX}(t_{\text{absRIN1}}, t_{\text{absRG1}}, t_{\text{absRIN2}}, t_{\text{absRG2}}) - \text{MIN}(t_{\text{absRIN1}}, t_{\text{absRG1}}, t_{\text{absRIN2}}, t_{\text{absRG2}})$			±140		ppm
RESISTANCE DRIFT							
TCR_{abs}	Absolute temperature coefficient of resistance (per resistor) ⁽⁶⁾	$(\Delta R_x / R_{x(25^\circ\text{C})}) / \Delta T_A$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			12	ppm/ $^\circ\text{C}$
			$T_A = -40^\circ\text{C}$ to -5°C			28	
			$T_A = -5^\circ\text{C}$ to $+65^\circ\text{C}$			15	
			$T_A = 65^\circ\text{C}$ to 105°C			3.2	
			$T_A = 105^\circ\text{C}$ to 125°C			-7.5	
$\text{TCR}_{\text{ratio}}$	Divider temperature coefficient of resistance (per divider) ⁽⁶⁾	$\Delta t_{Dx} / \Delta T_A$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	RES31A00	-2	-0.5	2	ppm/ $^\circ\text{C}$
			RES31A10, RES31A15 ⁽¹⁾ , RES31A16 ⁽¹⁾ , RES31A20, RES31A25, RES31A30, RES31A40, RES31A50, RES31A90 ⁽¹⁾	-2	±0.2	2	
			RES31A00	-5	-1.5	2	
TCR_M	Matching temperature coefficient of resistance ⁽⁶⁾	$\Delta t_M / \Delta T_A$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	RES31A00			±0.05	ppm/ $^\circ\text{C}$
			RES31A10, RES31A15 ⁽¹⁾ , RES31A16 ⁽¹⁾ , RES31A20, RES31A25, RES31A30, RES31A40, RES31A50, RES31A90 ⁽¹⁾			±0.05	
			RES31A00			-0.25	
VCR_{abs}	Absolute voltage coefficient of resistance (per resistor) ⁽⁴⁾ ⁽⁶⁾	$\Delta R_x / \Delta V_{R_x}$, $V_{Dx} = -V_{\text{RECMAX}}$ to V_{RECMAX}	RES31A10, RES31A15 ⁽¹⁾ , RES31A16 ⁽¹⁾ , RES31A20, RES31A25, RES31A30, RES31A40, RES31A50, RES31A90 ⁽¹⁾			±1.1	Ω/V
			RES31A00			±5.6	
$\text{VCR}_{\text{ratio}}$	Divider voltage coefficient of resistance (per divider) ⁽⁶⁾	$\Delta t_{Dx} / \Delta V_{Dx}$, $V_{Dx} = -V_{\text{RECMAX}}$ to V_{RECMAX}				±0.2	ppm/V
VCR_M	Matching voltage coefficient of resistance ⁽⁶⁾	$(\Delta t_{D2} - \Delta t_{D1}) / \Delta V_{Dx}$, $V_{Dx} = -V_{\text{RECMAX}}$ to V_{RECMAX}				±0.15	ppm/V
ARBITRARY MATCHING							
	R_G mismatch between dividers, absolute ⁽³⁾	$(R_{G2} - R_{G1}) / R_{G\text{nom}}$				±60	ppm

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	R_G mismatch between dividers, ratiometric ⁽³⁾	$(R_{G1} / R_{G2}) - 1$, and $(R_{G2} / R_{G1}) - 1$		±60		ppm
		$((R_{G1} / R_{IN2}) / G_{nom}) - 1$, and $((R_{G2} / R_{IN1}) / G_{nom}) - 1$		±87		
		$(R_{G1} / (R_{G2} + R_{IN2})) / (G_{nom} / (G_{nom} + 1)) - 1$, and $(R_{G2} / (R_{G1} + R_{IN1})) / (G_{nom} / (G_{nom} + 1)) - 1$		±59		
	R_{IN} mismatch between dividers, absolute ⁽³⁾	$(R_{IN2} - R_{IN1}) / R_{INnom}$		±91		ppm
	R_{IN} mismatch between dividers, ratiometric ⁽³⁾	$(R_{IN1} / R_{IN2}) - 1$, and $(R_{IN2} / R_{IN1}) - 1$		±91		ppm
		$(R_{IN1} / R_{G2}) \times (G_{nom}) - 1$, and $(R_{IN2} / R_{G1}) \times (G_{nom}) - 1$		±87		
		$(R_{IN1} / (R_{G2} + R_{IN2})) \times (G_{nom} + 1) - 1$, and $(R_{IN2} / (R_{G1} + R_{IN1})) \times (G_{nom} + 1) - 1$		±83		
	End-to-end mismatch between dividers, absolute ⁽³⁾	$((R_{G2} + R_{IN2}) - (R_{G1} + R_{IN1})) / (R_{INnom} + R_{Gnom})$		±57		ppm
	End-to-end mismatch between dividers, ratiometric ⁽³⁾	$((R_{G2} + R_{IN2}) / (R_{G1} + R_{IN1})) - 1$		±57		ppm
IMPEDANCE						
C_{IN}	Pin capacitance ⁽⁶⁾	RINx to GND/SUB		1.95		pF
		RGx to GND/SUB		1.45		
		RMIDx to GND/SUB		3.17		
	Crosstalk (RMID1 to RMID2) ⁽⁶⁾	Substrate biased to GND	f = 10kHz	-63		dB
			f = 1MHz	-42		
	-3dB bandwidth ⁽⁶⁾	Substrate biased to GND ⁽⁷⁾	RES31A10	570		kHz
			RES31A15 ⁽¹⁾ , RES31A16 ⁽¹⁾ , RES31A20	425		
			RES31A25, RES31A30	415		
			RES31A40	365		
			RES31A50	345		
			RES31A90 ⁽¹⁾ , RES31A00	280		
CMRR	Common-mode rejection ratio ⁽⁸⁾	RES31A10	66.0	86.3		dB
		RES31A15 ⁽¹⁾	68.0			
		RES31A16 ⁽¹⁾	68.5			
		RES31A20	69.5	88.8		
		RES31A25	70.9	89.1		
		RES31A30	72.0	93.1		
		RES31A40	74.0	97.1		
		RES31A50	75.6	88.9		
		RES31A90 ⁽¹⁾	80.0			
		RES31A00	80.8	100.9		

(1) Preview only.

(2) Relation of R_{G1} / R_{IN1} or R_{G2} / R_{IN2} to nominal ratio.

(3) Error term is zero-mean. Treat the typical value reported here as one standard deviation ($\pm 1\sigma$) for error analysis purposes.

(4) Relation of R_{G1} , R_{IN1} , R_{G2} , or R_{IN2} to nominal resistance.

(5) The specification is the result of this expression, given as a percentage (multiplied by 100%).

(6) Specified by characterization.

(7) If higher bandwidth is required, floating the substrate or using a guard buffer to drive the substrate can modestly increase bandwidth.

(8) The specification is the calculated CMRR when implemented in a difference amplifier configuration with an ideal op-amp, such that the only source of common-mode error is the resistor network. See the [Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs](#) application note for more information. Effects over frequency are not included. If the circuit is configured in an attenuating gain, this result changes accordingly.

5.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

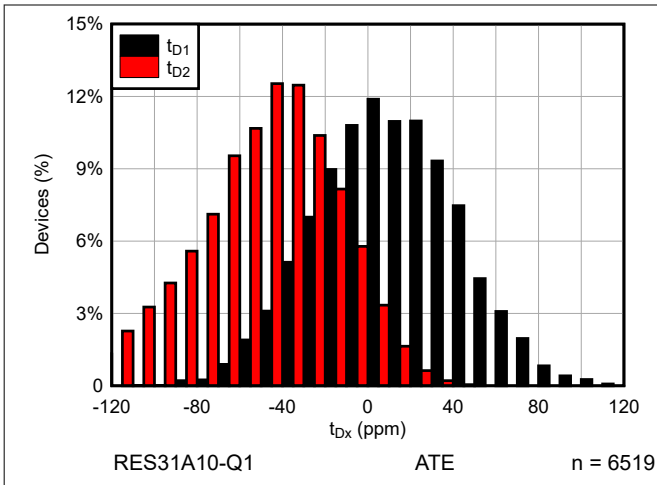


Figure 5-1. t_{Dx} Distribution

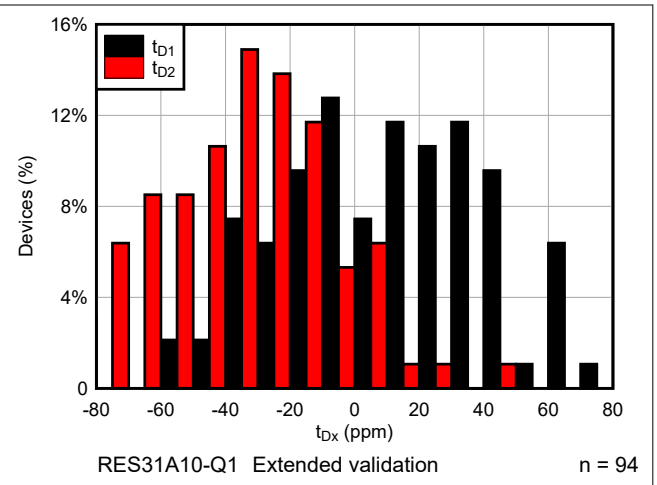


Figure 5-2. t_{Dx} Distribution

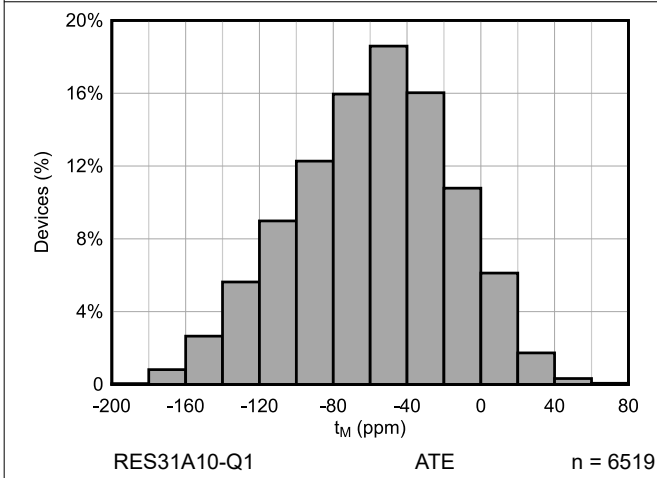


Figure 5-3. t_M Distribution

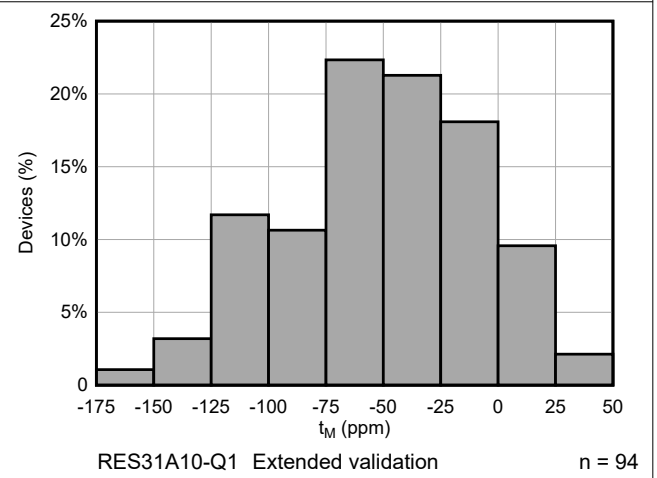


Figure 5-4. t_M Distribution

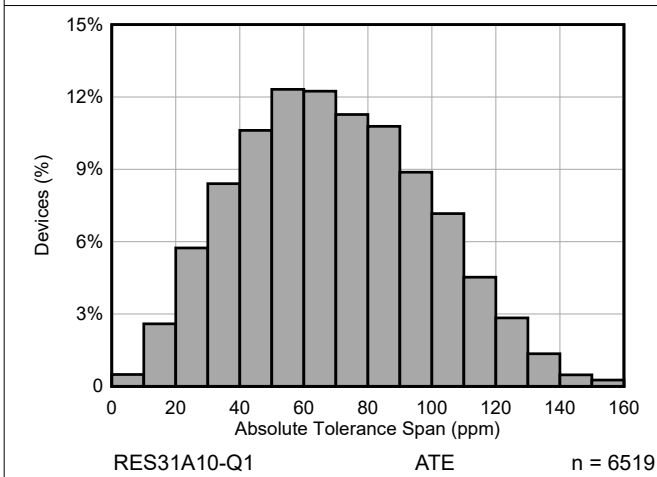


Figure 5-5. Absolute Tolerance Span Distribution

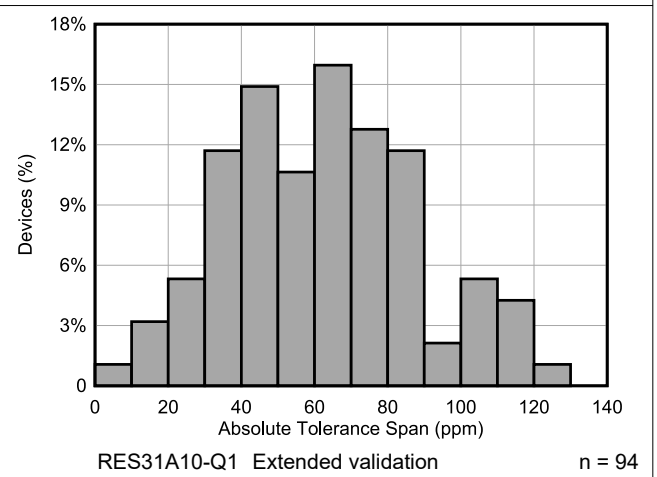


Figure 5-6. Absolute Tolerance Span Distribution

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

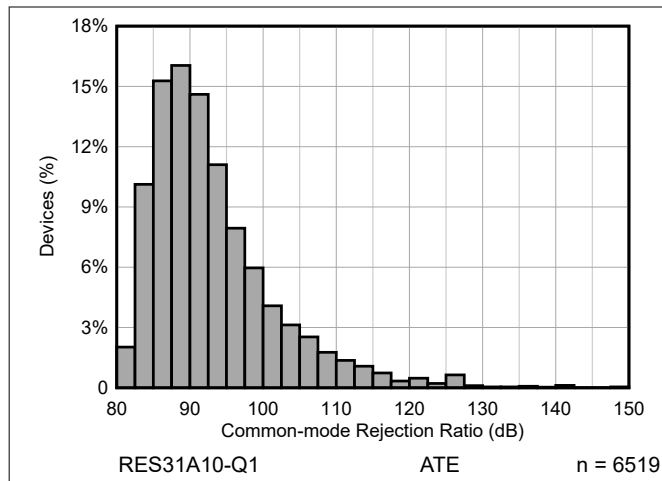


Figure 5-7. Common-mode Rejection Ratio Distribution

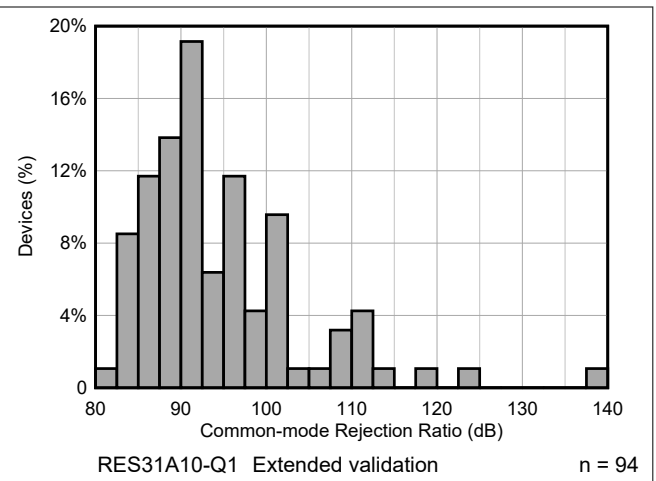


Figure 5-8. Common-mode Rejection Ratio Distribution

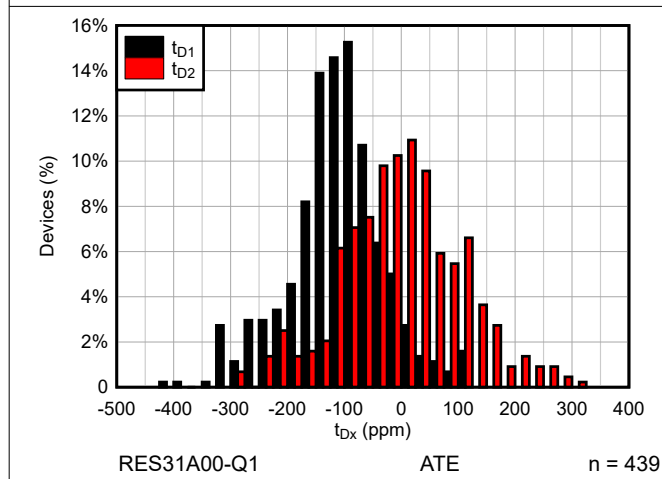


Figure 5-9. t_{Dx} Distribution

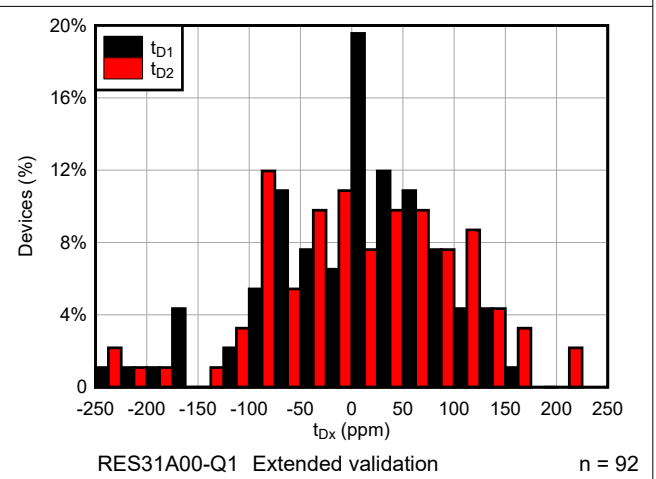


Figure 5-10. t_{Dx} Distribution

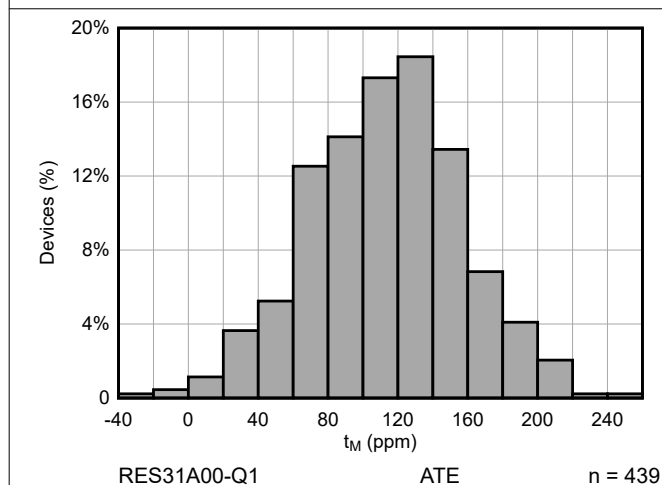


Figure 5-11. t_M Distribution

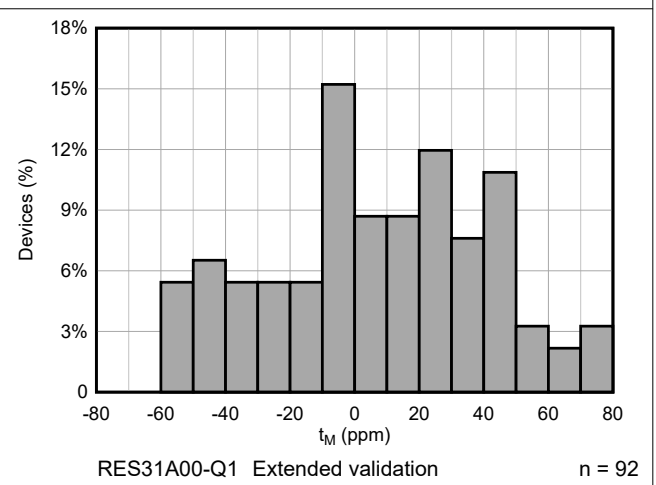


Figure 5-12. t_M Distribution

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

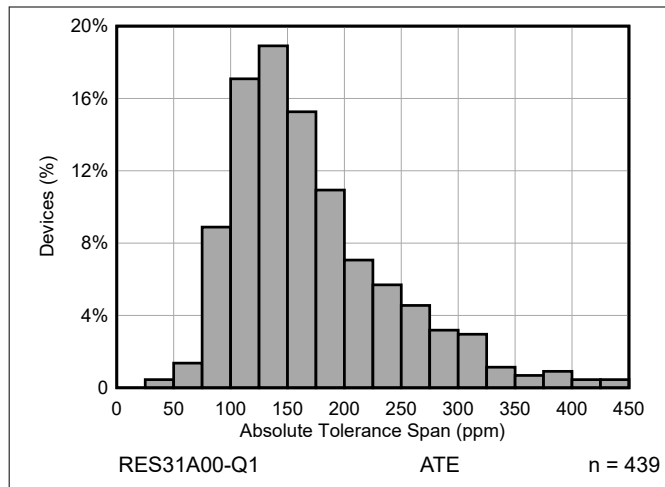


Figure 5-13. Absolute Tolerance Span Distribution

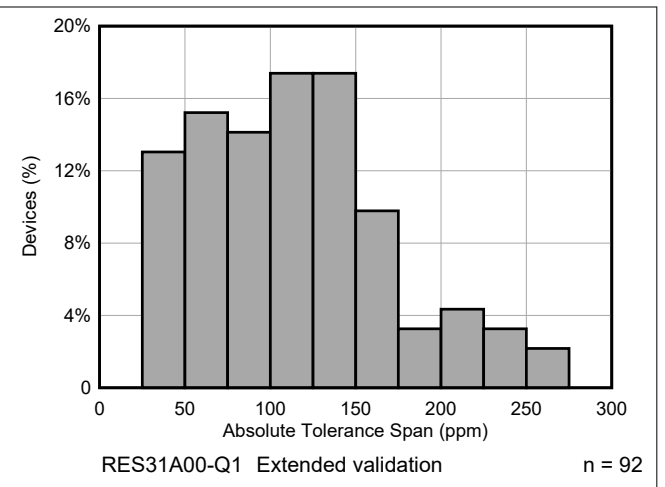


Figure 5-14. Absolute Tolerance Span Distribution

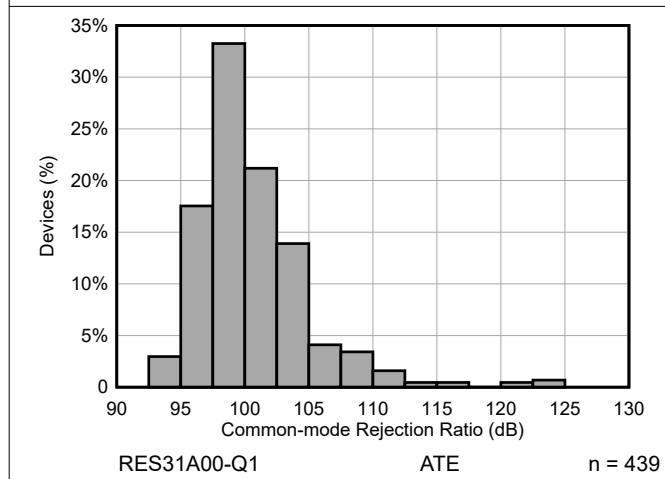


Figure 5-15. Common-mode Rejection Ratio Distribution

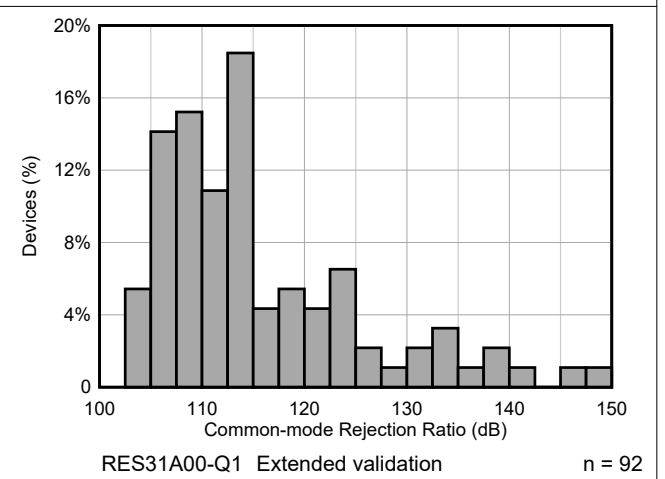


Figure 5-16. Common-mode Rejection Ratio Distribution

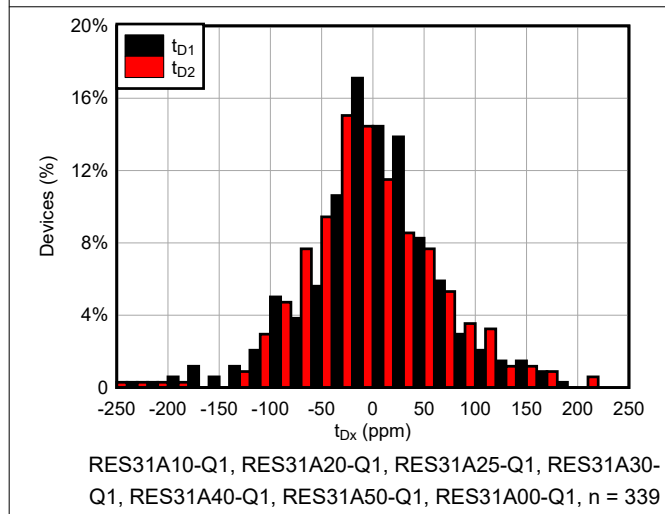


Figure 5-17. t_{Dx} Distribution, All Ratios

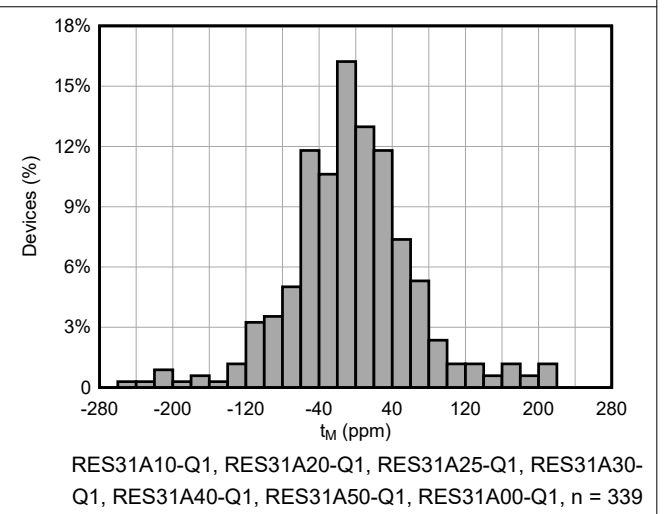


Figure 5-18. t_M Distribution, All Ratios

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

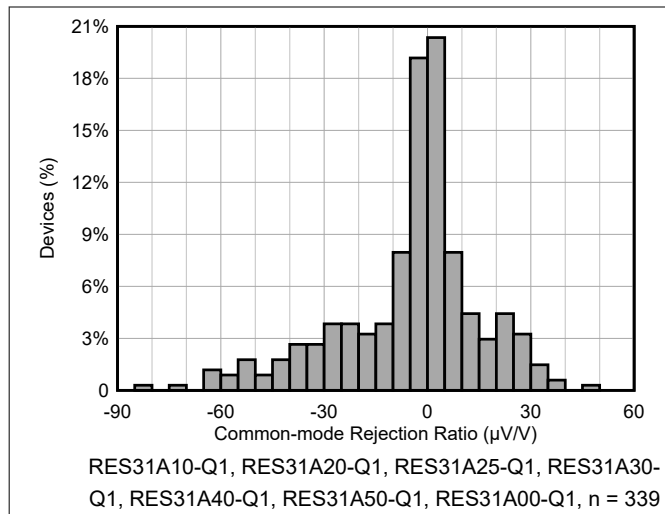


Figure 5-19. CMRR Distribution, All Ratios

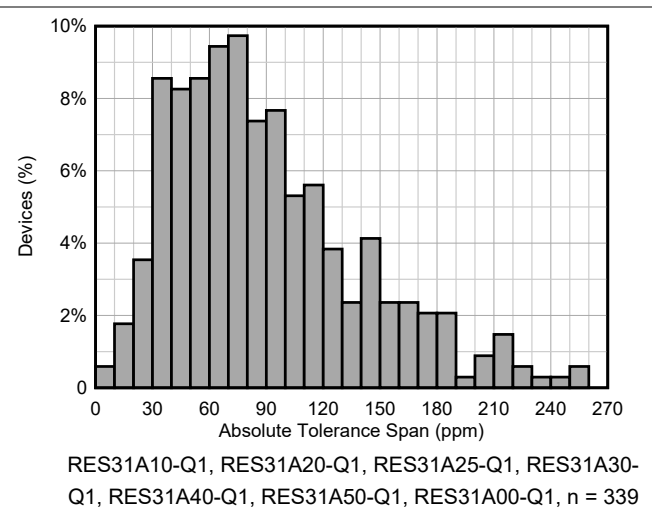


Figure 5-20. Absolute Tolerance Span Distribution, All Ratios

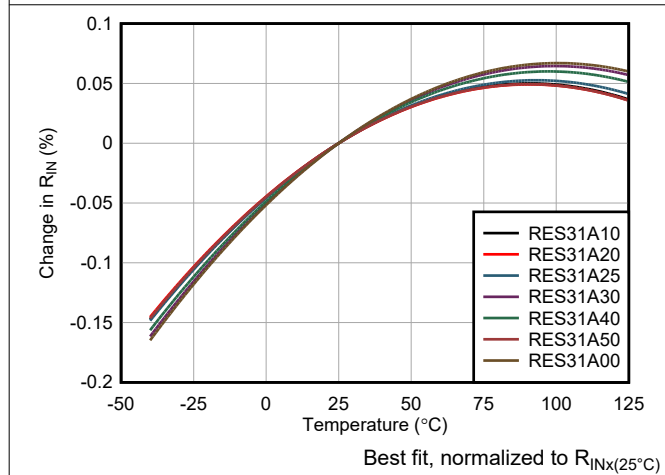


Figure 5-21. R_{INx} vs Temperature

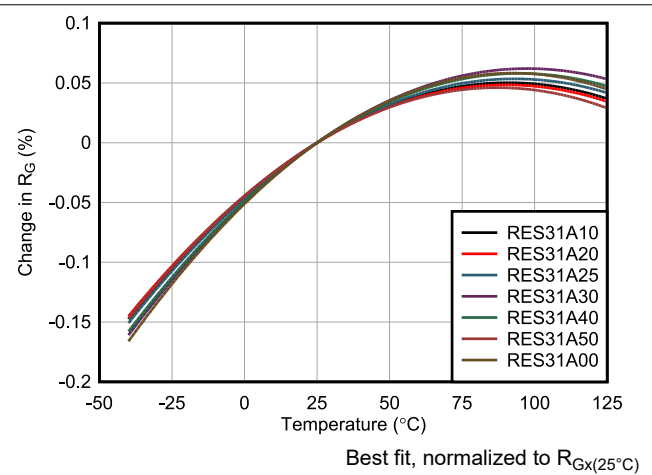


Figure 5-22. R_{Gx} vs Temperature

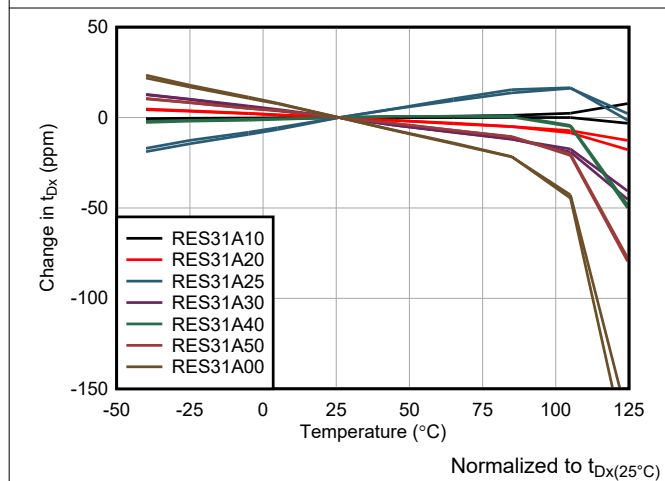


Figure 5-23. t_{Dx} vs Temperature

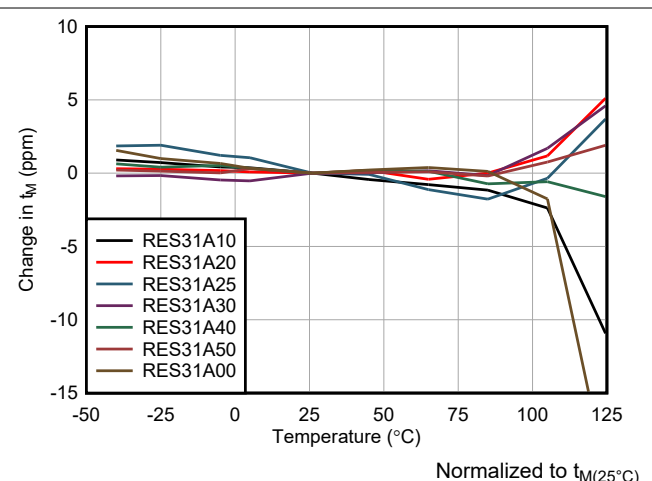
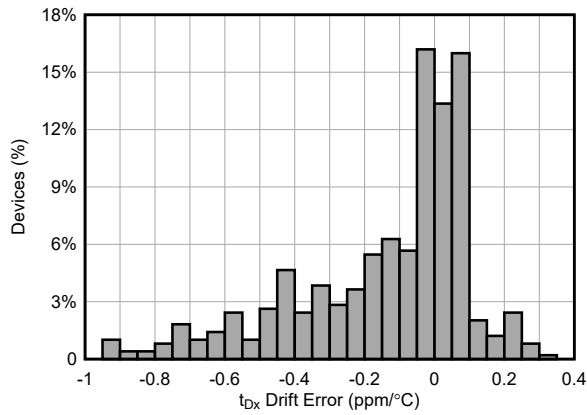


Figure 5-24. t_M vs Temperature

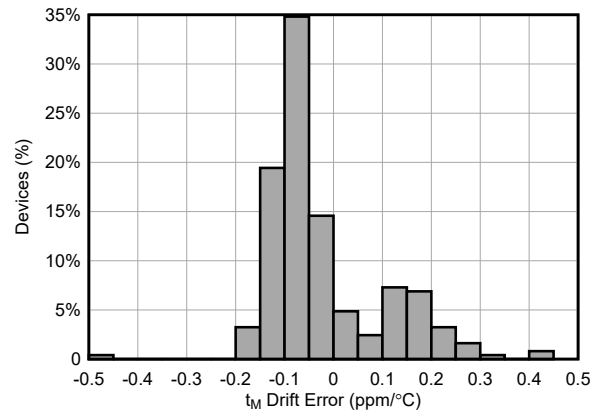
5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)



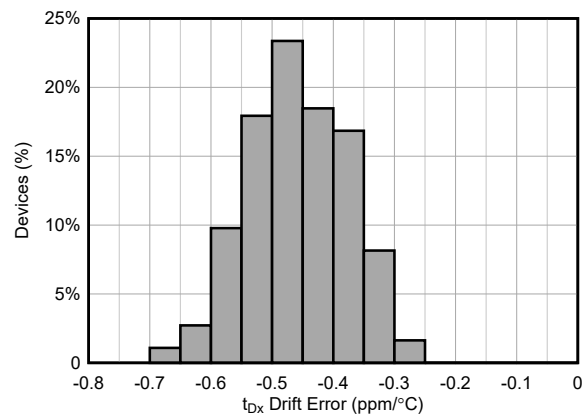
RES31A10-Q1, RES31A20-Q1, RES31A25-Q1, RES31A30-Q1, RES31A40-Q1, RES31A50-Q1, n = 494

Figure 5-25. $\text{TCR}_{\text{ratio}}$ Temperature Coefficient Distribution



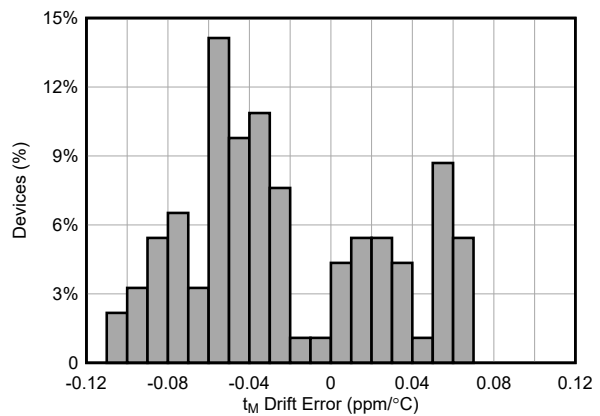
RES31A10-Q1, RES31A20-Q1, RES31A25-Q1, RES31A30-Q1, RES31A40-Q1, RES31A50-Q1, n = 247

Figure 5-26. TCR_M Temperature Coefficient Distribution



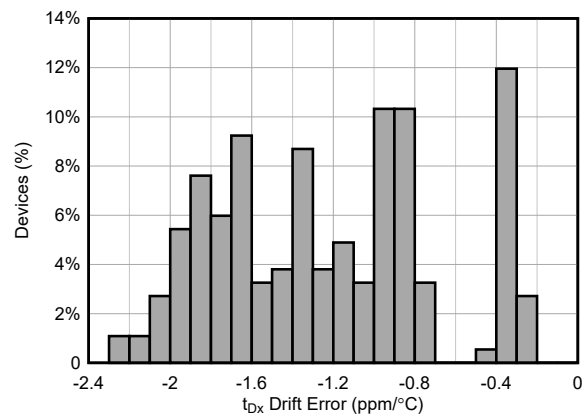
$T_A = -40\text{C to }+105^\circ\text{C}$ RES31A00-Q1, n = 184

Figure 5-27. RES31A00-Q1 $\text{TCR}_{\text{ratio}}$ Temperature Coefficient Distribution



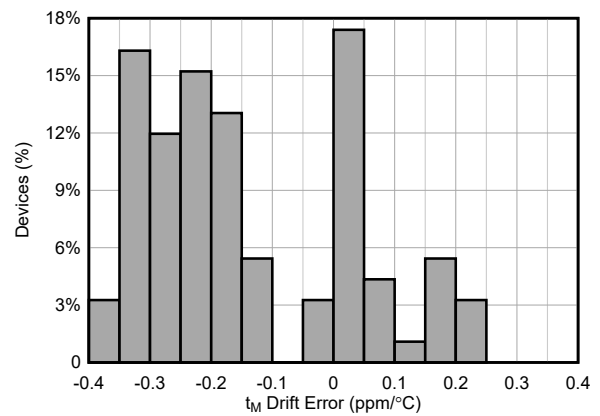
$T_A = -40\text{C to }+105^\circ\text{C}$ RES31A00-Q1, n = 92

Figure 5-28. RES31A00-Q1 TCR_M Temperature Coefficient Distribution



$T_A = -40\text{C to }+125^\circ\text{C}$ RES31A00-Q1, n = 184

Figure 5-29. RES31A00-Q1 $\text{TCR}_{\text{ratio}}$ Temperature Coefficient Distribution



$T_A = -40\text{C to }+125^\circ\text{C}$ RES31A00-Q1, n = 92

Figure 5-30. RES31A00-Q1 TCR_M Temperature Coefficient Distribution

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

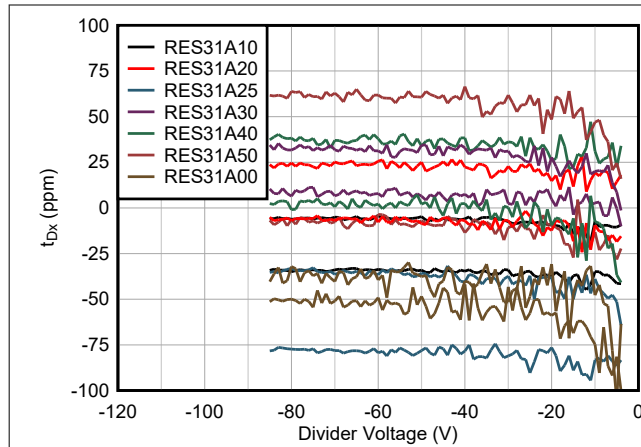


Figure 5-31. t_{Dx} vs Divider Voltage

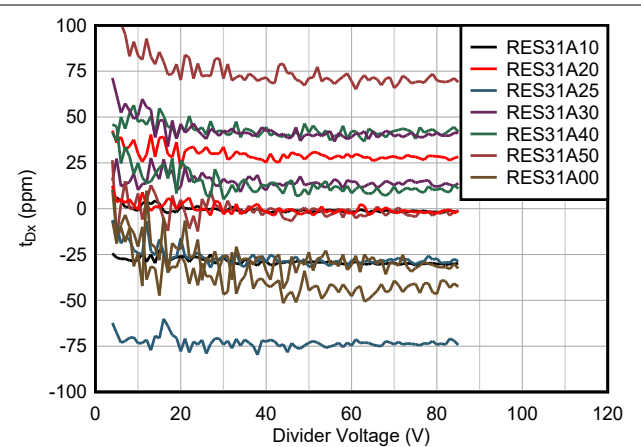


Figure 5-32. t_{Dx} vs Divider Voltage

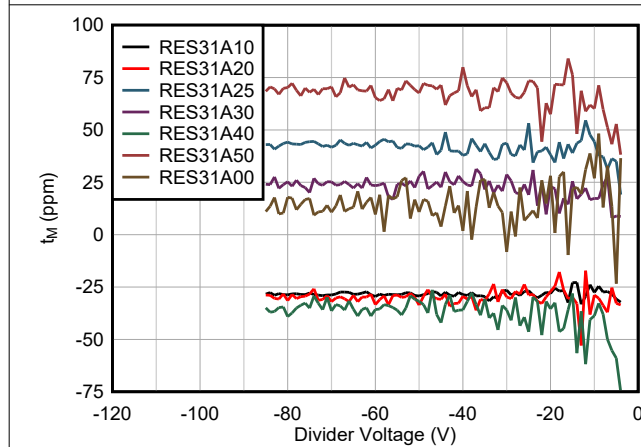


Figure 5-33. t_M vs Divider Voltage

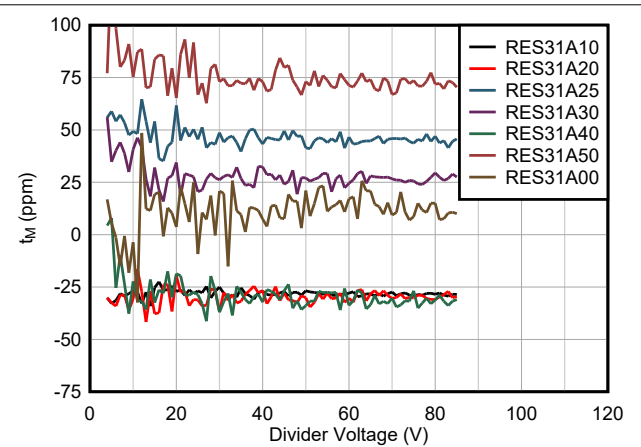


Figure 5-34. t_M vs Divider Voltage

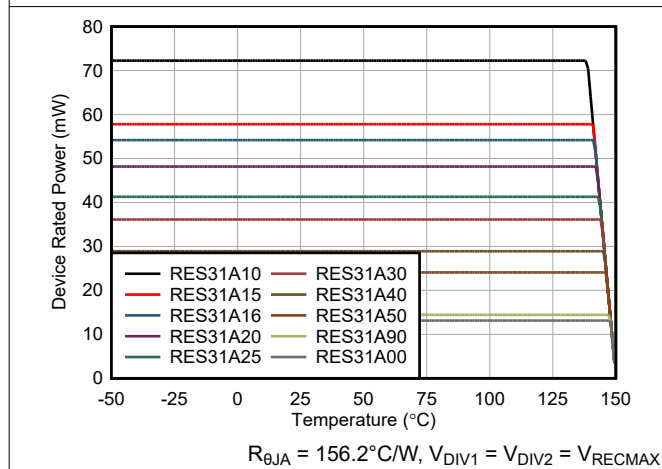


Figure 5-35. Device Rated Power vs Ambient Temperature

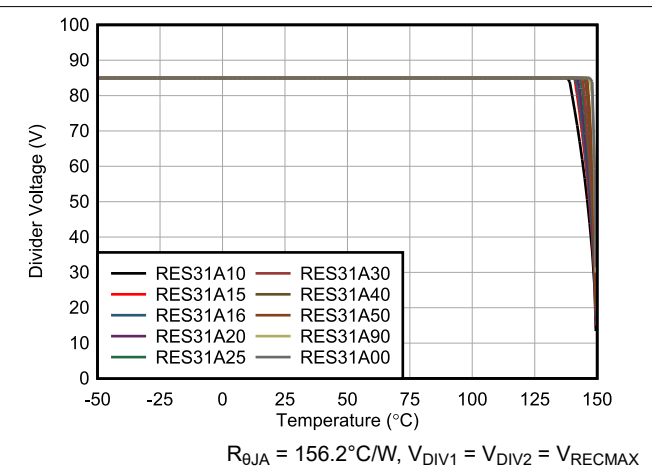


Figure 5-36. Maximum Recommended Divider Voltage vs Ambient Temperature

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

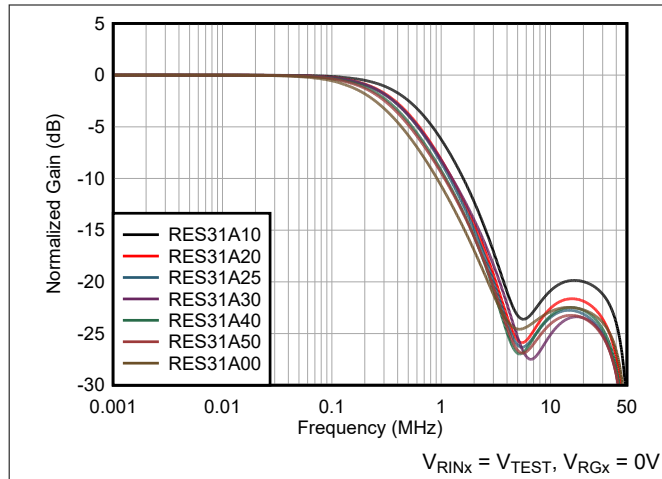


Figure 5-37. Bandwidth vs Frequency, R_{INx}

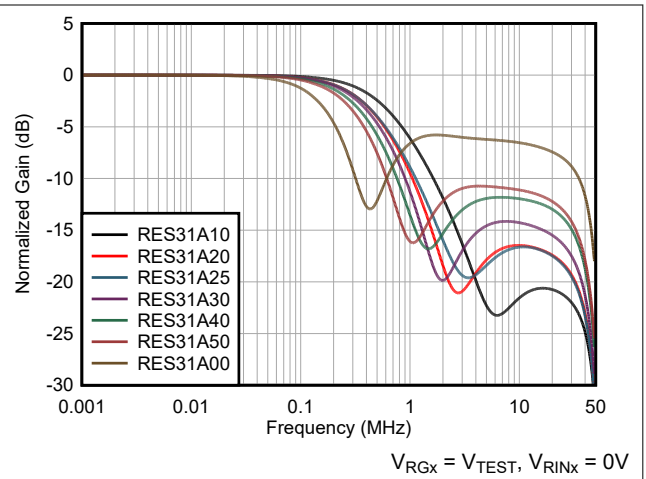


Figure 5-38. Bandwidth vs Frequency, R_{Gx}

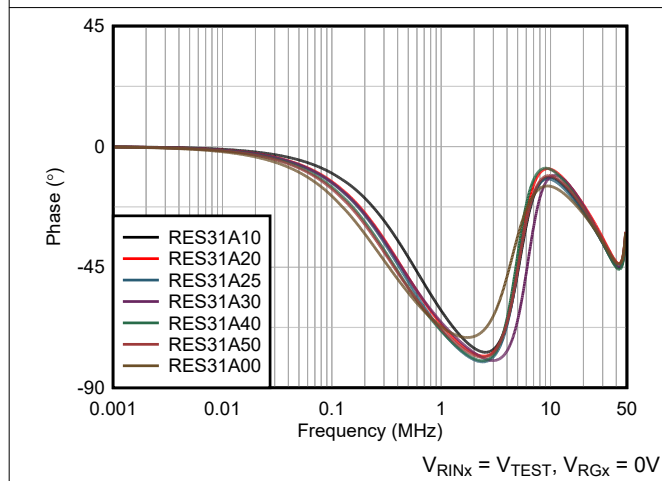


Figure 5-39. Phase vs Frequency, R_{INx}

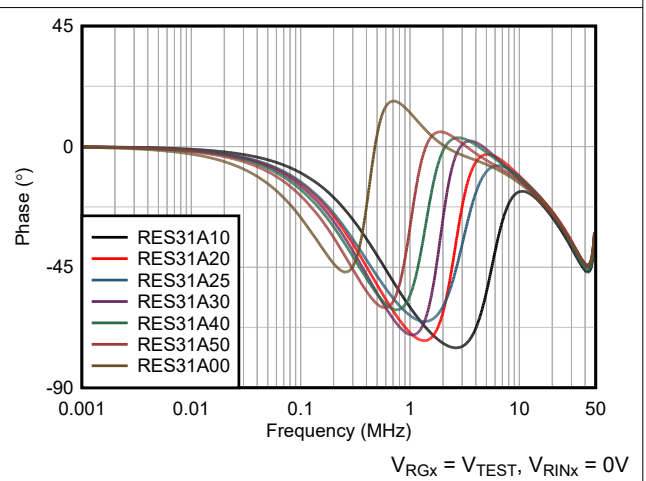


Figure 5-40. Phase vs Frequency, R_{Gx}

6 Parameter Measurement Information

6.1 DC Measurement Configurations

An example of the circuit configuration used for dc measurements is shown in [Figure 6-1](#). Voltage V_{Dx} refers to the voltage across a given divider, such as V_{D1} for divider 1. Voltage V_{Rx} refers to the voltage across a given resistor, such as V_{RIN1} for R_{IN1} or V_{RG1} for R_{G1} .

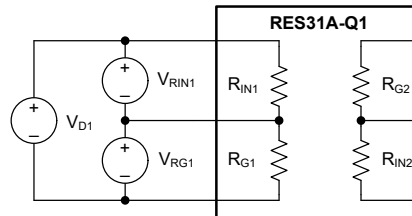


Figure 6-1. DC Measurement Terminology for Divider 1

When the RES31A-Q1 is used to set the gain of an op amp (shown in [Figure 6-2](#)), the ratio of the resistors in a divider sets the amplifier gain such that $V_{OUT} = -V_{IN} \times R_G / R_{IN}$. Discrete difference-amplifier and instrumentation-amplifier circuits are variations on this use case. Typical and maximum parameter values for ratio tolerance (t_{D1} , t_{D2}) are expressed in terms of R_{Gx} / R_{INx} to simplify calculations for these circuits. See [Section 7.3.1](#) for more detailed discussion of these error terms.

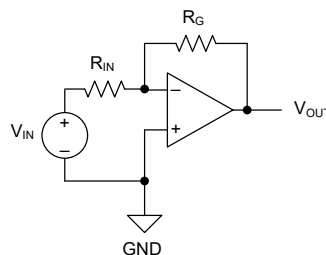


Figure 6-2. Amplifier Gain Circuit

Another valid use case of the RES31A-Q1 is a simple voltage divider. An example is shown in [Figure 6-3](#). For this implementation, the midpoint voltage V_{MID} is equal to the input voltage V_D multiplied by $R_{IN} / (R_{IN} + R_G)$.

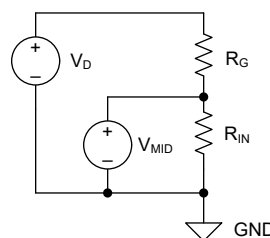


Figure 6-3. Voltage-divider circuit

While calculation of the error for a voltage divider use case is slightly more complex, the gain error of a voltage divider circuit constructed with the RES31A-Q1 is always *less* than that of an amplifier gain circuit implemented with the same device. Put another way, the values of t_{D1} or t_{D2} specified for the RES31A-Q1 in gain circuits are overly conservative for voltage-divider circuits. Refer to [Section 8.1.2](#) for detailed discussion and examples.

[Figure 6-4](#) shows the circuit configuration used for CMRR calculations. For an ideal amplifier with no offset and infinite CMRR, the effective circuit CMRR is entirely a function of the matching of the resistors. See [Section 8.1.3.1](#) and the [Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs](#) application note for more information.

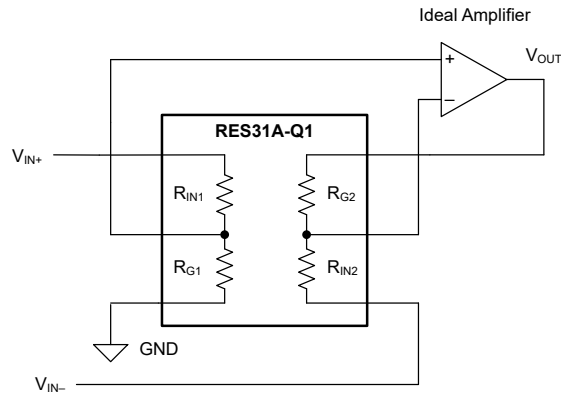


Figure 6-4. CMRR Calculation Reference Schematic

6.2 AC Measurement Configurations

Figure 6-5 shows the circuit configuration used for capacitance measurements. For the RES31A-Q1, a 1MΩ R_{KNOWN} resistance and 10pF C_{KNOWN} capacitance are used. The circuit creates an impedance divider; the resulting gain-vs-frequency relationship is used to calculate the parasitic capacitance in parallel with the resistor under test (in this case, R_{IN1}). Calibration with an empty socket is performed to account for board parasitics. The ac source is swept from 100Hz to 50MHz.

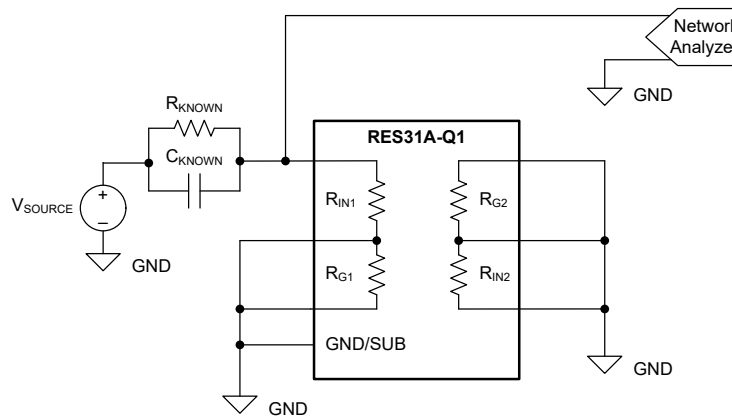


Figure 6-5. Capacitance Measurement Reference Schematic

Figure 6-6 shows the circuit configuration that is used for bandwidth measurements. The ac source is swept from 100kHz to 500MHz.

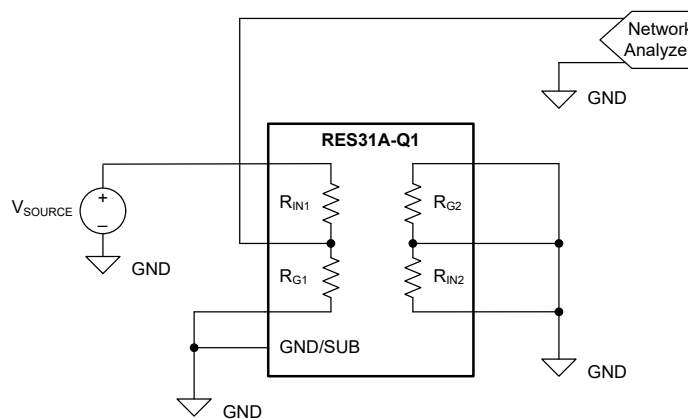


Figure 6-6. Bandwidth Measurement Reference Schematic

Figure 6-7 shows the circuit configuration used for crosstalk measurements. The ac source is swept from 100Hz to 100MHz.

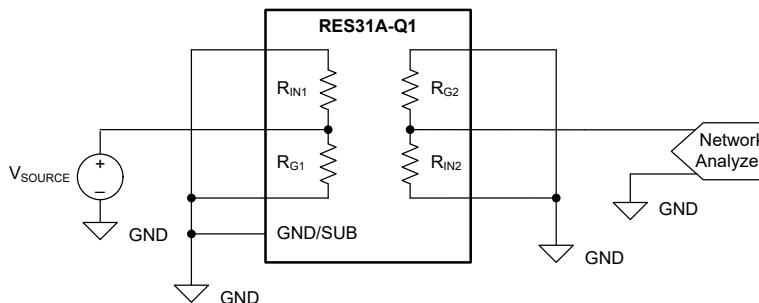


Figure 6-7. Crosstalk Measurement Reference Schematic

6.3 Error Notation and Units

This document uses the form

$$\text{Param}_{\text{actual}} = \text{Param}_{\text{nominal}} \times (1 + t_{\text{Param}}) \quad (1)$$

to describe the error of many of the RES31A-Q1 parameters in a *ratimetric* manner. This expression expands to

$$\text{Param}_{\text{actual}} = \text{Param}_{\text{nominal}} + (\text{Param}_{\text{nominal}} \times t_{\text{Param}}) \quad (2)$$

Thus, the difference or *absolute error* between the actual and nominal value of a given parameter is

$$\text{Param}_{\text{actual}} - \text{Param}_{\text{nominal}} = \text{Param}_{\text{nominal}} \times t_{\text{Param}} \quad (3)$$

$\text{Param}_{\text{actual}}$ shares the same units as $\text{Param}_{\text{nominal}}$, such as V/V or Ω/Ω when describing circuit gain, while t_{Param} is unitless by default. Because the error tolerances of the RES31A-Q1 are so low, t_{Param} errors are typically expressed in units of ppm, by multiplying the error by 10^6 . To convert t_{Param} from ppm back to a unitless decimal value for error calculations, divide the t_{Value} by 10^6 . Refer to [Section 7.3.1](#) for an example of this.

As many of the RES31A-Q1 error terms (such as gain error and gain temperature coefficients) scale according to the nominal gain, this notation provides a convenient way to standardize values across the various RES31A-Q1 ratios. When converting ratimetric errors to absolute errors (or vice versa) for error analysis calculations, be cautious of notation and remember to scale t_{Param} errors by $\text{Param}_{\text{nominal}}$ when appropriate. [Section 9.7](#) includes a list of the various error terms that appear throughout the document, and a summary or definition of each.

In some cases, such as when describing divider ratio or gain, the same equation applies to both divider 1 and divider 2. In this case, a notation of Param_x is used, where x is either 1 or 2. For example, when generically describing ratio error,

$$G_x = G_{\text{nom}} \times (1 + t_{Dx}) \quad (4)$$

For the ratio error of divider 2 specifically,

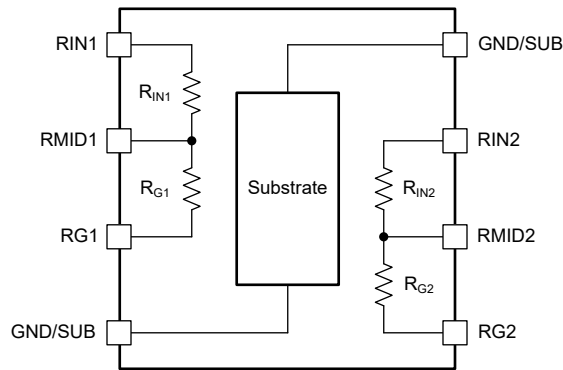
$$G_2 = G_{\text{nom}} \times (1 + t_{D2}) \quad (5)$$

7 Detailed Description

7.1 Overview

The RES31A-Q1 consists of four precision thin-film SiCr resistors, arranged to form two matched dividers. The device has two *input* resistors, R_{IN1} and R_{IN2} , both nominally 100k Ω . The device also has two *gain* resistors, R_{G1} and R_{G2} , with values that depend on the nominal ratio (R_{Gx} / R_{INx}) of the RES31A-Q1 device in question. The resistors are arranged with R_{IN1} and R_{G1} in series to form the first divider, and R_{IN2} and R_{G2} in series to form the second divider. Two GND pins are also provided to bias the device substrate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ratiometric Matching for Low Gain Error

The RES31A-Q1 is commonly used to establish the feedback path and set the gain of an amplifier circuit, or as a voltage divider to level-shift input signals. In both cases, the ratio of the resistors of the circuit describe the *nominal* circuit transfer function. Because the resistors of a given RES31A-Q1 are interdigitated and come from the same area of a silicon wafer, many of the absolute error terms of the resistors cancel out when calculating the *actual* or *effective* circuit transfer function. Detailed mathematical analyses and proofs are provided in [Section 7.3.1.1](#), but for most use cases, the error terms reported in *Electrical Characteristics* are directly used to calculate the associated maximum and typical circuit gain error.

The RES31A-Q1 is specified with a maximum *divider ratio tolerance* of 500ppm, effectively meaning that the relationship between the actual divider ratio G_x and nominal ratio G_{nom} of a given divider x is described by the following:

$$G_x = G_{nom} \times (1 + t_{Dx}) \quad (6)$$

such that $t_{Dx} \leq 500\text{ppm}$. For example, a RES31A40-Q1 has a nominal gain of $G_{nom} = 4$. If a particular unit has $t_{D1} = 130\text{ppm}$ and $t_{D2} = -40\text{ppm}$, the effective gains G_1 and G_2 are calculated as

$$G_1 = G_{nom} \times (1 + t_{D1}) = 4 \times (1 + 0.00013) = 4.00052 \quad (7)$$

$$G_2 = G_{nom} \times (1 + t_{D2}) = 4 \times (1 - 0.00004) = 3.99984 \quad (8)$$

The RES31A-Q1 is specified with a maximum *divider matching tolerance* of 1000ppm, meaning that the relationship between the ratio of divider 1 (G_1) and ratio of divider 2 (G_2) is described by the following:

$$t_M = t_{D2} - t_{D1} = \frac{G_2 - G_1}{G_{nom}} \quad (9)$$

By definition, $|t_M| \leq 1000\text{ppm}$. As a result of the interdigitated of the two dividers, the actual typical magnitude of t_M is about an order of magnitude less than this maximum value, depending on the specific RES31A-Q1 device. This value is used to approximate the common-mode rejection ratio (CMRR) when implementing a difference

amplifier circuit. For example, typical t_M for the RES31A40-Q1 is approximately 58ppm, and the typical CMRR is 97.1dB.

7.3.1.1 Absolute and Ratiometric Tolerances

The resistors of the RES31A-Q1 are described by the following equations:

$$R_{IN1} = R_{INnom} \times (1+t_{absRIN1}) = R_{INnom} \times (1+t_{RIN1}) \times (1+t_{SiCr}) \quad (10)$$

$$R_{IN2} = R_{INnom} \times (1+t_{absRIN2}) = R_{INnom} \times (1+t_{RIN2}) \times (1+t_{SiCr}) \quad (11)$$

$$R_{G1} = R_{Gnom} \times (1+t_{absRG1}) = R_{Gnom} \times (1+t_{RG1}) \times (1+t_{SiCr}) \quad (12)$$

$$R_{G2} = R_{Gnom} \times (1+t_{absRG2}) = R_{Gnom} \times (1+t_{RG2}) \times (1+t_{SiCr}) \quad (13)$$

R_{INnom} and R_{Gnom} are the nominal values of each resistor. The parameter t_{abs} is an error term that describes the absolute tolerance of the RES31A-Q1 resistor in question, such that $|t_{abs}| \leq 12\%$. For example, a nominally 100k Ω resistor with $t_{abs} = 10\%$ actually measures 110k Ω . This error is analogous to the specified *absolute tolerance* of most single-element resistors, or the end-to-end tolerance of more specialized resistor dividers.

Note

The RES31A-Q1 is not a laser-trimmed device. Each ratio of the RES31A-Q1 features a unique die specifically optimized for that ratio, providing the precise matching and consistent thermal characteristics necessary to achieve extremely low drift.

The absolute tolerance is dominated by the variation in the SiCr resistivity, t_{SiCr} . The four resistors of a given RES31A-Q1 are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for each of the four resistors, although t_{SiCr} varies on a part-to-part basis.

The following examples show that when each divider is considered in ratiometric terms, the t_{SiCr} error terms drop out. Parameter t_{Rx} is a residual error term that describes the remaining effective tolerance of each resistor of the given RES31A-Q1 device after accounting for the universal t_{SiCr} .

$$\frac{R_{Gx}}{R_{INx}} = \frac{R_{Gnom} \times (1+t_{RGx}) \times (1+t_{SiCr})}{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr})} = \frac{R_{Gnom} \times (1+t_{RGx})}{R_{INnom} \times (1+t_{RINx})} = G_{nom} \times \frac{(1+t_{RGx})}{(1+t_{RINx})} = G_x \quad (14)$$

$$\frac{R_{INx}}{R_{INx} + R_{Gx}} = \frac{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr})}{R_{INnom} \times (1+t_{RINx}) \times (1+t_{SiCr}) + R_{Gnom} \times (1+t_{RGx}) \times (1+t_{SiCr})} = \frac{R_{INnom} \times (1+t_{RINx})}{R_{INnom} \times (1+t_{RINx}) + R_{Gnom} \times (1+t_{RGx})} \quad (15)$$

The individual values of t_{RG1} , t_{RG2} , t_{RIN1} , and t_{RIN2} describe the tolerance of each individual resistor, but are not independent variables in a Gaussian sense. Rather, the matching of these values to each other (by design) is used to achieve highly stable ratiometric relationships between the resistors, giving an effective *ratio* with an extremely low error.

The limits of t_{Dx} for the RES31A-Q1 are enforced by precise parametric testing in production, with Kelvin connections used to better reject potential sources of error. Because the resulting t_{D1} and t_{D2} values are more randomized error terms, t_{D1} and t_{D2} can be treated as independent Gaussian distributions, making these variables much more useful for error analyses. Single-element resistors do not have an equivalent to t_{Dx} , because no part-to-part matching is considered other than the gradeout limit. In other divider data sheets, the equivalent of t_{Dx} is often called *ratio tolerance*.

Because any devices that do not meet these criteria are screened out at final test, these equations can technically be used with Equation 14 to prove additional relationships (such as effective maximum limits) between the values of t_{Rx} for a given device. This exercise ultimately gives overly conservative results, however. For more realistic statistical analysis with root-sum-of-squares methods, the *Arbitrary Matching* section of the *Electrical Characteristics* table provides measured standard deviations for some additional resistor-to-resistor relationships. See Section 8.1.3.2 for a practical example.

7.3.2 Ratiometric Drift

The ratiometric matching of the RES31A-Q1 provides a benefit not just for initial conditions, but also when considering parametric drift. The resistors must be considered individually, in absolute terms, and ratiometrically to each other, in matched terms. The absolute temperature coefficients of each resistor show strong correlation, with the coefficient of R_{IN1} comparable to that of R_{IN2} and the coefficient of R_{G1} comparable to that of R_{G2} . The absolute temperature coefficient (in $\Omega/^\circ\text{C}$) of each R_G is approximately G_{nom} times greater than that of the comparable R_{IN} ; therefore, the normalized absolute temperature coefficient (in ppm/ $^\circ\text{C}$) of every resistor is approximately the same.

The resistors of the RES31A-Q1 are interdigitated, and occupy a small footprint; thus, the die temperature of the device is effectively common to each of the four resistors. As the temperature changes, each resistor experiences a similar temperature rise. The resistors have very similar temperature coefficients; therefore, the ratio of R_G to R_{IN} is well preserved. For example, the RES31A40-Q1 has a typical absolute temperature coefficient of approximately 12ppm/ $^\circ\text{C}$ for R_{IN} or R_G . When considered in ratiometric terms, the typical temperature coefficient of t_{D1} or t_{D2} is $\pm 0.2\text{ppm}/^\circ\text{C}$, and the temperature coefficient of t_M is $\pm 0.05\text{ppm}/^\circ\text{C}$. Ambient temperature, humidity, heatsinking, board cleanliness, and other related factors can impact the settling time of the RES31A-Q1, so validation testing is performed in a low-humidity environment with rigorous board cleaning procedures.

7.3.3 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or $1/f$ noise, is extremely important for systems that require signal gain at frequencies less than 100Hz. The flicker noise for thin-film resistors, including the RES31A-Q1, is lower than that of thick-film resistor processes. Thermal noise typically dominates in the region greater than 1kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES31A-Q1, the thermal noise as measured at the center tap of two resistors R_{IN} and R_G is equivalent to the thermal noise of a resistor with value $R_{IN} \parallel R_G$:

$$e_N = \sqrt{(4k_B T R)} \quad (16)$$

where:

- e_N is the thermal noise density in nV/ $\sqrt{\text{Hz}}$
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, $1.381 \times 10^{-23}\text{J/K}$
- $R = R_{IN} \parallel R_G$

As an example, for the RES31A40-Q1 at 25 $^\circ\text{C}$:

$$e_N = \sqrt{(4k_B T R)} = \sqrt{4 \times 1.38\text{E}^{-23}\frac{\text{J}}{\text{K}} \times 278\text{K} \times (100\text{k}\Omega \parallel 400\text{k}\Omega)} = 35.1\text{nV}/\sqrt{\text{Hz}} \quad (17)$$

7.4 Device Functional Modes

The RES31A-Q1 is typically used with two independently biased resistor dividers. R_{IN1} and R_{G1} in series form a resistive divider, with R_{IN2} and R_{G2} in series forming another divider. However, the two dividers do not have to be used independently. The resistors can be connected in series or in parallel like any other resistor.

Use one of the two GND pins to bias the part substrate. Connect the substrate to signal ground or a similar low-impedance bias point or plane for best noise rejection. While two GND/SUB connection pins are available on the device, connect only *one* of these to the ground plane. The two GND pins are internally connected through the substrate, which is not intended to conduct significant currents. Connect only *one* GND pin at a time and leave the other pin floating to prevent current return paths from developing through the substrate.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Amplifier Feedback Circuit

The RES31A-Q1 is typically used to implement the feedback path of an operational amplifier, and thus set the circuit gain. This circuit is configured as either *inverting* or *noninverting*, with the input voltage being applied to that respective amplifier input, and is generically drawn in the following figure.

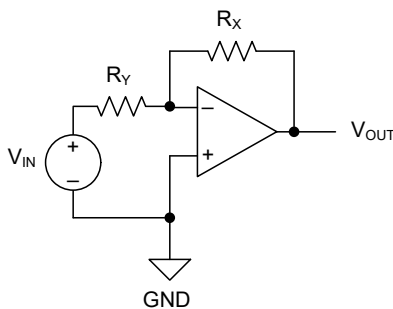


Figure 8-1. Inverting Amplifier Configuration

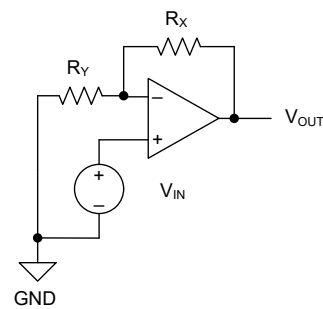


Figure 8-2. Noninverting Amplifier Configuration

For the inverting circuit configuration:

$$G_{\text{Inv}} = \frac{R_X}{R_Y} \quad (18)$$

$$V_{\text{OUT}} = -V_{\text{IN}} \times G_{\text{Inv}} \quad (19)$$

For the noninverting circuit configuration:

$$G_{\text{Noninv}} = 1 + \frac{R_X}{R_Y} \quad (20)$$

$$V_{\text{OUT}} = V_{\text{IN}} \times G_{\text{Noninv}} \quad (21)$$

Typically, $R_X = R_G$ and $R_Y = R_{\text{IN}}$, allowing noninverting gains from 2 to 11 to be achieved. Inverting gains range in this configuration from -1 to -10 . More unique configurations are also possible; see also [Section 8.1.6.2](#).

$$G_x = G_{\text{nom}}(1 + t_{\text{Dx}}) \quad (22)$$

8.1.1.1 Amplifier Feedback Circuit Example

Consider the following example. Divider 1 of the RES31A-Q1 is used in an inverting configuration, and divider 2 is used in a noninverting configuration. Both channels have the same input signal V_{IN} , but the circuits have differing transfer functions of $V_{OUT1} = V_{IN} \times (-G_1)$ and $V_{OUT2} = V_{IN} \times (1 + G_2)$.

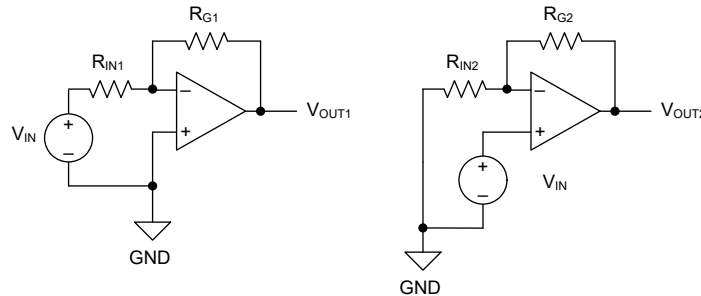


Figure 8-3. Amplifier Gain Example Circuit

The following table shows the calculated results for several example conditions to illustrate the effects of the various errors. The impact of amplifier offset or input bias currents on V_{OUTx} is not considered. Each row represents a different hypothetical condition for V_{IN} , G_{nom} , t_{D1} , and t_{D2} .

Table 8-1. Amplifier Gain Example Circuit Conditions, Using RES31A-Q1

V_{IN}	G_{nom}	t_{D1}	t_{D2}	G_1	G_2	V_{OUT1}	V_{OUT2}
1V	4	0ppm	0ppm	4	4	-4V	5V
1V	4	100ppm	-10ppm	4.00040	3.99996	-4.00040	4.99996
1V	4	40ppm	-80ppm	4.00016	3.99968	-4.00016	4.99968
1V	4	-80ppm	40ppm	3.99968	4.00016	-3.99968	5.00016
-2V	1.667	0ppm	0ppm	1.66667	1.66667	3.33333	-5.33333
-2V	1.667	100ppm	-10ppm	1.66683	1.66665	3.33367	-5.33330
-2V	1.667	40ppm	-80ppm	1.66673	1.66653	3.33347	-5.33307
-2V	1.667	-80ppm	40ppm	1.66653	1.66673	3.33307	-5.33347

8.1.2 Voltage Divider Circuit

As alluded in [Section 6.1](#), the RES31A-Q1 is typically used as an input signal level-shifter or voltage divider. This circuit is generically drawn in the following figure.

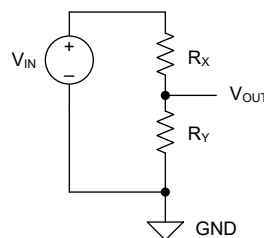


Figure 8-4. Generic Voltage Divider Circuit

$$G_{VD} = \frac{R_Y}{R_Y + R_X} \quad (23)$$

$$V_{OUT} = V_{IN} \times G_{VD} \quad (24)$$

$$G_{VDx} = G_{VD_{nom}}(1 + t_{VDx}) \quad (25)$$

Often, R_G and R_{IN} act as R_X and R_Y respectively in this circuit. Substituting these terms gives a transfer function of:

$$G_{VDx} = \frac{R_{INx}}{R_{INx} + R_{Gx}} = \frac{1}{G_x + 1} \quad (26)$$

Because G_{VDx} is a direct function of G_x , the ratio tolerance error t_{VDx} of these voltage-divider circuits is a direct function of t_{Dx} . Typical and maximum parameter values for t_{VDx} in this configuration are calculated from a given t_{Dx} value as follows:

$$t_{VDx} = \frac{-G_{nom} \times t_{Dx}}{G_{nom} \times t_{Dx} + G_{nom} + 1} \quad (27)$$

For example, if a RES31A40-Q1 with $t_{D1} = 130\text{ppm}$ is used in this configuration, the associated t_{VD1} error is -104ppm . The sign change occurs because a positive t_{Dx} error means $R_G > R_{Gnom}$ or $R_{IN} < R_{INnom}$. Since the resulting G_{VDx} is less than the nominal value, the error term is negative.

For the alternative case where the positions of R_G and R_{IN} are swapped, such that $R_X = R_{IN}$ and $R_Y = R_{IN}$, the transfer function is:

$$G_{VDx} = \frac{R_{Gx}}{R_{INx} + R_{Gx}} = \frac{G_x}{G_x + 1} \quad (28)$$

The error of this transfer function is described by:

$$t_{VDx} = \frac{t_{Dx}}{G_{nom} \times t_{Dx} + G_{nom} + 1} \quad (29)$$

If the same RES31A40-Q1 with $t_{D1} = 130\text{ppm}$ is used in this alternative configuration, the associated t_{VD1} error is 26ppm . A sign change does not occur because a positive t_{Dx} error means $R_G > R_{Gnom}$ or $R_{IN} < R_{INnom}$. Because the result G_{VDx} is greater than the nominal value, the error term is again positive.

8.1.2.1 Voltage Divider Circuit Example

Consider the following example. Dividers 1 and 2 of the RES31A-Q1 are both arranged as voltage dividers, but the relative positions of R_{G1} and R_{IN2} are swapped, as are the positions of R_{IN1} and R_{G2} . Both channels have the same input signal V_{IN} , but have differing transfer functions of $V_{OUT1} = V_{IN} \times G_1 / (1 + G_1)$ and $V_{OUT2} = V_{IN} \times 1 / (1 + G_2)$.

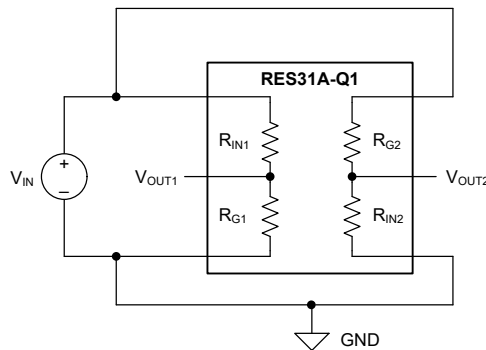


Figure 8-5. Voltage Divider Example Circuit

The following tables show the calculated results for several examples to illustrate the effects of the various errors. Each row in the tables represents a different hypothetical condition. The final rows of each table show the results when substituting the absolute maximum and minimum limits of t_{Dx} . The *final percent error* E_{OUTx} is calculated as:

$$E_{OUTx} = \frac{V_{OUTx} - V_{OUTnom}}{V_{OUTnom}} \quad (30)$$

Table 8-2. Calculated Errors for Voltage Divider Example, Divider 1

V _{IN}	G _{nom}	G _{VDnom}	V _{OUT1nom}	t _{D1}	t _{VD1}	G _{VD1}	V _{OUT1}	E _{OUT1}
5V	4	1/5	1V	60ppm	-48ppm	0.19999	0.99995	-48ppm
5V	4	1/5	1V	-80ppm	64ppm	0.20001	1.00006	64ppm
10V	4	1/5	2V	60ppm	-48ppm	0.19999	1.99990	-48ppm
10V	4	1/5	2V	-80ppm	64ppm	0.20001	2.00013	64ppm
10V	4	1/5	2V	500ppm	-400ppm	0.19992	1.99920	-400ppm
10V	4	1/5	2V	-500ppm	400ppm	0.20008	2.00080	400ppm

Table 8-3. Calculated Errors for Voltage Divider Example, Divider 2

V _{IN}	G _{nom}	G _{VDnom}	V _{OUT2nom}	t _{D2}	t _{VD2}	G _{VD2}	V _{OUT2}	E _{OUT2}
5V	4	4/5	4V	75ppm	15ppm	0.80001	4.00006	15ppm
5V	4	4/5	4V	-130ppm	-26ppm	0.79998	3.99990	-26ppm
10V	4	4/5	8V	75ppm	15ppm	0.80001	8.00012	15ppm
10V	4	4/5	8V	-130ppm	-26ppm	0.79998	7.99979	-26ppm
10V	4	4/5	8V	500ppm	100ppm	0.80008	8.00080	100ppm
10V	4	4/5	8V	-500ppm	-100ppm	0.79992	7.99920	-100ppm

As the examples show, the final error E_{OUTx} of the transfer function for each divider is equivalent to the corresponding effective voltage divider error t_{VDx}. In all cases, the magnitude of t_{VDx} is less than the magnitude of t_{Dx}.

8.1.2.2 Voltage-Divider Circuit Drift

As discussed in Section 8.1.2, the voltage-divider circuit error t_{VDx} of the RES31A-Q1 is related to the gain-circuit error t_{Dx} by one of the two following expressions (depending on the placement of R_G and R_{IN}):

$$G_{VDx} = \frac{R_{INx}}{R_{INx} + R_{Gx}} = G_{VDnom}(1 + t_{VDx}) \rightarrow t_{VDx} = \frac{-G_{nom} \times t_{Dx}}{G_{nom} \times t_{Dx} + G_{nom} + 1} \quad (31)$$

$$G_{VDx} = \frac{R_{Gx}}{R_{INx} + R_{Gx}} = G_{VDnom}(1 + t_{VDx}) \rightarrow t_{VDx} = \frac{t_{Dx}}{G_{nom} \times t_{Dx} + G_{nom} + 1} \quad (32)$$

Therefore, the change in the voltage divider transfer function G_{VDx} with temperature is a direct function of the change in t_{Dx} with temperature. Multiplying the temperature coefficient TCR_{ratio} by the change in ambient temperature gives the change in t_{Dx}, which is in turn substituted in the appropriate equation above to calculate the change in t_{VDx}. The change in t_{VDx} directly describes the change in G_{VDx}.

As an example, consider a RES31A40-Q1 with G_{nom} = 4 and a circuit configuration as shown in Figure 8-4, with R_X = R_{G1} and R_Y = R_{IN1}. Assume t_{D1} is initially 85ppm and increases by 5ppm due to a 25°C increase in ambient temperature. The initial value of t_{VD1}, before the temperature change, is calculated as:

$$t_{VD1} = \frac{-G_{nom} \times t_{D1}}{G_{nom} \times t_{D1} + G_{nom} + 1} = \frac{-4 \times 0.000085}{4 \times 0.000085 + 4 + 1} = -0.000068 = -68ppm \quad (33)$$

The new value of t_{VD1} after the temperature change is calculated as:

$$t_{VD1} = \frac{-G_{nom} \times t_{D1}}{G_{nom} \times t_{D1} + G_{nom} + 1} = \frac{-4 \times 0.000090}{4 \times 0.000090 + 4 + 1} = -0.000072 = -72ppm \quad (34)$$

In this first scenario, the shift in t_{D1} of 5ppm causes a shift in t_{VD1} of -4ppm.

If the circuit configuration is inverted so that $R_X = R_{IN1}$ and $R_Y = R_{G1}$, then the initial value of t_{VD1} is calculated as:

$$t_{VD1} = \frac{t_{D1}}{G_{nom} \times t_{D1} + G_{nom} + 1} = \frac{0.000085}{4 \times 0.000085 + 4 + 1} = 0.000017 = 17\text{ppm} \quad (35)$$

The new value of t_{VD1} after the temperature change is calculated as:

$$t_{VD1} = \frac{t_{D1}}{G_{nom} \times t_{D1} + G_{nom} + 1} = \frac{0.000090}{4 \times 0.000090 + 4 + 1} = 0.000018 = 18\text{ppm} \quad (36)$$

In this second scenario, the shift in t_{D1} of 5ppm causes a shift in t_{VD1} of only 1ppm.

8.1.3 Discrete Difference Amplifier

The RES31A-Q1 is commonly used to implement a simple difference amplifier. The ratiometric matching between the two resistor dividers improves CMRR performance and gain drift for the circuit, when compared to a similar implementation using unmatched discrete resistors. The basic circuit is shown in [Figure 8-6](#).

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_G}{R_{IN}}\right) + V_{REF} \quad (37)$$

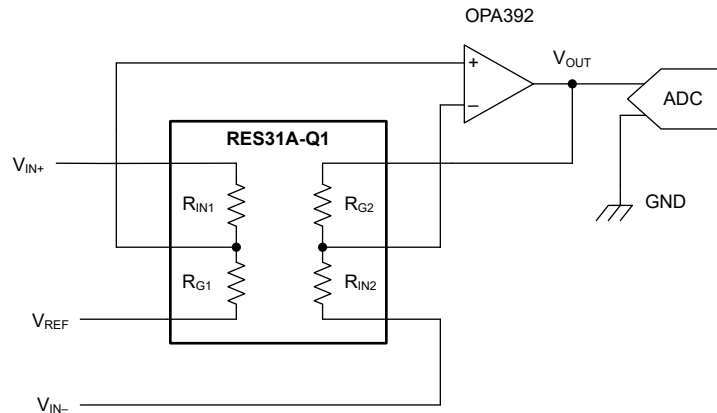


Figure 8-6. Discrete Difference Amplifier Using RES31A-Q1

8.1.3.1 Difference-Amplifier Common-Mode Rejection Analysis

In this simple difference amplifier configuration, the nominal CMRR is calculated as:

$$\text{CMRR} = 20 \times \log_{10} \left(\left| \frac{A_D}{A_{CM}} \right| \right) \quad (38)$$

The term A_D is the differential gain of the circuit, and the term A_{CM} is the common-mode gain of the circuit. These are defined as the following:

$$A_D \times = \frac{V_{OUT}}{V_D} = 0.5 \times \frac{\left(\frac{R_{G1}}{R_{G1} + R_{IN1}}\right) + \left(\frac{R_{G2}}{R_{G2} + R_{IN2}}\right)}{\left(\frac{R_{IN2}}{R_{G2} + R_{IN2}}\right)} \quad (39)$$

$$A_{CM} = \frac{V_{OUT}}{V_{CM}} = \frac{\left(\frac{R_{G1}}{R_{G1} + R_{IN1}}\right) - \left(\frac{R_{G2}}{R_{G2} + R_{IN2}}\right)}{\left(\frac{R_{IN2}}{R_{G2} + R_{IN2}}\right)} \quad (40)$$

Therefore,

$$\text{CMRR} = 20 \times \log_{10} \left(\left| 2 \times \frac{R_{G1} \times (R_{IN2} + R_{G2}) - R_{G2} \times (R_{IN1} + R_{G1})}{R_{G1} \times (R_{IN2} + R_{G2}) + R_{G2} \times (R_{IN1} + R_{G1})} \right| \right) \quad (41)$$

When this expression is evaluated with the definitions given in [Section 7.3.1](#), assuming the worst-case scenario of the most unbalanced divider matching possible,

$$\text{CMRR} = 20 \times \log_{10} \left(\left| \frac{G_{\text{nom}} + 1 + t_{R_x}^2 (1 - G_{\text{nom}})}{4 \times t_{R_x}} \right| \right) \quad (42)$$

$t_{R_x}^2 \ll 1$; therefore, the worst-case CMRR is approximated as:

$$\text{CMRR} = 20 \times \log_{10} \left(\left| \frac{G_{\text{nom}} + 1}{4 \times t_{R_x}} \right| \right) \quad (43)$$

By definition, the parameter t_M describes the effective error that is otherwise equivalent to $4 \times t_x$ for an unmatched divider network, and so the maximum value of t_M can be used to calculate the same worst-case result. Likewise, the typical value of t_M can be used to approximate the typical CMRR.

$$\text{CMRR} = 20 \times \log_{10} \left(\left| \frac{G_{\text{nom}} + 1}{t_M} \right| \right) \quad (44)$$

For example, the worst-case CMRR for a RES31A40-Q1 device with $G = 4$ is approximately 74.0dB, with a typical CMRR of approximately 97.1dB. In comparison, implementation of a comparable $G = 4$ difference amplifier with unmatched 0.1%-tolerance resistors results in a worst-case CMRR of approximately 62dB.

In a difference amplifier configuration, the CMRR of the op amp contributes error as well. The op-amp CMRR is considered in parallel with the CMRR of the resistor network, as per the following equation:

$$\frac{1}{\text{CMRR}_{\text{TOTAL}}} = \frac{1}{\text{CMRR}_{\text{AMP}}} + \frac{1}{\text{CMRR}_{\text{RESISTORS}}} \quad (45)$$

Additional mismatches in the divider end-to-end resistances reduce the effective CMRR of a difference amplifier. While the low absolute tolerance span of the RES31A-Q1 (140ppm typical) helps reduce these concerns, parasitic trace resistances can lead to additional mismatches that impact the CMRR specs.

8.1.3.2 Difference-Amplifier Gain Error Analysis

The transfer function [Equation 37](#) assumes that $R_{G1} = R_{G2}$ and $R_{IN1} = R_{IN2}$. Without this assumption, the transfer function of the difference amplifier is better described by the following:

$$V_{\text{OUT}} = V_{\text{IN}+} \times \left(\frac{R_{G1}}{R_{G1} + R_{IN1}} \right) \left(\frac{R_{G2} + R_{IN2}}{R_{IN2}} \right) - V_{\text{IN}-} \times \left(\frac{R_{G2}}{R_{IN2}} \right) + V_{\text{REF}} \quad (46)$$

If the end-to-end values of $R_{G2} + R_{IN2}$ and $R_{G1} + R_{IN1}$ are sufficiently matched, the correspond terms cancel out in the above equation. The *end-to-end mismatch* specification of the RES31A-Q1 describes the typical error of this in *ratimetric* terms; for brevity, this error term is denoted as t_{E2E} .

$$\frac{R_{G2} + R_{IN2}}{R_{G1} + R_{IN1}} = 1 + t_{E2E} \quad (47)$$

$$V_{\text{OUT}} = V_{\text{IN}+} \times \left(\frac{R_{G1}}{R_{IN2}} \right) (1 + t_{E2E}) - V_{\text{IN}-} \times \left(\frac{R_{G2}}{R_{IN2}} \right) + V_{\text{REF}} \quad (48)$$

The ratio error of R_{G2} / R_{IN2} is described by t_{D2} . The ratio error of R_{G1} / R_{IN2} is described by the *R_G mismatch between dividers*, *ratimetric* specification; for brevity, this error term is denoted as t_{D2D} .

$$\frac{R_{G2}}{R_{IN2}} = (1 + t_{D2}) \times G_{\text{nom}} \quad (49)$$

$$\frac{R_{G2}}{R_{IN1}} = (1 + t_{D2D}) \times G_{nom} \quad (50)$$

The effective transfer function is thus

$$V_{OUT} = V_{IN+} \times G_{nom} \times (1 + t_{E2E})(1 + t_{D2D}) - V_{IN-} \times G_{nom} \times (1 + t_{D2}) + V_{REF} \quad (51)$$

For further analysis, the input voltages V_{IN+} and V_{IN-} are first expressed as a common-mode input voltage (V_{CM}) and a differential input voltage (V_{DIFF}).

$$V_{CM} = \frac{(V_{IN+} + V_{IN-})}{2} \quad (52)$$

$$V_{DIFF} = V_{IN+} - V_{IN-} \quad (53)$$

Equation 51 is expressed in terms of V_{CM} and V_{DIFF} as

$$V_{OUT} = V_{CM} \times \left(\frac{\frac{R_{G1}}{R_{IN1} + R_{G1}} - \frac{R_{G2}}{R_{IN2} + R_{G2}}}{\frac{R_{IN2}}{R_{IN2} + R_{G2}}} \right) + V_{DIFF} \times \left(\frac{\frac{R_{G1}}{R_{IN1} + R_{G1}} + \frac{R_{G2}}{R_{IN2} + R_{G2}}}{2 \times \frac{R_{IN2}}{R_{IN2} + R_{G2}}} \right) \quad (54)$$

$$V_{OUT} = V_{CM} \times \left(\frac{R_{G1}}{R_{IN2}} \times \frac{R_{IN2} + R_{G2}}{R_{IN1} + R_{G1}} - \frac{R_{G2}}{R_{IN2}} \right) + \frac{V_{DIFF}}{2} \times \left(\frac{R_{G1}}{R_{IN2}} \times \frac{R_{IN2} + R_{G2}}{R_{IN1} + R_{G1}} + \frac{R_{G2}}{R_{IN2}} \right) \quad (55)$$

$$V_{OUT} = V_{CM} \times G_{nom} \times ((1 + t_{D2D}) \times (1 + t_{E2E}) - (1 + t_{D2})) + \frac{V_{DIFF}}{2} \times G_{nom} \times ((1 + t_{D2D}) \times (1 + t_{E2E}) + (1 + t_{D2})) \quad (56)$$

The gain error with respect to V_{CM} or to V_{DIFF} is calculated by taking a partial derivative of Equation 56 with respect to the given variable.

$$\frac{\partial V_{OUT}}{\partial V_{CM}} = G_{nom} \times ((1 + t_{D2D}) \times (1 + t_{E2E}) - (1 + t_{D2})) \quad (57)$$

$$\frac{\partial V_{OUT}}{\partial V_{DIFF}} = \frac{G_{nom}}{2} \times ((1 + t_{D2D}) \times (1 + t_{E2E}) + (1 + t_{D2})) \quad (58)$$

Because the error tolerance terms $(1 + t_{D2D})$ and $(1 + t_{E2E})$ are multiplicative, and t_{D2D} and t_{E2E} are both zero-mean with a standard deviation in the sub-200ppm range, the error contribution of $t_{D2D} \times t_{E2E}$ is less than 0.01ppm and is assumed to be negligible. The result is an algebraic sum of three terms, all considered as independent zero-mean Gaussian values, such that:

$$\frac{t_{ERR_{effective}}}{1} = \sqrt{\left(\frac{t_{D2D}}{1}\right)^2 + \left(\frac{t_{E2E}}{1}\right)^2 + \left(\frac{t_{D2}}{1}\right)^2} \quad (59)$$

By substituting the typical values of t_{D2D} , t_{E2E} , and t_{D2} , root sum of squares error analysis is performed on the resulting terms to describe a typical error for the transfer function.

Consider an example where a RES31A25-Q1 is used, such that $G_{nom} = 2.5$. Assume $t_{D2} = 64$ ppm, $t_{E2E} = 57$ ppm, and $t_{D2D} = 87$ ppm. Using Equation 59, $t_{ERR_{effective}}$ is calculated as ± 122 ppm, and is used to calculate ∂V_{OUT} with respect to V_{CM} and to V_{DIFF} . The former is the common-mode gain error, while the latter is composed of the desired nominal gain term (G_{nom}) and an undesired gain error.

$$\frac{\partial V_{OUT}}{\partial V_{CM}} = G_{nom} \times t_{ERR_{effective}} = G_{nom} \times \pm 122\text{ppm} = \pm 305\text{ppm} \quad (60)$$

$$\frac{\partial V_{OUT}}{\partial V_{DIFF}} = \frac{G_{nom}}{2} \times (2 + t_{ERR_{effective}}) = G_{nom} \pm 153\text{ppm} \quad (61)$$

Multiplication of the $t_{\text{ERP, effective}}$ error by the desired process control value, such as $\times 6$ for a six-sigma approach, gives conservative maximum bounds. Because the $\pm 1\sigma$ values reported in *Electrical Characteristics* already include guardbanding and account for mean shifts, in many cases a lower process control value (such as five-sigma) is sufficient. For example, solving the previous expressions for CMRR yields only 78.3dB, whereas the actual typical CMRR for the RES31A25-Q1 is 89.1dB. The discrepancy arises because the ATE measurement resolution of t_{D1} , t_{D2} , t_{M} , and CMRR is higher than that of t_{D2D} and t_{E2E} , and therefore the reported typical values of the latter parameters include additional guardbanding. Additionally, the conservative modeling approach assumes t_{D2D} , t_{E2E} , and t_{D2} are uncorrelated, whereas for many devices there are weak correlations (such as t_{D2D} and t_{E2E} having different polarities) that cause the actual observed error to be lower than the modeled error.

8.1.4 Discrete Instrumentation Amplifiers

The RES31A-Q1 can be used in conjunction with a dual-channel operational amplifier to implement a discrete instrumentation amplifier (INA). The ratiometric matching between the two resistor dividers improves CMRR performance for the circuit when compared to a similar implementation using unmatched discrete resistors, and results in better overtemperature and overaging gain drift characteristics. INAs are often used instead of difference amplifiers when high input impedance and low bias currents are needed, such as when measuring bridge sensors.

Discrete INAs are often configured as a differential-input differential-output circuit as shown in Figure 8-7. While not shown, if needed, use an additional discrete difference amplifier stage (requiring a second RES31A-Q1 and another op-amp channel) to convert the differential output voltage to a single-ended voltage (for example, when driving a single-ended ADC). This extra stage can also add an additional offset and provide additional gain, effectively mimicking the common three-amplifier INA architecture.

$$V_{\text{OUT+}} - V_{\text{OUT-}} = (V_{\text{IN+}} - V_{\text{IN-}}) \times \left(1 + \frac{R_{\text{G}}}{R_{\text{IN}}} \right) \quad (62)$$

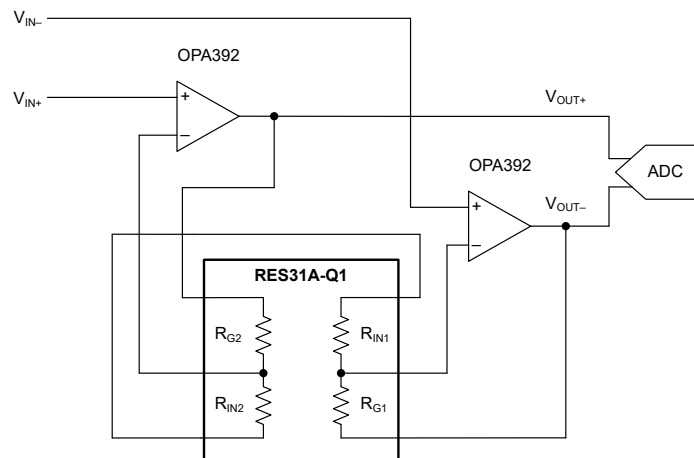


Figure 8-7. Differential-Input, Differential-Output Instrumentation Amplifier Using the RES31A-Q1

Less commonly, a discrete INA can be implemented as a differential-input, single-ended output circuit as shown in Figure 8-8. This topology maintains high input impedances, allows an offset to be applied, and gives a single-ended output without requiring a third amplifier channel. The offset must be driven by a low-impedance source, such as a reference buffer. When designing a discrete INA, carefully consider the output swing and input common-mode range limitations of the amplifiers used in the circuit design process.

$$V_{\text{OUT}} = (V_{\text{IN+}} - V_{\text{IN-}}) \times \left(1 + \frac{R_{\text{G}}}{R_{\text{IN}}} \right) + V_{\text{REF}} \quad (63)$$

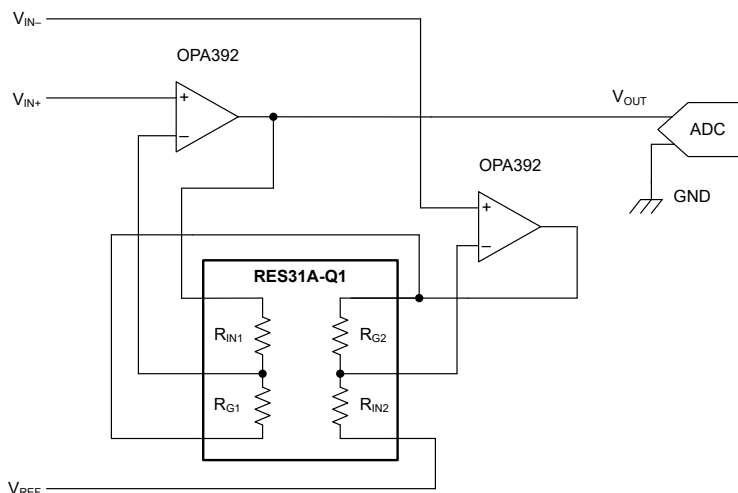


Figure 8-8. Differential-Input, Single-Ended Output Instrumentation Amplifier Using the RES31A-Q1

8.1.5 Fully Differential Amplifier

The RES31A-Q1 can be used to set the gain of a fully differential amplifier, such as the THP210. The ratiometric matching between the two resistor dividers leads to improved gain matching and CMRR performance for the circuit, when compared to a similar implementation using unmatched discrete resistors.

Figure 8-9 shows a generic schematic representation of a fully differential amplifier driving a differential ADC, with a RES31A-Q1 used to set the amplifier gain.

$$V_{OUT+} - V_{OUT-} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_G}{R_{IN}} \right) \quad (64)$$

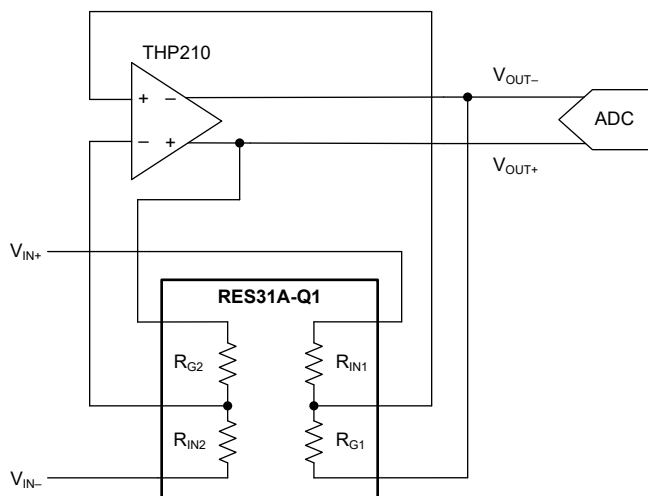


Figure 8-9. Fully-differential Amplifier Gain Setting Using RES31A-Q1

8.1.6 Unconventional Circuits

The two matched dividers of a RES31A-Q1 are typically used independently of each other, as two well-matched channels. The resistors are also useful in less conventional orientations, where resistors from both channels are linked to achieve a wider range of transfer functions and effective "gains". While voltage dividers or amplifier feedback paths are obvious candidates for this use, more unique applications such as "unbalanced" instrumentation amplifier circuits also benefit from this approach.

8.1.6.1 Single-Channel Voltage Divider

As discussed in [Section 8.1.2](#), the RES31A-Q1 is commonly used as an input signal level-shifter or voltage divider. Typically, R_G and R_{IN} act as R_X and R_Y respectively (or vice versa) in this circuit, and are arranged with the two dividers of the RES31A-Q1 acting as independent channels. If unconventional values of G_{VD} are required, combine the four resistors of a single RES31A-Q1 in various series and parallel combinations to achieve the desired effective gain, though the device channel count is effectively reduced from two to one. The following tables showcase some of the permutations of possible RES31A-Q1 connections, and reports the transfer function associated with each. Because the value of G_{VD} is always less than 1, for readability, the value given in the tables is G_{VD}^{-1} or $1 / G_{VD}$.

Table 8-4. Effective Transfer Function G_{VD}^{-1} for Some RES31A-Q1 Resistor Permutations, Adjusting R_Y

R_X	R_G	R_{G1}	R_{G1}	R_{G1}	R_{IN}	R_{IN1}	R_{IN1}	R_{IN1}
R_Y	R_{IN}	$R_{IN1} + R_{IN2}$	$R_{IN1} + R_{G2}$	$R_{IN1} + R_{IN2} + R_{G2}$	R_G	$R_{G1} + R_{IN2}$	$R_{G1} + R_{G2}$	$R_{G1} + R_{G2} + R_{IN2}$
G_{R31}	EFFECTIVE TRANSFER FUNCTION G_{VD}^{-1}							
1	2	1.5	1.5	1.3333	2	1.5	1.5	1.3333
1.5	2.5	1.75	1.6	1.4286	1.6667	1.4	1.3333	1.25
1.6667	2.6667	1.8333	1.625	1.4545	1.6	1.375	1.3	1.2308
2	3	2	1.6667	1.5	1.5	1.3333	1.25	1.2
2.5	3.5	2.25	1.7143	1.5556	1.4	1.2857	1.2	1.1667
3	4	2.5	1.75	1.6	1.3333	1.25	1.1667	1.1429
4	5	3	1.8	1.6667	1.25	1.2	1.125	1.1111
5	6	3.5	1.8333	1.7143	1.2	1.1667	1.1	1.0909
9	10	5.5	1.9	1.8182	1.1111	1.1	1.0556	1.0526
10	11	6	1.9091	1.8333	1.1	1.0909	1.05	1.0476

Table 8-5. Effective Transfer Function G_{VD}^{-1} for Some RES31A-Q1 Resistor Permutations, Adjusting R_X

R_X	R_{IN}	$R_{IN1} + R_{IN2}$	$R_{IN1} + R_{G2}$	$R_{IN1} + R_{IN2} + R_{G2}$	R_G	$R_{G1} + R_{IN2}$	$R_{G1} + R_{G2}$	$R_{G1} + R_{G2} + R_{IN2}$
R_Y	R_G	R_{G1}	R_{G1}	R_{G1}	R_{IN}	R_{IN1}	R_{IN1}	R_{IN1}
G_{R31}	EFFECTIVE TRANSFER FUNCTION G_{VD}^{-1}							
1	2	3	3	4	2	3	3	4
1.5	1.6667	2.3333	2.6667	3.3333	2.5	3.5	4	5
1.6667	1.6	2.2	2.6	3.2	2.6667	3.6667	4.3333	5.3333
2	1.5	2	2.5	3	3	4	5	6
2.5	1.4	1.8	2.4	2.8	3.5	4.5	6	7
3	1.3333	1.6667	2.3333	2.6667	4	5	7	8
4	1.25	1.5	2.25	2.5	5	6	9	10
5	1.2	1.4	2.2	2.4	6	7	11	12
9	1.1111	1.2222	2.1111	2.2222	10	11	19	20
10	1.1	1.2	2.1	2.2	11	12	21	22

For example, consider a voltage divider constructed with $R_X = R_{IN1} + R_{IN2} + R_{G2}$ and $R_Y = R_{G1}$. Using a RES31A15-Q1 device with $G_{nom} = 1.5$ for this implementation gives an effective transfer function $G_{VD} = R_Y / (R_X + R_Y) = 150k\Omega / (100k\Omega + 100k\Omega + 150k\Omega + 150k\Omega) = 150k\Omega / 500k\Omega = 0.3$, such that $G_{VD}^{-1} = 3.3333$. Therefore, $V_{OUT} = V_{IN} \times G_{VD} = V_{IN} / 3.3333$.

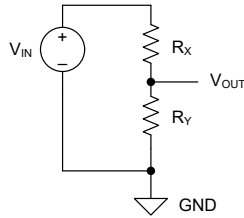


Figure 8-10. 1/3.3333 Voltage Divider, Effective Circuit

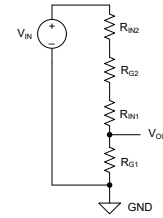


Figure 8-11. 1/3.3333 Voltage Divider, Implemented With the RES31A15-Q1

8.1.6.2 Single-Channel Amplifier Gain

The RES31A-Q1 is often used to implement the feedback network of an amplifier and set the circuit gain, as discussed in Section 8.1.1. Typically, R_G and R_{IN} act as R_X and R_Y respectively (or vice versa) in this circuit, and dividers 1 and 2 are arranged as two independent channels. If, however, unconventional values of G_{Inv} or G_{NonInv} are required, combining the four resistors of a single RES31A-Q1 in various series and parallel combinations achieves this requirement, but at the expense of a reduction in channel count. The following tables showcase some of the permutations of possible RES31A-Q1 connections, and report the G_{Inv} transfer function associated with each. To calculate G_{NonInv} for each scenario, simply add 1 to the magnitude of the given G_{Inv} .

Table 8-6. Effective Transfer Function G_{Inv} for Some RES31A-Q1 Resistor Permutations, Adjusting R_Y

R_X	R_{IN}	R_{IN1}	R_{IN1}	R_{IN1}	R_G	R_{G1}	R_{G1}	R_{G1}
R_Y	R_G	$R_{G1} + R_{IN2}$	$R_{G1} + R_{G2}$	$R_{G1} + R_{G2} + R_{IN2}$	R_{IN}	$R_{IN1} + R_{IN2}$	$R_{IN1} + R_{G2}$	$R_{IN1} + R_{G2} + R_{IN2}$
G_{R31} EFFECTIVE TRANSFER FUNCTION G_{Inv}								
1	1	0.5	0.5	0.3333	1	0.5	0.5	0.3333
1.5	0.6667	0.4	0.3333	0.25	1.5	0.75	0.6	0.4286
1.6667	0.6	0.375	0.3	0.2308	1.6667	0.8333	0.625	0.4545
2	0.5	0.3333	0.25	0.2	2	1	0.6667	0.5
2.5	0.4	0.2857	0.2	0.1667	2.5	1.25	0.7143	0.5556
3	0.3333	0.25	0.1667	0.1429	3	1.5	0.75	0.6
4	0.25	0.2	0.125	0.1111	4	2	0.8	0.6667
5	0.2	0.1667	0.1	0.0909	5	2.5	0.8333	0.7143
9	0.1111	0.1	0.0556	0.0526	9	4.5	0.9	0.8182
10	0.1	0.0909	0.05	0.0476	10	5	0.9091	0.8333

Table 8-7. Effective Transfer Function G_{Inv} for Some RES31A-Q1 Resistor Permutations, Adjusting R_X

R_X	R_G	$R_{G1} + R_{IN2}$	$R_{G1} + R_{G2}$	$R_{G1} + R_{G2} + R_{IN2}$	R_{IN}	$R_{IN1} + R_{IN2}$	$R_{IN1} + R_{G2}$	$R_{IN1} + R_{G2} + R_{IN2}$
R_Y	R_{IN}	R_{IN1}	R_{IN1}	R_{IN1}	R_G	R_{G1}	R_{G1}	R_{G1}
G_{R31} EFFECTIVE TRANSFER FUNCTION G_{Inv}								
1	1	2	2	3	1	2	2	3
1.5	1.5	2.5	3	4	0.6667	1.3333	1.6667	2.3333
1.6667	1.6667	2.6667	3.3333	4.3333	0.6	1.2	1.6	2.2
2	2	3	4	5	0.5	1	1.5	2
2.5	2.5	3.5	5	6	0.4	0.8	1.4	1.8
3	3	4	6	7	0.3333	0.6667	1.3333	1.6667
4	4	5	8	9	0.25	0.5	1.25	1.5
5	5	6	10	11	0.2	0.4	1.2	1.4
9	9	10	18	19	0.1111	0.2222	1.1111	1.2222
10	10	11	20	21	0.1	0.2	1.1	1.2

For example, consider an inverting amplifier circuit constructed with $R_X = R_{G1} + R_{G2}$ and $R_Y = R_{IN1}$. Using a RES31A00-Q1 device with $G_{nom} = 10$ for this implementation gives an effective transfer function $G_{INV} = R_X / R_Y = (1M\Omega + 1M\Omega) / 100k\Omega = 20$. Therefore, $V_{OUT} = -V_{IN} \times G_{INV} = V_{IN} \times -20$.

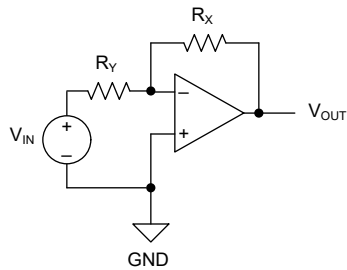


Figure 8-12. $V_{OUT} = -20 \times V_{IN}$, Effective Circuit

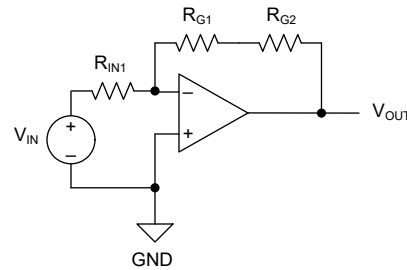


Figure 8-13. $V_{OUT} = -20 \times V_{IN}$, Implemented With RES31A00-Q1

8.1.6.3 Unconventional Instrumentation Amplifiers

The basic instrumentation amplifier circuits shown in Figure 8-7 and Figure 8-8 place the two R_{IN} resistors of the RES31A-Q1 in series between the inverting input pins of the two amplifiers. Instead, combine these resistors in parallel, or connect only one of the two R_{IN} resistors and leave the other resistor floating, to achieve a wider variety of effective circuit gains.

Another option is the *unbalanced* INA, where the feedback paths of the two input amplifiers have different effective gains. With the RES31A-Q1, this configuration is achieved by using series or parallel combinations of the divider elements to achieve a different effective feedback resistance for one amplifier. With the normal or balanced INA approach, if the input signal V_{CM} is not near midsupply, the amplifiers run out of headroom and rail out as the input approaches one of the power-supply voltages. By implementing asymmetric gains, the dynamic range of the circuit is maximized, though at the minor expense of bandwidth and phase mismatches (largely trivial for dc and low-frequency applications). While the transfer function and stability and error analyses of the circuit are relatively complex, the unbalanced INA nevertheless is a useful tool for this scenario.

8.2 Typical Application

8.2.1 Common-Mode Shifting Input Stage

The RES31A-Q1 can be used to implement a common-mode attenuator at the high-impedance inputs of an instrumentation amplifier (INA). This configuration extends the usable signal range, so long as the maximum differential voltage limitation of each resistor divider is respected.

Figure 8-14 shows an example of a high-side current-sense circuit where a differential voltage, V_{SHUNT} , develops across a sense resistor with an undesirably high common-mode voltage V_{CM} . V_{REF} is used to shift input common-mode voltages V_{MID1} and V_{MID2} to levels within the specified input common-mode range of the INA. The amplifier output, V_{OUT} , is a scaled function of V_{SHUNT} , such that nominally:

$$V_{OUT} = V_{SHUNT} \times \left(\frac{R_{IN}}{R_G + R_{IN} + R_{EQUIV}} \right) \quad (65)$$

V_{OUT} can be gained up further by the INA stage, to make maximal use of the effective resolution of a downstream ADC. In practice R_{EQUIV} is optional; however, if $R_{EQUIV} = R_{SHUNT}$, this resistance equalizes the nominal impedance between V_{CM} and each of the INA high-impedance inputs, thus improving CMRR performance. Select an INA with input bias currents I_{B1} and $I_{B2} \ll I_{STATIC1}$ and $I_{STATIC2}$, such as the [INA333](#) or [INA823](#). Select a RES31A-Q1 device with a sufficiently high divider series resistance so that $I_{STATIC1}$ and $I_{STATIC2} \ll I_{LOAD}$.

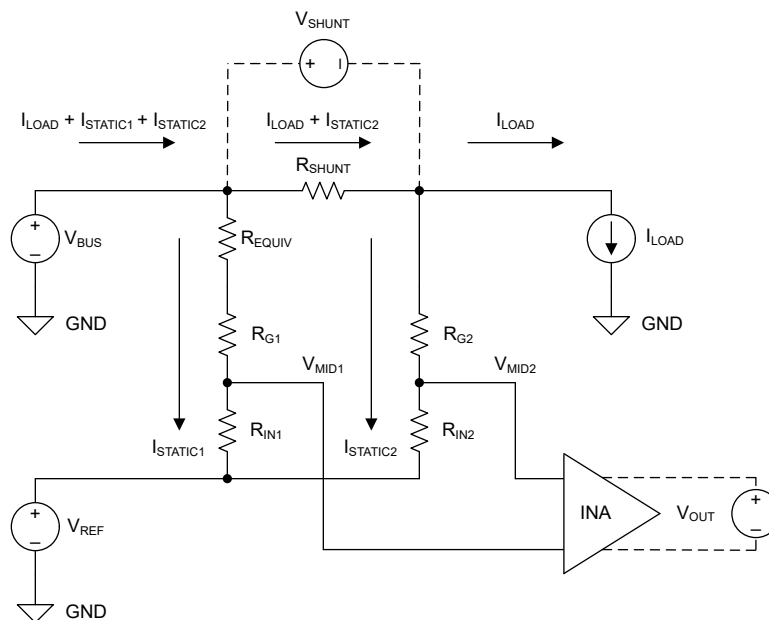


Figure 8-14. RES31A-Q1 Common-Mode Shifting Circuit

To achieve a desired nominal input common-mode voltage, $V_{MID1TARGET}$, set V_{REF} as follows:

$$V_{REF} = V_{MID1TARGET} \times \left(\frac{R_G + R_{IN} + R_{EQUIV}}{R_G + R_{EQUIV}} \right) - V_{CM} \times \left(\frac{R_G + R_{IN} + R_{EQUIV}}{R_G + R_{EQUIV}} - 1 \right) \quad (66)$$

8.2.1.1 Design Requirements

Consider a level-shifting application where a high-side current shunt measurement from an 50V supply rail must be measured by a 3.3V amplifier and ADC.

PARAMETER	DESIGN GOAL
Input V_{BUS}	50V
I_{LOAD}	25A (maximum)
R_{SHUNT}	10m Ω
ADC full-scale range (target V_{OUT})	3.3V
Possible V_{REF} voltages	3.3V, -3.3V, 0V

8.2.1.2 Detailed Design Procedure

The design parameters are used with the aforementioned equations to select a nominal target G . When the possible V_{REF} voltages available in the system are considered, $V_{REF} = -3.3V$ with $G = 10$ is found to result in a V_{MID1} value of 1.54V, well within the input common-mode range of a 3.3V rail-to-rail amplifier such as the OPA392. When the corresponding RES31A00-Q1 is employed, the loss terms $I_{STATIC1}$ and $I_{STATIC2}$ are nominally 48.45 μA and 48.23 μA for $I_{LOAD} = 25A$. For simplicity, the error contributions of the INA stage V_{OS} and I_B are ignored.

For the INA stage, an integrated TI instrumentation amplifier (IA) can be used. Alternatively, a discrete approach can be implemented using additional RES31A-Q1 or RES21A-Q1 devices, and one or more op amps. For this example, an IA stage is constructed with two channels of a OPA4392 and a RES21A00-Q1 (R_{IN3} , R_{G3} , R_{IN4} , and R_{G4}). This stage is in turn cascaded with a difference amplifier stage, constructed with the third amplifier channel and a RES21A00-Q1 (R_{IN5} , R_{G5} , R_{IN6} , and R_{G6}). The level-shifting stage gain of 11^{-1} , multiplied by the instrumentation amplifier stage gain of 11, results in an effective unity-gain transfer function for V_{SHUNT} . Therefore, the differential output voltage for this stage is approximately 0.25V, with amplifier outputs of 1.67V and 1.42V. After the final difference amplifier stage gain of $G = 10$, the common-mode voltage drops out and the maximum value of the resulting V_{OUT} is nominally 2.5V, compatible with a single-ended 3.3V ADC. If desired, the fourth channel of the OPA4392 can be used to buffer this output signal and serve as a dedicated ADC driver.

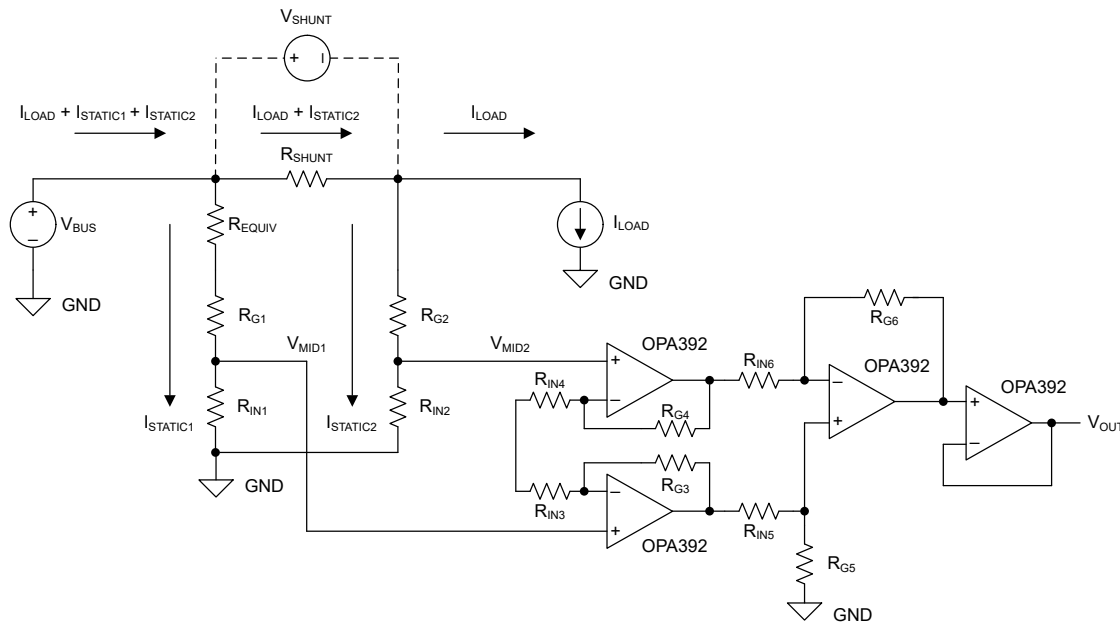


Figure 8-15. High-Side Current Shunt Common-Mode Shifting Circuit

8.2.1.3 Application Curves

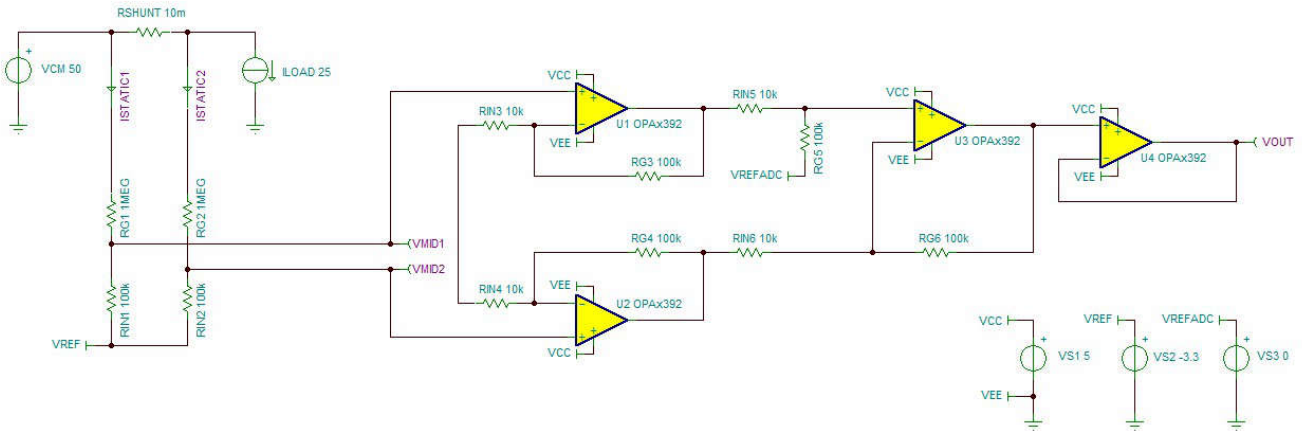


Figure 8-16. Circuit Model in TINA-TI

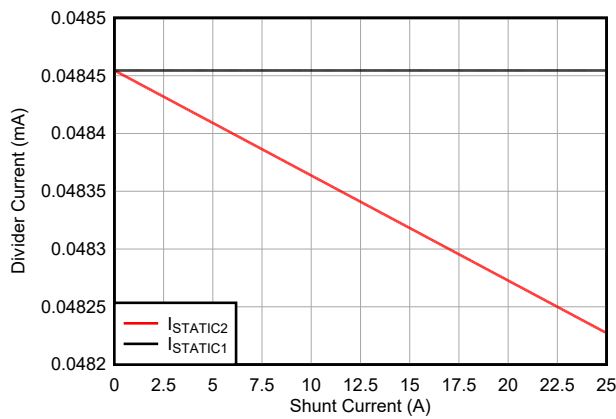


Figure 8-17. Simulation Result for I_STATIC

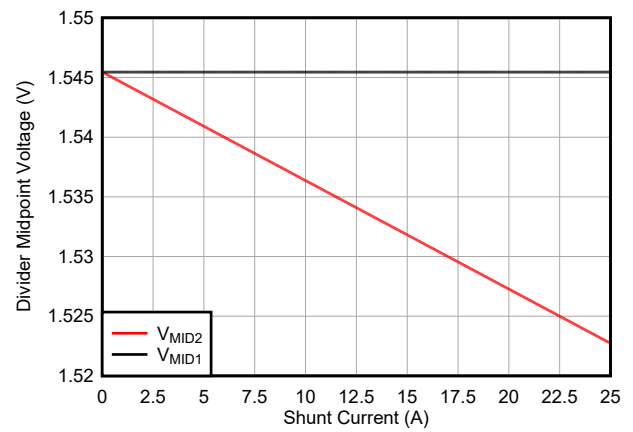


Figure 8-18. Simulation Result for V_MID

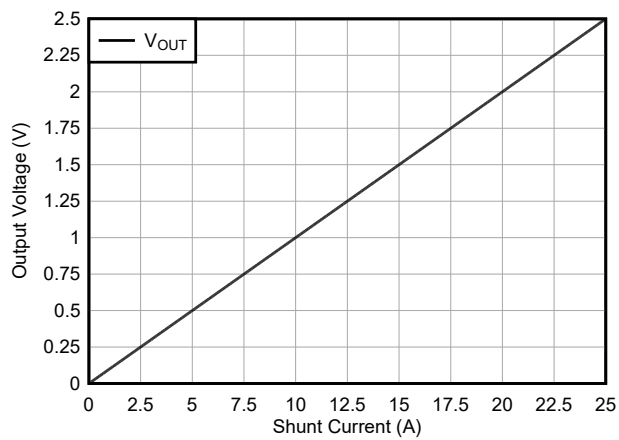


Figure 8-19. Simulation Result for V_OUT

8.3 Power Supply Recommendations

The qualification limits of the CMOS process used to implement the RES31A-Q1 dictate the maximum common-mode and differential voltage rating for the resistor dividers of each device. See the *Absolute Maximum Ratings* and *Recommended Operating Conditions* for device-specific values under transient and sustained bias conditions, respectively.

If the device voltage is expected to exceed the maximum sustained divider voltage rating, consider additional protective circuit elements. Avoid using external current-limiting resistors in series, as these unbalance the divider and cancel out many of the ratiometric and over-temperature benefits of the RES31A-Q1. The easiest way to protect a RES31A-Q1 divider from overload conditions is to place a reverse-biased or bidirectional zener diode in parallel with the divider, to clamp the effective divider voltage without drawing any leakage current *through* the divider. Choose a diode with a breakdown voltage approximately equal to the maximum divider voltage.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running input traces as far away from supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit. For differential circuits, match the length of the input traces as best possible.
- Keep high impedance input signals away from noisy traces.
- Make sure system supply voltages are adequately filtered.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Only connect one of the two GND/SUB pins to the ground plane, to prevent the formation of current return paths through the device substrate. Float the other GND/SUB pin.

8.4.2 Layout Examples

In the following examples, the RES31A-Q1 is shown with a VSSOP amplifier and 0402-size decoupling capacitors.

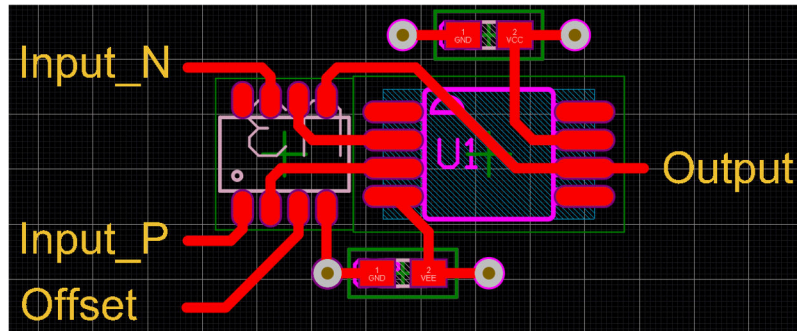


Figure 8-20. Single-Layer Difference Amplifier Implementation

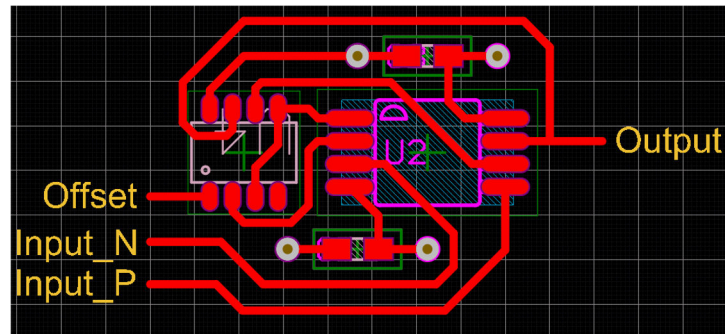


Figure 8-21. Single-Layer Instrumentation Amplifier Implementation

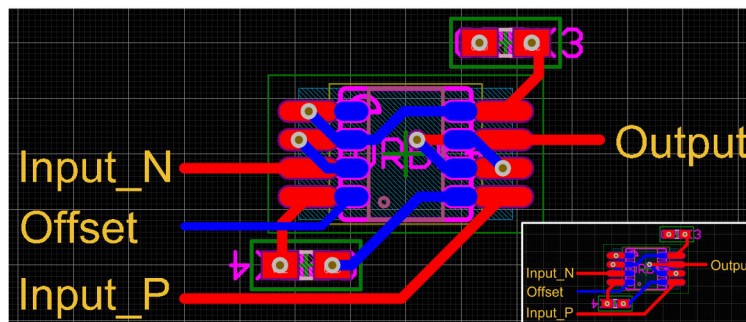


Figure 8-22. Front-and-Back Instrumentation Amplifier Implementation

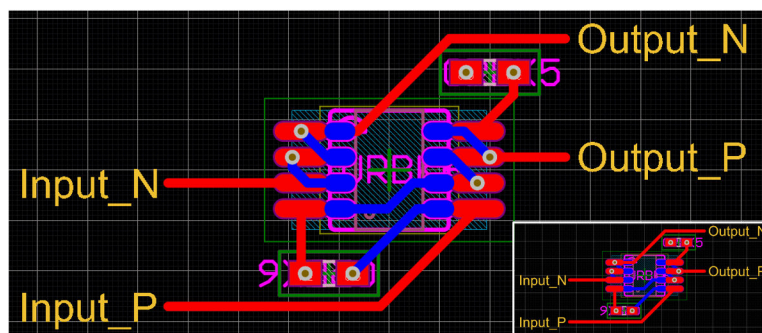


Figure 8-23. Front-and-Back, Differential-Output Instrumentation Amplifier Implementation

For [Figure 8-24](#), two RES31A-Q1 devices (bottom side) and one dual-channel op-amp (top side) are used.

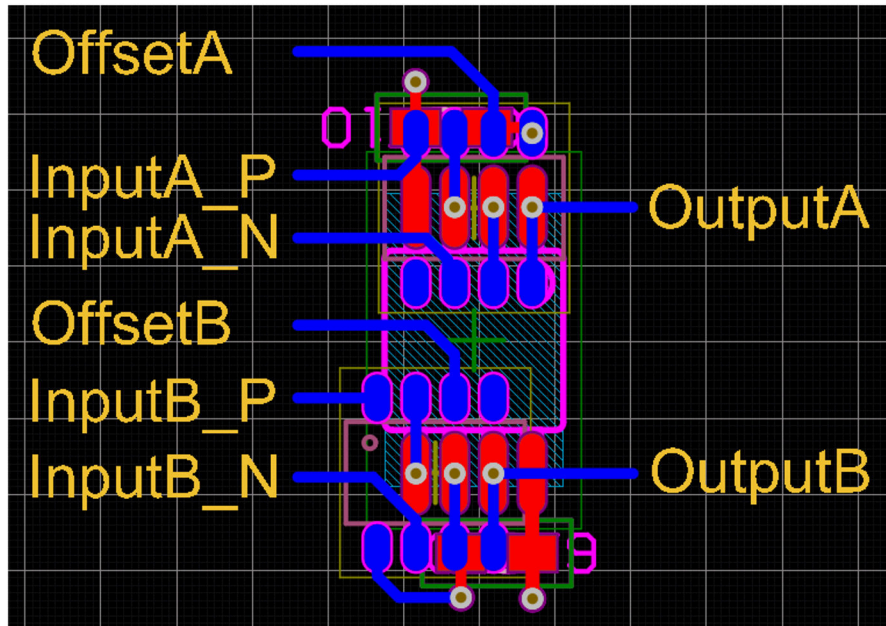


Figure 8-24. Front-and-Back Dual Difference Amplifiers Implementation

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design and simulation tools](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

9.1.1.3 TI Reference Designs

TI reference designs are analog designs created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at <https://www.ti.com/reference-designs>.

9.1.1.4 Analog Filter Designer

Available as a web-based tool from the [Design and simulation tool](#) web page, the [Analog Filter Designer](#) allows the user to design, optimize, and simulate complete multistage active filter designs within minutes.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [RES11A-Q1 Automotive, Matched, Thin-Film Resistor Dividers With 1kΩ Inputs](#)
- Texas Instruments, [RES21A-Q1 Automotive, Matched, Thin-Film Resistor Dividers With 10kΩ Inputs](#)
- Texas Instruments, [RES60A-Q1 Automotive, 1400V_{DC}, Precision Resistive Divider](#)
- Texas Instruments, [Optimizing CMRR in Differential Amplifier Circuits With Precision Matched Resistor Divider Pairs application note](#)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains common TI terms, acronyms, and definitions.

Divider	The series combination of a matched R_G and R_{IN} resistor. Two resistors, R_{Gx} and R_{INx} , connected in series form a given divider x . The midpoint of divider x is measured at pin MID x . The RES31A-Q1 has two divider channels, divider 1 ($R_{G1} + R_{IN1}$) and divider 2 ($R_{G2} + R_{IN2}$).
G_{nom}	The nominal gain or ratio of a given divider. Calculated as R_{Gnom} / R_{INnom} . Each orderable of the RES31A-Q1 has a different associated divider ratio, and thus a different G_{nom} .
G_x	The actual, measured gain or ratio of a given divider x when the divider gain error is considered. Calculated as R_{Gx} / R_{INx} .
G_{VDnom}	The nominal or ideal voltage-divider circuit gain of a given divider. Calculated as either $R_{Gnom} / (R_{INnom} + R_{Gnom})$ or as $R_{INnom} / (R_{INnom} + R_{Gnom})$, depending on circuit configuration.
G_{VDx}	The actual, measured voltage-divider circuit gain for a divider x when the divider gain error is considered. Calculated as either $R_{Gx} / (R_{INx} + R_{Gx})$ or as $R_{INx} / (R_{INx} + R_{Gx})$, depending on circuit configuration.
t_{Dx}	The normalized gain error associated with a given divider x . When calculating effective gain, $G_x = G_{nom} \times (1 + t_{Dx})$. For an ideal divider, $t_{Dx} = 0$ and $G_x = G_{nom}$.

t_M	The mismatch of the two divider gain errors for a given RES31A-Q1 device. Calculated as $t_M = t_{D2} - t_{D1}$. Equivalent to $(G_2 - G_1) / G_{nom}$. Used for simplified CMRR calculations.
t_{VDx}	The normalized voltage-divider circuit gain error associated with a given divider x . When calculating effective voltage-divider circuit gain, $G_{VDx} = G_{VDnom} \times (1 + t_{VDx})$. For an ideal circuit, $t_{VDx} = 0$ and $G_{VDx} = G_{VDnom}$.
V_{Dx}	The voltage applied across a given divider x .
V_{Rx}	The voltage applied across a given resistor R_x . For example, V_{RIN1} describes the voltage across R_{IN1} .

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RES31A00QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R300Q
RES31A10QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R310Q
RES31A20QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R320Q
RES31A25QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R325Q
RES31A30QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R330Q
RES31A40QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R340Q
RES31A50QDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R350Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF RES31A-Q1 :

- Catalog : [RES31A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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