REF50xx-EP Low-Noise, Very Low Drift, Precision Voltage Reference

1 Features

- Low Temperature Drift: 5 ppm/°C (Maximum)
- High Accuracy: 0.08% (Maximum)
- Low Noise: 3 μV_{PP}/V
- High Output Current: ±10 mA
- Available in Military (–55°C to 125°C) Temperature Range (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

2 Applications

- 16-Bit Data Acquisition Systems
- ATE Equipment
- Industrial Process Control
- Medical Instrumentation
- Optical Control Systems
- Precision Instrumentation
- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site

(1) Custom temperature ranges available

3 Description

The REF50xx is a family of low-noise, very low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

Excellent temperature drift and high accuracy are achieved using proprietary design techniques. These features, combined with very low noise, make the REF50xx family ideal for use in high-precision data acquisition systems.

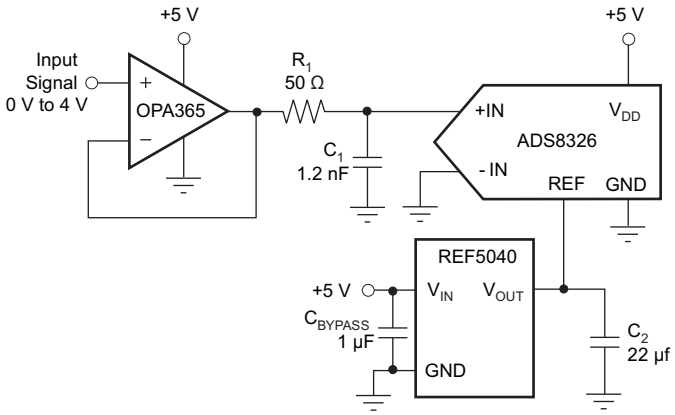
They are offered in SOIC-8 packages, and are specified from –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF50xx-EP	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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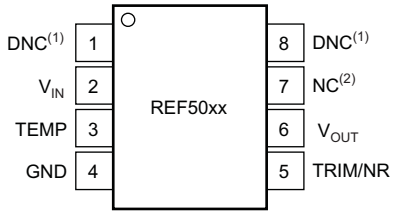
4 Revision History

Changes from Revision A (October 2012) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 3
- Changed title of *Supply Voltage* to *Low Dropout Voltage* ... 19

5 Pin Configuration and Functions

D Package
8- Pin SOIC
Top View



NOTES: (1) DNC = Do not connect.
(2) NC = No internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	1	—	Do not connect
VIN	2	Power	Power supply voltage. Range from V_{OUT} + 0.2 V up to 18 V. Recommended bypass capacitor from 1 µF up to 10 µF
TEMP	3	O	Temperature monitoring pin provides a temperature-dependent voltage output
GND	4	Power	System ground
TRIM/NR	5	I	Output adjustment and noise reduction input. Connecting 1 µF to this pin will create low pas filter at the bandgap and reduce output noise
VOUT	6	O	Very accurate, factory-trimmed voltage output. Recommended bypass capacitor from 1 µF up to 50 µF with ESR between 1 and 1.5 Ω
NC	7	—	No internal connection
DNC	8	—	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}		18	V
Output short-circuit			30	mA
Operating temperature		–55	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	V_{OUT} + 0.2 V	18	V
I_{OUT}	–10	10	mA

6.4 Thermal Information

THERMAL METRIC[1]		REF502x-EP D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Per Device

At T_A = 25°C, I_{LOAD} = 0, C_L = 1 µF, and V_{IN} = (V_{OUT} + 0.2 V) to 18 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T_A = 25°C			T_A = –55°C to 125°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REF5020 (V_{OUT} = 2.048V)[1]								
OUTPUT VOLTAGE								
Output Voltage V_{OUT}	2.7 V < V_{IN} < 18 V		2.048					V
Initial Accuracy		–0.05%		0.05%				
Over Temperature					–0.08%		0.08%	
NOISE								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		6					μV_{PP}
REF5025 (V_{OUT} = 2.5 V)								
OUTPUT VOLTAGE								
Output Voltage V_{OUT}			2.5					V
Initial Accuracy		–0.05%		0.05%				
NOISE								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		7.5					μV_{PP}
REF5040 (V_{OUT} = 4.096V)								
OUTPUT VOLTAGE								
Output Voltage V_{OUT}			4.096					V
Initial Accuracy		–0.05%		0.05%				
Over Temperature					–0.08%		0.08%	
NOISE								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		12					μV_{PP}
REF5050 (V_{OUT} = 5 V)								
OUTPUT VOLTAGE								
Output Voltage V_{OUT}			5					V
Initial Accuracy		–0.05%		0.05%				
Over Temperature					–0.08%		0.08%	
NOISE								
Output Voltage Noise	f = 0.1 Hz to 10 Hz		15					μV_{PP}

(1) For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

6.6 Electrical Characteristics: All Devices

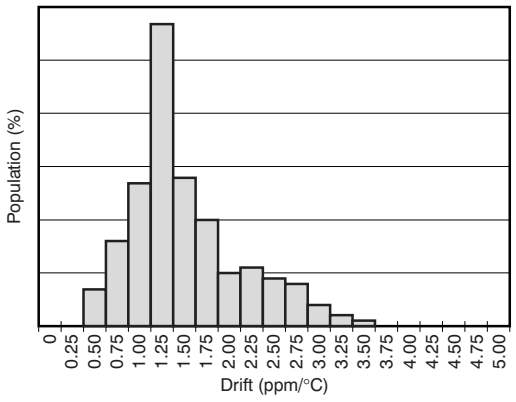
At T_A = 25°C, I_{LOAD} = 0, C_L = 1 µF, and V_{IN} = (V_{OUT} + 0.2 V) to 18 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = 25°C			T_A = –55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE TEMPERATURE DRIFT									
Output Voltage Temperature Drift	dV_{OUT}/dT								
REF5025							4	6.5	ppm/°C
REF5050							4	6.5	ppm/°C
All other devices							3	5	ppm/°C
LINE REGULATION									
Line Regulation	dV_{OUT}/dV_{IN}								
REF5020[1]		V_{IN} = 2.7 V to 18V		0.1	1				ppm/V
All other devices		V_{IN} = V_{OUT} + 0.2 V		0.1	1				ppm/V
Over Temperature							1	3	ppm/V
LOAD REGULATION									
Load Regulation	dV_{OUT}/d_{ILOAD}								
REF5020		–10 mA < I_{LOAD} < +10 mA, V_{IN} = 3 V		20	30				ppm/mA
All other devices		–10 mA < I_{LOAD} < +10 mA, V_{IN} = V_{OUT} + 0.75 V		20	30				ppm/mA
Over Temperature								60	ppm/mA
SHORT-CIRCUIT CURRENT									
Short-Circuit Current	I_{SC}	V_{OUT} = 0		25					mA
TEMP PIN									
Voltage Output		At T_A = 25°C		575					mV
Temperature Sensitivity							2.64		mV/°C
TURNON SETTLING TIME									
Turnon Settling Time		To 0.1% with C_L = 1 µF		200					µs
POWER SUPPLY									
Supply Voltage	V_{IN}	See Note [1]	V_{OUT} + 0.2[1]		18				V
Quiescent Current				0.8	1				mA
Over Temperature								1.25	mA
TEMPERATURE RANGE									
Specified Range			–55		125				°C
Operating Range			–55		125				°C
Thermal Resistance	θ_{JA}			150					°C/W

(1) For V_{OUT} ≤ 2.5 V, the minimal supply voltage is 2.7 V.

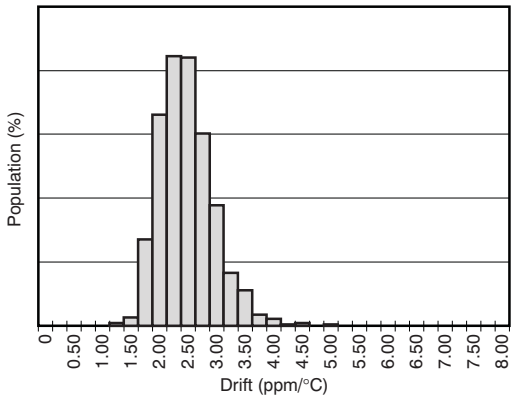
6.7 Typical Characteristics

At T_A = 25°C, I_{LOAD} = 0, and V_{IN} = V_{OUT} + 0.2 V, unless otherwise noted. For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.



0°C to 85°C

Figure 1. Temperature Drift



–40°C to 125°C

Figure 2. Temperature Drift

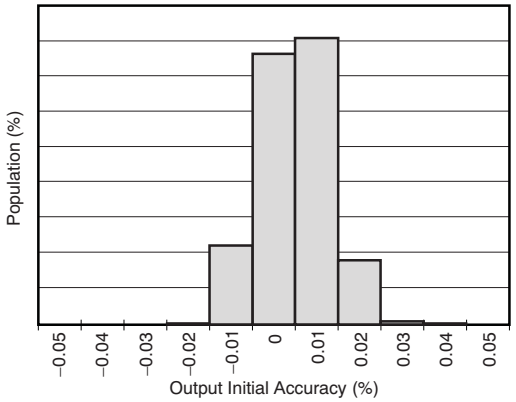


Figure 3. Output Voltage Initial Accuracy

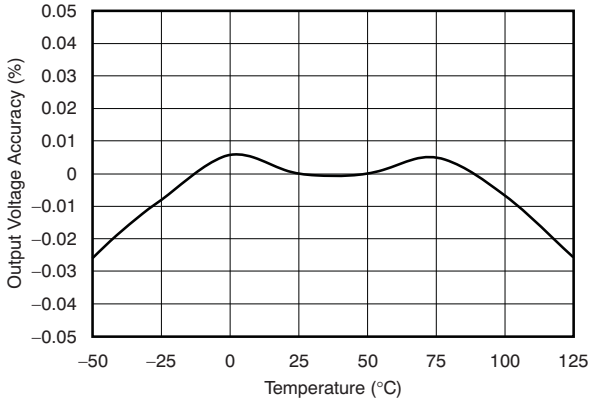


Figure 4. Output Voltage Accuracy vs Temperature

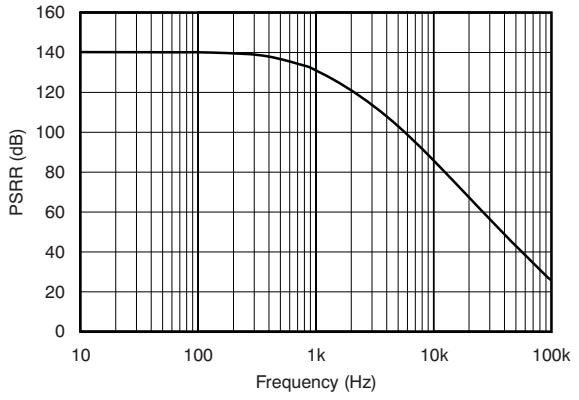


Figure 5. Power-Supply Rejection Ratio vs Frequency

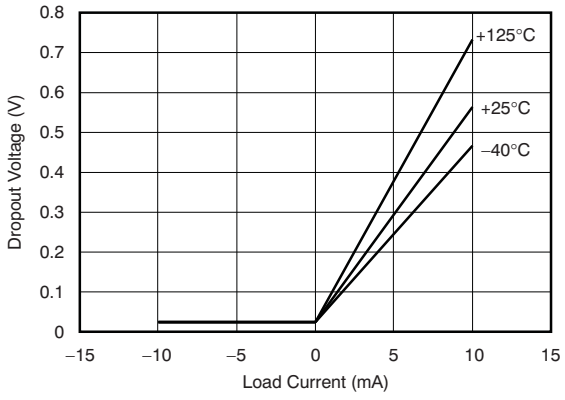


Figure 6. Dropout Voltage vs Load Current

Typical Characteristics (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_{IN} = V_{OUT} + 0.2 V, unless otherwise noted. For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

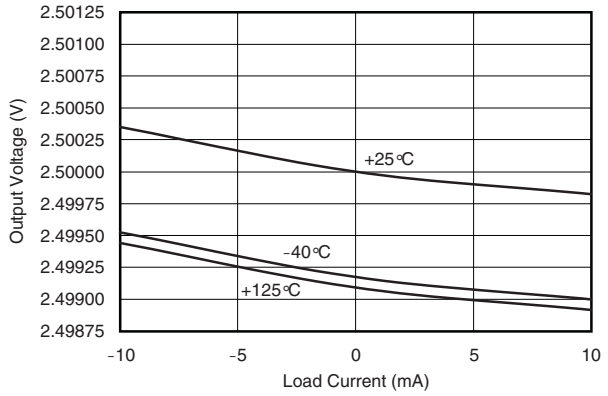


Figure 7. REF5025 Output Voltage vs Load Current

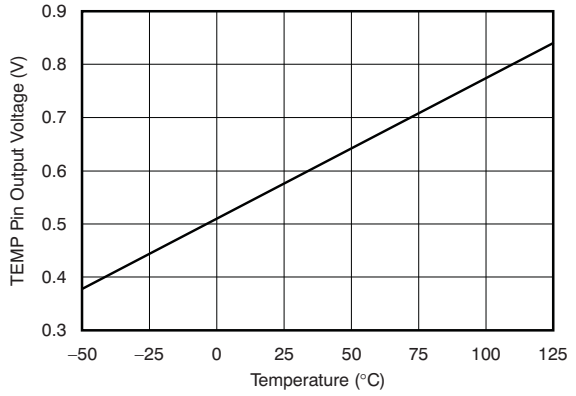


Figure 8. Temp Pin Output vs Voltage Temperature

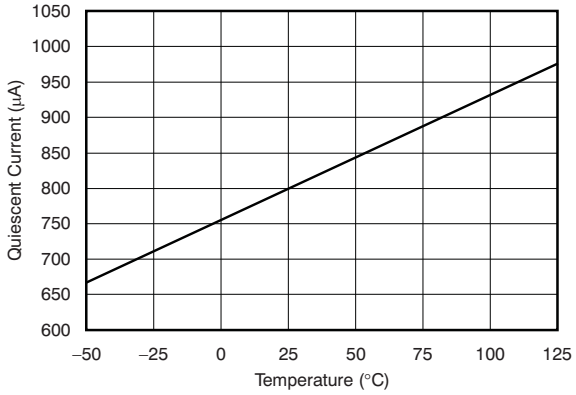


Figure 9. Quiescent Current vs Temperature

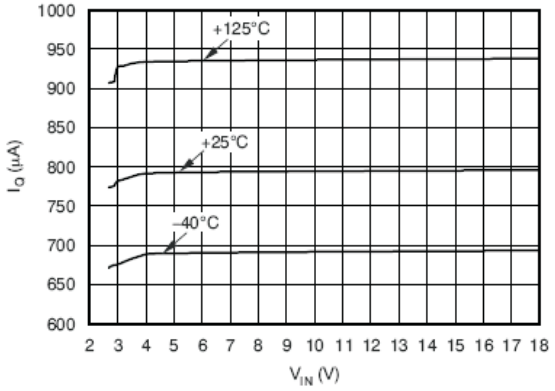


Figure 10. Quiescent Current vs Input Voltage

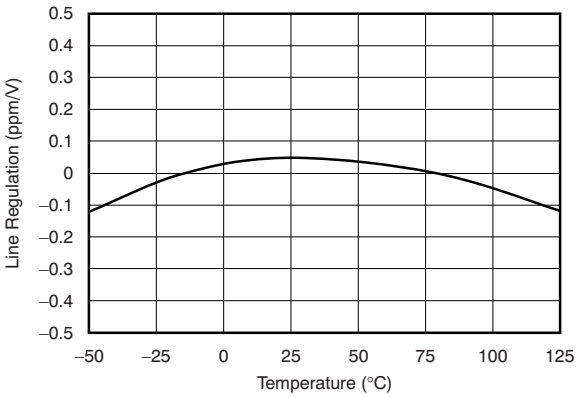


Figure 11. Line Regulation vs Temperature

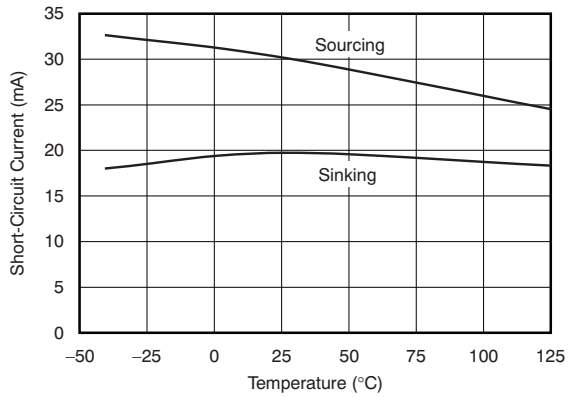


Figure 12. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_{IN} = V_{OUT} + 0.2 V, unless otherwise noted. For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.

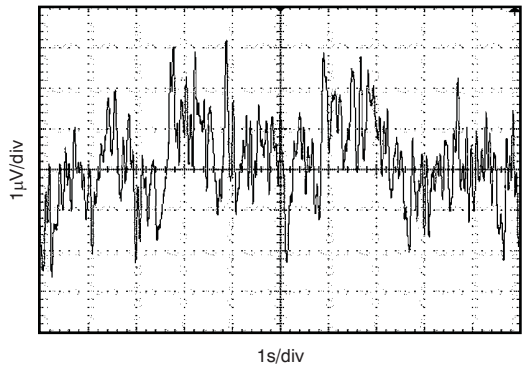
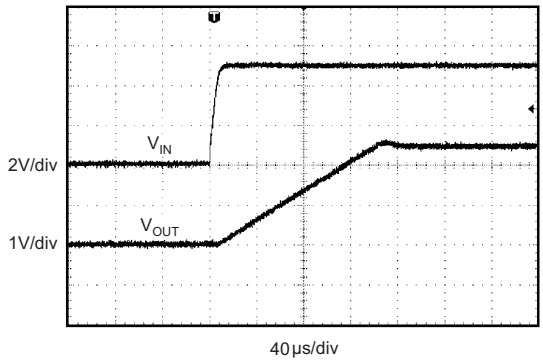
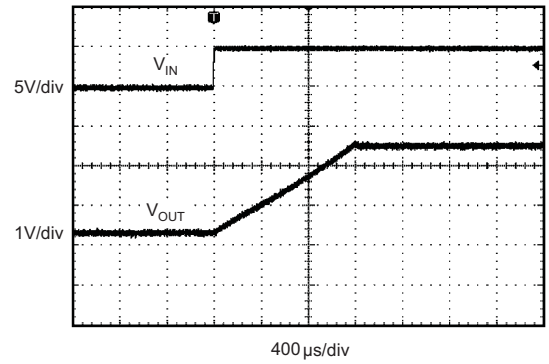


Figure 13. NOISE



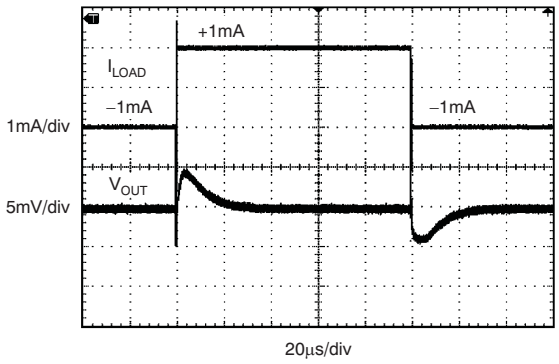
REF5025, C_L = 1 µF

Figure 14. Start-up



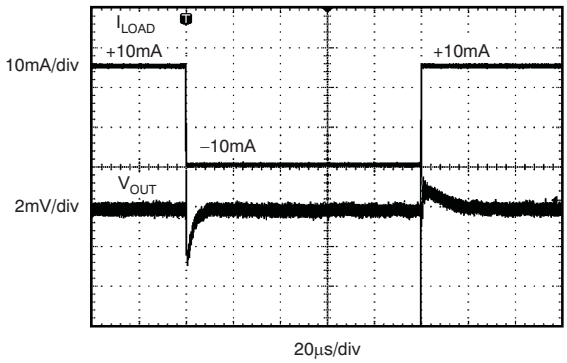
REF5025, C_L = 10 µF

Figure 15. Start-up



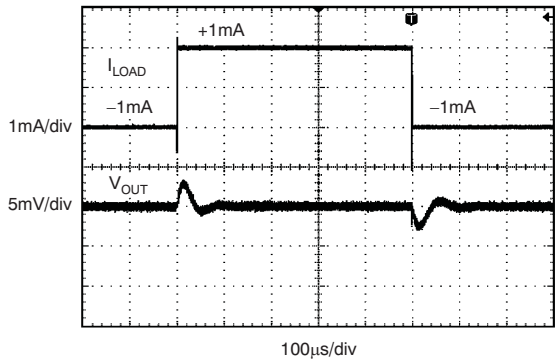
C_L = 1 µF, I_{OUT} = 1 mA

Figure 16. Load Transient



C_L = 1 µF, I_{OUT} = 10 mA

Figure 17. Load Transient

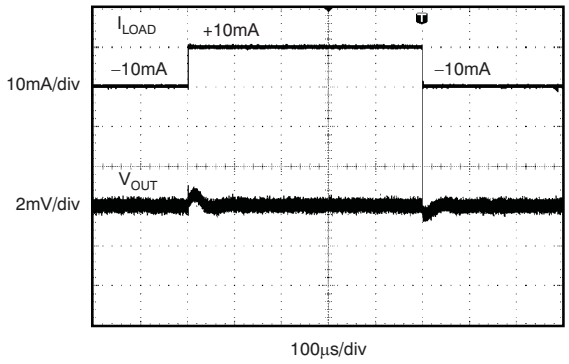


C_L = 10 µF, I_{OUT} = 1 mA

Figure 18. Load Transient

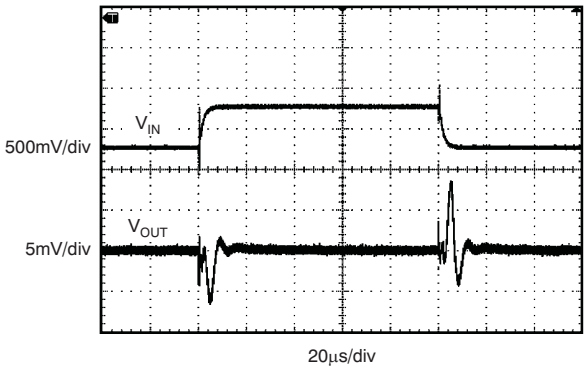
Typical Characteristics (continued)

At T_A = 25°C, I_{LOAD} = 0, and V_{IN} = V_{OUT} + 0.2 V, unless otherwise noted. For V_{OUT} ≤ 2.5 V, the minimum supply voltage is 2.7 V.



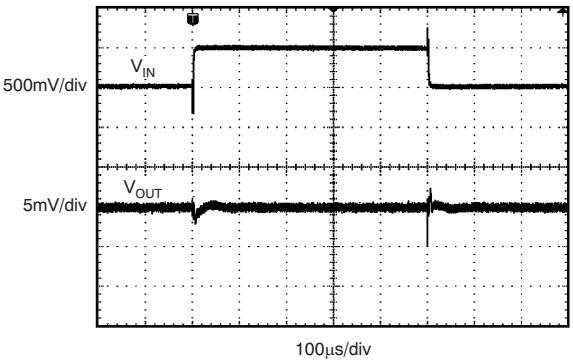
C_L = 10 µF, I_{OUT} = 10 mA

Figure 19. Load Transient



C_L = 1 µF

Figure 20. Line Transient



C_L = 10 µF

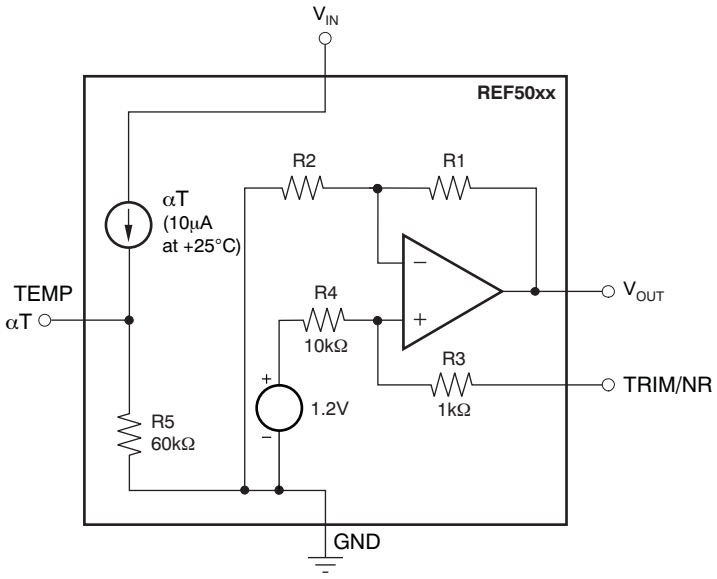
Figure 21. Line Transient

7 Detailed Description

7.1 Overview

The REF50xx devices are low-noise, low-drift, very high precision voltage references. These references can both sink and source, and are very robust with regard to line and load changes.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Adjustment Using The TRIM/NR Pin

The REF50xx provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 22 shows a typical circuit that allows an output adjustment of ±15 mV

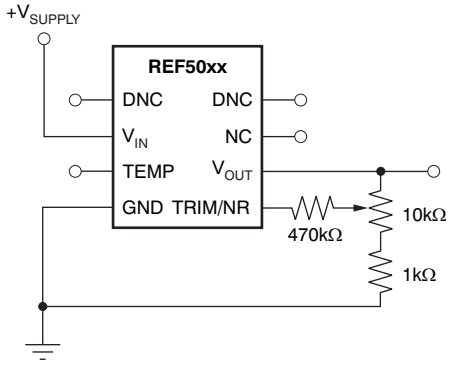


Figure 22. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see Figure 24) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1 μF creates a low-pass filter with the corner frequency between 10 Hz and 20 Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Use of this capacitor increases start-up time.

Feature Description (continued)

7.3.2 Low Temperature Drift

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 1:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3 ppm/°C for the high-grade version, and 8 ppm/°C for the standard-grade.

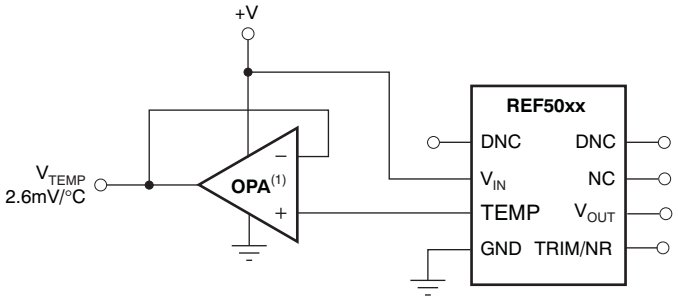
7.3.3 Temperature Monitoring

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As seen in Figure 8, the output voltage follows the nominal relationship:

$$V_{TEMP\ PIN} = 509\ \text{mV} + 2.64 \times T(°C) \quad (2)$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79 mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see *Functional Block Diagram*). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift operational amplifiers, such as the OPA333, OPA335, or OPA376, as shown in Figure 23.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 23. Buffering the TEMP Pin Output

7.3.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for each member of the REF50xx family is specified in the *Electrical Characteristics: Per Device* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although take care to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. This three-part series is available for download from the TI website under three literature numbers: SLYT331, SLYT339, and SLYT355, respectively.

Feature Description (continued)

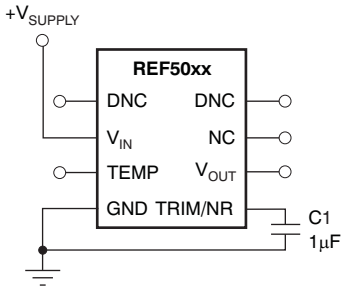


Figure 24. Noise Reduction Using the TRIM/NR Pin

7.4 Device Functional Modes

The REF50xx is powered on when the voltage on the V_{IN} pin is greater than VOUT + 0.2 V, except for the REF5020 and REF5025, where the minimum supply voltage is 2.7 V. The maximum input voltage for the REF50xx is 18 V. Use a supply bypass capacitor ranging from 1 µF to 10 µF. The total capacitive load at the output must be between 1 µF to 50 µF to ensure best output stability.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

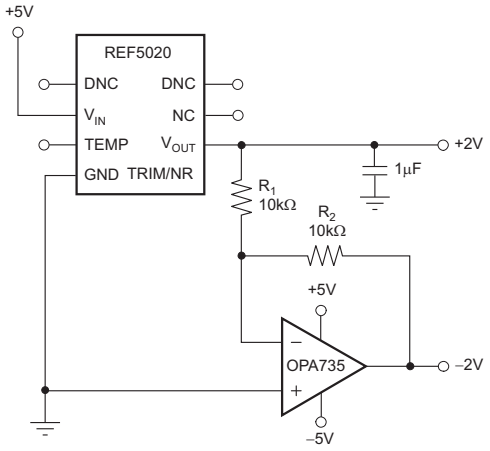
The REF50xx devices are low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. View the *Functional Block Diagram* of the REF50xx.

When designing circuits with a voltage reference, output noise is one of the main concerns. The main source of voltage noise in the reference voltages originates from the bandgap and output amplifier, which contribute significantly to the overall noise. During the design process, it is important to minimize these sources of voltage noise.

8.2 Typical Applications

8.2.1 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 25 shows the REF5020 used to provide a 2.5-V supply reference voltage. The low-drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2.



NOTE: Bypass capacitors not shown.

Figure 25. The REF5020 and OPA735 Create Positive and Negative Reference Voltages

8.2.1.1 Design Requirements

When using REF50xx in the design, it is important to select proper capacitive load that will not create gain peaking adding noise to the output voltage. At the same time, the capacitor must be selected to provide required filtering performance for the system. In addition, input bypass capacitor and noise reduction capacitors must be added for optimum performances.

8.2.1.2 Detailed Design Procedure

Proper design procedure will require first to select output capacitor. If the ESR of the capacitor is not in 1-Ω range additional resistor must be added in series with the load capacitor. Next, add a 1-µF capacitor to the NR pin to reduce internal noise of the REF50xx. Measuring output noise will confirm if the design has met the initial target.

Typical Applications (continued)

8.2.1.3 Application Curves

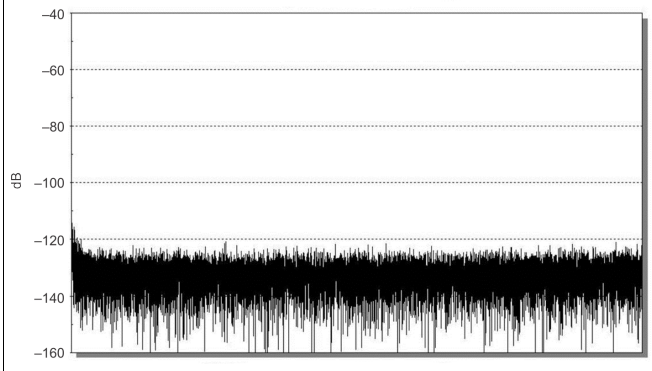


Figure 26. Noise Measurements of Properly Design REF50xx Data Acquisition System from Figure 33

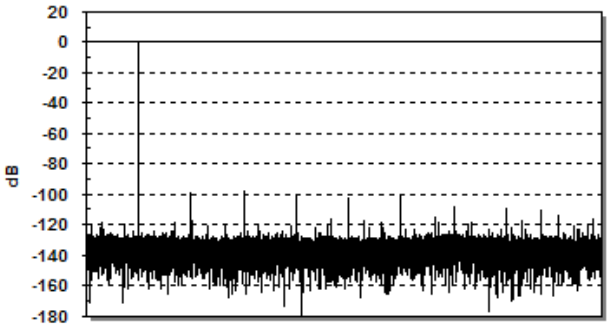


Figure 27. FFT of Data Acquisition System Design With REF50xx from Figure 33

8.2.2 Positive Reference Voltage

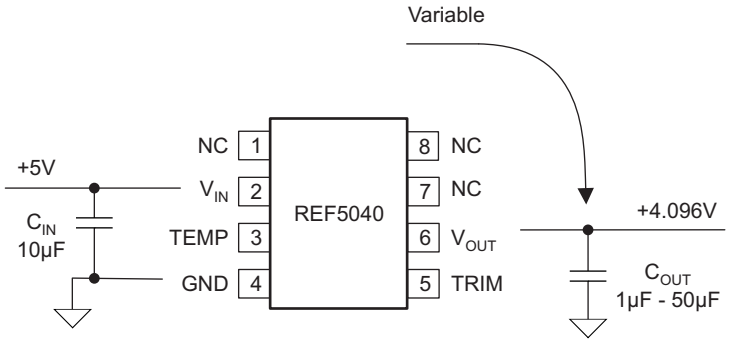


Figure 28. REF50xx With Load Capacitor

8.2.2.1 Detailed Design Procedure

8.2.2.1.1 Load Capacitance

To determine how much noise the reference voltage is contributing in a real application, this design uses the circuit presented in Figure 28. For the same conditions as power supply, input decoupling, and load current, measure the output noise for different output decoupling or load capacitors. The load capacitor type will change the low-pass filter frequency that is created on the output. This filter is determined by an added capacitor value and two parasitic components: the open-loop output impedance of the internal amplifier to the reference voltage, and the ESR of the external capacitor.

Figure 29 shows a fast-Fourier-transform (FFT) plot of the output signal of the reference voltage circuit with a 10-µF ceramic capacitor load. The output noise level peaks at around 9 kHz because of the response of the internal amplifier of the circuit to the capacitive load (C_L).

This peaking is the main contributor to the overall measured noise. This output noise, measured with an analog meter over a frequency range of up to 80 kHz, is approximately 16.5 µVRMS. If the voltage-reference circuit was connected to the input of an ADC, the measured noise across a 65-kHz frequency range would be 138 µVPP. This noise level makes this solution adequate for 8- to 14-bit converters.

Typical Applications (continued)

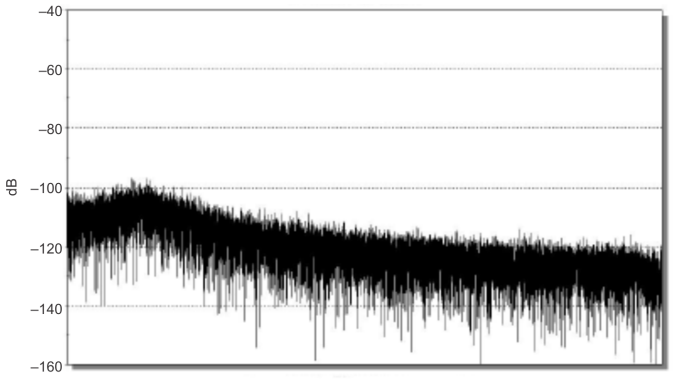
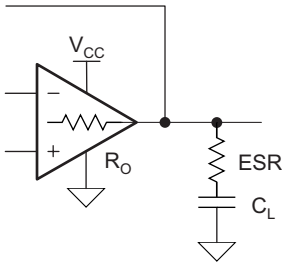


Figure 29. REF50xx FFT Plot of the Noise With 10-µF Load Capacitor and 10-µΩ ESR

Every capacitor can be represented with a complicated equivalent model, which is voltage and frequency dependent with a large number of passive components. For the purposes of this design, this model is limited to the few components. The biggest impact on the creation of the low-pass filter and stability analysis is the simplified model of equivalent series inductance and resistance. Considering good layout practice and inherently low equivalent series inductance of today's components, this model in the future analysis will be presented only by equivalent capacitance and series resistance.



$$f_P = \frac{1}{2\pi \cdot (R + ESR) \cdot C_L}$$

$$f_Z = \frac{1}{2\pi \cdot ESR \cdot C_L}$$

Figure 30. Equivalent SCH Of REF50xx With Load Capacitor for Stability Analysis

When evaluating the impact of ESR and C_L on the performance the reference voltage, it is important to include the effect of the open-loop output resistance (R_O) of the output amplifier. The combination of R_O, ESR, and C_L modifies the open-loop response curve by introducing one pole (f_P) and one zero (f_Z). The values R_O, ESR, and C_L determine the corner frequency of the added pole f_P; and the values of ESR and C_L determine the corner frequency of the added zero.

The introduction of the external ESR-CL on the output of the reference voltage modifies the output amplifier open-loop gain curve. The added pole modifies the open-loop gain curve of the reference voltage output amplifier by introducing a –20 dB/decade change at the frequency f_P to the already –20 dB/decade slope of the open-loop gain curve, making the slope equal to –40 dB/decade. The added zero at frequency f_Z changes the open-loop gain curve back to –20 dB/decade.

Typical Applications (continued)

Table 1. Noise Measurement Results for Different Load Capacitors

NOISE	22 kHz LP-5P	30 kHz LP-3P	80 kHz LP-3P	>500 kHz	UNIT
GND	0.8	1	1.8	4.9	μV_{RMS}
1 µF	37.8	41.7	53.7	9,017	
2.2 µF (cer)	41.7	46.2	55.1	60.8	
10 µF	33.4	33.4	35.2	38.5	
10 µF (cer)	37.1	37.2	37.8	39.1	
20 µF (cer)	33.1	33.1	33.2	34.5	
47 µF	23.2	23.8	24.1	26.5	

Table 1 shows the measured noise values for different frequency bandwidths as well as different values and types of external capacitors. These measurements show that low-ESR (approximately 100-mΩ) ceramic capacitors tend to increase the noise, compared to normal-ESR (approximately 2-Ω) tantalum capacitors. This tendency is caused by a stability issue with the output amplifier and gain peaking in the amplifier frequency response.

8.2.2.1.2 Bandgap Noise Reduction

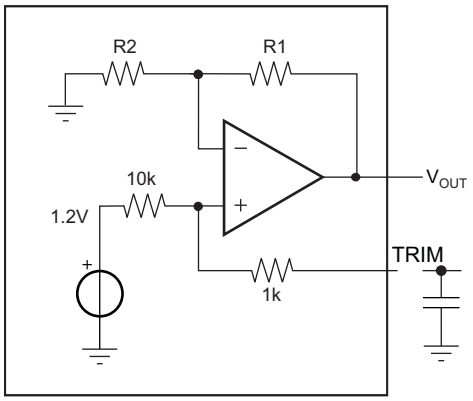


Figure 31. REF50xx Internal Structure of Trim/NR Pin

The internal schematic of the REF50xx device shows that the trim pin allows direct access to the bandgap output. Figure 31 shows the trim pin connection to the internal bandgap circuit through a resistor. Adding a capacitor on the trim pin creates a lowpass filter that has a broadband attenuation of −21 dB.

For example, a small 1-µF capacitor adds a pole at 14.5 Hz and a zero at 160 Hz. If more filtering is needed, a larger value capacitor can be added, which will lower the filter cutoff frequency and the noise contributed by the bandgap.

Table 2. Measured Noise (μV_{RMS}) for Four Bandwidths

NOISE	22 kHz (LOW-PASS 5-POLE)	30 kHz (LOW-PASS 3-POLE)	80 kHz (LOW-PASS 3-POLE)	> 500 kHz	UNIT
GND	0.8	1	1.8	4.6	μV_{RMS}
2.2 µF (ceramic)	42.5	47.2	61.2	68.3	
2.2 µF + 1 µF	17.5	19.4	22.6	24.5	
10 µF (ceramic)	34.4	35.6	37.7	44.5	
10 µF + 1 µF	14.1	14.4	14.9	16.4	
20 µF (ceramic)	34.8	34.9	35.1	35.2	
20 µF + 1 µF	14.4	14.4	14.7	15.1	

Adding a 1-µF capacitor in this example filters the noise contribution of the bandgap and lowers the total noise by a factor of 2.5 times.

8.3 System Example

8.3.1 Data Acquisition

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 32 shows the REF5040 in a basic data acquisition system.

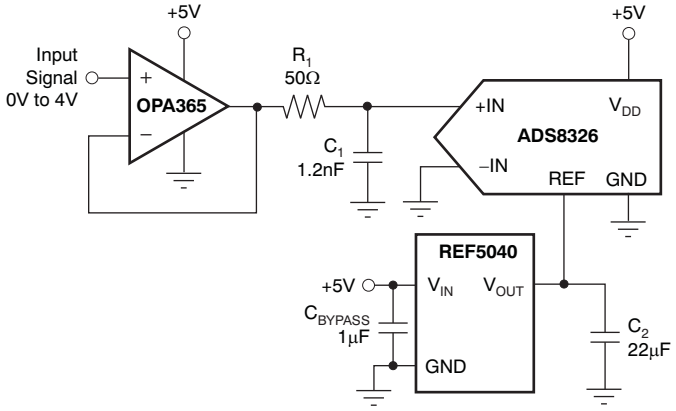


Figure 32. Basic Data Acquisition System

During the design of the data acquisition system, equal consideration must be given to the buffering analog input signal as well as the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement, but does not ensure the maximum performance.

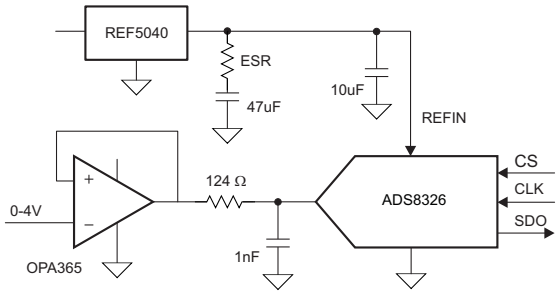


Figure 33. Complete Data Acquisition System Using REF50xx

Three measurements using different components of the output are shown for this data acquisition system.

System Example (continued)

Table 3. Data Acquisition Measurement Results for Different Conditions

OPA365 REF5040 TRIM	124 Ω, 1 nF 10 µF 0 µF	124 Ω, 1 nF 10 µF + 47 µF 1 µF	124 Ω, 100 µF 10 µF + 47 µF 1 µF	UNIT
Resolution	16	16	16	Bits
States	65536	65536	65536	
V_{REF}	4.096	4.096	4.096	V
LSB	62.5	62.5	62.5	µV
V_{IN}	4.02	4.02	4.02	V
Data Std	1.07	0.53	0.41	LSB
Noise	67.0	33.4	25.8	μV_{RMS}
Noise	442.3	220.5	170.2	μV_{PP}
SNR	86.7	92.8	95.0	dB
FTT Points	32768	32768	32768	
Noise Flor	–128.8	–134.9	–131.7	dB

Once the correct components for data acquisition system from Figure 33 are selected, measurement results can be compared to the ADS8326 data sheet specifications.

Table 4. AC Performance for Data Acquisition System from Figure 33

REF5040 TRIM	ADS8326 DATA SHEET	ADS8326B DATA SHEET	SYSTEM LOW ESR	SYSTEM 10 µF + 47 µF 1µF	UNIT
SNR	91	91.5	90.6	92.2	dB
SINAD	87.5	88	85.7	89.5	dB
SFDR	94	95	88.3	98.4	dB
THD	–90	–91	–87.3	–92.9	dB
ENOB	14.28	14.35	13.94	14.58	Bits

Table 3 shows improvements on the FFT for a properly designed system.

9 Power Supply Recommendations

The maximum voltage drop between the input and output pin is 0.2 V. The minimum power supply voltage for the specific REF50xx device depends on the value of the output voltage, (V_{INMIN} = V_{OUT} + 0.2 V). The exception to this rule is the REF5020, which requires a minimum 2.7-V power supply for proper operation. The maximum power supply voltage for the REF50xx series is 18 V. TI recommends adding a bypass capacitor of 1 µF to 10 µF at the input to compensate for the layout and power supply source impedance.

9.1 Basic Connections

Figure 34 shows the typical connections for the REF50xx. TI recommends a supply bypass capacitor ranging from 1 µF to 10 µF. A 1-µF to 50-µF output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value of C_L must be less than or equal to 1.5 Ω to ensure output stability. To minimize noise, the recommended ESR of C_L is between 1 Ω and 1.5 Ω.

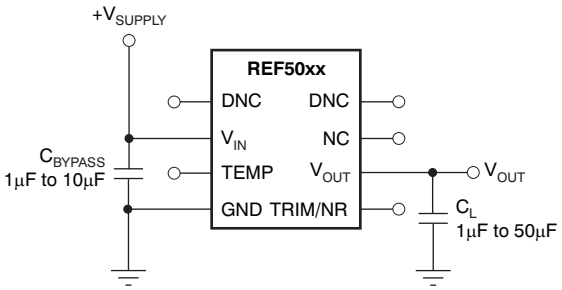


Figure 34. Basic Connections

9.2 Low Dropout Voltage

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7 V, these references can be operated with a supply of 200 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 6 in *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the VIN pin and ground pins. The recommended value of this bypass capacitor is 1 µF to 10 µF. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Place a 1-µF noise filtering capacitor between the NR pin and ground.
- The output must be decoupled with a 1-µF to 50-µF capacitor. In series with load capacitor, add an ESR of 1 Ω for the best noise performance.
- A high-frequency, 1-µF capacitor can be added in parallel between the output and ground to filter noise and help with switching loads as data converters.

10.2 Layout Example

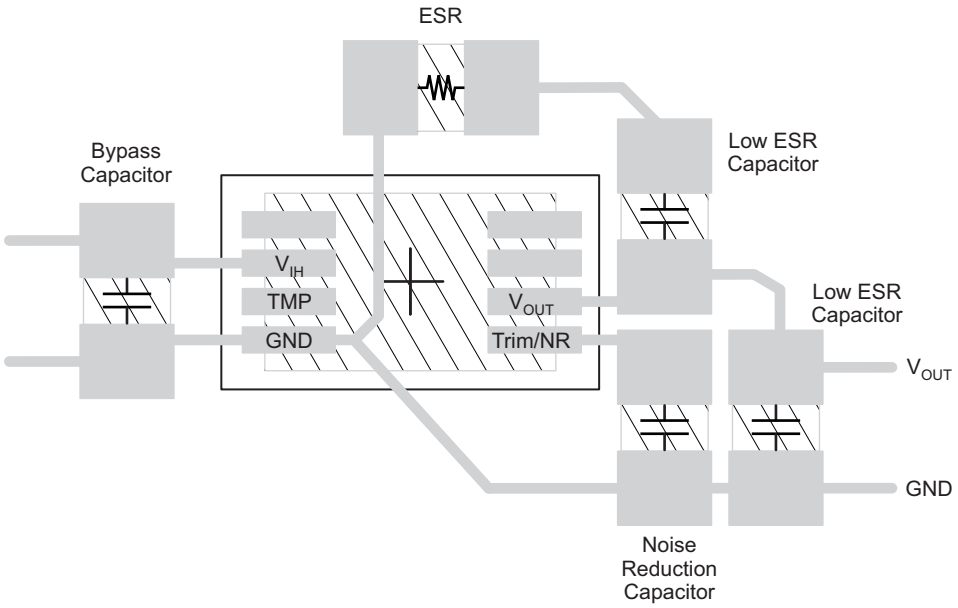


Figure 35. Recommended Layout for REF50xx

10.3 Power Dissipation

The REF50xx family is specified to deliver current loads of ±10 mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- T_J = Junction temperature (°C)
- T_A = Ambient temperature (°C)
- P_D = Power dissipated (W)
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W) (3)

The REF50xx junction temperature must not exceed the absolute maximum rating of 150°C.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *0.05uV/degC (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier*, SBOS282
- REF5020 PSpice Model, SLIM160
- REF5020 TINA-TI Reference Design, SLIM159
- REF5020 TINA-TI Spice Model, SLIM158
- INA270 PSpice Model, SBOM485
- INA270 TINA-TI Reference Design, SBOC246
- INA270 TINA-TI Spice Model, SBOM306

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REF5020-EP	Click here	Click here	Click here	Click here	Click here
REF5025-EP	Click here	Click here	Click here	Click here	Click here
REF5040-EP	Click here	Click here	Click here	Click here	Click here
REF5050-EP	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF5020MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5020EP
REF5020MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5020EP
REF5025MDTEP	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5025EP
REF5025MDTEP.A	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5025EP
REF5040MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5040EP
REF5040MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5040EP
REF5050MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5050EP
REF5050MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5050EP
V62/10613-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5020EP
V62/10613-02XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5040EP
V62/10613-03XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5050EP
V62/10613-04XE	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5025EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

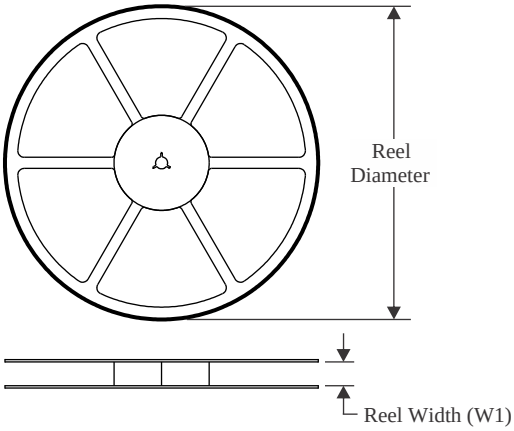
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF REF5025-EP :

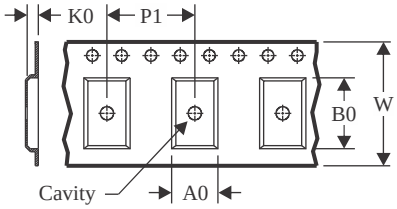
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

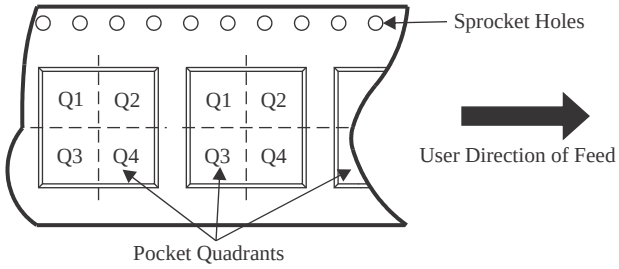


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

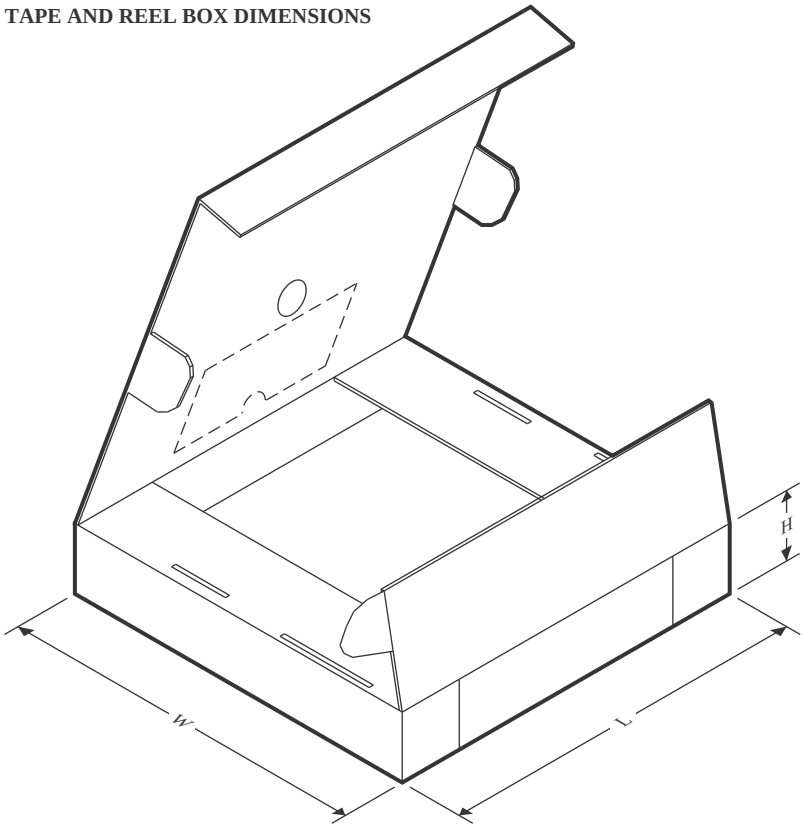
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

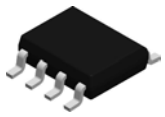
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5020MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025MDTEP	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5020MDREP	SOIC	D	8	2500	353.0	353.0	32.0
REF5025MDTEP	SOIC	D	8	250	213.0	191.0	35.0
REF5040MDREP	SOIC	D	8	2500	353.0	353.0	32.0
REF5050MDREP	SOIC	D	8	2500	353.0	353.0	32.0

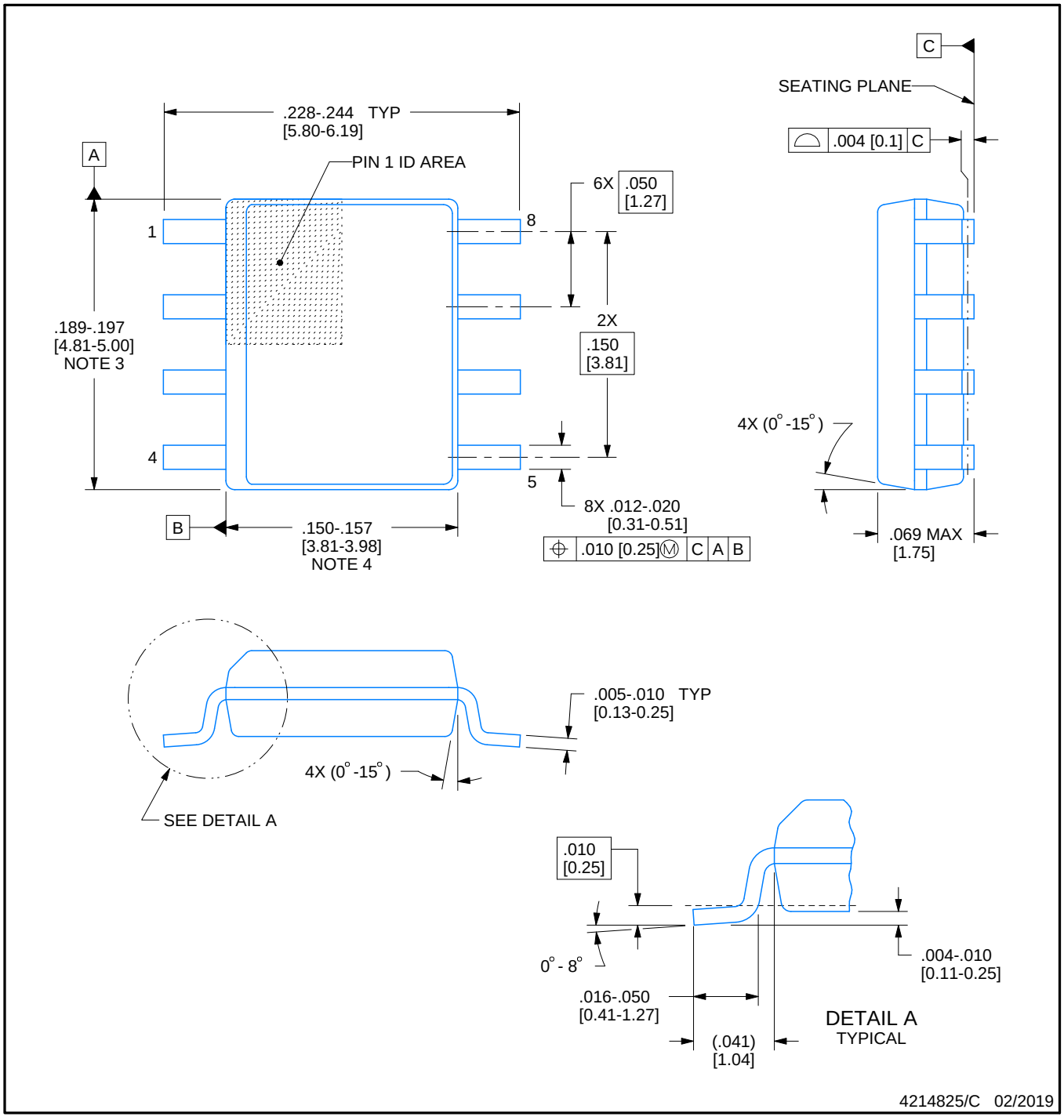


PACKAGE OUTLINE

D0008A

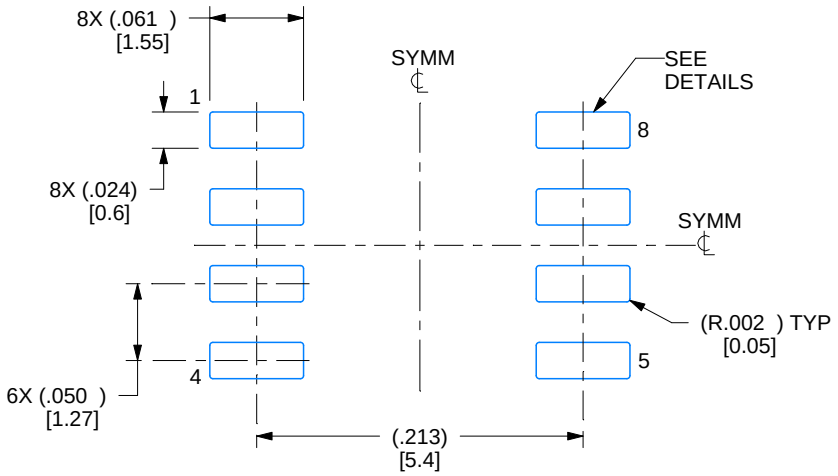
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

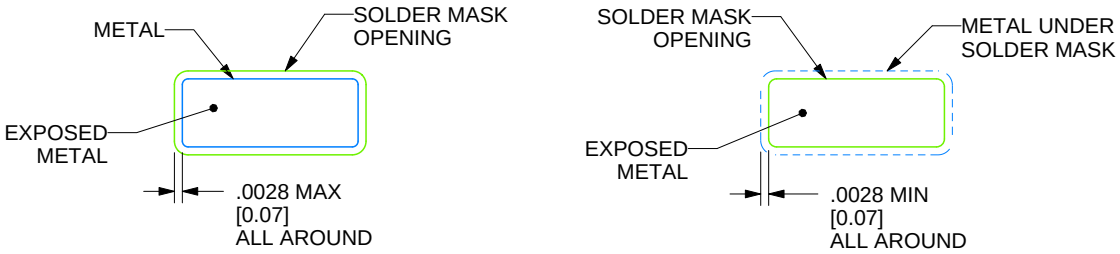


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

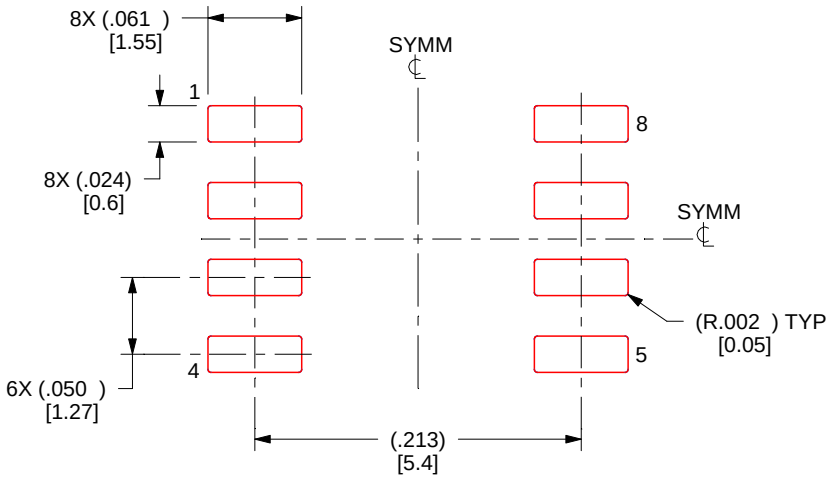
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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