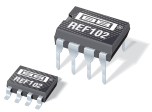


SBVS022B – SEPTEMBER 2000 – REVISED JUNE 2009

10V Precision Voltage Reference

FEATURES

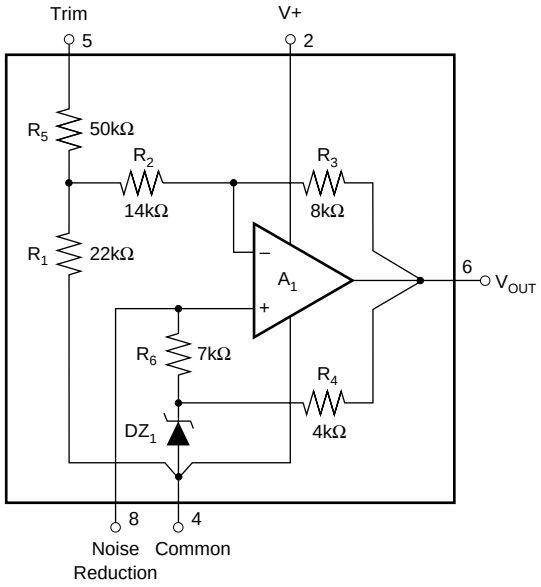
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μV_{PP} typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage	+40V
Operating Temperature	
P, U	–25°C to +85°C
Storage Temperature Range	
P, U	–40°C to +125°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

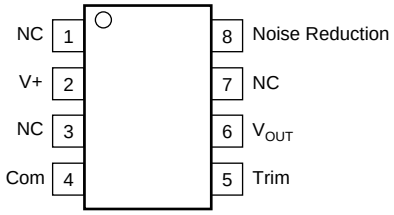
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
REF102AU	±10	±10	SO-8	D	REF102AU
REF102AP	±10	±10	DIP-8	P	REF102AP
REF102BU	±5	±5	SO-8	D	REF102BU
REF102BP	±5	±5	DIP-8	P	REF102BP
REF102CU	±2.5	±2.5	SO-8	D	REF102CU
REF102CP	±2.5	±2.5	DIP-8	P	REF102CP

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP, SO**



NC = Not Connected

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = +15V power supply, unless otherwise noted.

		REF102A			REF102B			REF102C			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature [1]				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = +25°C										
M Package			5			*			*		ppm/1000hr
P, U Packages [2]			20			*					ppm/1000hr
Trim Range [3]		±3			*			*			%
Capacitive Load, max			1000			*			*		pF
NOISE	0.1Hz to 10Hz		5			*			*		μV_{PP}
OUTPUT CURRENT		+10, –5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	I_{OUT} = 0			+1.4			*			*	mA
WARM-UP TIME [4]	To 0.1%		15			*			*		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	*		*	*		*	°C

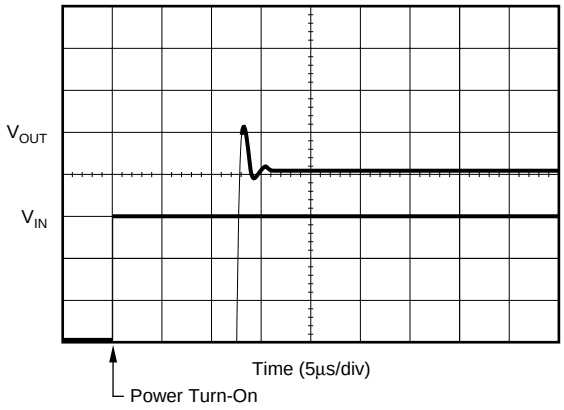
* Specifications same as REF102A.

NOTES: (1) The *box* method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.
(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
(4) With noise reduction pin floating. See Typical Characteristics for details.

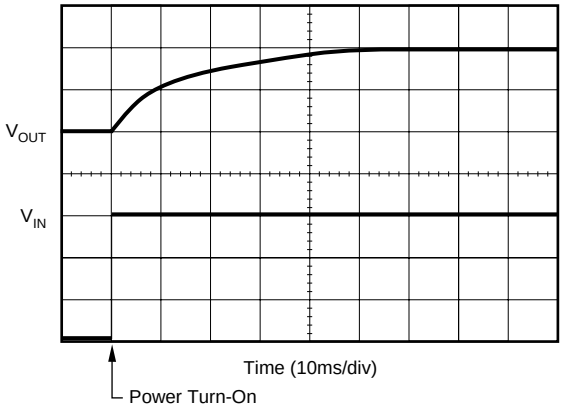
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +15V, unless otherwise noted.

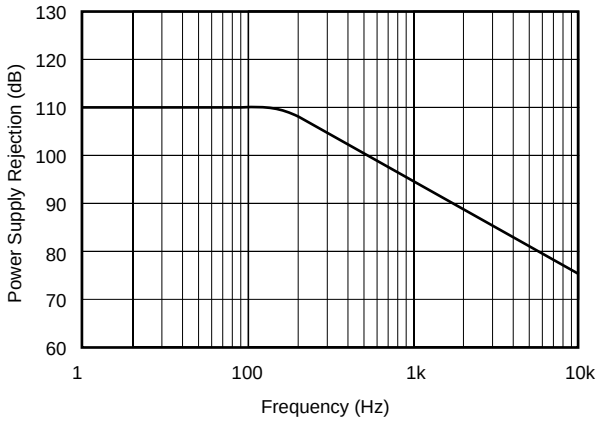
POWER TURN-ON RESPONSE



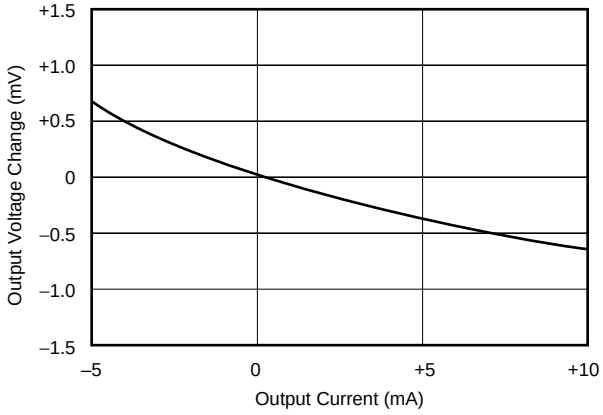
POWER TURN-ON RESPONSE with 1µF C_N



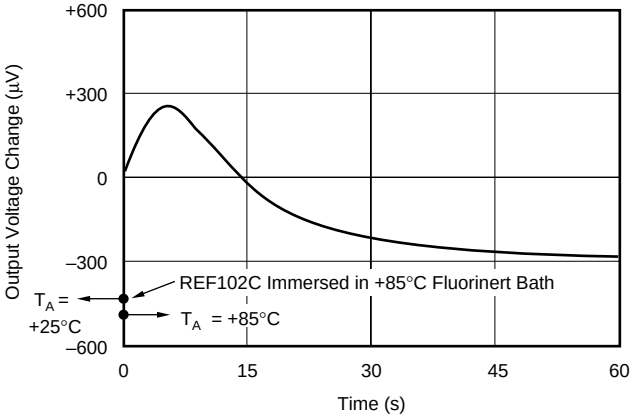
POWER SUPPLY REJECTION vs FREQUENCY



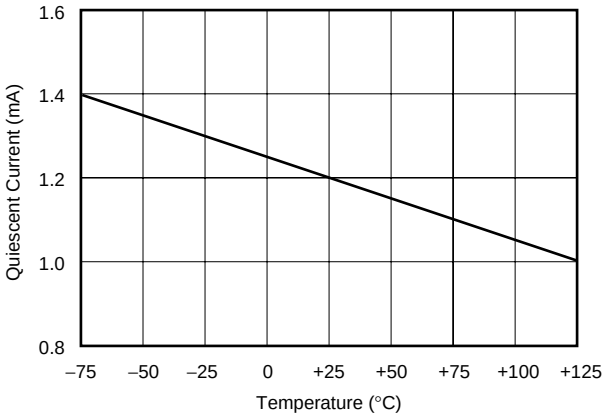
LOAD REGULATION



RESPONSE TO THERMAL SHOCK



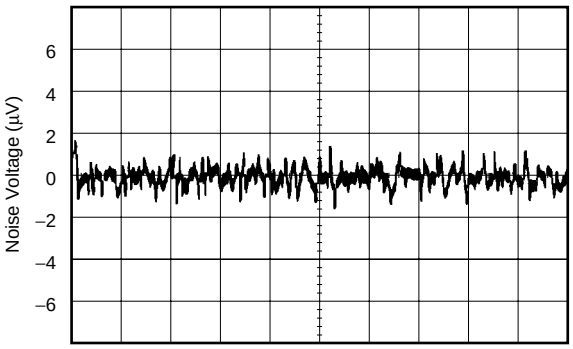
QUIESCENT CURRENT vs TEMPERATURE



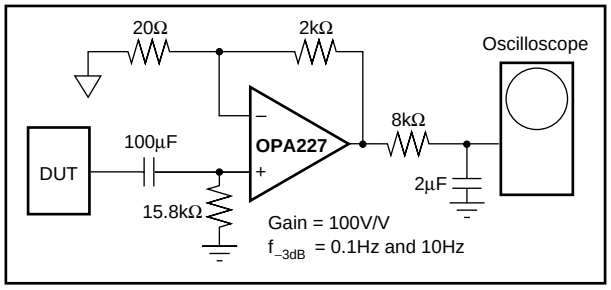
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +15V, unless otherwise noted.

TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s/div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network $R_1 – R_6$.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of of R_5 closely matches the TCR of R_1, R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the *butterfly method* and the *box method*. The REF102 is specified by the more commonly-used *box method.* The *box* is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The *box* height, V_1 to V_2, is 2.75mV.

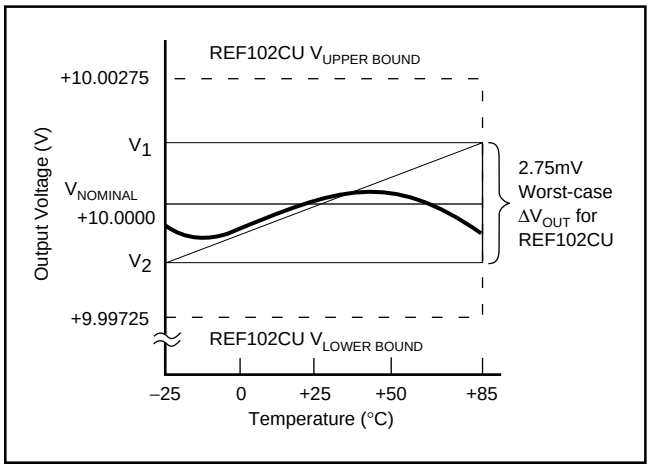
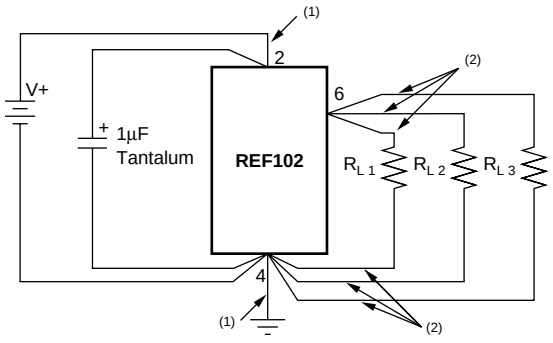


FIGURE 1. REF102CU Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

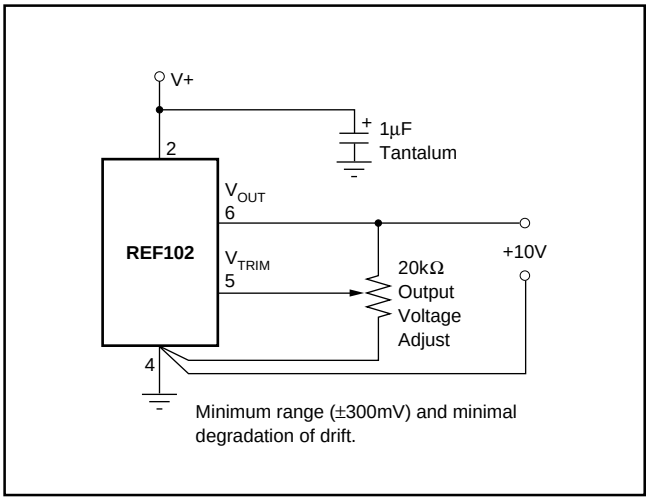


FIGURE 3. REF102 Optional Output Voltage Adjust.

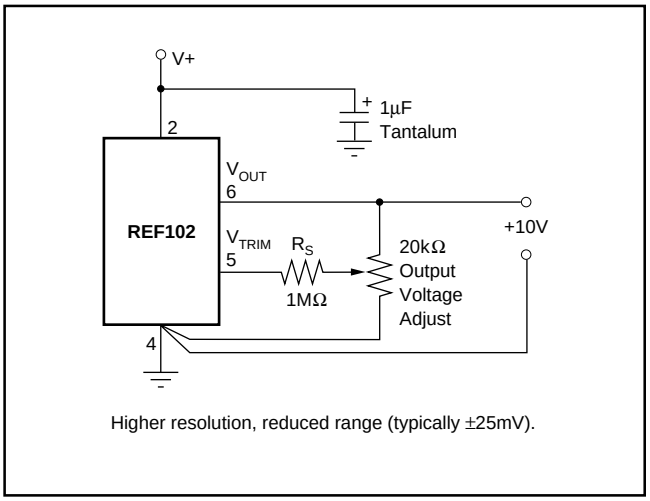


FIGURE 4. REF102 Optional Output Voltage, Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with R_6 (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high-frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about $800\mu V_{PP}$ to under $200\mu V_{PP}$. If further noise reduction is required, use the circuit in Figure 14.

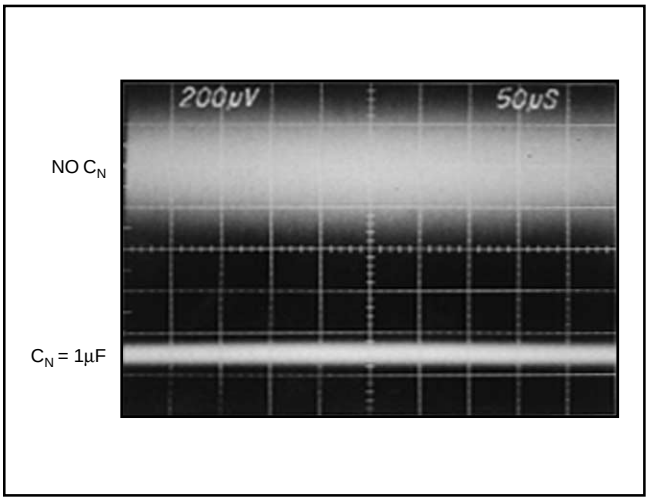


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

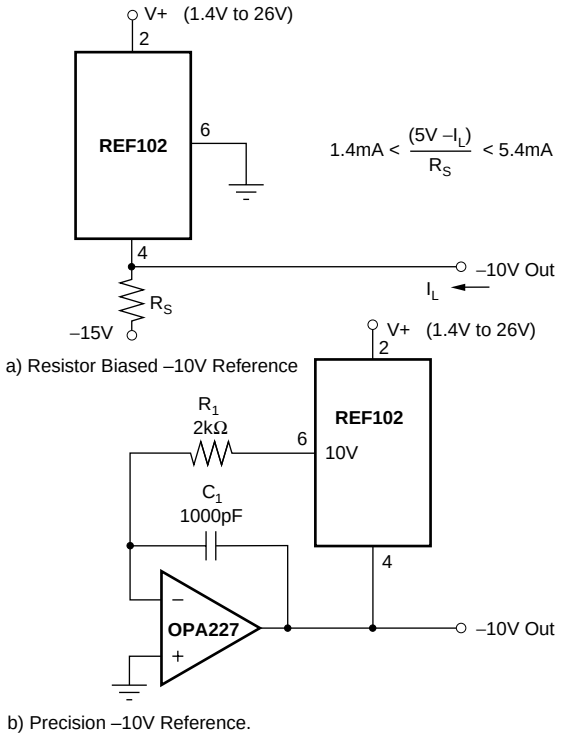


FIGURE 6. –10V Reference Using a) Resistor or b) OPA227.

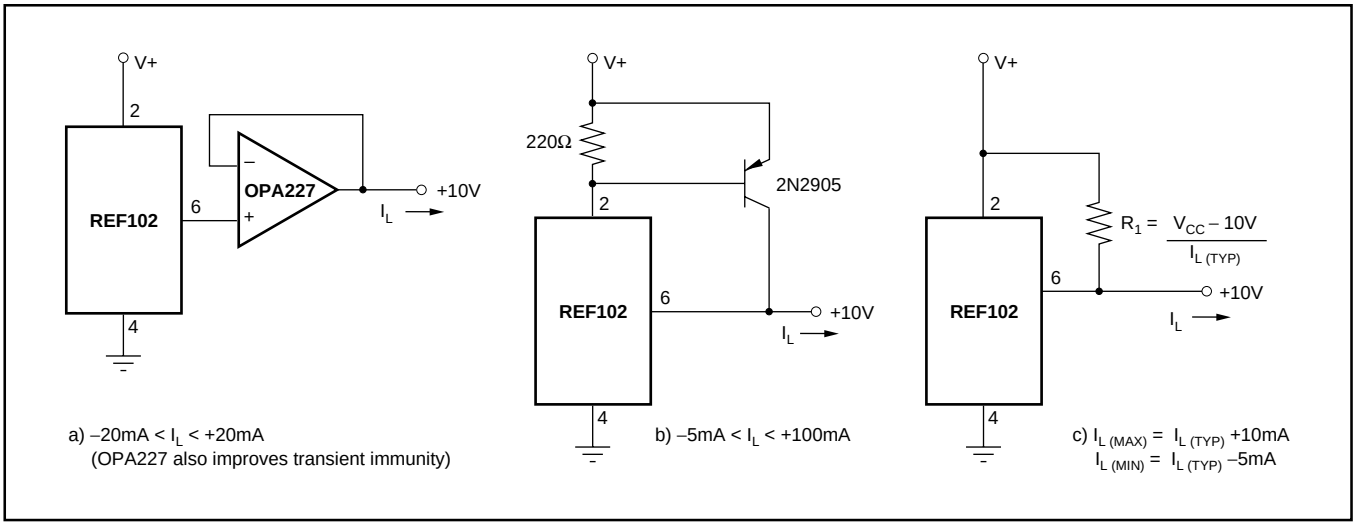


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\ (TYP)}$ +10mA, –5A.

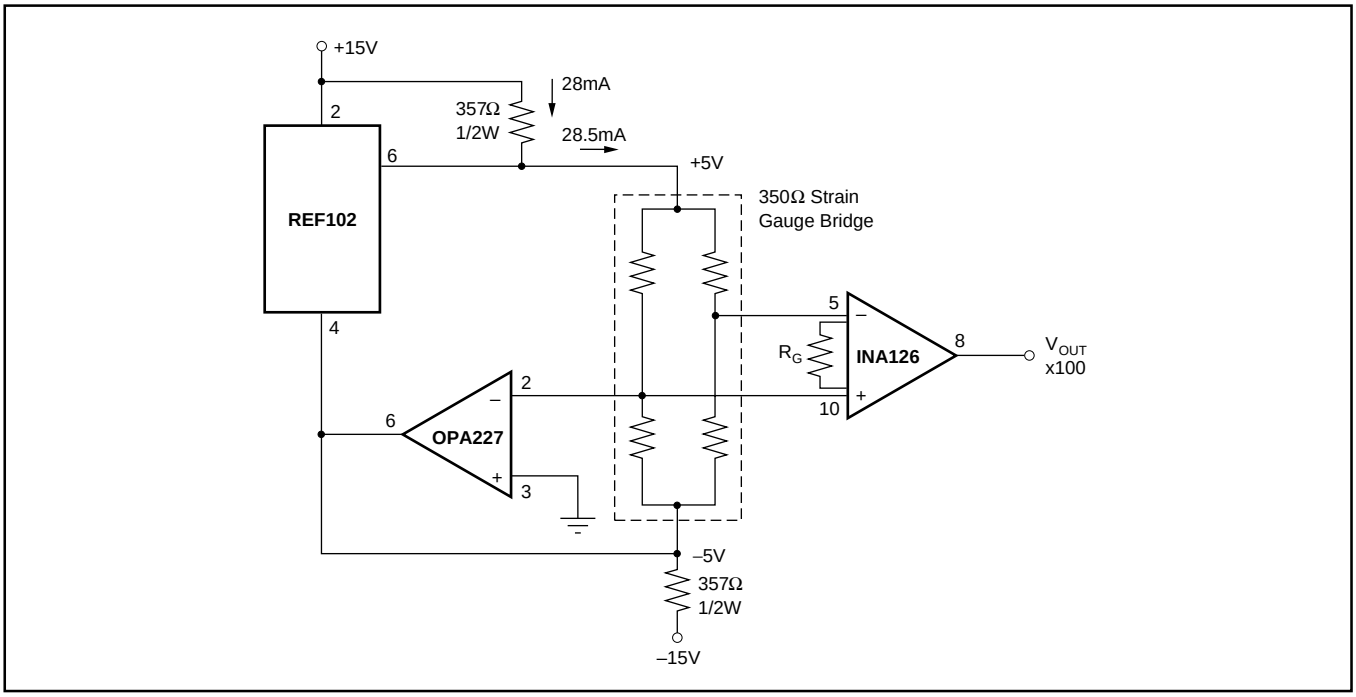


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

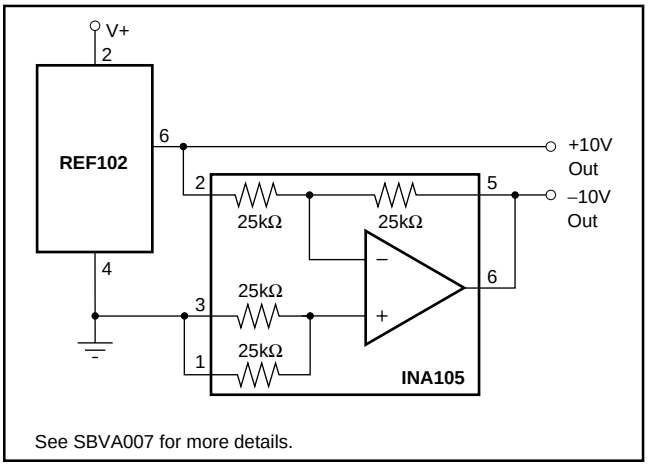


FIGURE 9. ±10V Reference.

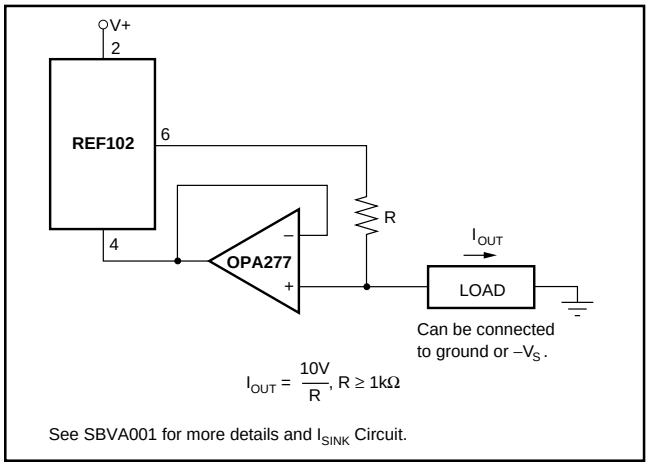
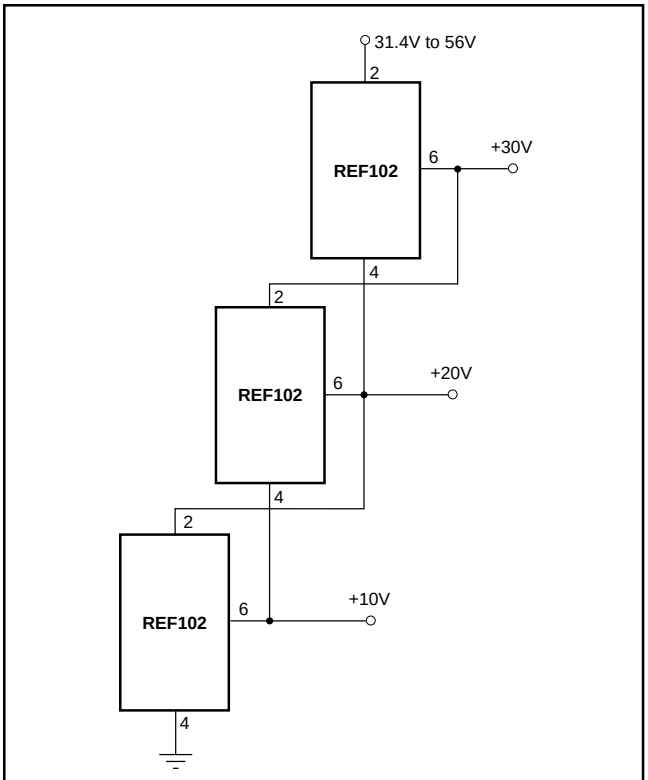


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where *n* is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

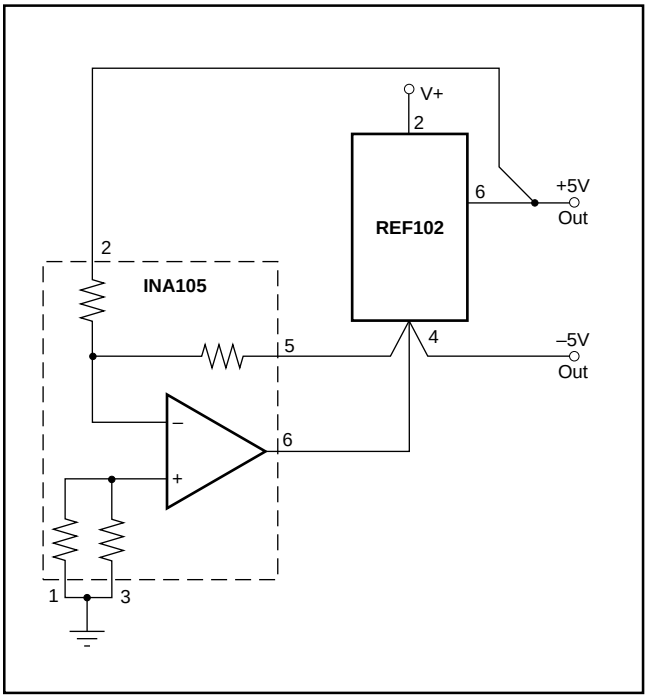


FIGURE 12. ±5V Reference.

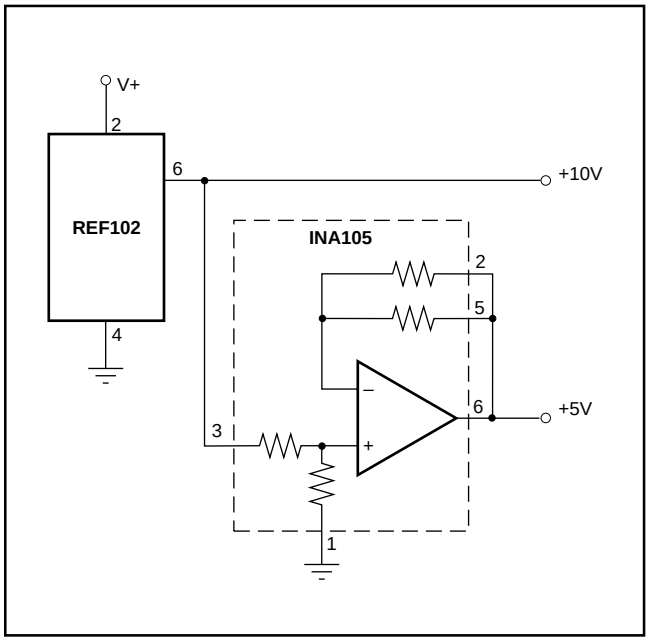


FIGURE 13. +5V and +10V Reference.

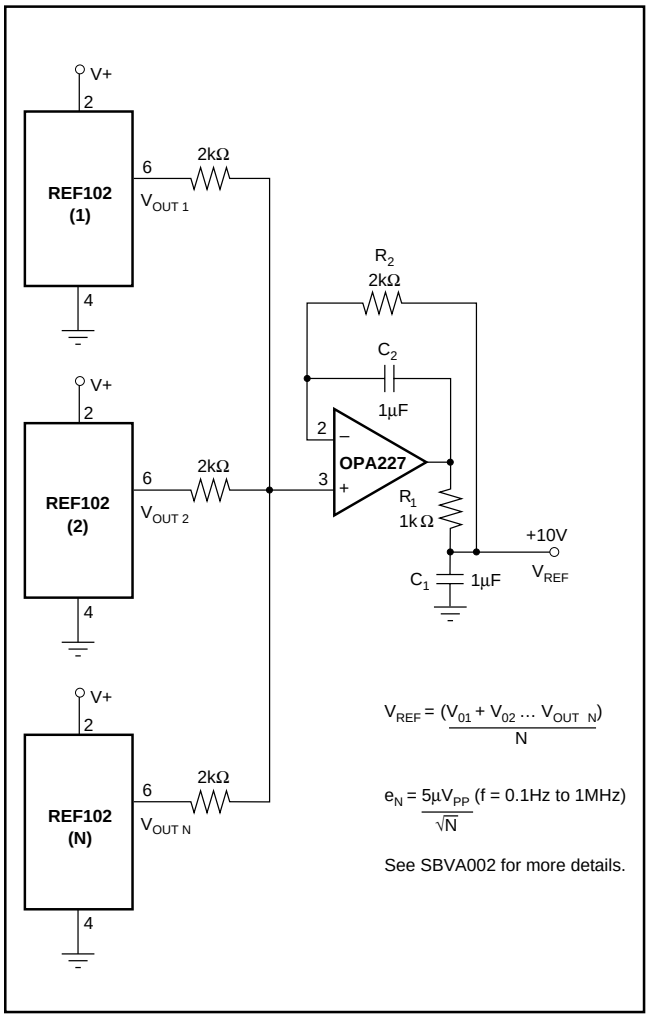


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/09	B	2	Absolute Maximum Ratings	Deleted lead temperature rating.
			Package/Ordering Information	Changed Package Ordering Information table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF102AU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-	REF 102U A
REF102AU.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U A
REF102AU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	REF 102U A
REF102AU/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U A
REF102BU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B
REF102BU.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B
REF102CU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C
REF102CU.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C
REF102CU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-25 to 85	REF 102U C
REF102CU/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-25 to 85	REF 102U C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

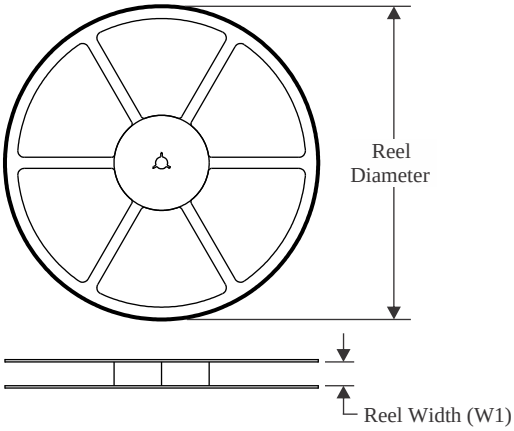
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

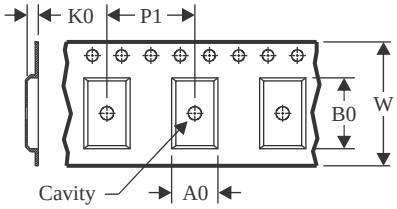
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

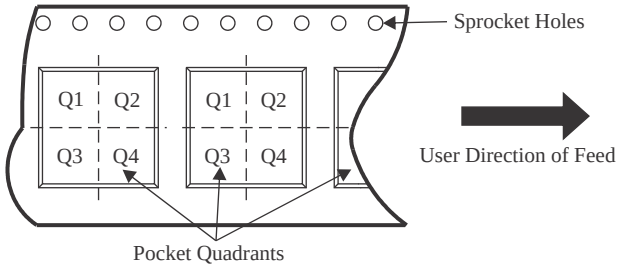


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

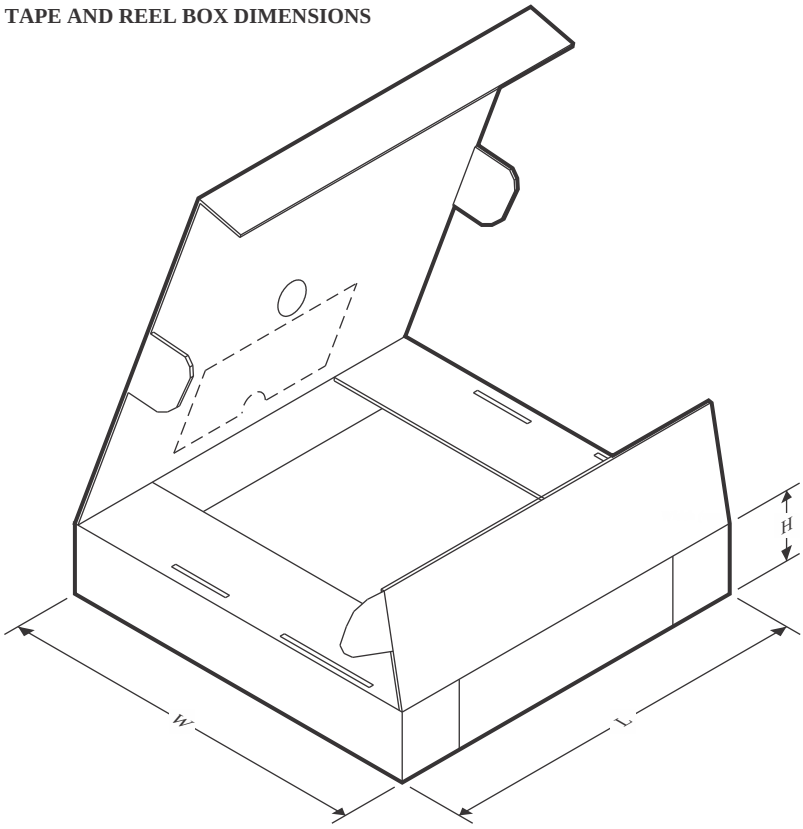
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF102AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF102CU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

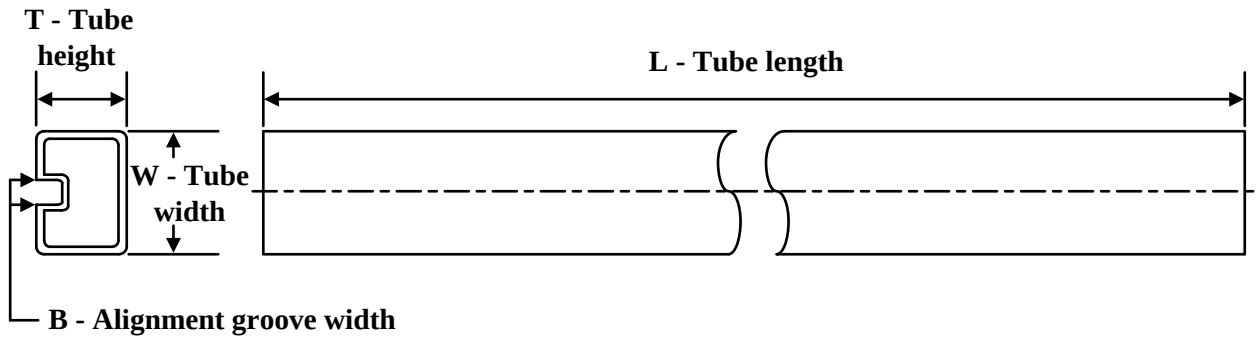
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

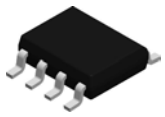
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF102AU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
REF102CU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
REF102AU	D	SOIC	8	75	506.6	8	3940	4.32
REF102AU.A	D	SOIC	8	75	506.6	8	3940	4.32
REF102BU	D	SOIC	8	75	506.6	8	3940	4.32
REF102BU.A	D	SOIC	8	75	506.6	8	3940	4.32
REF102CU	D	SOIC	8	75	506.6	8	3940	4.32
REF102CU.A	D	SOIC	8	75	506.6	8	3940	4.32

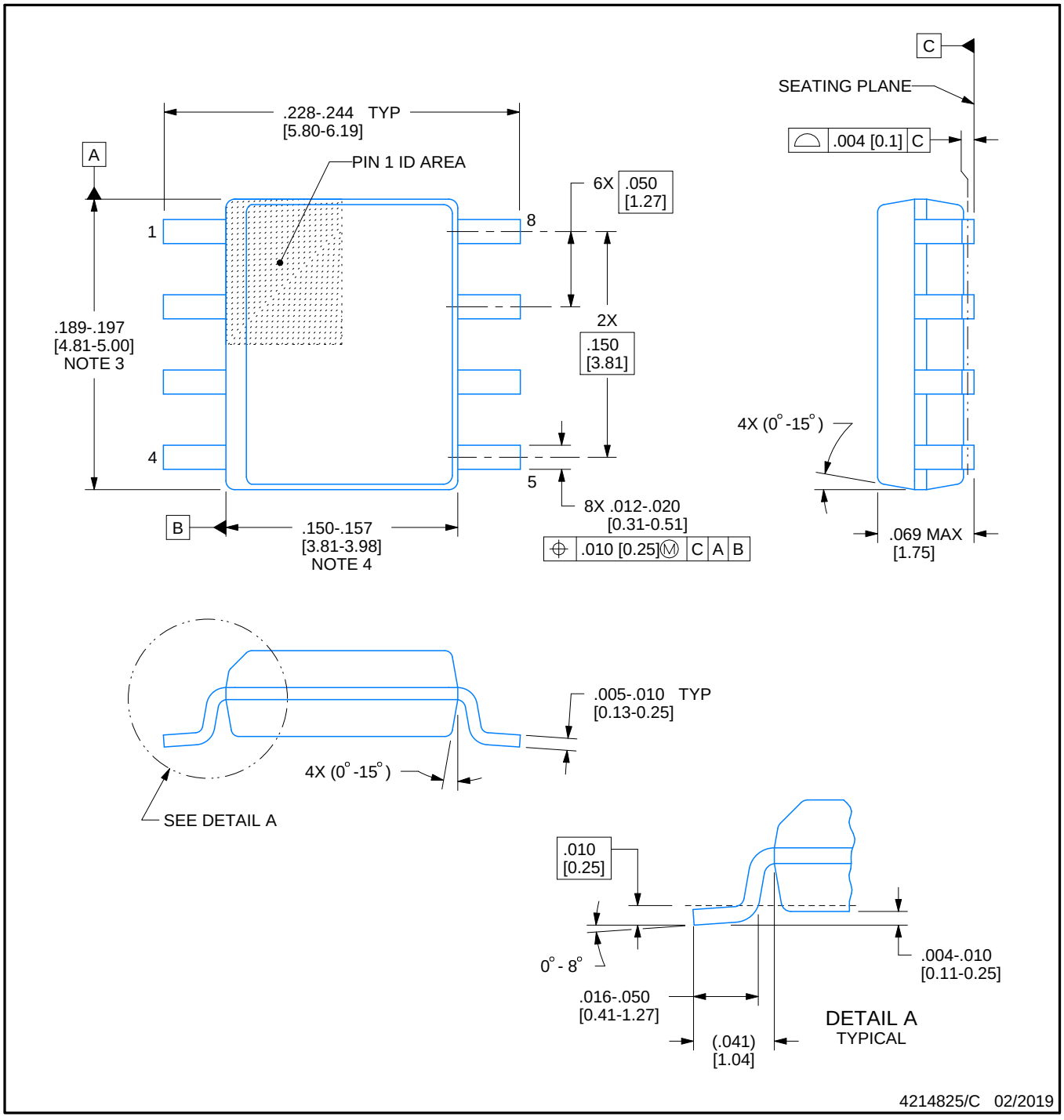


PACKAGE OUTLINE

D0008A

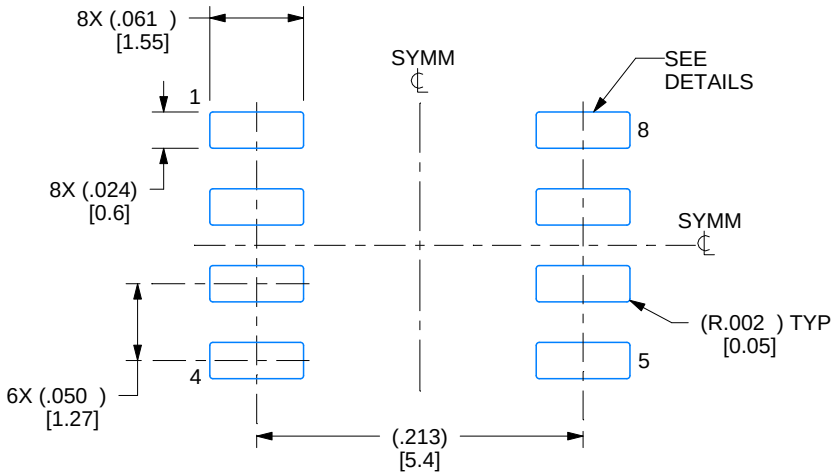
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

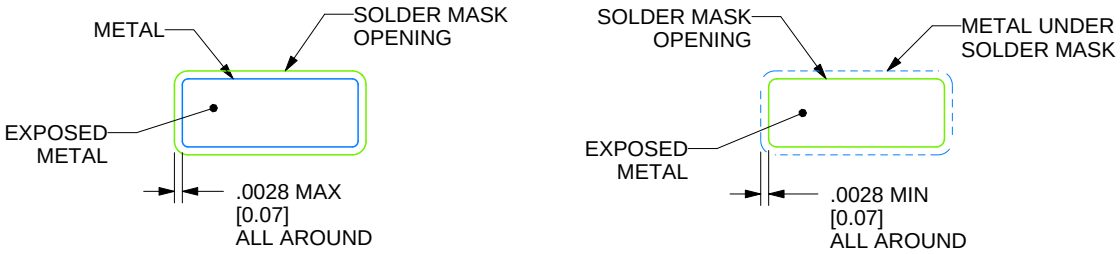


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

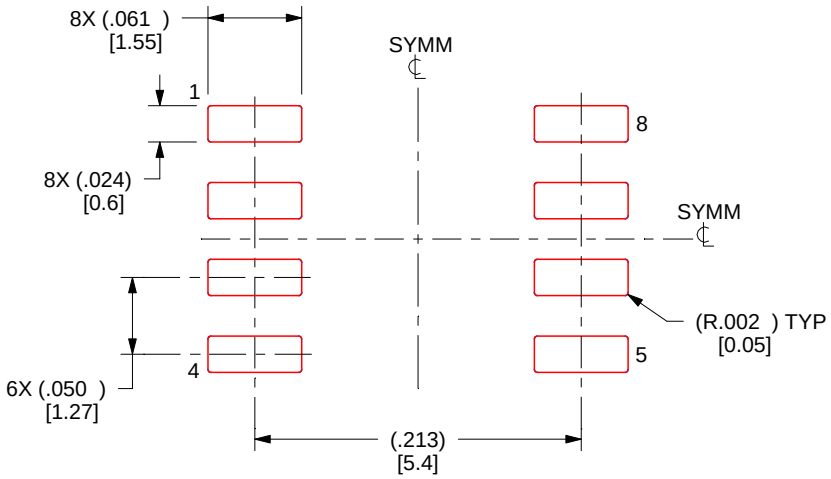
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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