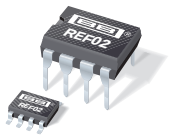


SBVS003B – JANUARY 1993 – REVISED JANUARY 2005

+5V Precision VOLTAGE REFERENCE

FEATURES

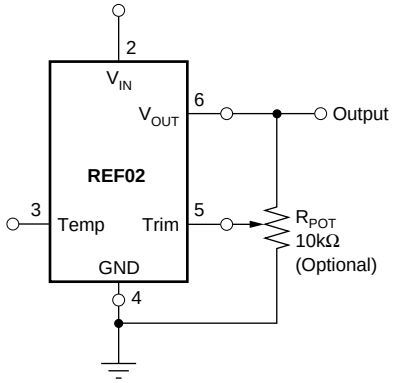
- **OUTPUT VOLTAGE: +5V ±0.2% max**
- **EXCELLENT TEMPERATURE STABILITY: 10ppm/°C max (–40°C to +85°C)**
- **LOW NOISE: 10μV_{PP} max (0.1Hz to 10Hz)**
- **EXCELLENT LINE REGULATION: 0.01%/V max**
- **EXCELLENT LOAD REGULATION: 0.008%/mA max**
- **LOW SUPPLY CURRENT: 1.4mA max**
- **SHORT-CIRCUIT PROTECTED**
- **WIDE SUPPLY RANGE: 8V to 40V**
- **INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C**
- **PACKAGE OPTIONS: DIP-8, SO-8**

APPLICATIONS

- **PRECISION REGULATORS**
- **CONSTANT CURRENT SOURCE/SINK**
- **DIGITAL VOLTMETERS**
- **V/F CONVERTERS**
- **A/D AND D/A CONVERTERS**
- **PRECISION CALIBRATION STANDARD**
- **TEST EQUIPMENT**

DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 10ppm/°C max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a ±6% range with minimal effect on temperature stability. The REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. Available package options are DIP-8 and SO-8. The REF02 is an ideal choice for portable instrumentation, temperature transducers, Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters, and digital voltmeters.



+5V Reference with Trimmed Output

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{IN} = +15V power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF02A			REF02B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE Change with Temperature[1, 2] (ΔV_{OT}) –40°C to +85°C	I_{LOAD} = 0mA	4.985	5.0 0.05	5.015 0.19	4.990	* 0.05	5.010 0.13	V %
OUTPUT VOLTAGE DRIFT[3] –40°C to +85°C (TCV_O)			4	15		4	10	±ppm/°C
LONG-TERM STABILITY First 1000h Second 1000h	2000h Test		 100 50			 100 50		 ±ppm ±ppm
OUTPUT ADJUSTMENT RANGE	R_{POT} = 10kΩ[6]	±3	±6		*	*		%
CHANGE IN V_O TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (–55°C to +125°C)	R_{POT} = 10kΩ		0.7			*		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz[5]		4	10		*	*	μV_{PP}
LINE REGULATION[4] –40°C to +85°C	V_{IN} = 8V to 33V V_{IN} = 8.5V to 33V		0.006 0.008	0.010 0.012		* *	* *	%/V
LOAD REGULATION[4] –40°C to +85°C	I_L = 0mA to +10mA I_L = 0mA to +10mA		0.005 0.007	0.010 0.012		* *	0.008 0.010	%/mA
TURN-ON SETTLING TIME	To ±0.1% of Final Value		5			*		µs
QUIESCENT CURRENT	No Load		1.0	1.4		*	*	mA
LOAD CURRENT (SOURCE)		10	21		*	*		mA
LOAD CURRENT (SINK)		–0.3	–0.5		*	*		mA
SHORT-CIRCUIT CURRENT	V_{OUT} = 0		30			*		mA
POWER DISSIPATION	No Load		15	21		*	*	mW
TEMPERATURE VOLTAGE OUTPUT[7]			630			*		mV
TEMPERATURE COEFFICIENT of Temperature Pin Voltage –55°C to +125°C			 2.1					 mV/°C
TEMPERATURE RANGE Specification REF02A, B, C		 –40		 +85	 *		 *	 °C

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_O = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

(2) ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

(3) TCV_O is defined as ΔV_{OT} divided by the temperature range.

(4) Line and load regulation specifications include the effect of self heating.

(5) Sample tested.

(6) 10kΩ potentiometer connected between V_{OUT} and ground with wiper connected to Trim pin. See figure on page 1.

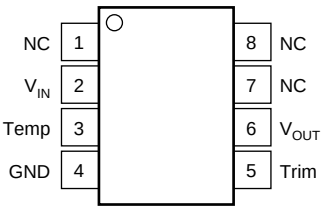
(7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each µA of loading.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
P, U	–40°C to +85°C
Storage Temperature Range	
P, U	–65°C to +125°
Output Short Circuit Duration (to Ground or V_{IN})	Indefinite
Junction Temperature	–65°C to +150°
θ_{JA} P	120°C/W
U	80°C/W
Lead Temperature (soldering, 60s)	+300°C

PIN CONFIGURATIONS

Top View **DIP/SO**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

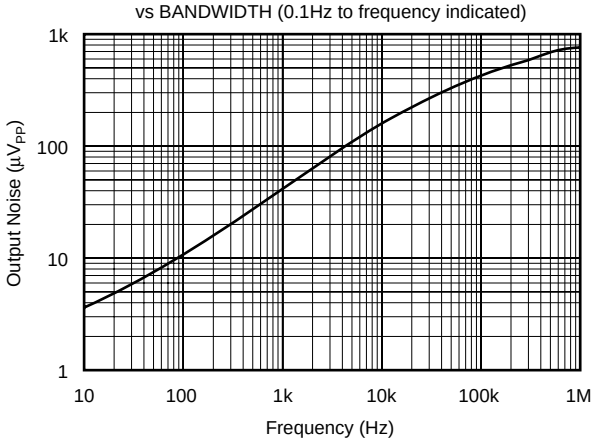
PRODUCT	V_{OUT} at 25°C	MAX DRIFT (ppm/°C)	PACKAGE	PACKAGE DRAWING DESIGNATOR	SPECIFICATION TEMPERATURE RANGE
REF02AU	5V±15mV	±15	SO-8	D	–40°C to +85°C
REF02BU	5V±10mV	±10	SO-8	D	–40°C to +85°C
REF02AP	5V±15mV	±15	DIP-8	P	–40°C to +85°C
REF02BP	5V±10mV	±10	DIP-8	P	–40°C to +85°C

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

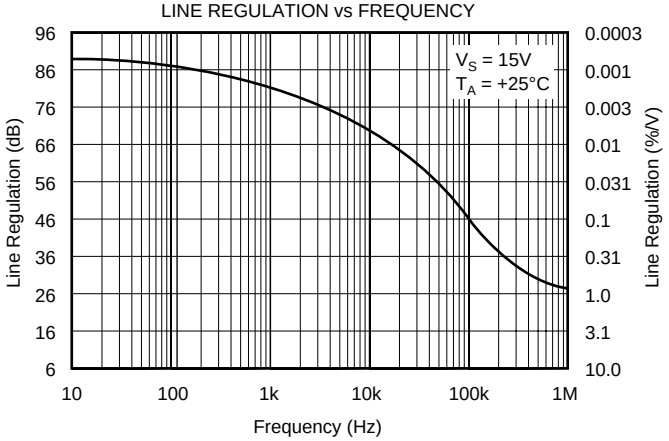
TYPICAL PERFORMANCE CURVES

AT T_A = +25°C, unless otherwise noted.

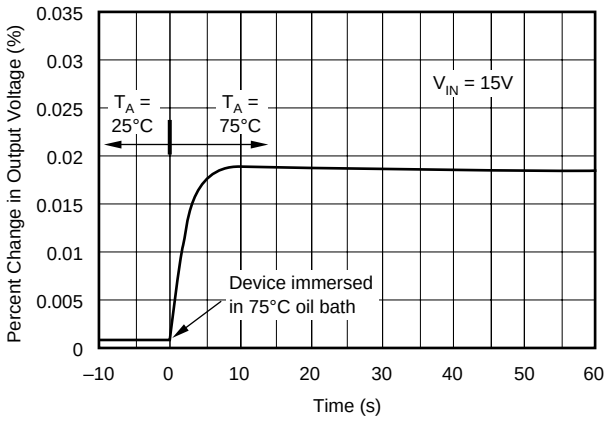
OUTPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz to frequency indicated)



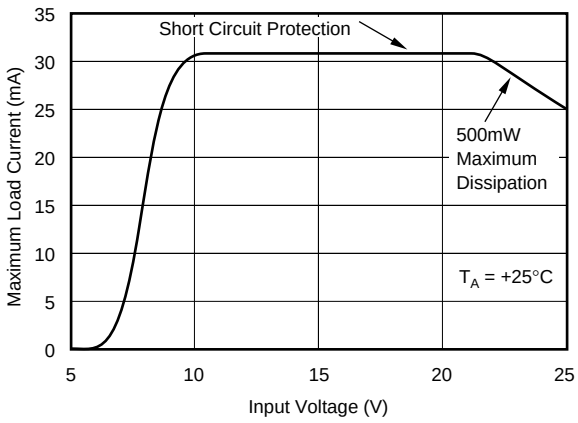
LINE REGULATION vs FREQUENCY



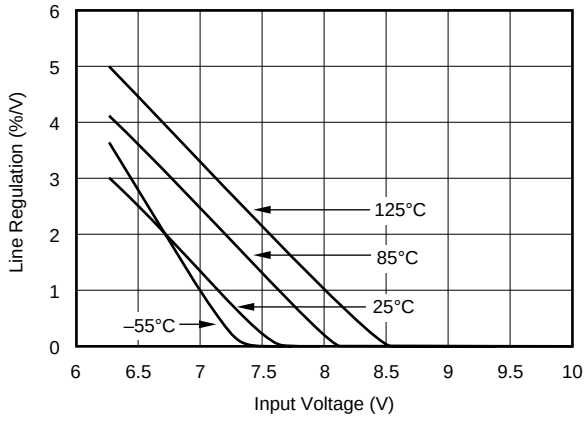
OUTPUT CHANGE DUE TO THERMAL SHOCK



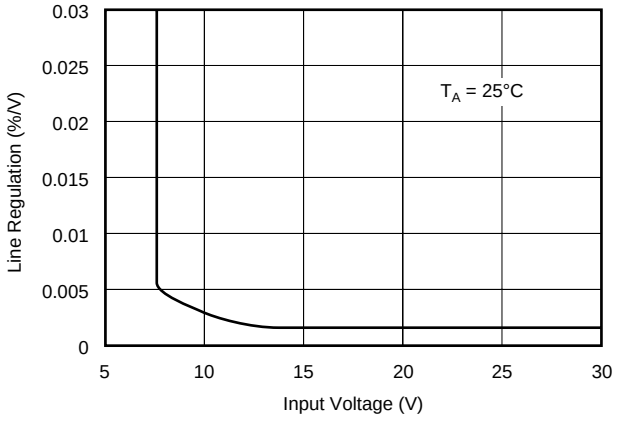
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



LINE REGULATION vs SUPPLY VOLTAGE



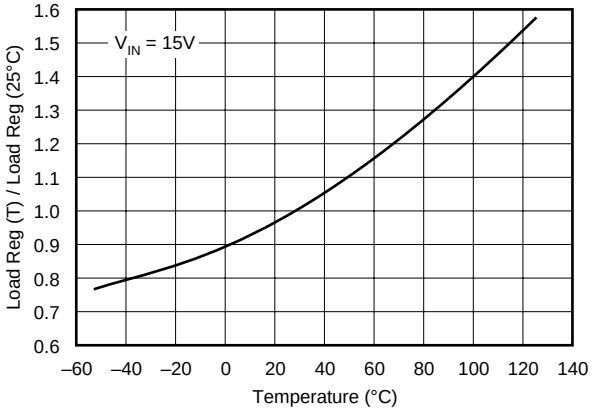
LINE REGULATION vs SUPPLY VOLTAGE



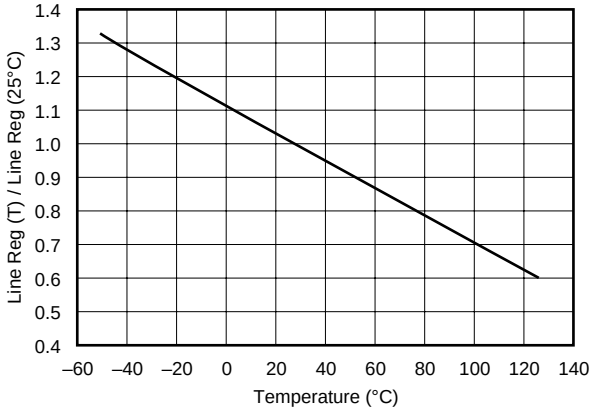
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, unless otherwise noted.

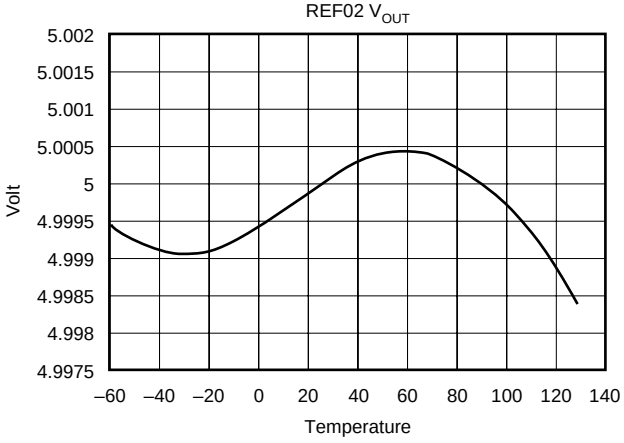
NORMALIZED LOAD REGULATION (ΔIL = 10mA) vs TEMPERATURE



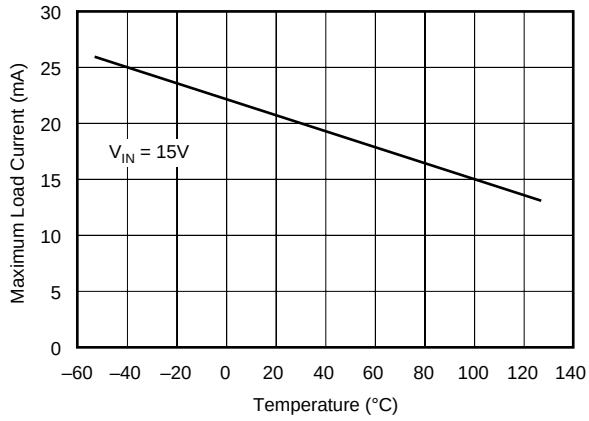
NORMALIZED LINE REGULATION vs TEMPERATURE



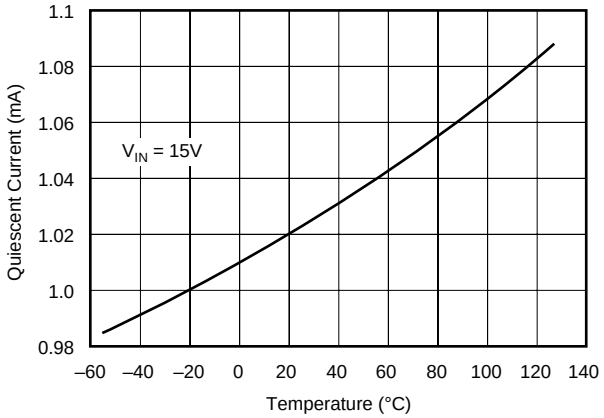
REF02 V_{OUT}



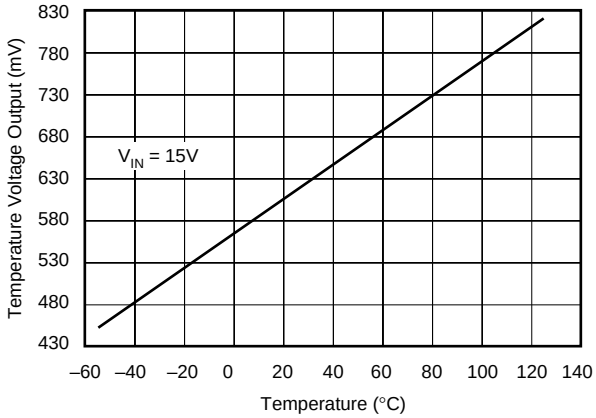
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



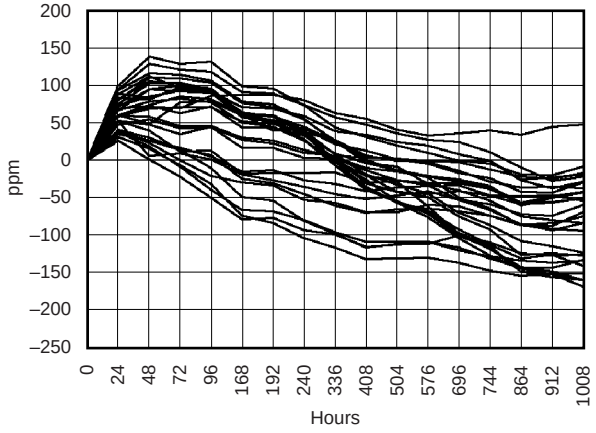
TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE



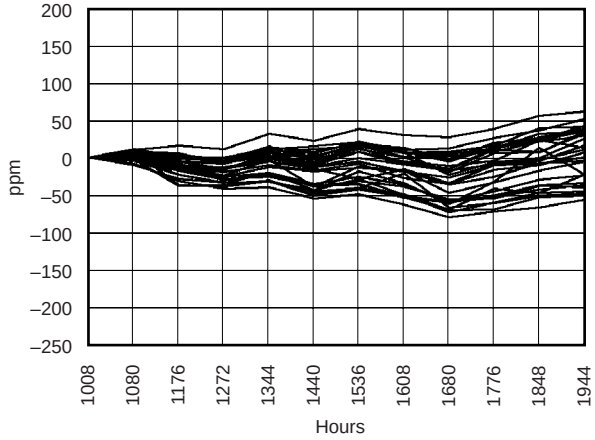
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, unless otherwise noted.

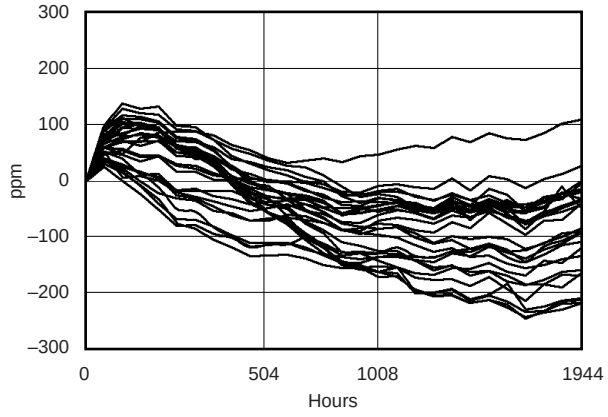
LONG-TERM STABILITY (1st 1000h)



LONG-TERM STABILITY (2nd 1000h)



LONG TERM STABILITY (2000h)



OUTPUT ADJUSTMENT

The REF02 trim terminal can be used to adjust the voltage over a 5V ±150mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V, including 5.12V(1) for binary applications (see circuit on page 1).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment.

NOTE: (1) 20mV LSB for 8-bit applications.

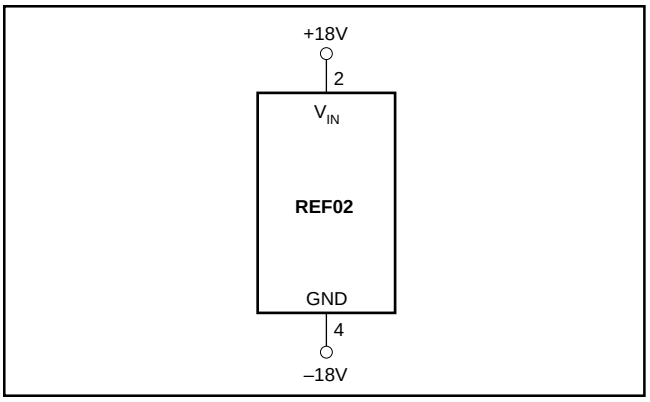


FIGURE 1. Burn-In Circuit.

REFERENCE STACKING PROVIDES OUTSTANDING LINE REGULATION

By stacking two REF01s and one REF02, a systems designer can achieve 5V, 15V, and 25V outputs. One very important advantage of this circuit is the near-perfect line regulation at 5V and 15V outputs. This circuit can accept a 27V to 55V change to the input with less than the noise voltage as a change to the output voltage. R_B, a load bypass resistor, supplies current I_{SY} for the 15V regulator.

Any number of REF01s and REF02s can be stacked in this configuration. For example, if ten devices are stacked in this configuration, ten 5V or five 10V outputs are achieved. The line voltage may range from 100V to 130V. Care should be exercised to insure that the total load currents do not exceed the maximum usable current, which is typically 21mA.

TYPICAL APPLICATIONS

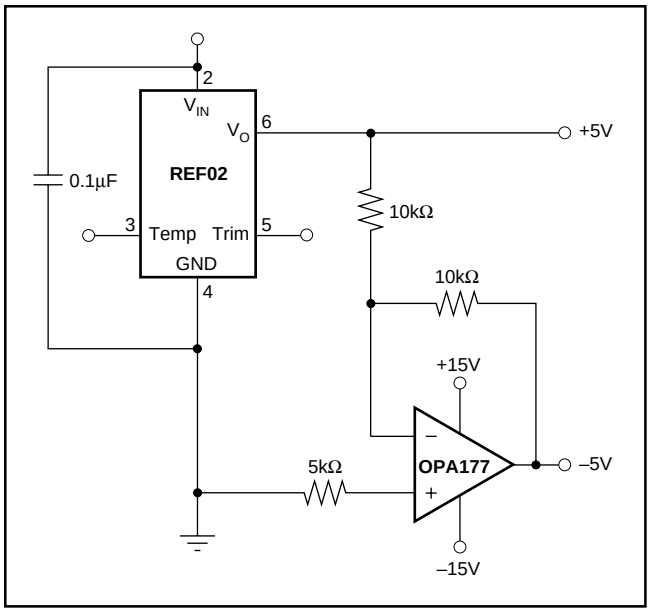


FIGURE 2. ±5V Precision Reference.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF02AU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02AU
REF02AU.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02AU
REF02AU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02AU
REF02AU/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02AU
REF02BU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02BU
REF02BU.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02BU
REF02BU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02BU
REF02BU/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	REF 02BU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

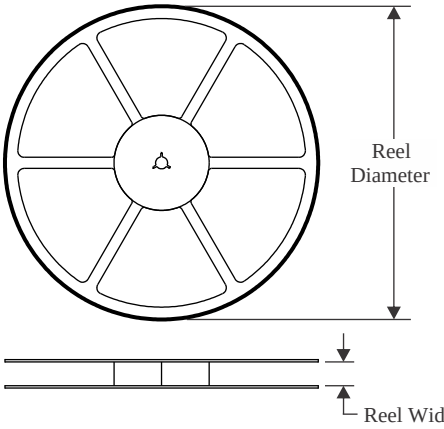
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

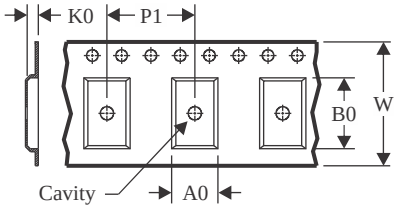
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

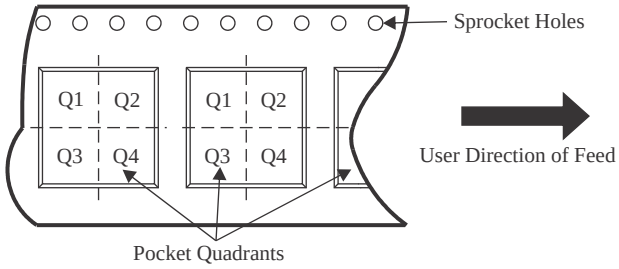


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

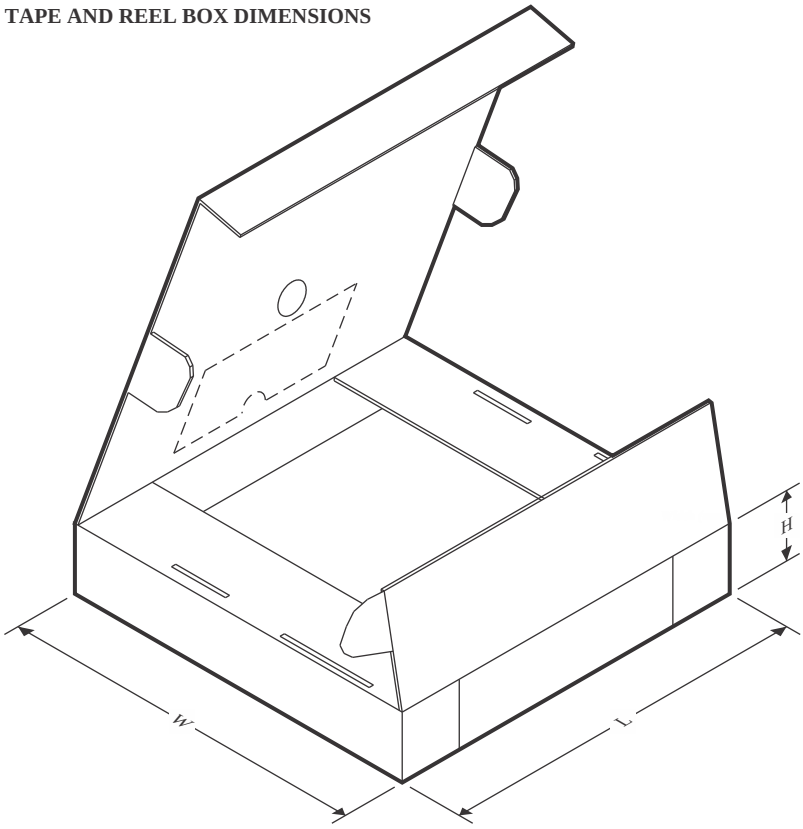
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF02AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF02BU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

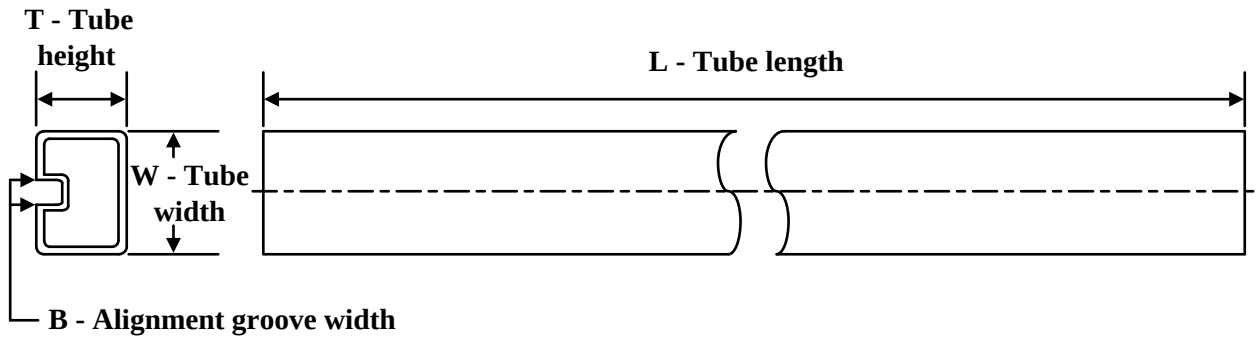
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

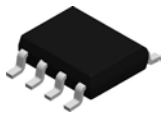
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF02AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0
REF02BU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
REF02AU	D	SOIC	8	75	506.6	8	3940	4.32
REF02AU.A	D	SOIC	8	75	506.6	8	3940	4.32
REF02BU	D	SOIC	8	75	506.6	8	3940	4.32
REF02BU.A	D	SOIC	8	75	506.6	8	3940	4.32

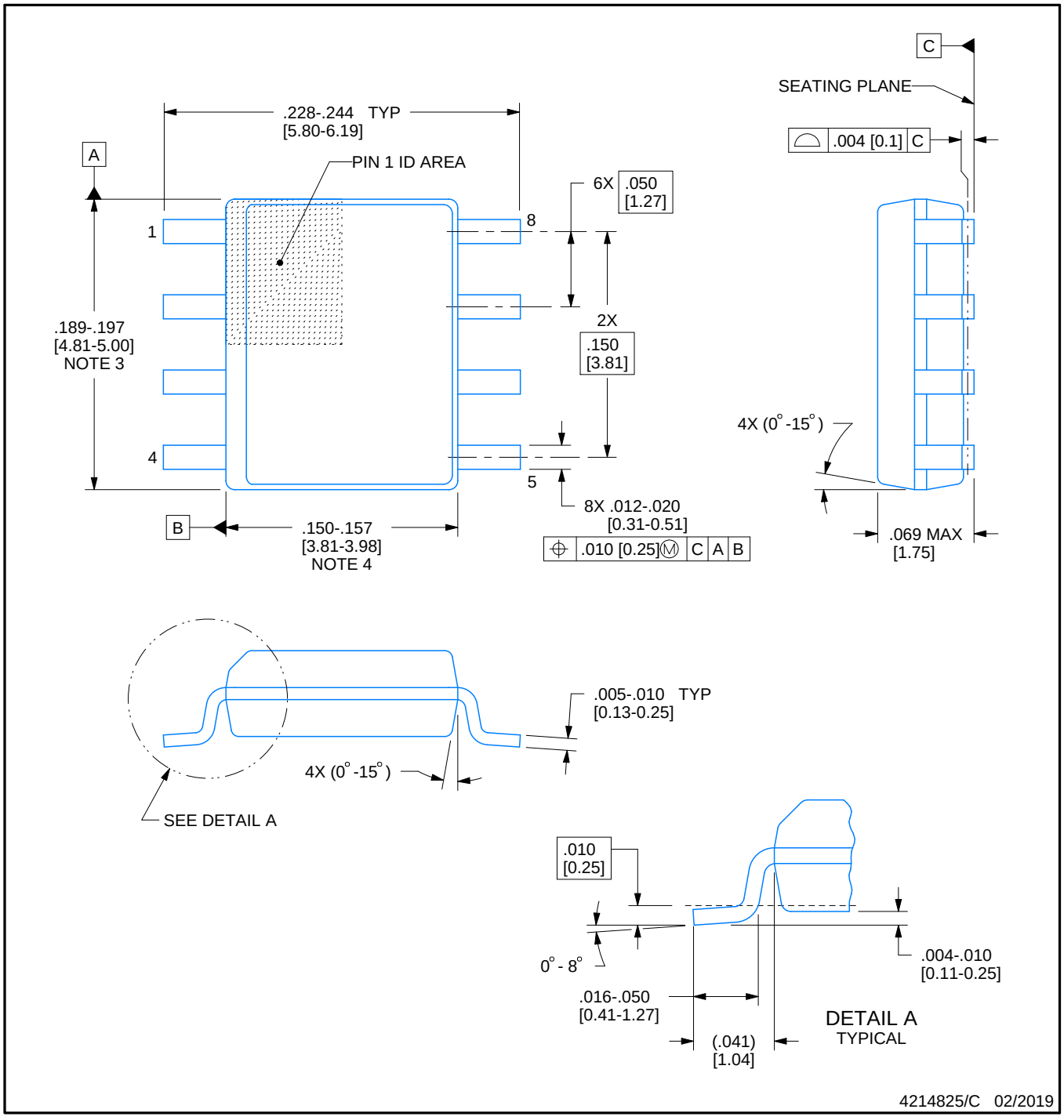


PACKAGE OUTLINE

D0008A

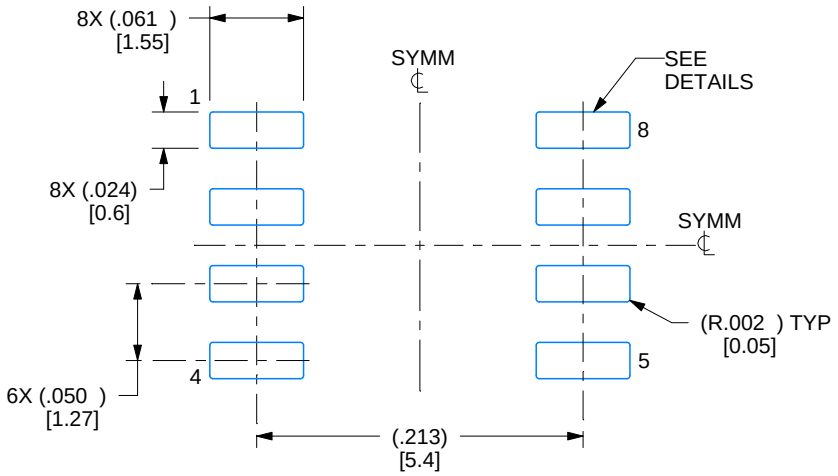
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

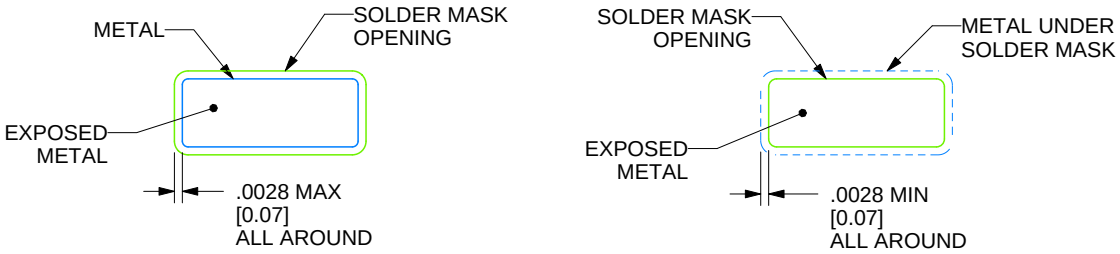


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

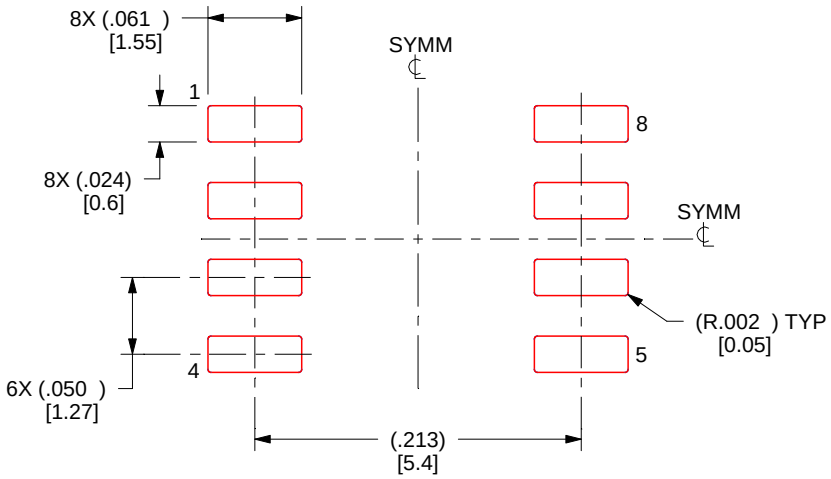
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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