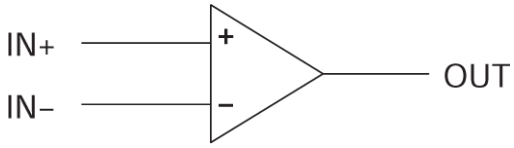
RC4559 Dual High-Performance Operational Amplifier

1 Features

- Matched gain and offset between amplifiers
- Unity-gain bandwidth: 3MHz typical
- Slew rate: 1.5V/µs typical
- Low equivalent input noise voltage 2µV/Hz maximum (20Hz to 20kHz)
- No frequency compensation required
- No latch up
- Wide common-mode voltage range
- Low power consumption

2 Applications

- AV receivers
- Professional audio mixers
- Soundbars
- Wireless speakers



Symbol (Each Amplifier)

3 Description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier suitable for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a dynamic performance that is specified by design and an output drive capability that far exceeds general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

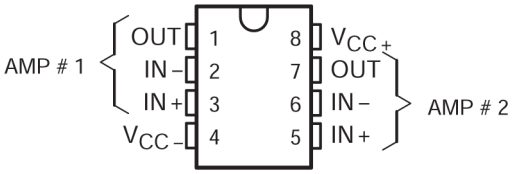
Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
RC4559	D (SOIC, 8)	4.90 mm × 3.90 mm
	P (PDIP, 8)	9.81 mm × 6.30 mm

Device Information (2)

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} max at 25°C
DEVICE	PACKAGE SUFFIX		
RC4559	D, P	−0°C to 70°C	6 mV

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The D packages are available taped and reeled. Add the suffix R to the device type when ordering (for example, RC4559DR).



D or P Package, SOIC or PDIP 8-Pin (Top View)

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage V_{CC+} (see (1))		18	V
Supply voltage V_{CC-} (see (1))		−18	V
Differential input voltage (see (2))		±30	V
Input voltage (any input, see (1) and 3)		±15	V
Short-circuit output current (see (4))		125	mA
Continuous total dissipation		500	mW
Operating free-air temperature range	0	70	°C
Storage temperature range	−65	125	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
(2) Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
(4) Temperature or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

4.2 Electrical Characteristics

at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS (1)	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		2	6	mV
			Full Range			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	100	nA
			Full range			200	
I_{IB}	Input bias current	V_O = 0	25°C		40	250	nA
			Full range			500	
V_I	Input voltage range		25°C	± 12	± 13		V
V_{OM}	Maximum peak output voltage swing	R_L ≥ 3 kΩ	25°C	± 12	± 13		
		R_L= 600 Ω	25°C	± 9.5	± 10		V
		R_L ≥ 2 kΩ	Full range	± 10			
V_I	Input voltage range	V_O = ± 10 V, R_L = 2 kΩ	25°C	20	300		V/mV
			Full range	15			
B_{OM}	Maximum output-swing bandwidth	V_{OPP} = 20 V, R_L = 2 kΩ	25°C	24	32		kHz
B_1	Unity-gain bandwidth		25°C		4		MHz
r_i	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	V_O = 0	25°C	80	100		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_O = 0	25°C		10	75	µV/V
V_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, R_S = 1 kΩ, f = 20 Hz to 20 kHz	25°C		1.4	2	µV
I_n	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		pA
I_{CC}	Supply current (both amplifiers)	No load, No signal	25°C		3.3	5.6	mA
			0°C		4	6.6	
			70°C		3	5	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, R_S = 1 kΩ, f = 10 kHz	25°C		90		dB

(1) All characteristics are specified under open-loop operation, unless otherwise noted.
(2) Full range operating free-air temperature range is 0°C to 70°C.

4.3 Matching Characteristics

at V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		± 0.2		mV
I_{IO}	Input offset current	V_O = 0		± 7.5		nA
I_{IB}	Input bias current	V_O = 0		± 15		nA
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 2 kΩ		± 1		dB

4.4 Operating Characteristics

V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		80		µs
	Overshoot			18%		
SR	Slew rate at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 100 pF	1.5	2		V/µs

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.3 Trademarks

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 1988) to Revision A (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Removed from *Features*: Designed to be Interchangeable with Raytheon RC4559	1
• Removed duration of output short-circuit to ground specification in *Absolute Maximum Ratings* table	3
• Added maximum output short-circuit value of 125mA to *Absolute Maximum Ratings* table	3
• Removed the minimum limit for the *unity-gain bandwidth* parameter in the *Electrical Characteristics* table	3
• Removed the minimum limit for the *Maximum output-swing bandwidth* parameter in the *Electrical Characteristics* table	3

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RC4559D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	RC4559
RC4559DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4559
RC4559DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4559
RC4559P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	RC4559P
RC4559P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	RC4559P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

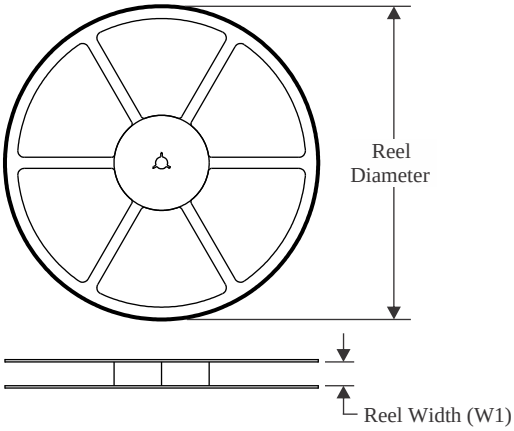
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

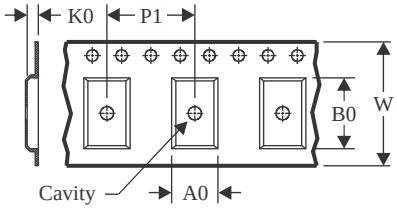
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

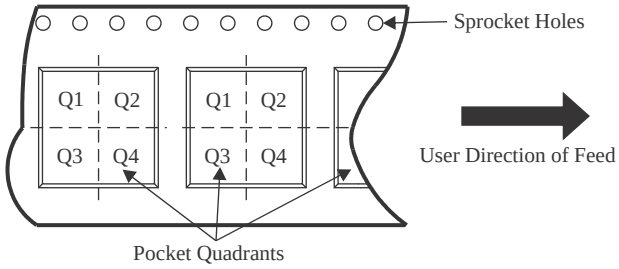


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

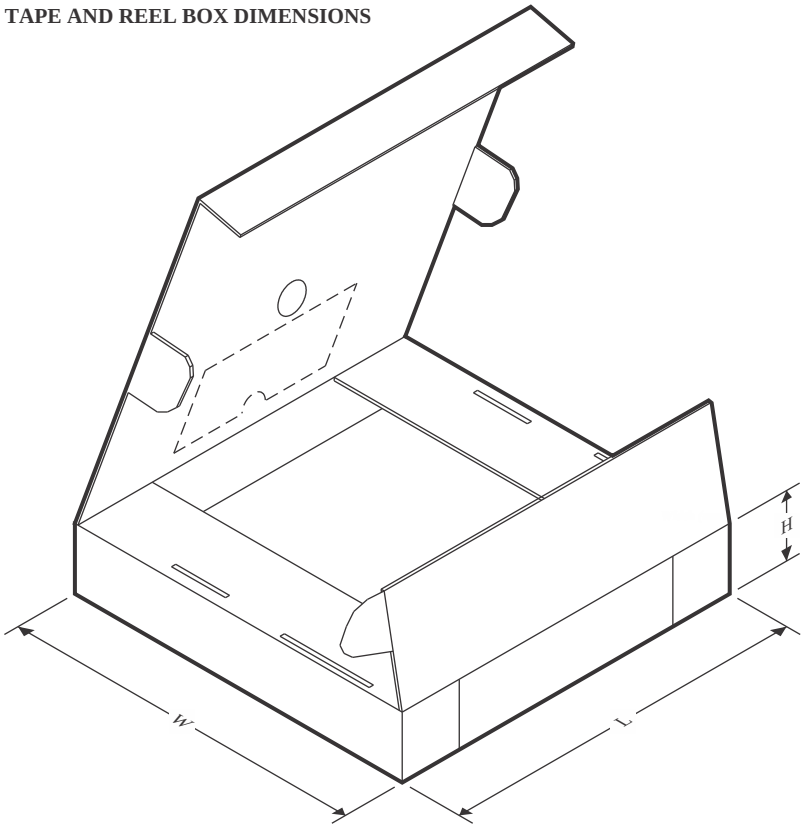
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4559DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

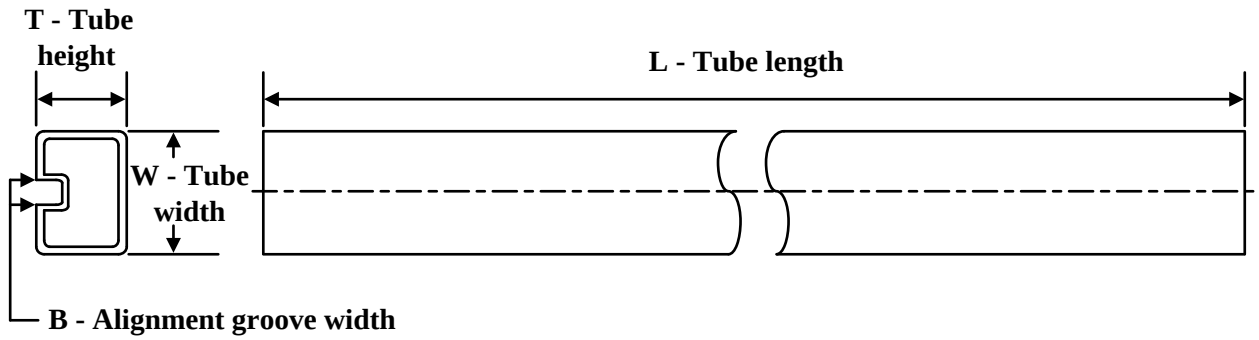
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

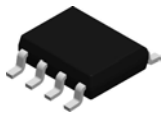
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4559DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
RC4559P	P	PDIP	8	50	506	13.97	11230	4.32
RC4559P.A	P	PDIP	8	50	506	13.97	11230	4.32

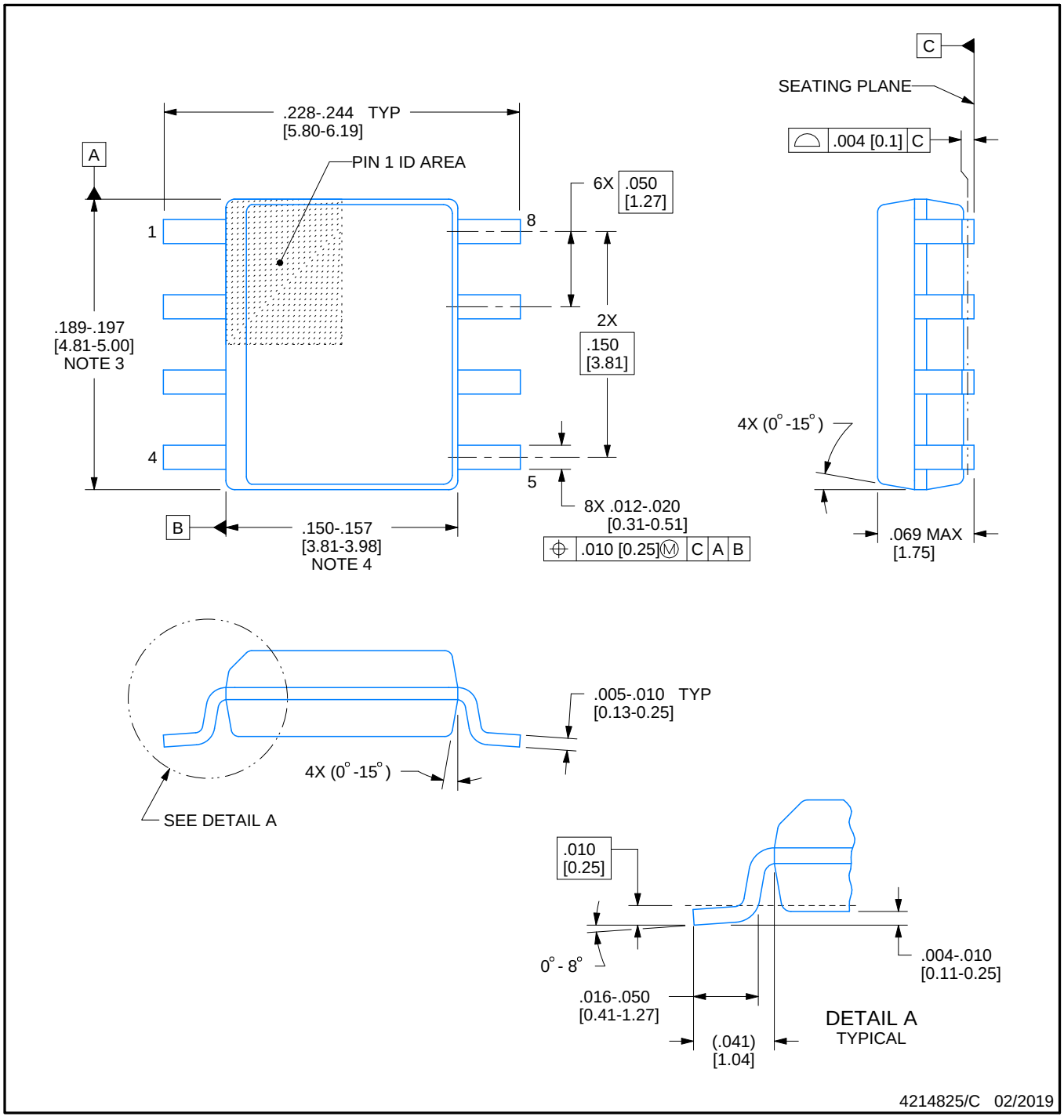


PACKAGE OUTLINE

D0008A

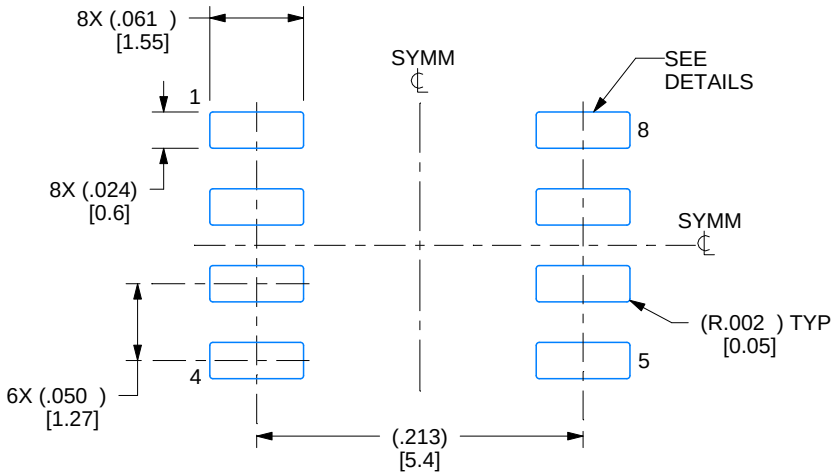
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

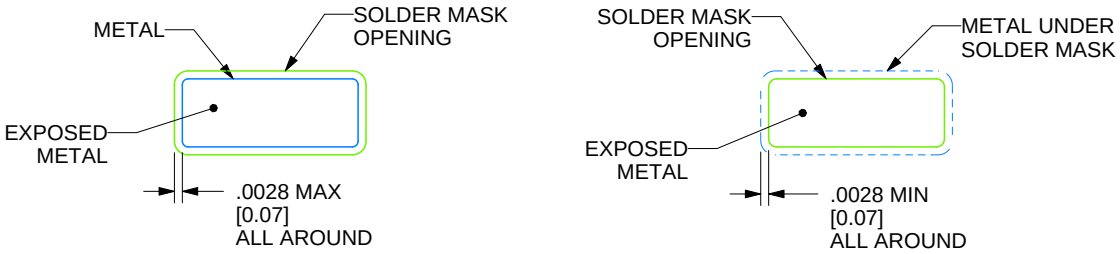


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

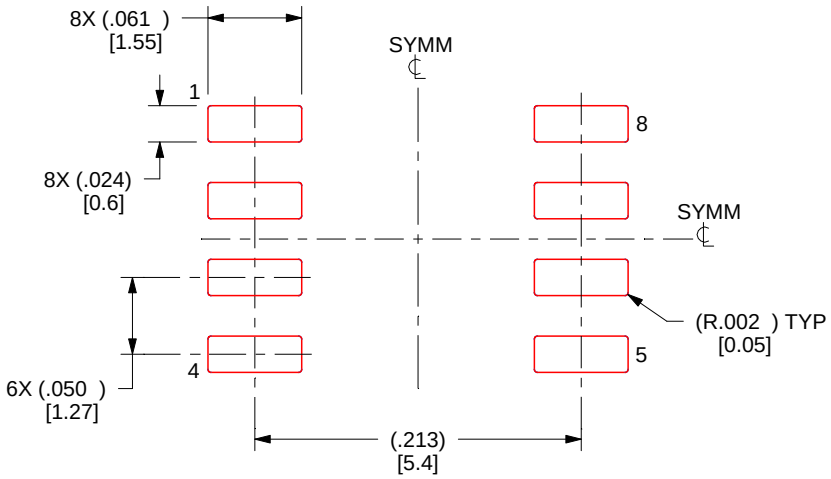
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



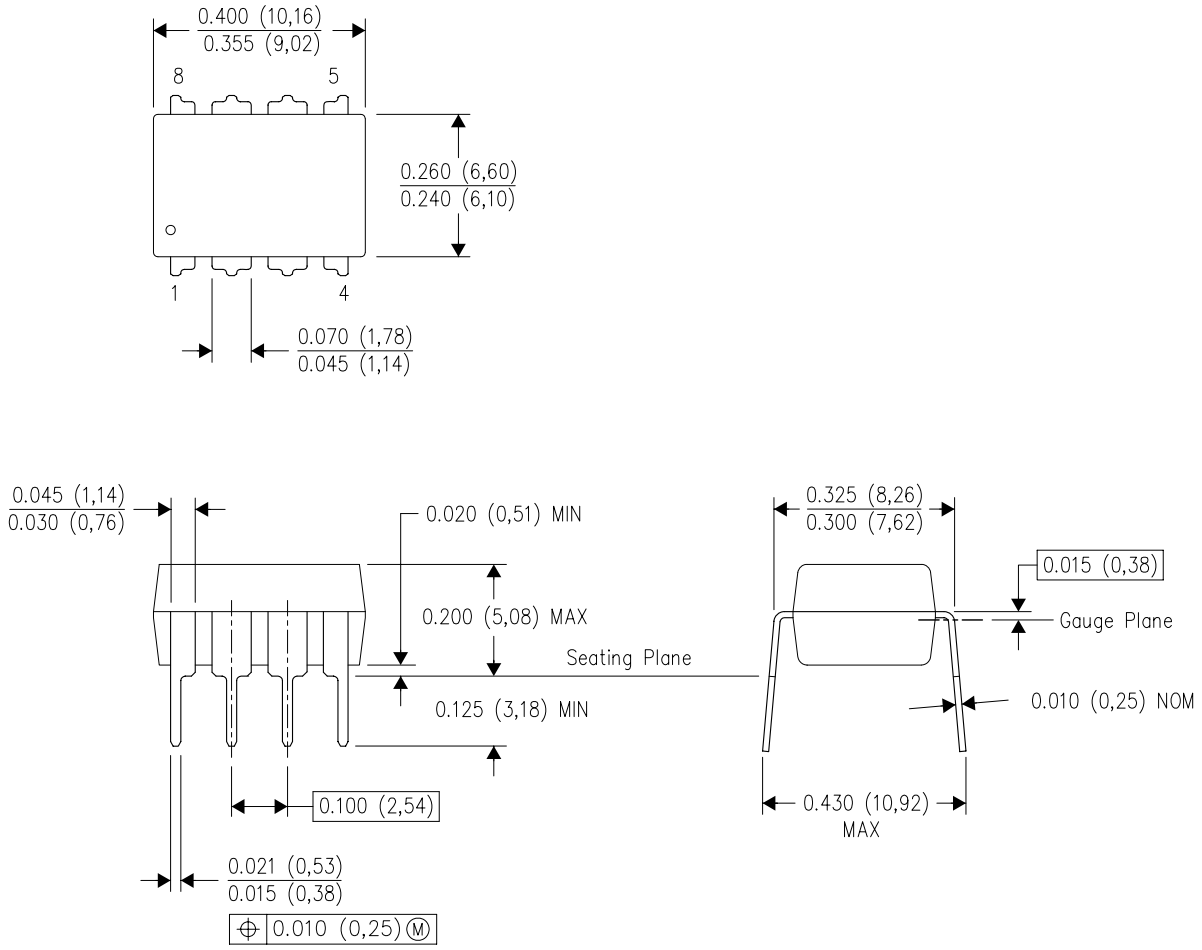
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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