PCMD3140-Q1 Quad-Channel, PDM Input to TDM or I²S Output Converter

1 Features

- 4-channel PDM microphones simultaneous conversion
- PDM input to TDM or I²S output converter performance:
  - 127-dB dynamic range (DR) with high-performance, 5th-order PDM input
  - 117-dB dynamic range (DR) with high-performance, 4th-order PDM input
- Channel summing mode, DR performance with high-performance, 4th-order PDM input:
  - 120-dB, 2-channel summing
- Programmable PDM clock output:
  - 768 kHz to 6.144 MHz
- Programmable output sample rate (f_S):
  - 8 kHz to 768 kHz
- Programmable channel settings:
  - Digital volume control: –100 dB to 27 dB
  - Gain calibration: 0.1-dB resolution
  - Phase calibration: 163-ns resolution
- Microphone bias or supply voltage generation
- Voice activity detection (VAD)
- Low-latency signal processing filter selection
- Programmable HPF and biquad digital filters
- I²C control
- Integrated high-performance audio PLL
- Automatic clock divider setting configurations
- Audio serial data interface:
  - Format: TDM, I²S, or left-justified (LJ)
  - Word length: 16 bits, 20 bits, 24 bits, or 32 bits
  - Master or slave interface
- Single-supply operation: 3.3 V or 1.8 V
- I/O-supply operation: 3.3 V or 1.8 V
- Power consumption for 1.8-V supply:
  - 2.8mW/channel at 16-kHz sample rate
  - 3.6 mW/channel at 48-kHz sample rate

2 Applications

- Automotive Active Noise Cancellation
- Automotive Head Unit
- Rear Seat Entertainment
- Digital Cockpit Processing Unit
- Telematics Control Unit

3 Description

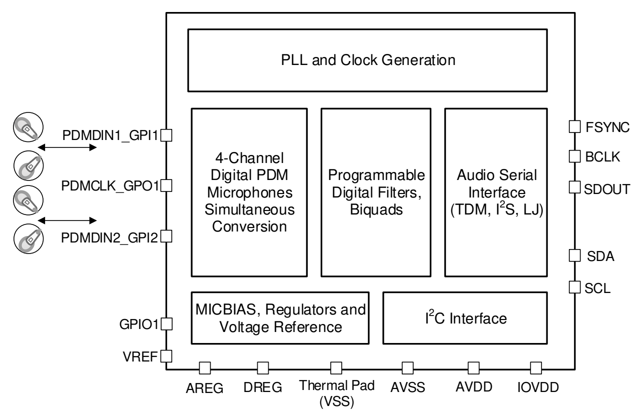
The PCMD3140-Q1 is a high-performance, pulse-density-modulation (PDM) input to time-division multiplexing (TDM) or I²S output converter that supports simultaneous sampling of up to four digital channels for the PDM microphone input. The device integrates programable digital volume control, a microphone bias voltage, a phase-locked loop (PLL), a programmable high-pass filter (HPF), biquad filters, low-latency filter modes, and allows for output sample rates up to 768 kHz. The device supports time-division multiplexing (TDM), I²S, or left-justified (LJ) audio formats, and can be controlled with the I²C interface. Additionally, the PCMD3140-Q1 supports master and slave mode selection for the audio bus interface operation. These integrated high-performance features, along with the ability to be powered from a single-supply of 3.3 V or 1.8 V, make the device an excellent choice for space-constrained audio systems in far-field microphone recording applications.

The PCMD3140-Q1 is specified from –40°C to +125°C, and is offered in a 20-pin WQFN package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
PCMD3140-Q1	WQFN (20)	3.00 mm × 3.00 mm with 0.5-mm pitch

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (September 2022) — **Page**

- Changed document status from advance information to production data....... 1
- Updated device status to Production Data....... 1

5 Pin Configuration and Functions

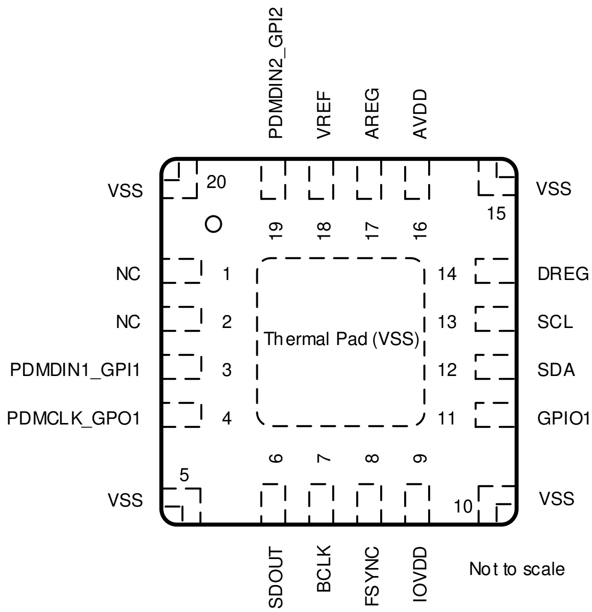


Figure 5-1. RTE Package, 20-Pin WQFN With Exposed Thermal Pad, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	No connect	No connection
2	NC	No connect	No connection
3	PDMDIN1_GPI1	Digital input	Digital input 1 (multipurpose functions such as digital microphones data, PLL input clock source, and so forth).
4	PDMCLK_GPO1	Digital output	General-purpose digital output 1 (multipurpose functions such as digital microphone clock, interrupt, and so forth).
5	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawing at the end of this document for corner pin dimensions.
6	SDOUT	Digital output	Audio serial data interface bus output.
7	BCLK	Digital I/O	Audio serial data interface bus bit clock.
8	FSYNC	Digital I/O	Audio serial data interface bus frame synchronization signal.
9	IOVDD	Digital supply	Digital I/O power supply (1.8 V or 3.3 V, nominal).
10	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawing at the end of this document for corner pin dimensions.
11	GPIO1	Digital I/O	General-purpose digital input/output 1 (multipurpose functions such as digital microphones clock or data, PLL input clock source, interrupt, and so forth).
12	SDA	Digital I/O	Data pin for I^2C control bus.
13	SCL	Digital input	Clock pin for I^2C control bus.
14	DREG	Digital supply	Digital regulator output voltage for digital core supply (1.5 V, nominal). Connect a 10-µF and a 0.1-µF low ESR capacitor in parallel to the device ground (VSS).
15	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawing at the end of this document for corner pin dimensions.
16	AVDD	Analog supply	Analog power (1.8 V or 3.3 V, nominal).
17	AREG	Analog supply	Analog on-chip regulator output voltage for analog supply (1.8 V, nominal) or external analog power (1.8 V, nominal). Connect a 10-µF and a 0.1-µF low ESR capacitor in parallel to the analog ground (AVSS).
18	VREF	Analog	Analog reference voltage filter output. Connect a 1-µF to the analog ground (AVSS).

Table 5-1. Pin Functions (continued)

PIN NO.	PIN NAME	TYPE	DESCRIPTION
19	PDMDIN2_GPI2	Analog output/digital input	Digital Input 2. MICBIAS output or general-purpose digital input 2 (multipurpose functions such as digital microphones data, MICBIAS, PLL input clock source, and so forth). If used as MICBIAS output, then connect a 1 µF to analog ground (AVSS)
20	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawing at the end of this document for corner pin dimensions.
Thermal Pad	Thermal Pad (VSS)	Ground supply	Thermal pad is shorted to the internal device ground. Short the thermal pad directly to the board ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	AREG to AVSS	–0.3	2.0	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Digital input voltage	Digital input except PDMDINx_GPIx pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
	Digital input PDMDINx_GPIx pins voltage to VSS (thermal pad)	–0.3	AVDD + 0.3	
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD, AREG(1)	Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator) - AVDD 3.3-V operation	3.0	3.3	3.6	V
	Analog supply voltage AVDD and AREG to AVSS (AREG internal regulator is shutdown) - AVDD 1.8-V operation	1.7	1.8	1.9	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
INPUTS					
	Digital input except PDMDIN1_GPI1 and PDMDIN2_GPI2 pins voltage to VSS (thermal pad)	0		IOVDD	V
	Digital input PDMDIN1_GPI1 and PDMDIN2_GPI2 pins voltage to VSS (thermal pad)	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C
OTHERS					
	GPIOx or GPIx (used as MCLK input) clock frequency			36.864	MHz
C_b	SCL and SDA bus capacitance for I^2C interface supports standard-mode and fast-mode			400	pF
	SCL and SDA bus capacitance for I^2C interface supports fast-mode plus			550	
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

6.4 Thermal Information

THERMAL METRIC(1)		PCMD3140 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, PDMCLKx = 64 × f_S, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERFORMANCE FOR PDM INPUT CONVERSION						
SNR	Signal-to-noise ratio, A-weighted(1) (2) (3)	No signal, input generated using 5th-order PDM modulator		130		dB
		No signal, input generated using 4th-order PDM modulator		118		
DR	Dynamic range, A-weighted(2) (3)	–60-dB full-scale signal input, input generated using 5th-order PDM modulator		127		dB
		–60-dB full-scale signal input, input generated using 4th-order PDM modulator		116		
OTHER PARAMETERS						
	Digital volume control range	Programmable 0.5-dB steps	–100		27	dB
	Output data sample rate	Programmable	7.35		768	kHz
	Output data sample word length	Programmable	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		12		Hz
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS		2.1		μV_{RMS}
	MICBIAS voltage	MICBIAS programmed to VREF and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V		VREF		V
	MICBIAS voltage	MICBIAS programmed to VREF × 1.096 and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V		VREF × 1.096		V
	MICBIAS voltage	Bypass to AVDD with 5-mA load		AVDD – 0.2		V
	MICBIAS current drive				5	mA
	MICBIAS load regulation	MICBIAS programmed to either VREF or VREF × 1.096, measured up to max load	0	0.6	1	%
	MICBIAS overcurrent protection threshold		6.1			mA
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2, SDA and SCL, IOVDD 1.8-V operation	–0.3		0.35 × IOVDD	V
		All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2, SDA and SCL, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2, SDA and SCL, IOVDD 1.8-V operation	0.65 × IOVDD		IOVDD + 0.3	V
		All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2, SDA and SCL, IOVDD 3.3-V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins except PDMCLK_GPO1, SDA and SCL, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins except PDMCLK_GPO1, SDA and SCL, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins except PDMCLK_GPO1, SDA and SCL, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins except PDMCLK_GPO1, SDA and SCL, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold	SDA and SCL	–0.5		0.3 x IOVDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold	SDA and SCL	0.7 x IOVDD		IOVDD + 0.5	V
$V_{OL1(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –3 mA, IOVDD > 2 V			0.4	V
$V_{OL2(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –2 mA, IOVDD ≤ 2 V			0.2 x IOVDD	V

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, PDMCLKx = 64 × f_S, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OL(I2C)}$	Low-level digital output current	SDA, $V_{OL(I2C)}$ = 0.4 V, standard-mode or fast-mode	3			mA
		SDA, $V_{OL(I2C)}$ = 0.4 V, fast-mode plus	20			
I_{IH}	Input logic-high leakage for digital inputs	All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2 pins, input = IOVDD	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins except PDMDIN1_GPI1, PDMDIN2_GPI2 pins, input = 0 V	–5	0.1	5	µA
$V_{IL(GPIx)}$	Low-level digital input logic voltage threshold	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, AVDD 1.8-V operation	–0.3		0.35 × AVDD	V
		PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, AVDD 3.3-V operation	–0.3		0.8	
$V_{IH(GPIx)}$	High-level digital input logic voltage threshold	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, AVDD 1.8-V operation	0.65 × AVDD		AVDD + 0.3	V
		PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, AVDD 3.3-V operation	2		AVDD + 0.3	
$V_{OL(GPOx)}$	Low-level digital output voltage	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, I_{OL} = –2 mA, AVDD 1.8-V operation			0.45	V
		PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, I_{OL} = –2 mA, AVDD 3.3-V operation			0.4	
$V_{OH(GPOx)}$	High-level digital output voltage	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, I_{OH} = 2 mA, AVDD 1.8-V operation	AVDD – 0.45			V
		PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, I_{OH} = 2 mA, AVDD 3.3-V operation	2.4			
$I_{IH(GPIx)}$	Input logic-high leakage for digital inputs	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, input = AVDD	–5	0.1	5	µA
$I_{IL(GPIx)}$	Input logic-high leakage for digital inputs	PDMDIN1_GPI1, PDMDIN2_GPI2 digital pins, input = 0 V	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All external clocks stopped, AVDD = 3.3 V		5		µA
I_{AVDD}		All external clocks stopped, AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		10		
I_{IOVDD}		All external clocks stopped, IOVDD = 3.3 V		0.5		
I_{IOVDD}		All external clocks stopped, IOVDD = 1.8 V		0.3		
I_{AVDD}	Current consumption with 4-channel PDM input recording	AVDD = 3.3 V		9.1		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		8.1		
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		
I_{AVDD}	Current consumption with 4-channel PDM input recording, f_S = 16 kHz, PDMCLKx = 96 × f_S, PLL on and BCLK = 384 × f_S	AVDD = 3.3 V		7.3		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		6.3		
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with no signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) The device performance parameters, SNR, DR and THD+N, are mainly limited by single-bit PDM modulator generated data output. The THD+N peformance for single-bit PDM modulator output itself is generally not so good for signal above –10-dB full-scale.

6.6 Timing Requirements: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 6-1 for timing diagram

		MIN	NOM	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HIGH}	High period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time	0		3.45	µs
$t_{SU;DAT}$	Data setup time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Setup time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST-MODE					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0		0.9	µs
$t_{SU;DAT}$	Data setup time	100			ns
t_r	SDA and SCL rise time	20		300	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		300	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HIGH}	High period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time	0			µs
$t_{SU;DAT}$	Data setup time	50			ns
t_r	SDA and SCL rise time			120	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		120	ns
$t_{SU;STO}$	Setup time for STOP condition	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

6.7 Switching Characteristics: I^2C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 6-1 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDA)}$	SCL to SDA delay	Standard-mode	250		1250	ns
		Fast-mode	250		850	
		Fast-mode plus			400	

6.8 Timing Requirements: TDM, I^2S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 6-2 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		25			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		25			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time(2)			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time(2)			10	ns

(1) The BCLK minimum high or low pulse duration can be relaxed to 14 ns (to meet the timing specifications), if the SDOUT data line is latched on the same BCLK edge polarity as the edge used by the device to transmit SDOUT data.
(2) BCLK maximum rise and fall time can be relaxed to 13ns if BCLK frequency used in the system is below 20MHz. This can cause noise increase due to higher clock jitter.

6.9 Switching Characteristics: TDM, I^2S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 6-2 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT	3		18	ns
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT			18	ns
$f_{(BCLK)}$	BCLK output clock frequency: master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration: master mode		14			ns
$t_{L(BCLK)}$	BCLK low pulse duration: master mode		14			ns
$t_{d(FSYNC)}$	BCLK to FSYNC delay: master mode	50% of BCLK to 50% of FSYNC	3		18	ns
$t_{r(BCLK)}$	BCLK rise time: master mode	10% - 90% rise time			8	ns
$t_{f(BCLK)}$	BCLK fall time: master mode	90% - 10% fall time			8	ns

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

Timing Requirements: PDM Digital Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 6-3 for timing diagram

		MIN	NOM	MAX	UNIT
$t_{SU(PDMDINx)}$	PDMDINx setup time	30			ns
$t_{HLD(PDMDINx)}$	PDMDINx hold time	0			ns

6.10 Switching Characteristics: PDM Digial Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 6-3 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(PDMCLK)}$	PDMCLK clock frequency		0.768		6.144	MHz
$t_{H(PDMCLK)}$	PDMCLK high pulse duration		72			ns
$t_{L(PDMCLK)}$	PDMCLK low pulse duration		72			ns
$t_{r(PDMCLK)}$	PDMCLK rise time	10% - 90% rise time			18	ns
$t_{f(PDMCLK)}$	PDMCLK fall time	90% - 10% fall time			18	ns

6.11 Timing Diagrams

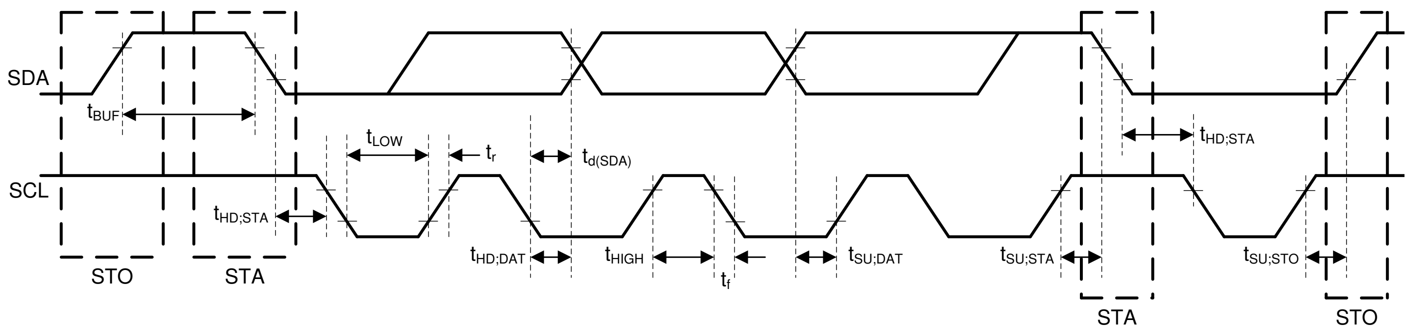


Figure 6-1. I²C Interface Timing Diagram

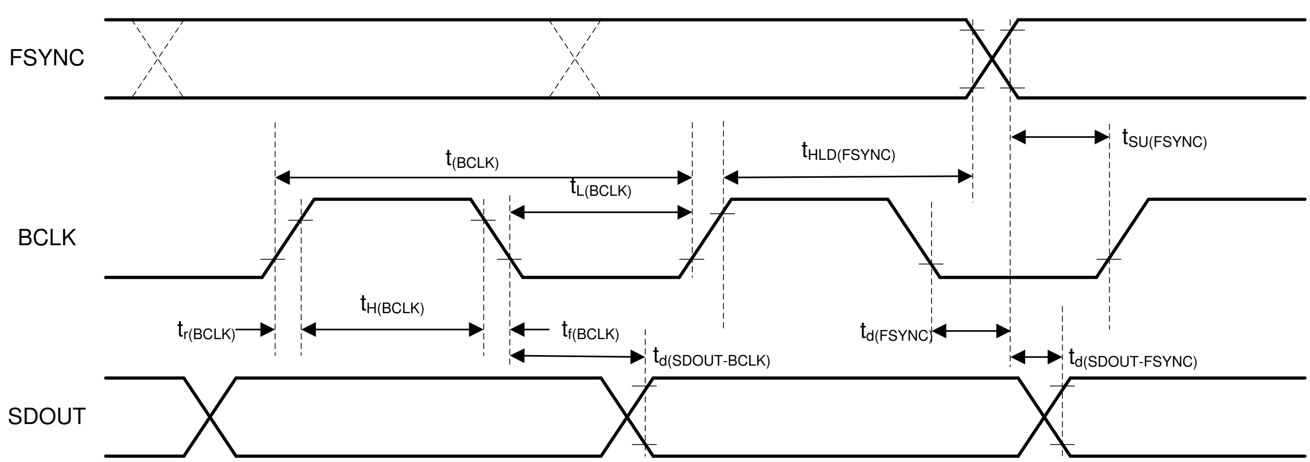


Figure 6-2. TDM (With BCLK_POL = 1), I²S, and LJ Interface Timing Diagram

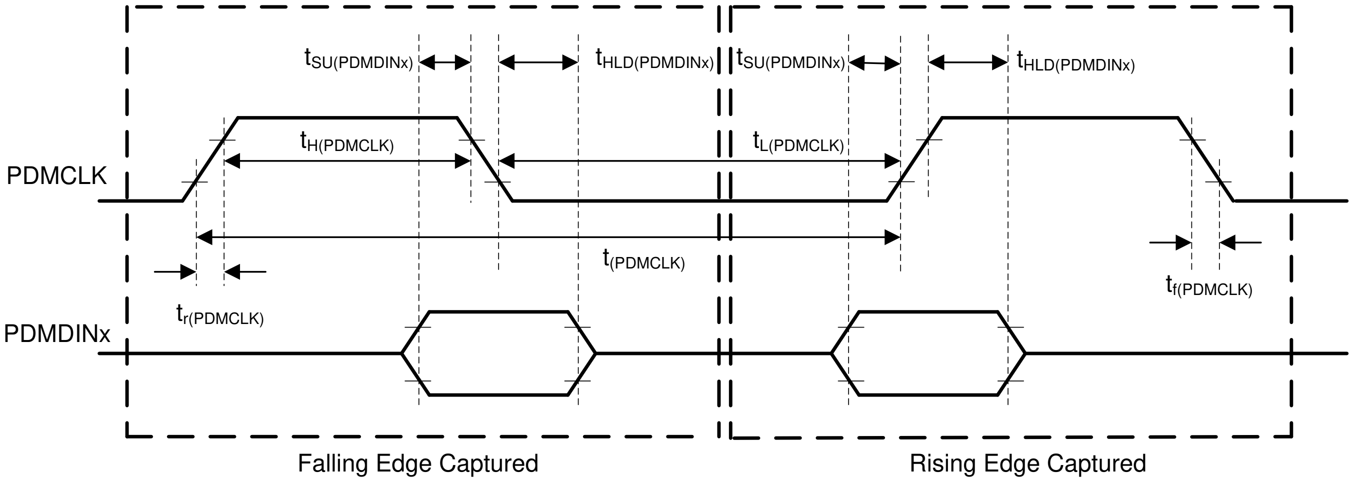
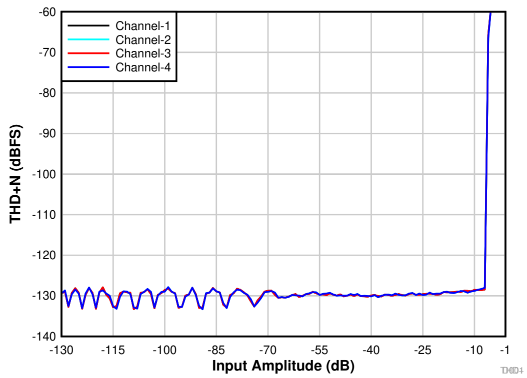


Figure 6-3. PDM Digital Microphone Interface Timing Diagram

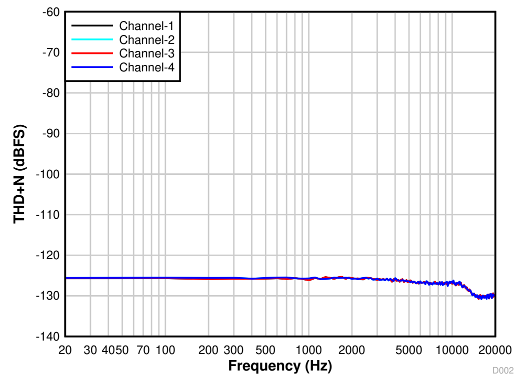
6.12 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, PDMCLKx = 64 × f_S, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted); all measurements are done by feeding the device PDM digital input signal using audio precision



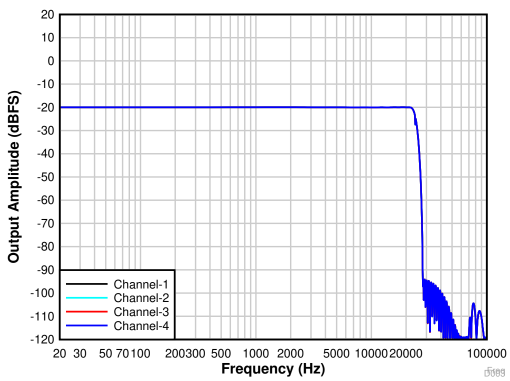
5th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-4. THD+N vs Input Amplitude



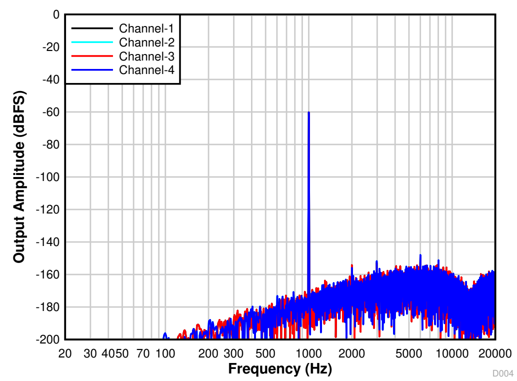
5th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-5. THD+N vs Input Frequency With a –20-dBr Input



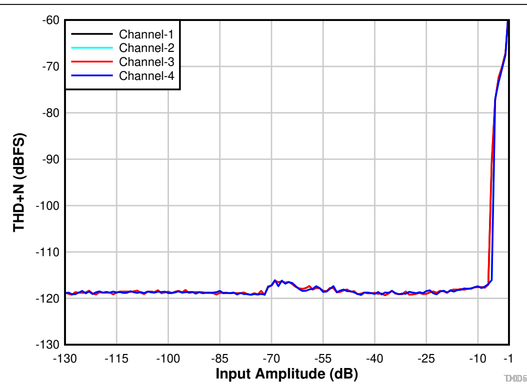
5th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-6. Frequency Response With a –20-dBr Input



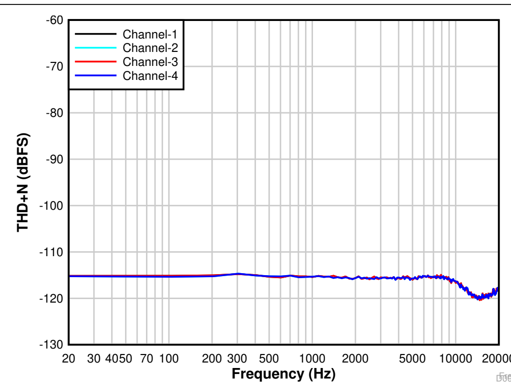
5th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-7. FFT With a –60-dBr Input



4th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-8. THD+N vs Input Amplitude

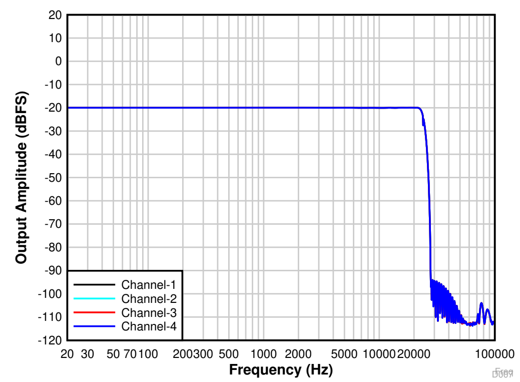


4th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-9. THD+N vs Input Frequency With a –20-dBr Input

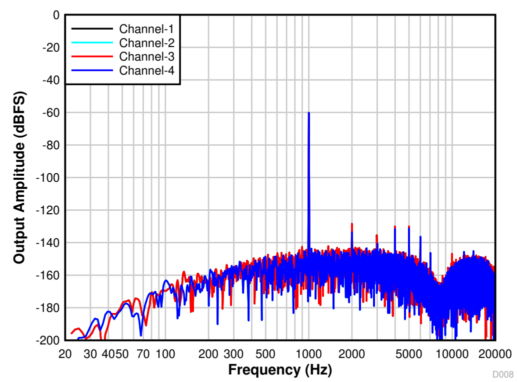
6.12 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, PDMCLKx = 64 × f_S, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted); all measurements are done by feeding the device PDM digital input signal using audio precision



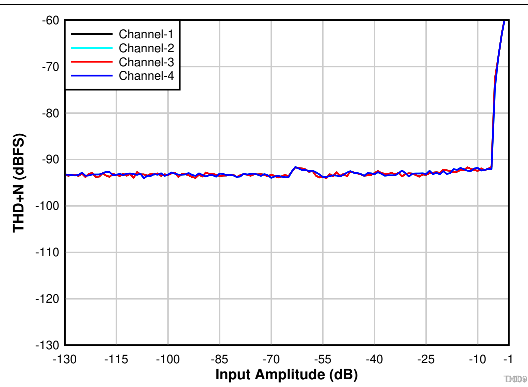
4th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-10. Frequency Response With a –20-dBr Input



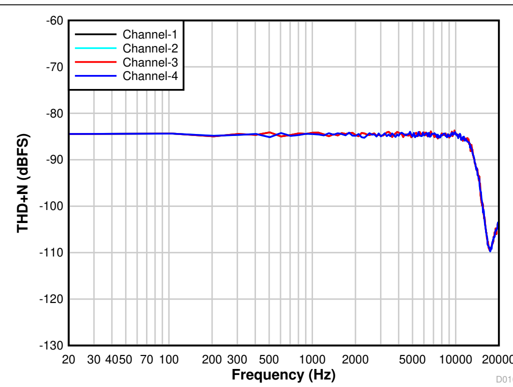
4th-order PDM modulator with PDMCLKx = 3.072 MHz

Figure 6-11. FFT With a –60-dBr Input



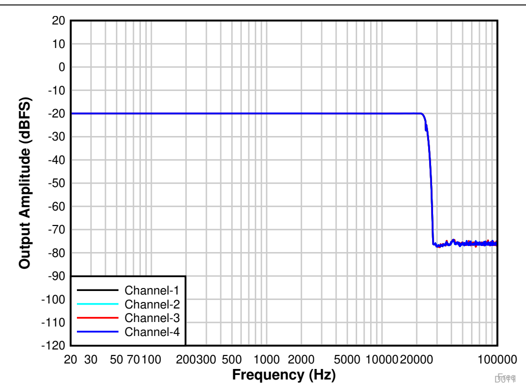
4th-order PDM modulator with PDMCLKx = 1.536 MHz

Figure 6-12. THD+N vs Input Amplitude



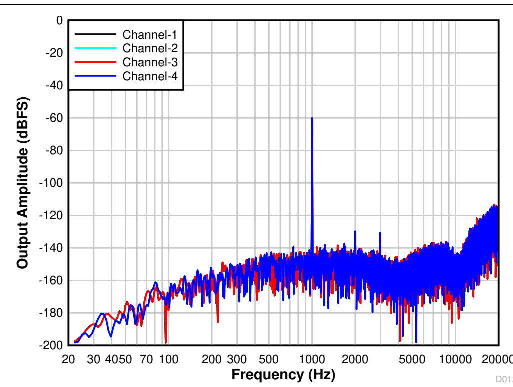
4th-order PDM modulator with PDMCLKx = 1.536 MHz

Figure 6-13. THD+N vs Input Frequency With a –20-dBr Input



4th-order PDM modulator with PDMCLKx = 1.536 MHz

Figure 6-14. Frequency Response With a –20-dBr Input

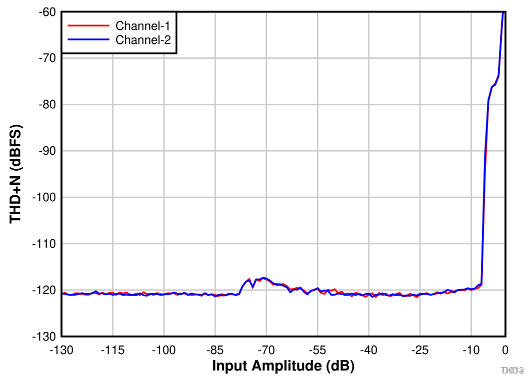


4th-order PDM modulator with PDMCLKx = 1.536 MHz

Figure 6-15. FFT With a –60-dBr Input

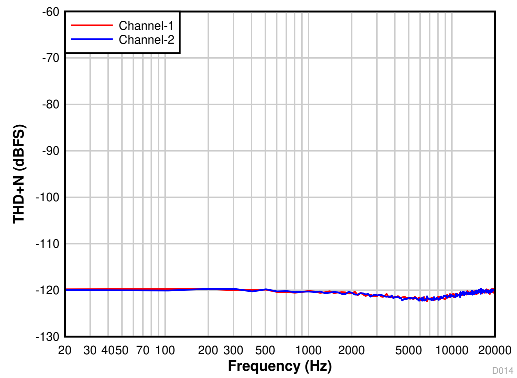
6.12 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, PDMCLKx = 64 × f_S, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted); all measurements are done by feeding the device PDM digital input signal using audio precision



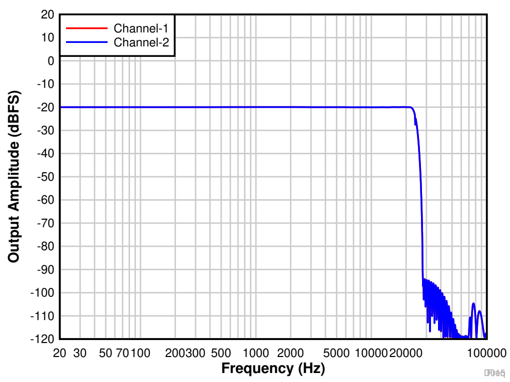
4th-order PDM modulator with PDMCLKx = 6.144 MHz

Figure 6-16. THD+N vs Input Amplitude



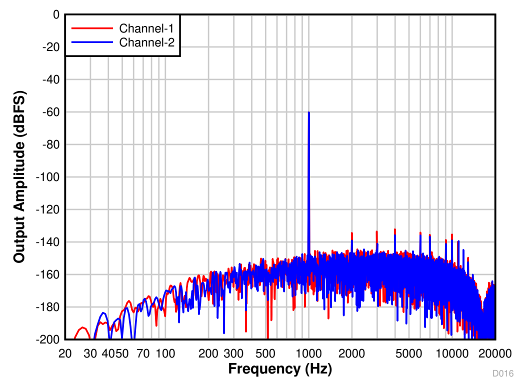
4th-order PDM modulator with PDMCLKx = 6.144 MHz

Figure 6-17. THD+N vs Input Frequency With a –20-dBr Input



4th-order PDM modulator with PDMCLKx = 6.144 MHz

Figure 6-18. Frequency Response With a –20-dBr Input



4th-order PDM modulator with PDMCLKx = 6.144 MHz

Figure 6-19. FFT With a –60-dBr Input

7 Detailed Description

7.1 Overview

The PCMD3140-Q1 is a high-performance, low-power, flexible, 4-channel, pulse-density-modulation (PDM) input to time-division multiplexing (TDM) or I²S audio output converter with extensive feature integration. This device is intended for applications in voice-activated systems, portable computing, communication, and entertainment applications. The low power consumption makes this device suitable for battery-powered, portable audio systems. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications.

The PCMD3140-Q1 consists of the following blocks:

- Four-channel, pulse density modulation (PDM) digital microphone interface with high-performance decimation filter
- Low-noise, microphone bias output to power the digital microphone
- Programmable decimation filters with linear-phase or low-latency filter
- Programmable digital volume control, biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF), and digital channel mixer
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the PCMD3140-Q1 to configure the control registers is supported using an I²C interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I²S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

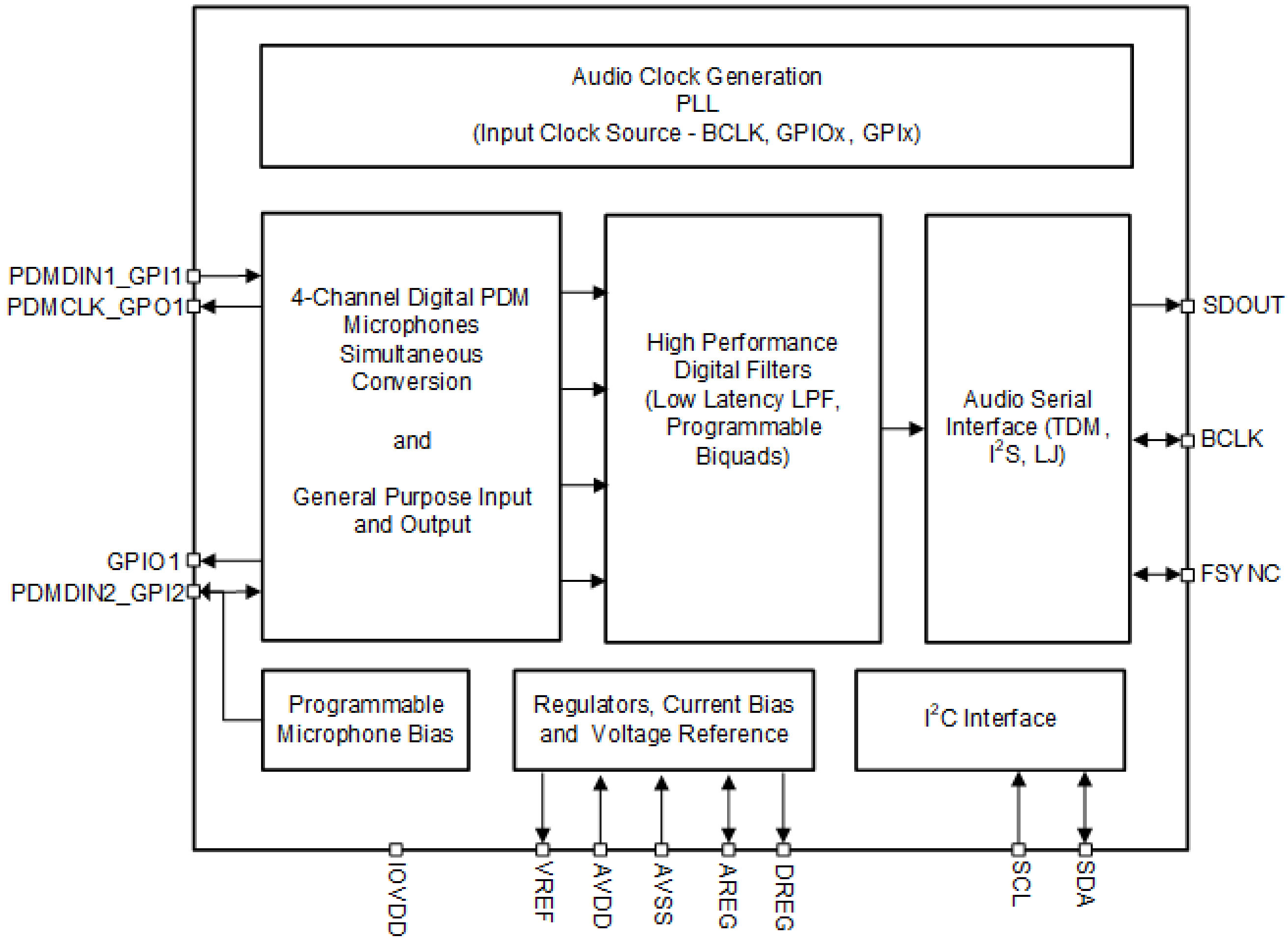
The device can support multiple devices by sharing the common TDM buses across devices. Moreover, the device includes a daisy-chain feature as well. These features relax the shared TDM bus timing requirements and board design complexities when operating multiple devices for applications requiring high audio data bandwidth.

Table 7-1 lists the reference abbreviations used throughout this document to registers that control the device.

Table 7-1. Abbreviations for Register References

REFERENCE	ABBREVIATION	DESCRIPTION	EXAMPLE
Page y, register z, bit k	Py_Rz_Dk	Single data bit. The value of a single bit in a register.	Page 4, register 36, bit 0 = P4_R36_D0
Page y, register z, bits k-m	Py_Rz_D[k:m]	Range of data bits. A range of data bits (inclusive).	Page 4, register 36, bits 3-0 = P4_R36_D[3:0]
Page y, register z	Py_Rz	One entire register. All eight bits in the register as a unit.	Page 4, register 36 = P4_R36
Page y, registers z-n	Py_Rz-Rn	Range of registers. A range of registers in the same page.	Page 4, registers 36, 37, 38 = P4_R36-R38

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

7.3.1.1 Control Serial Interfaces

The device control registers can be accessed using I^{2}C communication to the device. The device operates with a fixed I^{2}C address and can be configured using this address.

7.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCMD3140-Q1 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^{2}S or left-justified protocols format, programmable data length options, very flexible master-slave configurability for bus clock lines, and the ability to communicate with multiple devices within a system directly.

The bus protocol TDM, I^2S, or left-justified (LJ) format can be selected by using the ASI_FORMAT[1:0] (P0_R7_D[7:6]) register bits. As shown in Table 7-2 and Table 7-3, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the ASI_WLEN[1:0] (P0_R7_D[5:4]) register bits.

Table 7-2. Audio Serial Interface Format

P0_R7_D[7:6] : ASI_FORMAT[1:0]	AUDIO SERIAL INTERFACE FORMAT
00 (default)	Time division multiplexing (TDM) mode
01	Inter IC sound (I^2S) mode
10	Left-justified (LJ) mode
11	Reserved (do not use this setting)

Table 7-3. Audio Output Channel Data Word-Length

P0_R7_D[5:4] : ASI_WLEN[1:0]	AUDIO OUTPUT CHANNEL DATA WORD-LENGTH
00	Output channel data word-length set to 16 bits
01	Output channel data word-length set to 20 bits
10	Output channel data word-length set to 24 bits
11 (default)	Output channel data word-length set to 32 bits

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 64) to allow all output channel audio data transmissions to complete on the audio bus by a device or PCMD3140-Q1 and other Audio devices sharing the same bus. The device supports up to four output channels that can be configured to place their audio data on bus slot 0 to slot 63. Table 7-4 lists the output channel slot configuration settings. In I^2S and LJ mode, the slots are divided into two sets, left-channel slots and right-channel slots, as described in the *Section 7.3.1.2.2* and *Section 7.3.1.2.3* sections.

Table 7-4. Output Channel Slot Assignment Settings

P0_R11_D[5:0] : CH1_SLOT[5:0]	OUTPUT CHANNEL 1 SLOT ASSIGNMENT
00 0000 = 0d (default)	Slot 0 for TDM or left slot 0 for I^2S, LJ.
00 0001 = 1d	Slot 1 for TDM or left slot 1 for I^2S, LJ.
…	…
01 1111 = 31d	Slot 31 for TDM or left slot 31 for I^2S, LJ.
10 0000 = 32d	Slot 32 for TDM or right slot 0 for I^2S, LJ.
…	…
11 1110 = 62d	Slot 62 for TDM or right slot 30 for I^2S, LJ.
11 1111 = 63d	Slot 63 for TDM or right slot 31 for I^2S, LJ.

Similarly, the slot assignment setting for output channel 2 to channel 4 can be done using the CH2_SLOT (P0_R12) to CH8_SLOT (P0_R18) registers, respectively.

The slot word length is the same as the output channel data word length set for the device. The output channel data word length must be set to the same value for all PCMD3140-Q1 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

The device also includes a feature that offsets the start of the slot data transfer with respect to the frame sync by up to 31 cycles of the bit clock. Table 7-5 lists the programmable offset configuration settings.

Table 7-5. Programmable Offset Settings for the ASI Slot Start

P0_R8_D[4:0] : TX_OFFSET[4:0]	PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START
0 0000 = 0d (default)	The device follows the standard protocol timing without any offset.
0 0001 = 1d	Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing.
......	......
1 1110 = 30d	Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.
1 1111 = 31d	Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the FSYNC_POL (P0_R7_D3) register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the BCLK_POL (P0_R7_D2) register bit.

7.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 7-1 to Figure 7-4 illustrate the protocol timing for TDM operation with various configurations.

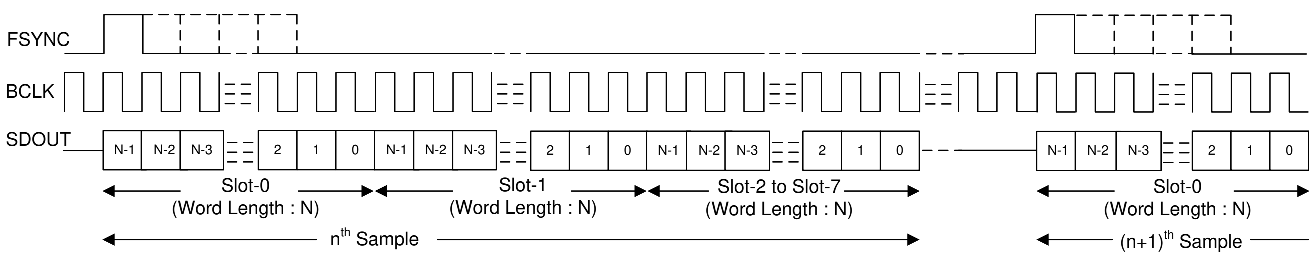


Figure 7-1. TDM Mode Standard Protocol Timing (TX_OFFSET = 0)

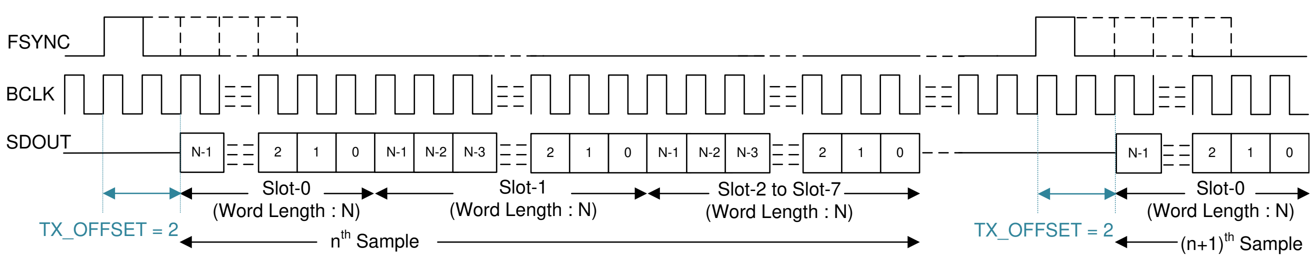


Figure 7-2. TDM Mode Protocol Timing (TX_OFFSET = 2)

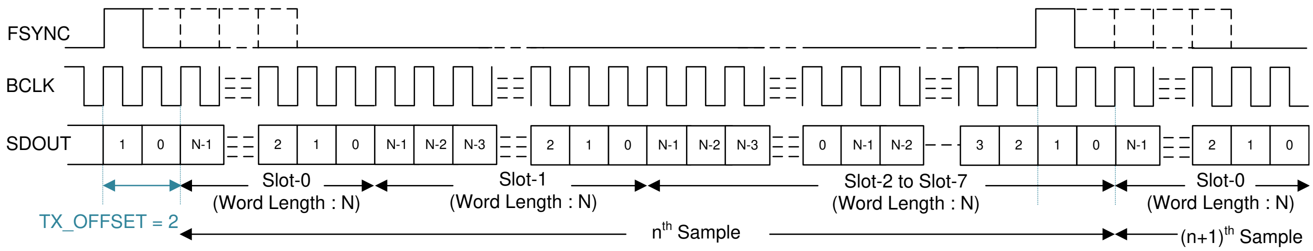


Figure 7-3. TDM Mode Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 2)

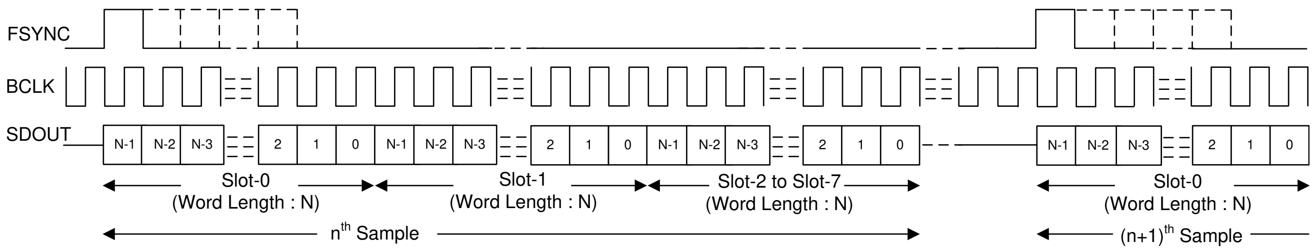


Figure 7-4. TDM Mode Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a TX_OFFSET value higher than 0 is recommended.

7.3.1.2.2 Inter IC Sound (I^{2}S) Interface

The standard I^{2}S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I^{2}S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. Figure 7-5 to Figure 7-8 illustrate the protocol timing for I^{2}S operation with various configurations.

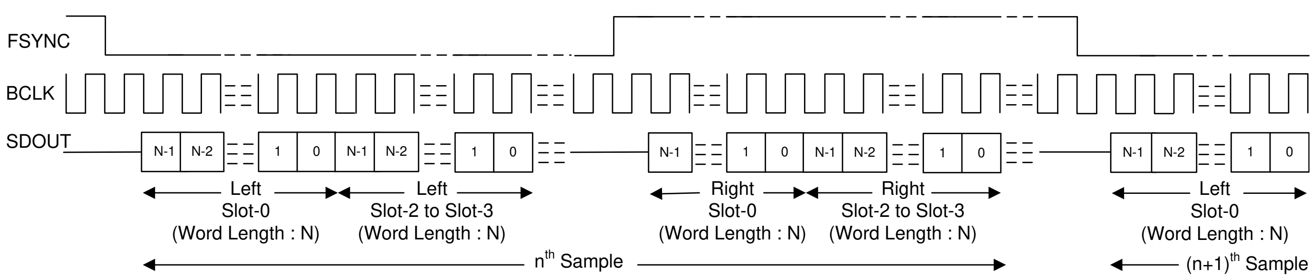


Figure 7-5. I^{2}S Mode Standard Protocol Timing (TX_OFFSET = 0)

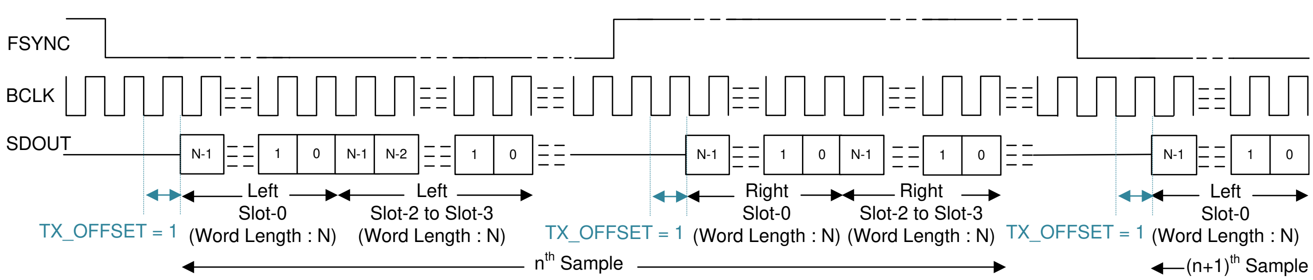


Figure 7-6. I^{2}S Protocol Timing (TX_OFFSET = 1)

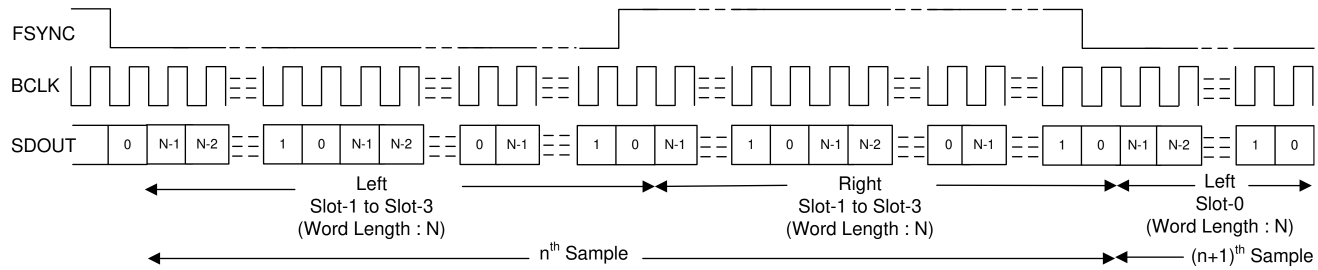


Figure 7-7. I²S Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

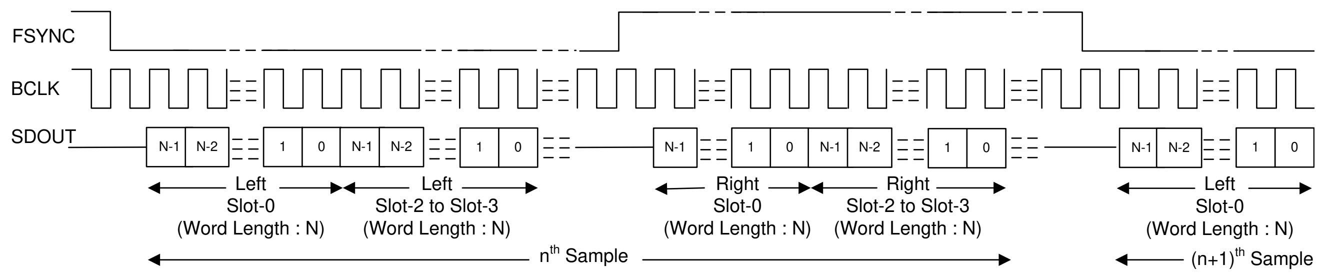


Figure 7-8. I²S Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

7.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. Figure 7-9 to Figure 7-12 illustrate the protocol timing for LJ operation with various configurations.

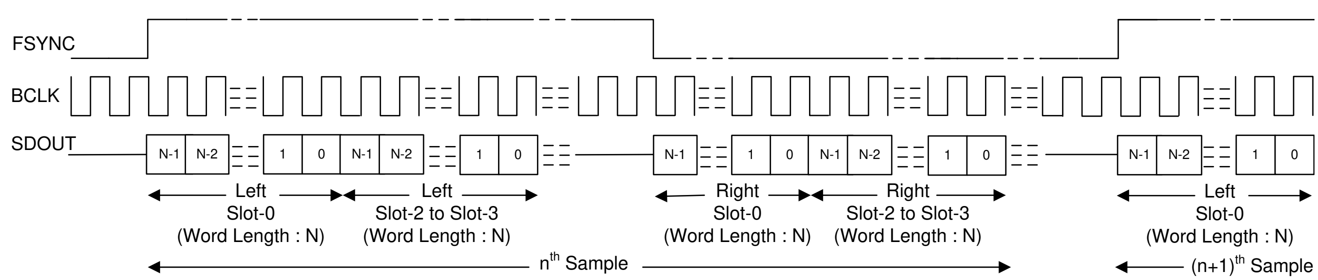


Figure 7-9. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)

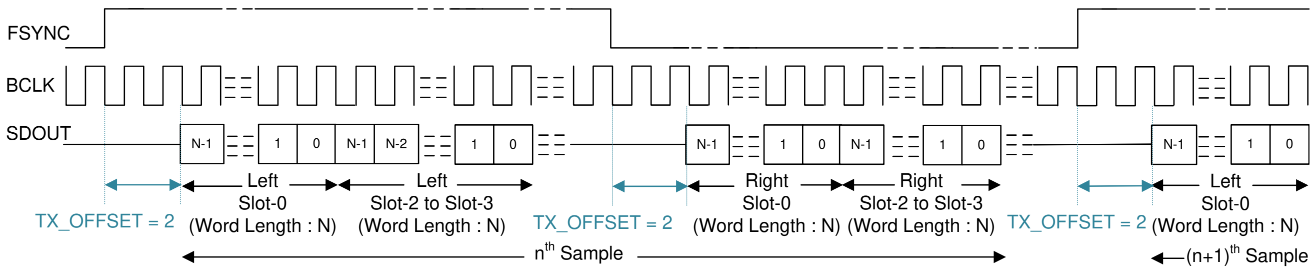


Figure 7-10. LJ Protocol Timing (TX_OFFSET = 2)

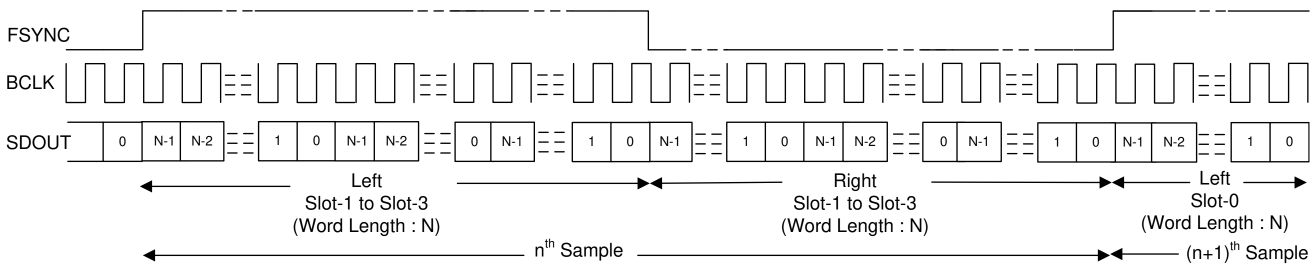


Figure 7-11. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

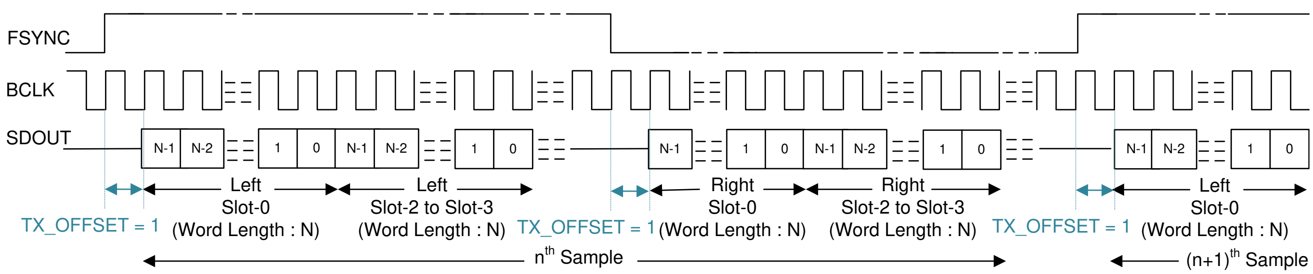


Figure 7-12. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

7.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect the PCMD3140-Q1 and any other audio device by sharing a single common I^2C control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone array for beam-forming operations, audio conferencing, noise cancellation, and so forth. Figure 7-13 shows a diagram of the PCMD3140-Q1 and PCMD3180 devices in a configuration where the control and audio data buses are shared.

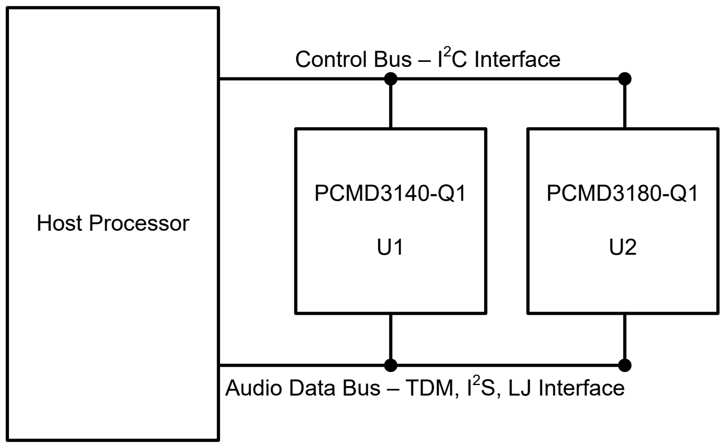


Figure 7-13. Multiple Devices With Shared Control and Audio Data Buses

The PCMD3140-Q1 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- I^2C broadcast simultaneously writes to (or triggers) the PCMD3140-Q1 and PCMD3180-Q1 devices
- Supports up to 64 configuration output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIO1 or PDMCLK_GPO1 pin can be configured as a secondary output data lane for the audio serial interface
- The GPIO1 or PDMDINx_GPIx pin can be used in a daisy-chain configuration of multiple devices
- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable master and slave options for the audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices

The system can also connect multiple PCMD3140-Q1 devices in combination with PCMx120-Q1 devices by sharing a single common I^2C control bus and an audio serial interface bus. See the *Multiple TLV320ADCx140 & TLV320ADCx120 Devices With Shared TDM and I^2C Bus* application report for further details.

7.3.2 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the PDM clock generation and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio bus.

The device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 7-6 and Table 7-7 list the supported FSYNC and BCLK frequencies.

Table 7-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)	FSYNC (384 kHz)	FSYNC (768 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072	6.144	12.288
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608	9.216	18.432
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144	12.288	24.576
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216	18.432	**Reserved**
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288	24.576	**Reserved**
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432	**Reserved**	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576	**Reserved**	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	8.192	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	16.384	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

Table 7-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224	5.6448	11.2896
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336	8.4672	16.9344
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448	11.2896	22.5792
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672	16.9344	**Reserved**
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896	22.5792	**Reserved**
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344	**Reserved**	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792	**Reserved**	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	7.5264	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	15.0528	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

The status register ASI_STS (P0_R21) captures the device auto detect result for the FSYNC frequency and the BCLK to FSYNC ratio. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes the record channels accordingly.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the PDM clock generation and digital filter engine, as well as other control blocks. The device also supports an option to use BCLK, GPIO1, or the GPIx pin (as MCLK) as the audio clock source without using the PLL to reduce power consumption. However, the PDM microphone performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the *TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios* application report.

The device also supports an audio bus master mode operation using the GPIO1 or GPIx pin (as MCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on master mode configuration and operation are discussed in the *Configuring and Operating TLV320ADCx120 as an Audio Bus Master* application report.

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the ASI_ERR (P0_R9_D5) and AUTO_CLK_CFG (P0_R19_D6) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the *ADCx120EVM-PDK Evaluation module* user's guide and the PurePath™ Console Graphical Development Suite for Audio System Design and Development.

7.3.3 Reference Voltage

The PCMD3140-Q1 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance and must be filtered externally using a 1-µF capacitor connected from the VREF pin to analog ground (AVSS).

The value of this reference voltage can be configured using the P0_R59_D[1:0] register bits and must be set to an appropriate value based on the AVDD supply voltage available in the system. The default VREF value is set to 2.75 V, which require minimum AVDD voltage for this mode is 3 V. Table 7-8 lists the various VREF settings supported along with required AVDD range for that configuration.

Table 7-8. VREF Programmable Settings

P0_R59_D[1:0] : VREF_SEL[1:0]	VREF OUTPUT VOLTAGE	AVDD RANGE REQUIREMENT
00 (default)	2.75 V	3 V to 3.6 V
01	2.5 V	2.8 V to 3.6 V
10	1.375 V	1.7 V to 1.9 V
11	Reserved	Reserved

To achieve low-power consumption, this audio reference block is powered down as described in the *Section 7.4.1* section. When exiting sleep mode, the audio reference block is powered up using the internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1-µF decoupling capacitor. If a higher-value decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG (P0_R2_D[4:3]) register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

7.3.4 Microphone Bias

The device integrates a built-in, low-noise programmable microphone bias pin that can be used in the system for providing the supply to the MEMS digital microphone. The MICBIAS pin must be connected to an external 1-µF capacitor to analog ground (AVSS). The MICBIAS pin supports up to 5 mA of load current that can be used for multiple microphones. When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. In the system, if the MICBIAS pin is used as a supply for digital microphones, then TI recommends using the MICBIAS configuration as AVDD, so that the digital microphone PDMCLKx and PDMDINx signals can be directly interface to the PCMD3140-Q1 without using any external level shifters. Table 7-9 shows the available microphone bias programmable options.

Table 7-9. MICBIAS Programmable Settings

P0_R59_D[6:4] : MBIAS_VAL[2:0]	P0_R59_D[1:0] : VREF_SEL[1:0]	MICBIAS OUTPUT VOLTAGE
000 (default)	00 (default)	2.75 V (same as the VREF output)
	01	2.5 V (same as the VREF output)
	10	1.375 V (same as the VREF output)
001 to 101	XX	Reserved (do not use these settings)
110	XX	Same as AVDD
111	XX	Reserved (do not use this setting)

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ (P0_R117_D7) register bit. Additionally, the device provides an option to configure the GPIO1 or GPIx pin to directly control the microphone bias output powering on or off. This feature is useful to control the microphone directly without engaging the host for I^2C communication. The MICBIAS_PDZ (P0_R117_D7) register bit value is ignored if the GPIO1 or GPIx pin is configured to set the microphone bias on or off.

7.3.5 Digital PDM Microphone Record Channel

The device interfaces up to four digital pulse-density-modulation (PDM) microphones for simultaneous conversion and uses high-order and high-performance decimation filters to generate pulse code modulation (PCM) output data that can be transmitted on the audio serial interface to the host using either time-division multiplexing (TDM), I^2S, or left-justified (LJ) audio formats.

The device internally generates PDMCLK with a programmable frequency of either 6.144 MHz, 3.072 MHz, 1.536 MHz, or 768 kHz (for output data sample rates in multiples or submultiples of 48 kHz) or 5.6448 MHz, 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (for output data sample rates in multiples or submultiples of 44.1 kHz) using the PDMCLK_DIV[1:0] (P0_R31_D[1:0]) register bits. PDMCLK can be routed on the PDMCLKx_GPOx pin. This clock can be connected to the external digital microphone device. The device also support control register to independently configure each channel PDMDINx data to be latched using either rising edge or falling edge. Figure 7-14 shows a connection diagram of the digital PDM microphones.

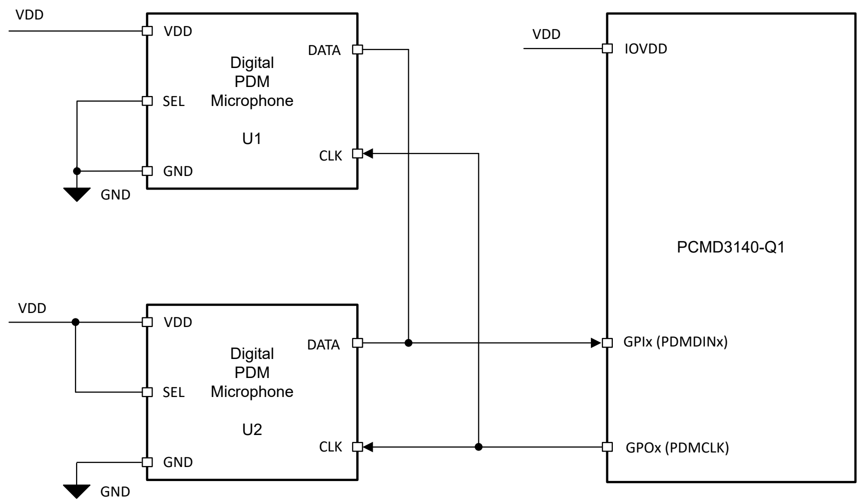


Figure 7-14. Digital PDM Microphones Connection Diagram to the PCMD3140-Q1

The single-bit output of the external digital microphone device can be connected to the GPIx pin. This single data line can be shared by two digital microphones to place their data on the opposite edge of PDMCLK. Internally, the device latches the steady value of the data on the rising edge of PDMCLK or the falling edge of PDMCLK based on the configuration register bits set in P0_R32_D[7:4]. Figure 7-15 shows the digital PDM microphone interface timing diagram.

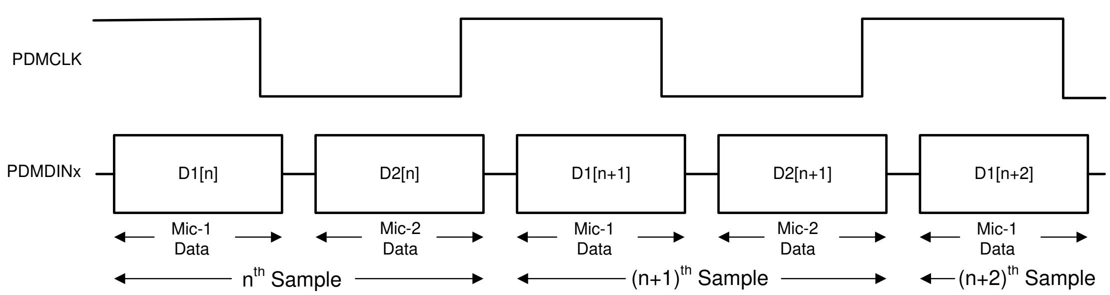


Figure 7-15. Digital PDM Microphone Protocol Timing Diagram

7.3.6 Signal-Chain Processing

The PCMD3140-Q1 signal chain is comprised of high-performance, low-power, and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the PCMD3140-Q1 optimized for a wide variety of end-equipment and applications that require multichannel audio capture. Figure 7-16 shows a conceptual block diagram that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.

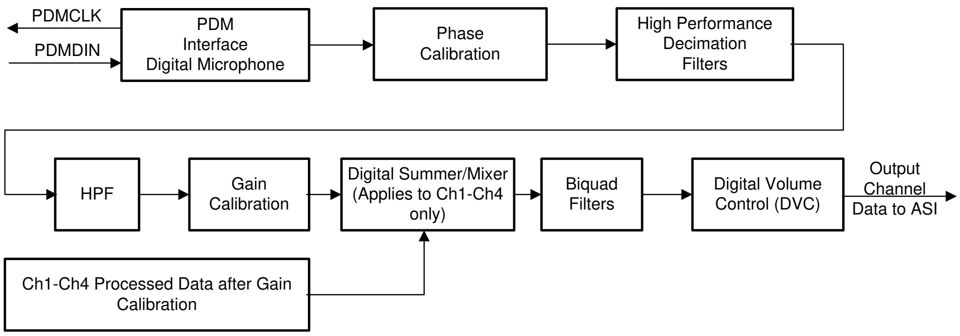


Figure 7-16. Signal-Chain Processing Flowchart

The device supports up to four digital PDM microphone recording channels for simultaneous operation. The signal chain consists of various highly programmable digital processing blocks such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, and volume control. The details on these processing blocks are discussed further in this section. Channels 1 to 4 in the signal chain block diagram of Figure 7-16 are as described in this section.

The desired input channels for recording can be enabled or disabled by using the IN_CH_EN (P0_R115) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI_OUT_EN (P0_R116) register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel recording is on, then that use case is supported by setting the DYN_CH_PUPD_EN (P0_R117_D4) register bit to 1'b1 but do not power-down channel 1 in this mode of operation.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

For output sample rates of 48 kHz or lower, the device supports all features for 4-channel recording and various programmable processing blocks. However, for output sample rates higher than 48 kHz, there are limitations in the number of simultaneous channel recordings supported and the number of biquad filters and such. See the *TLV320ADCx120 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

7.3.6.1 Programmable Digital Volume Control

The device has a programmable digital volume control with a range from –100 dB to 27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically when the channel is powered-up and recording. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang-up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the DVOL_GANG (P0_R108_D7) register bit.

Table 7-10 shows the programmable options available for the digital volume control.

Table 7-10. Digital Volume Control (DVC) Programmable Settings

P0_R62_D[7:0] : CH1_DVOL[7:0]	DVC SETTING FOR OUTPUT CHANNEL 1
0000 0000 = 0d	Output channel 1 DVC is set to mute
0000 0001 = 1d	Output channel 1 DVC is set to –100 dB
0000 0010 = 2d	Output channel 1 DVC is set to –99.5 dB
0000 0011 = 3d	Output channel 1 DVC is set to –99 dB
…	…
1100 1000 = 200d	Output channel 1 DVC is set to –0.5 dB
1100 1001 = 201d (default)	Output channel 1 DVC is set to 0 dB
1100 1010 = 202d	Output channel 1 DVC is set to 0.5 dB
…	…
1111 1101 = 253d	Output channel 1 DVC is set to 26 dB
1111 1110 = 254d	Output channel 1 DVC is set to 26.5 dB
1111 1111 = 255d	Output channel 1 DVC is set to 27 dB

Similarly, the digital volume control setting for output channel 2 to channel 4 can be configured using the CH2_DVOL (P0_R67) to CH4_DVOL (P0_R77) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

7.3.6.2 Programmable Channel Gain Calibration

Along with the programmable channel gain and digital volume, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. Table 7-11 shows the programmable options available for the channel gain calibration.

Table 7-11. Channel Gain Calibration Programmable Settings

P0_R63_D[7:4] : CH1_GCAL[3:0]	CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 = 0d	Input channel 1 gain calibration is set to –0.8 dB
0001 = 1d	Input channel 1 gain calibration is set to –0.7 dB
…	…
1000 = 8d (default)	Input channel 1 gain calibration is set to 0 dB
…	…
1110 = 14d	Input channel 1 gain calibration is set to 0.6 dB
1111 = 15d	Input channel 1 gain calibration is set to 0.7 dB

Similarly, the channel gain calibration setting for input channel 2 to channel 4 can be configured using the CH2_GCAL (P0_R68) to CH4_GCAL (P0_R78) register bits, respectively.

7.3.6.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error. Phase calibration clock is dependent on PDM clock used. For a PDM_CLK of 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz), the phase calibration clock is the same as the PDM_CLK. For a PDM_CLK equal to or lower than 3.072 MHz (the output data sample rate is multiples or submultiples of 48 kHz), the phase calibration clock used is 3.072 MHz. Similarly, for a PDM_CLK of 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (the output data sample rate is multiples or submultiples of 44.1 kHz), the phase calibration clock used is 2.8224MHz. This feature is very useful for many applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. Table 7-12 shows the available programmable options for channel phase calibration for a digital microphone with a PDM_CLK of 6.144 MHz or 5.6448 MHz.

Table 7-12. Channel Phase Calibration Programmable Settings

P0_R64_D[7:0] : CH1_PCAL[7:0]	CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 0000 = 0d (default)	Input channel 1 phase calibration with no delay
0000 0001 = 1d	Input channel 1 phase calibration delay is set to one cycle of the modulator clock
0000 0010 = 2d	Input channel 1 phase calibration delay is set to two cycles of the modulator clock
…	…
1111 1110 = 254d	Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock
1111 1111 = 255d	Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock

For a digital microphone interface with a PDM_CLK frequency below 3.072 MHz, the phase calibration range is from 0 to 127 of the phase calibration clock (3.072 MHz for the output data sample rate is multiples or submultiples of 48 kHz and 2.8224 MHz for the output data sample rate is multiples or submultiples of 44.1 kHz). The phase calibration for a PDM_CLK frequency below 3.072 MHz can be configured using the CH1_PCAL[7:1] register bits for channel 1.

Similarly, the channel phase calibration setting for input channel 2 to channel 4 can be configured using the CH2_PCAL (P0_R69) to CH4_PCAL (P0_R79) register bits, respectively.

7.3.6.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all the channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. Table 7-13 shows the predefined –3-dB cutoff frequencies available that can be set by using the HPF_SEL[1:0] register bits of P0_R107. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF_SEL[1:0] register bits are set to 2'b00. Figure 7-17 illustrates a frequency response plot for the HPF filter.

Table 7-13. HPF Programmable Settings

P0_R107_D[1:0] : HPF_SEL[1:0]	-3-dB CUTOFF FREQUENCY SETTING	-3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	-3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
00	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter
01 (default)	$0.00025 \times f_S$	4 Hz	12 Hz
10	$0.002 \times f_S$	32 Hz	96 Hz
11	$0.008 \times f_S$	128 Hz	384 Hz

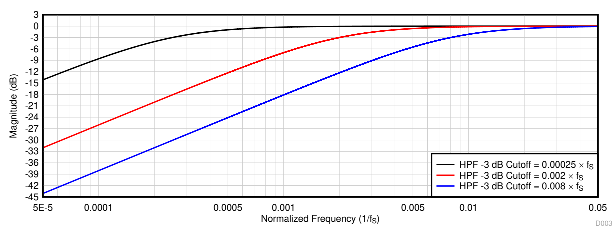


Figure 7-17. HPF Filter Frequency Response Plot

Equation 1 gives the transfer function for the first-order programable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \tag{1}$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in Table 7-14 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any PDM channel for recording. These programmable coefficients are 32-bit, two's complement numbers. Table 7-14 shows the filter coefficients for the first-order IIR filter.

Table 7-14. 1st-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	DEFAULT COEFFICIENT VALUE	COEFFICIENT REGISTER MAPPING
Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter)	N_0	0x7FFFFFFF	P4_R72-R75
	N_1	0x00000000	P4_R76-R79
	D_1	0x00000000	P4_R80-R83

7.3.6.5 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters. These highly efficient filters achieve the desired frequency response. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. Equation 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \tag{2}$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in the *Section 7.6.3.1* and *Section 7.6.3.2* sections. If biquad filtering is required, then the host device must write these coefficients values before powering up any PDM channels for recording. These programmable coefficients are 32-bit, two's complement numbers. As described in Table 7-15, these biquad filters can be allocated for each output channel based on the BIQUAD_CFG[1:0] register setting of P0_R108. By setting BIQUAD_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional filtering is required for the system application. See the *TLV320ADCx140 Programmable Biquad Filter Configuration and Applications* application report for further details.

Table 7-15. Biquad Filter Allocation to the Record Output Channel

PROGRAMMABLE BIQUAD FILTER	RECORD OUTPUT CHANNEL ALLOCATION USING P0_R108_D[6:5] REGISTER SETTING		
	BIQUAD_CFG[1:0] = 2'b01 (1 Biquad per Channel)	BIQUAD_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	BIQUAD_CFG[1:0] = 2'b11 (3 Biquads per Channel)
	SUPPORTS ALL 8 CHANNELS	SUPPORTS UP TO 6 CHANNELS	SUPPORTS UP TO 4 CHANNELS
Biquad filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 5	Not used	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 6	Not used	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 7	Not used	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 8	Not used	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 9	Not used	Not used	Allocated to output channel 1
Biquad filter 10	Not used	Not used	Allocated to output channel 2
Biquad filter 11	Not used	Not used	Allocated to output channel 3
Biquad filter 12	Not used	Not used	Allocated to output channel 4

Table 7-16 shows the biquad filter coefficients mapping to the register space.

Table 7-16. Biquad Filter Coefficients Register Mapping

PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING	PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING
Biquad filter 1	P2_R8-R27	Biquad filter 7	P3_R8-R27
Biquad filter 2	P2_R28-R47	Biquad filter 8	P3_R28-R47
Biquad filter 3	P2_R48-R67	Biquad filter 9	P3_R48-R67
Biquad filter 4	P2_R68-R87	Biquad filter 10	P3_R68-R87
Biquad filter 5	P2_R88-R107	Biquad filter 11	P3_R88-R107
Biquad filter 6	P2_R108-R127	Biquad filter 12	P3_R108-R127

7.3.6.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise. Table 7-17 lists the configuration settings available for channel summing mode.

Table 7-17. Channel Summing Mode Programmable Settings

P0_R107_D[3:2] : CH_SUM[2:0]	CHANNEL SUMMING MODE FOR INPUT CHANNELS	SNR AND DYNAMIC RANGE BOOST
00 (default)	Channel summing mode is disabled	Not applicable
01	Output channel 1 = (input channel 1 + input channel 2) / 2	3-dB boost in SNR and dynamic range
	Output channel 2 = (input channel 1 + input channel 2) / 2	
	Output channel 3 = (input channel 3 + input channel 4) / 2	3-dB boost in SNR and dynamic range
	Output channel 4 = (input channel 3 + input channel 4) / 2	
10	Reserved (do not use this setting)	Not applicable
11	Reserved (do not use this setting)	Not applicable

The device additionally supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. The programmable mixer feature is available only if CH_SUM[2:0] is set to 2'b00. The mixer function is supported for all 4 input channels. Figure 7-18 shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the *Section 7.6.3.3* section. All mixer coefficients are 32-bit, two's complement numbers using a 1.31 number format. The value of 0x7FFFFFFF is equivalent to +1 (0-dB gain), the value 0x00000000 is equivalent to mute (zero data), and any values in between set the mixer attenuation computed using Equation 3. If the MSB is set to '1' then the attenuation remains the same but the signal phase is inverted.

$$\text{hex2dec (value)} / 2^{31} \tag{3}$$

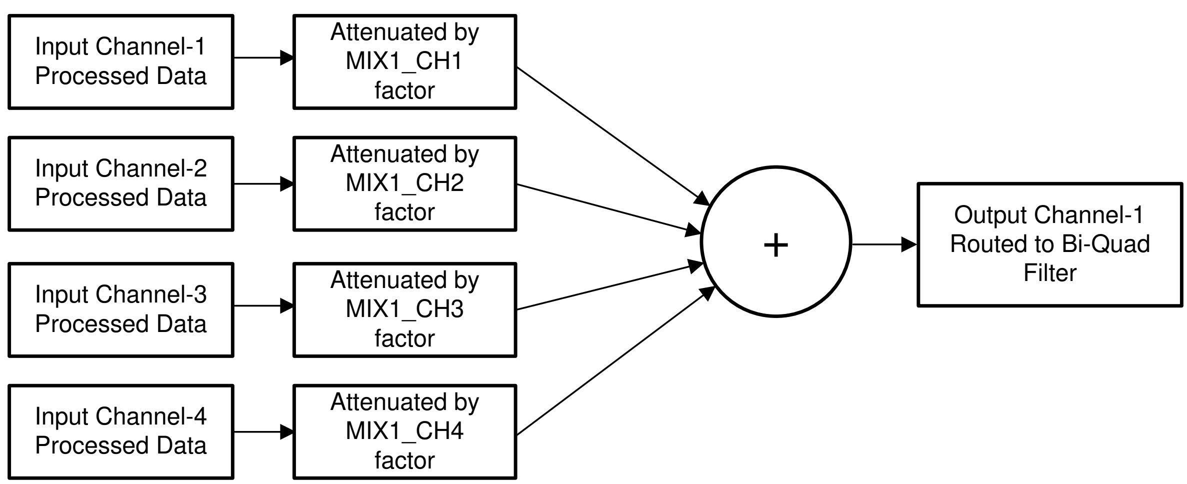


Figure 7-18. Programmable Digital Mixer Block Diagram

A similar mixer operation is performed by mixer 2, mixer 3, and mixer 4 to generate output channel 2, channel 3, and channel 4, respectively.

7.3.6.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled PDM data stream from the digital microphone to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the DECI_FILT (P0_R107_D[5:4]) register bits. Table 7-18 shows the configuration register setting for the decimation filter mode selection for the record channel.

Table 7-18. Decimation Filter Mode Selection for the Record Channel

P0_R107_D[5:4] : DECI_FILT[1:0]	DECIMATION FILTER MODE SELECTION
00 (default)	Linear phase filters are used for the decimation
01	Low latency filters are used for the decimation
10	Ultra-low latency filters are used for the decimation
11	Reserved (do not use this setting)

7.3.6.7.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.6.7.1.1 Sampling Rate: 7.35 kHz to 8 kHz

Figure 7-19 and Figure 7-20 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 7.35 kHz to 8 kHz. Table 7-19 lists the specifications for a decimation filter with a 7.35-kHz to 8-kHz sampling rate.

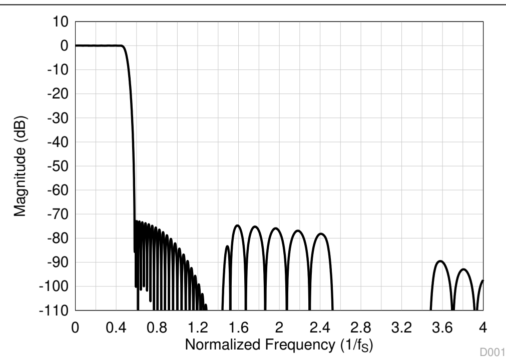


Figure 7-19. Linear Phase Decimation Filter Magnitude Response

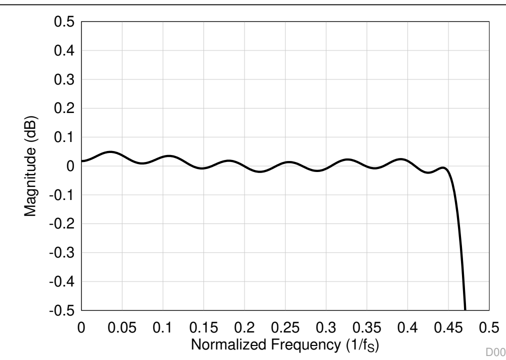


Figure 7-20. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-19. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

7.3.6.7.1.2 Sampling Rate: 14.7 kHz to 16 kHz

Figure 7-21 and Figure 7-22 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 14.7 kHz to 16kHz. Table 7-20 lists the specifications for a decimation filter with a 14.7-kHz to 16 kHz sampling rate.

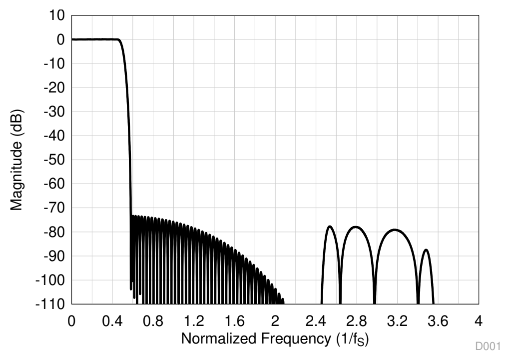


Figure 7-21. Linear Phase Decimation Filter Magnitude Response

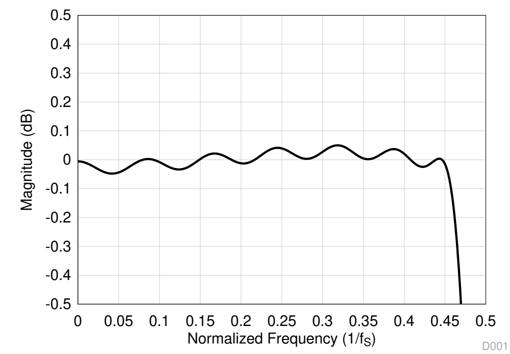


Figure 7-22. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-20. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		$1/f_S$

7.3.6.7.1.3 Sampling Rate: 22.05 kHz to 24 kHz

Figure 7-23 and Figure 7-24 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 7-21 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

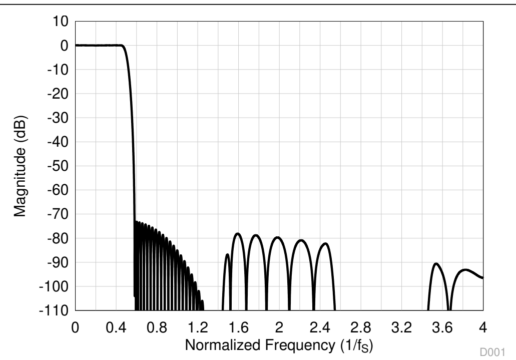


Figure 7-23. Linear Phase Decimation Filter Magnitude Response

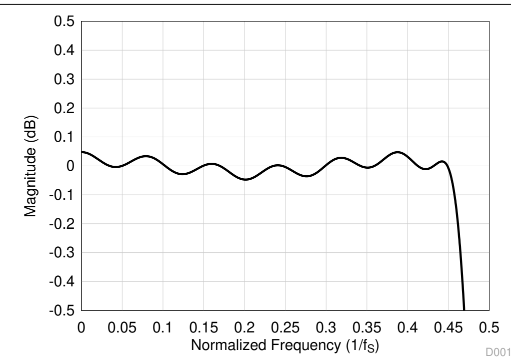


Figure 7-24. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-21. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		$1/f_S$

7.3.6.7.1.4 Sampling Rate: 29.4 kHz to 32 kHz

Figure 7-25 and Figure 7-26 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 7-22 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

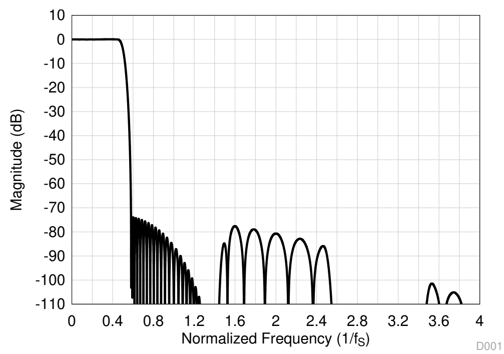


Figure 7-25. Linear Phase Decimation Filter Magnitude Response

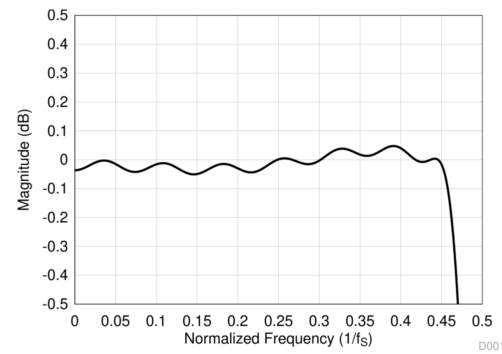


Figure 7-26. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-22. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		$1/f_S$

7.3.6.7.1.5 Sampling Rate: 44.1 kHz to 48 kHz

Figure 7-27 and Figure 7-28 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 7-23 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

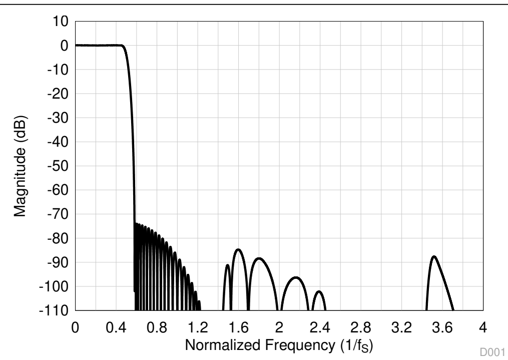


Figure 7-27. Linear Phase Decimation Filter Magnitude Response

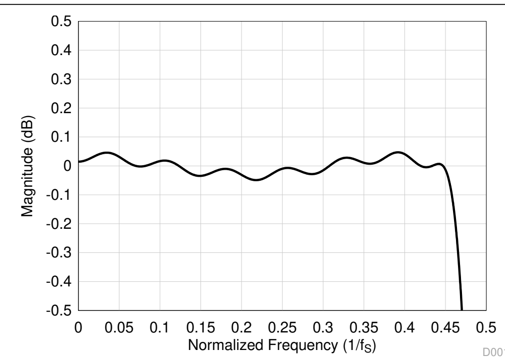


Figure 7-28. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-23. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

7.3.6.7.1.6 Sampling Rate: 88.2 kHz to 96 kHz

Figure 7-29 and Figure 7-30 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 7-24 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

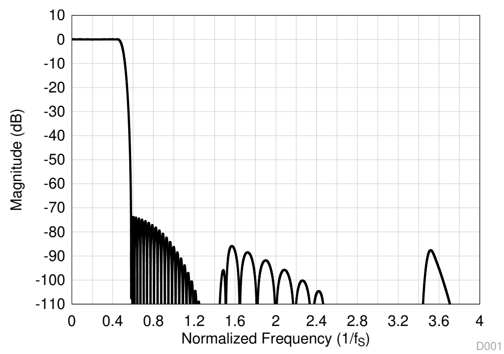


Figure 7-29. Linear Phase Decimation Filter Magnitude Response

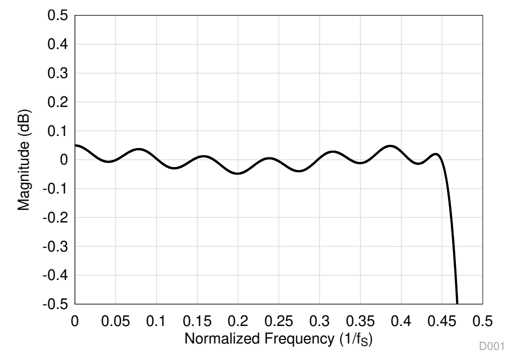


Figure 7-30. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-24. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

7.3.6.7.1.7 Sampling Rate: 176.4 kHz to 192 kHz

Figure 7-31 and Figure 7-32 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 7-25 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

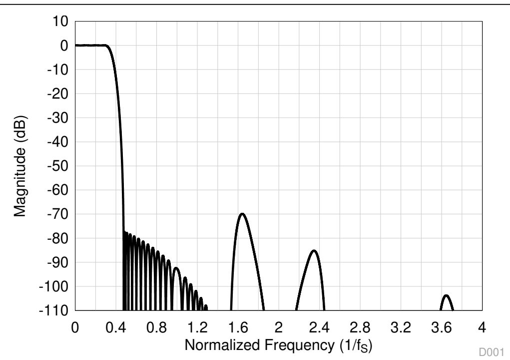


Figure 7-31. Linear Phase Decimation Filter Magnitude Response

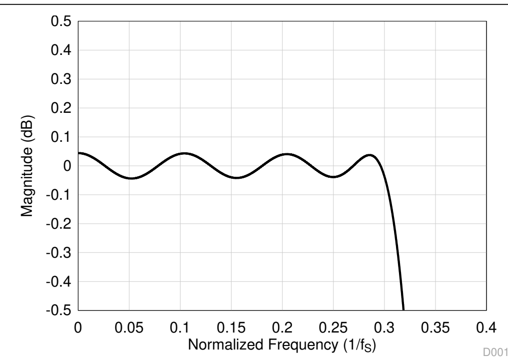


Figure 7-32. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-25. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		$1/f_S$

7.3.6.7.1.8 Sampling Rate: 352.8 kHz to 384 kHz

Figure 7-33 and Figure 7-34 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. Table 7-26 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

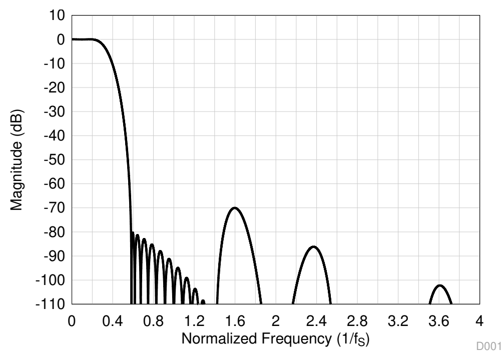


Figure 7-33. Linear Phase Decimation Filter Magnitude Response

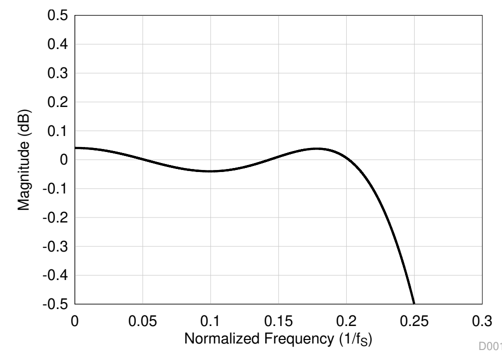


Figure 7-34. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-26. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.212 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	108.8			
Group delay or latency	Frequency range is 0 to 0.212 × f_S		7.2		1/f_S

7.3.6.7.1.9 Sampling Rate: 705.6 kHz to 768 kHz

Figure 7-35 and Figure 7-36 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 705.6 kHz to 768 kHz. Table 7-27 lists the specifications for a decimation filter with a 705.6-kHz to 768-kHz sampling rate.

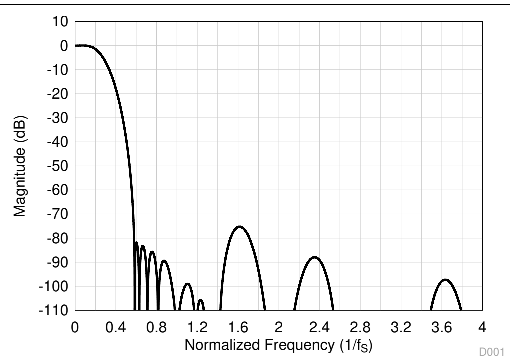


Figure 7-35. Linear Phase Decimation Filter Magnitude Response

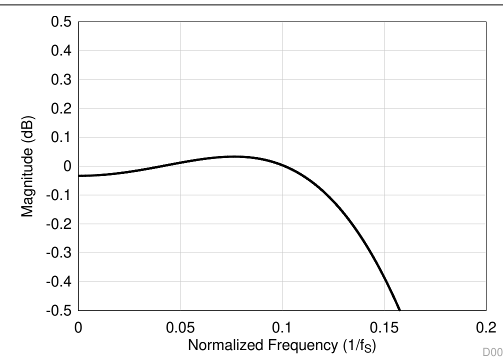


Figure 7-36. Linear Phase Decimation Filter Pass-Band Ripple

Table 7-27. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.113 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 2 × f_S	75.0			dB
	Frequency range is 2 × f_S onwards	88.0			
Group Delay or Latency	Frequency range is 0 to 0.113 × f_S		5.9		1/f_S

7.3.6.7.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCMD3140-Q1 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

7.3.6.7.2.1 Sampling Rate: 14.7 kHz to 16 kHz

Figure 7-37 shows the magnitude response and Figure 7-38 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. Table 7-28 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

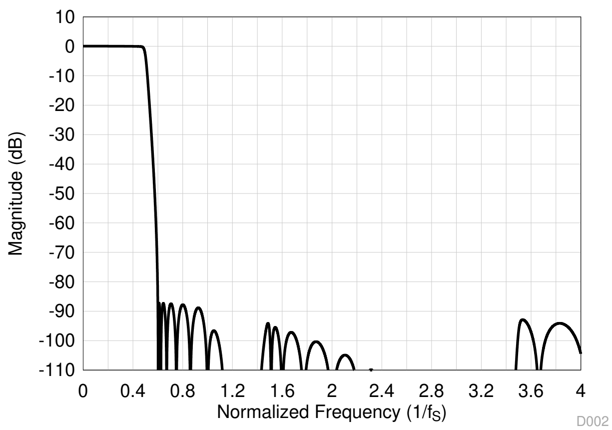


Figure 7-37. Low-Latency Decimation Filter Magnitude Response

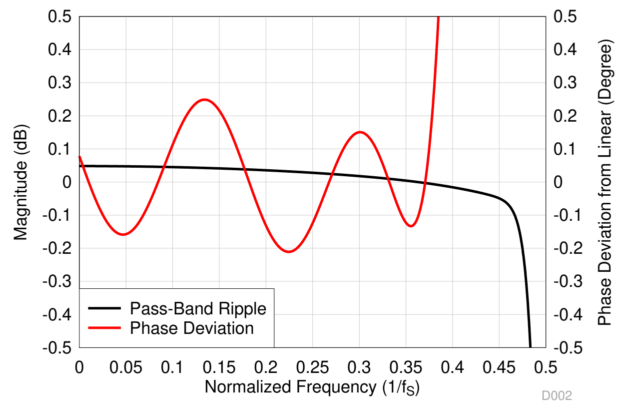


Figure 7-38. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-28. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	$1/f_S$
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

7.3.6.7.2.2 Sampling Rate: 22.05 kHz to 24 kHz

Figure 7-39 shows the magnitude response and Figure 7-40 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 7-29 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

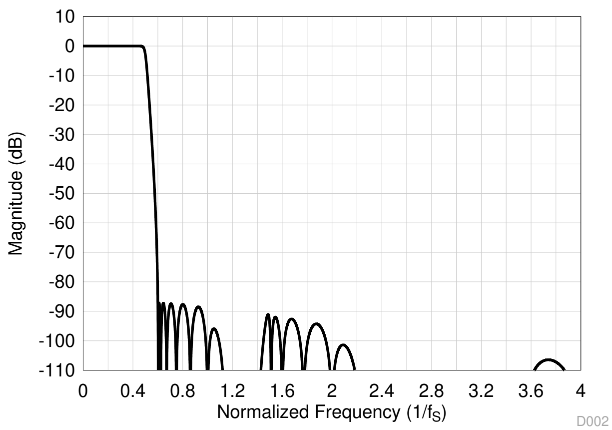


Figure 7-39. Low-Latency Decimation Filter Magnitude Response

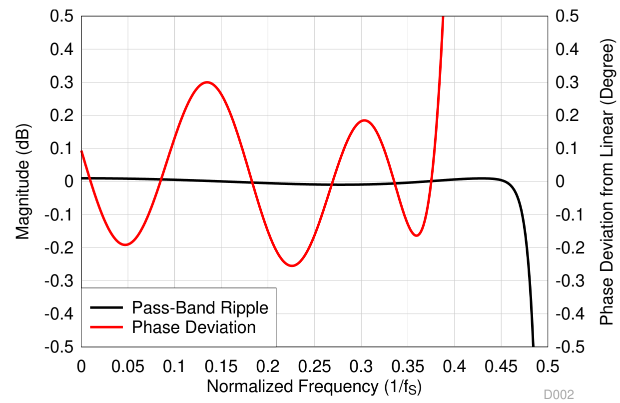


Figure 7-40. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-29. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

7.3.6.7.2.3 Sampling Rate: 29.4 kHz to 32 kHz

Figure 7-41 shows the magnitude response and Figure 7-42 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 7-30 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

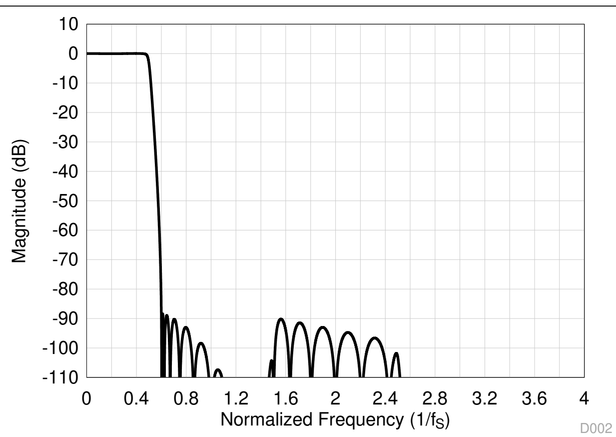


Figure 7-41. Low-Latency Decimation Filter Magnitude Response

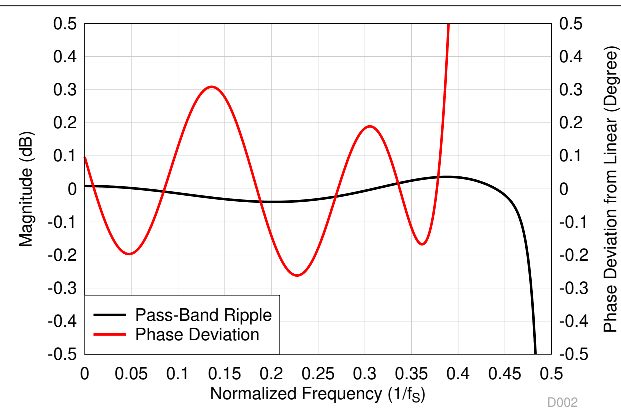


Figure 7-42. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-30. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

7.3.6.7.2.4 Sampling Rate: 44.1 kHz to 48 kHz

Figure 7-43 shows the magnitude response and Figure 7-44 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 7-31 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

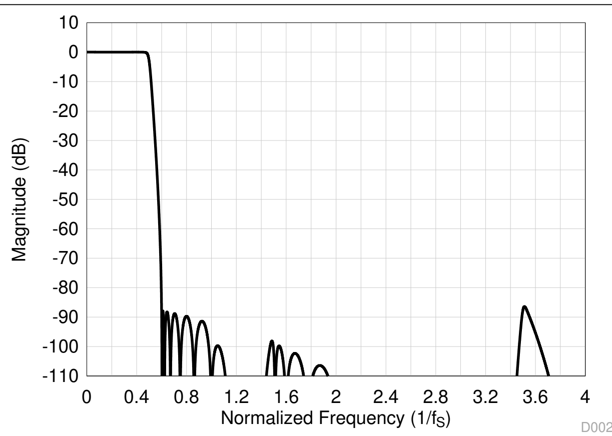


Figure 7-43. Low-Latency Decimation Filter Magnitude Response

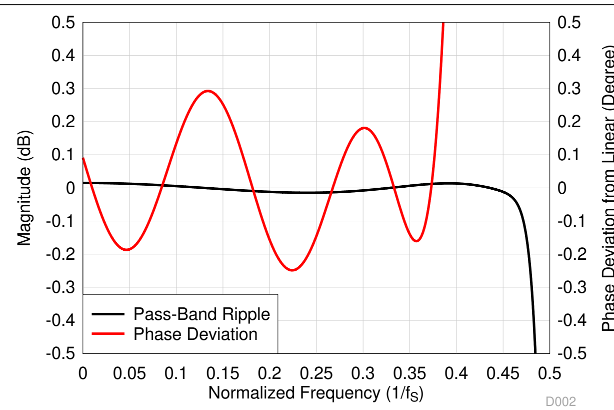


Figure 7-44. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-31. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

7.3.6.7.2.5 Sampling Rate: 88.2 kHz to 96 kHz

Figure 7-45 shows the magnitude response and Figure 7-46 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 7-32 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

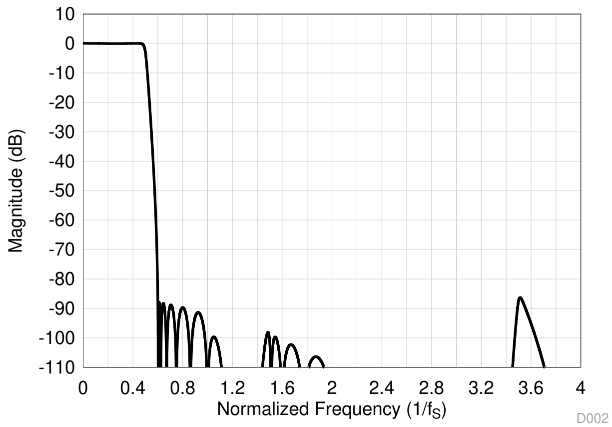


Figure 7-45. Low-Latency Decimation Filter Magnitude Response

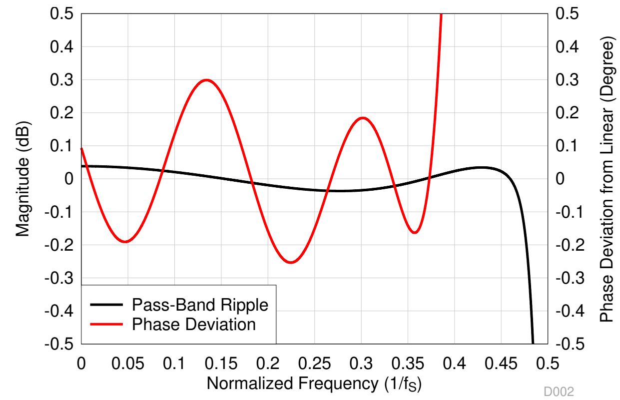


Figure 7-46. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-32. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

7.3.6.7.2.6 Sampling Rate: 176.4 kHz to 192 kHz

Figure 7-47 shows the magnitude response and Figure 7-48 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 7-33 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

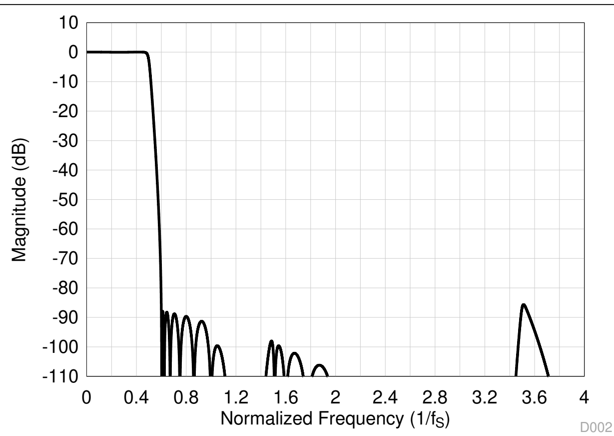


Figure 7-47. Low-Latency Decimation Filter Magnitude Response

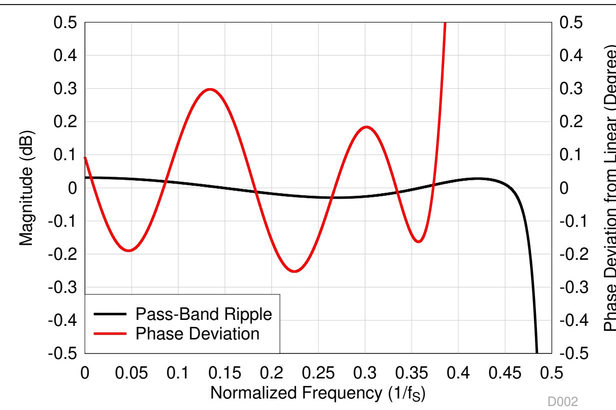


Figure 7-48. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-33. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

7.3.6.7.3 Ultra-Low-Latency Filters

For applications where ultra-low latency (within the audio band) is critical, the ultra-low-latency decimation filters on the PCMD3140-Q1 can be used. The device supports these filters with a group delay of approximately four samples with an almost linear phase response within the 0.325 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the ultra-low-latency filters.

7.3.6.7.3.1 Sampling Rate: 14.7 kHz to 16 kHz

Figure 7-49 shows the magnitude response and Figure 7-50 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. Table 7-34 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

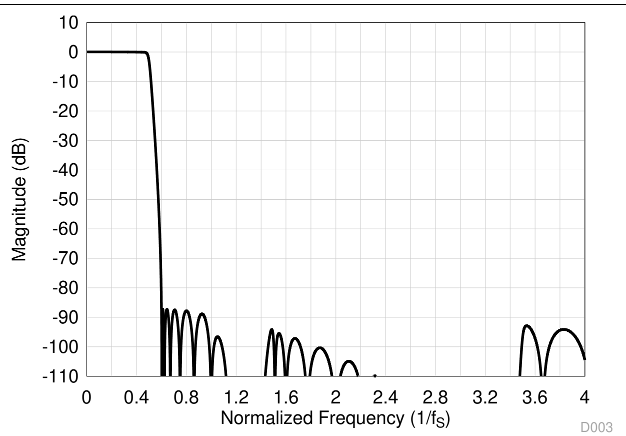


Figure 7-49. Ultra-Low-Latency Decimation Filter Magnitude Response

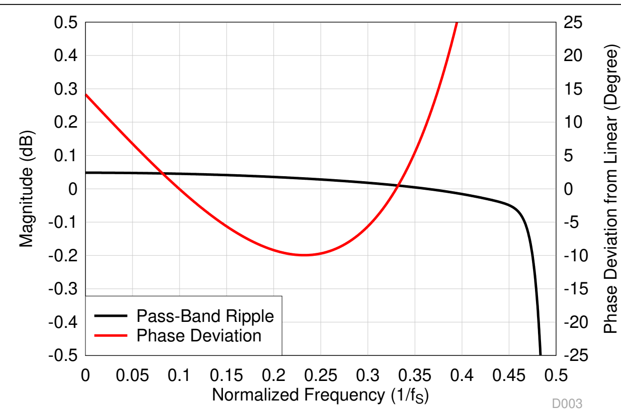


Figure 7-50. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-34. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.45 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.3		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.512		0.512	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.2	Degrees

7.3.6.7.3.2 Sampling Rate: 22.05 kHz to 24 kHz

Figure 7-51 shows the magnitude response and Figure 7-52 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 7-35 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

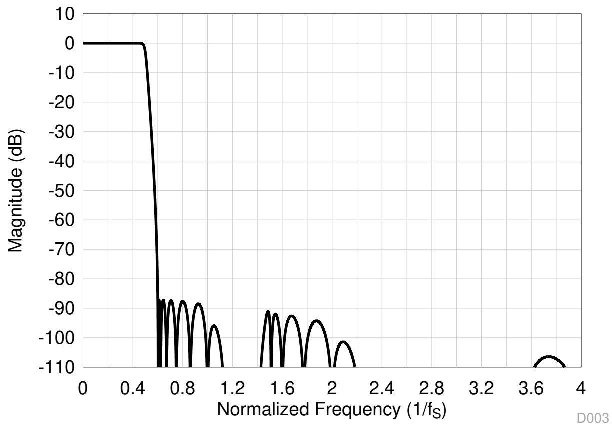


Figure 7-51. Ultra-Low-Latency Decimation Filter Magnitude Response

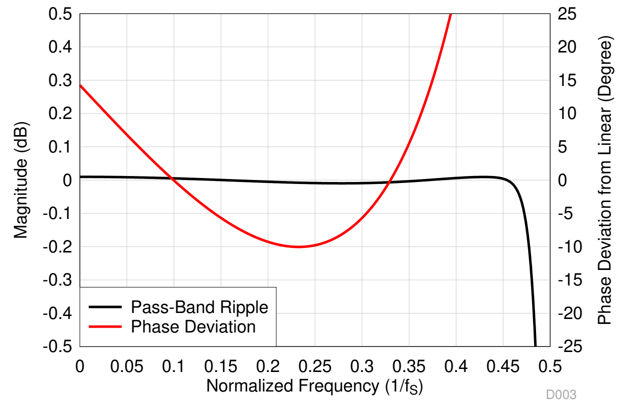


Figure 7-52. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-35. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.46 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.1			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.514		0.514	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.3	Degrees

7.3.6.7.3.3 Sampling Rate: 29.4 kHz to 32 kHz

Figure 7-53 shows the magnitude response and Figure 7-54 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 7-36 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

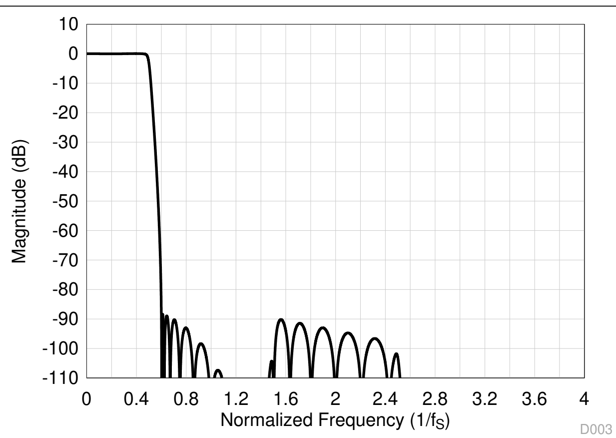


Figure 7-53. Ultra-Low-Latency Decimation Filter Magnitude Response

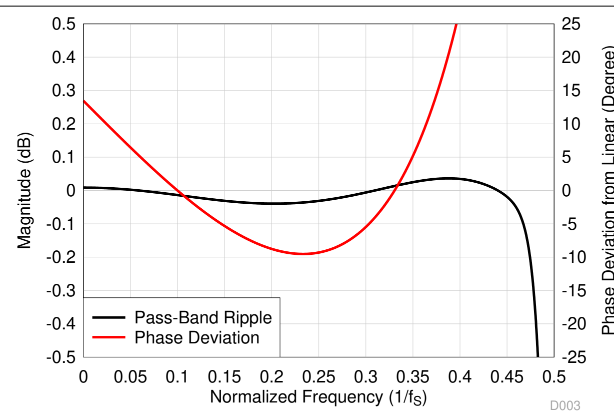


Figure 7-54. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-36. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		5.2		1/f_S
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.492		0.492	1/f_S
Phase deviation	Frequency range is 0 to 0.325 × f_S	–9.5		13.5	Degrees

7.3.6.7.3.4 Sampling Rate: 44.1 kHz to 48 kHz

Figure 7-55 shows the magnitude response and Figure 7-56 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 7-37 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

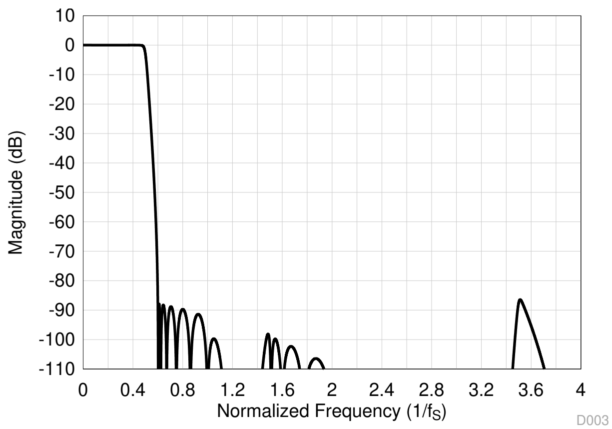


Figure 7-55. Ultra-Low-Latency Decimation Filter Magnitude Response

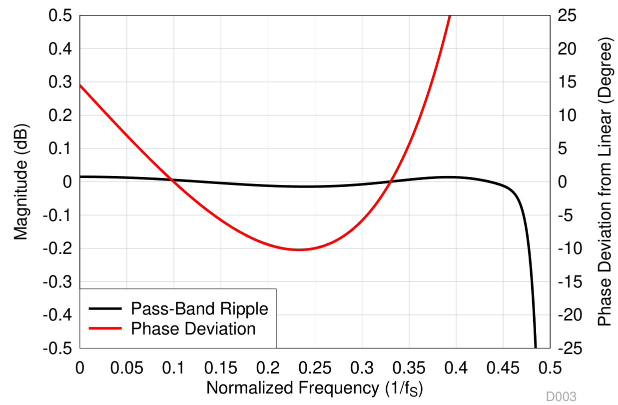


Figure 7-56. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-37. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		1/f_S
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.525		0.525	1/f_S
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.3		14.5	Degrees

7.3.6.7.3.5 Sampling Rate: 88.2 kHz to 96 kHz

Figure 7-57 shows the magnitude response and Figure 7-58 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 7-38 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

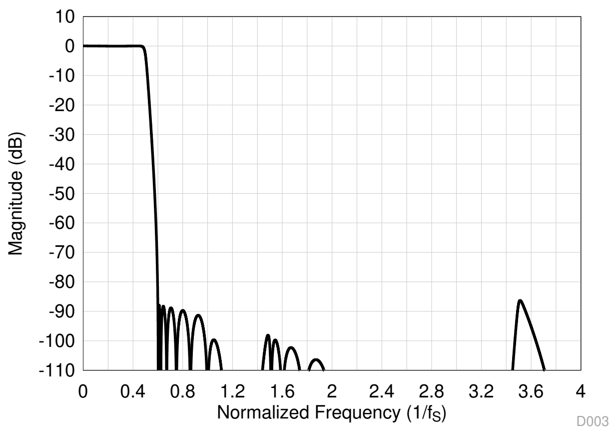


Figure 7-57. Ultra-Low-Latency Decimation Filter Magnitude Response

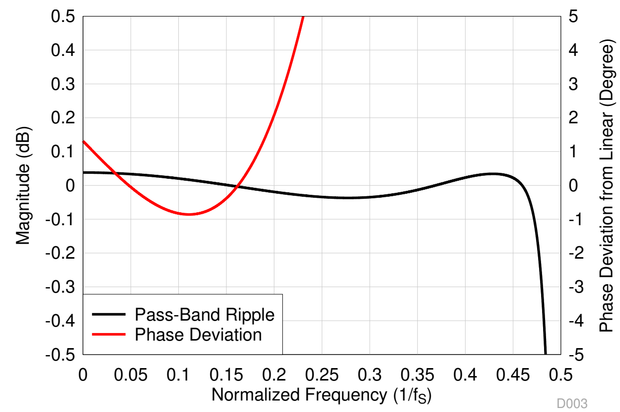


Figure 7-58. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-38. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.1625 × f_S		3.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.1625 × f_S	–0.091		0.091	$1/f_S$
Phase deviation	Frequency range is 0 to 0.1625 × f_S	–0.86		1.30	Degrees

7.3.6.7.3.6 Sampling Rate: 176.4 kHz to 192 kHz

Figure 7-59 shows the magnitude response and Figure 7-60 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 7-39 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

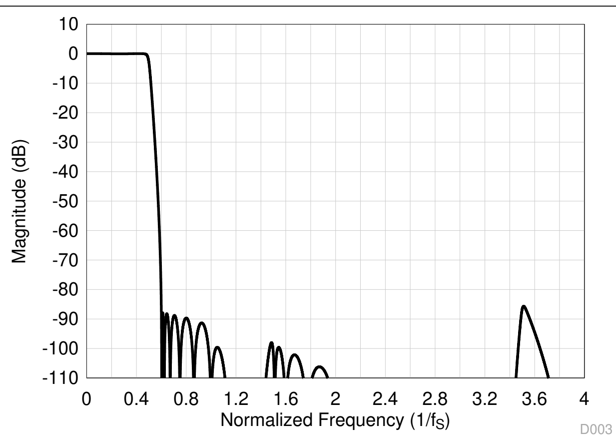


Figure 7-59. Ultra-Low-Latency Decimation Filter Magnitude Response

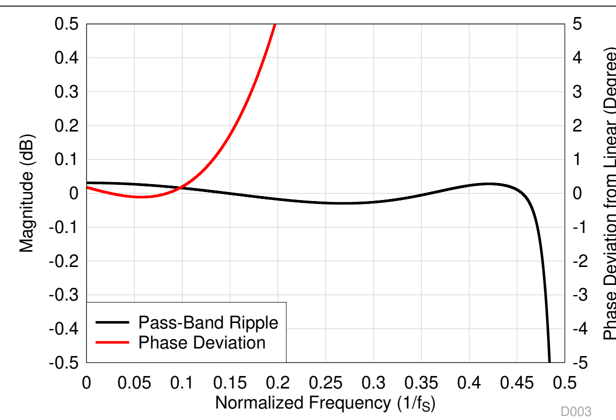


Figure 7-60. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-39. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.085 × f_S		3.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.085 × f_S	–0.024		0.024	$1/f_S$
Phase deviation	Frequency range is 0 to 0.085 × f_S	–0.12		0.18	Degrees

7.3.6.7.3.7 Sampling Rate: 352.8 kHz to 384 kHz

Figure 7-61 shows the magnitude response and Figure 7-62 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. Table 7-40 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

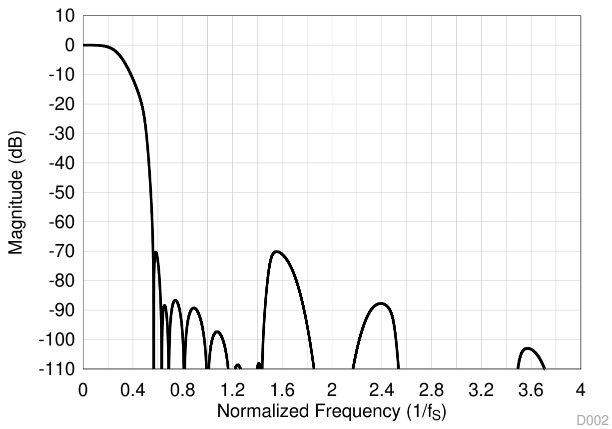


Figure 7-61. Ultra-Low-Latency Decimation Filter Magnitude Response

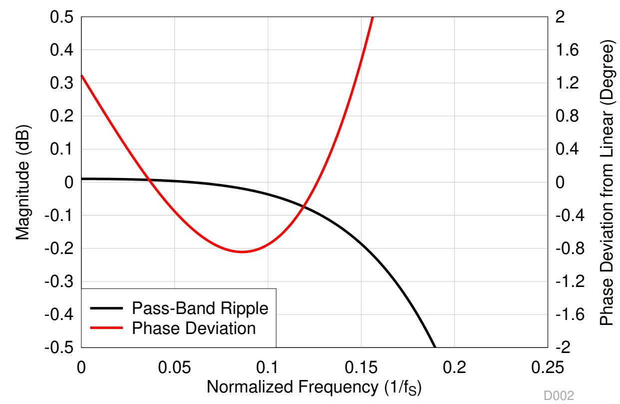


Figure 7-62. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-40. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.1 × f_S	–0.04		0.01	dB
Stop-band attenuation	Frequency range is 0.56 × f_S onwards	70.1			dB
Group delay or latency	Frequency range is 0 to 0.157 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.157 × f_S	–0.18		0.18	$1/f_S$
Phase deviation	Frequency range is 0 to 0.157 × f_S	–0.85		2.07	Degrees

7.3.7 Voice Activity Detection (VAD)

The PCMD3140-Q1 supports voice activity detection (VAD) mode. In this mode, the PCMD3140-Q1 continuously monitors one of the input channels for voice detection. The device consumes low quiescent current from the AVDD supply in this mode. This feature can be enabled by setting the VAD_EN (P0_R117_D0) bit to 1'b1. On detecting voice activity, the PCMD3140-Q1 can alert the host through an interrupt or auto wake up and start recording based on the I^2C programmed configuration. This feature can configured through the VAD_MODE (P1_R30_D[7:6]) register bits.

The input channel for the VAD can be selected by setting the VAD_CH_SEL (P1_R30_D[5:4]) register bits to an appropriate value. See the *Using the Voice Activity Detector (VAD) in the TLV320ADCx120 and PCMx120-Q1* application report for further details.

7.3.8 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down the record channel as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the record channel. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7] (P0_R51_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT_LTCH0 (P0_R54), which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIO1 or GPOx pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT_POL (P0_R50_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0] (P0_R50_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV_STS0 (P0_R118) and DEV_STS1 (P0_R119) registers.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. Additionally, GPIx and GPOx can be repurposed as multifunction pins GPIx and GPOx respectively, as required for system application. Table 7-41 shows all possible allocations of these multifunctional pins for the various features.

Table 7-41. Multifunction Pin Assignments

ROW	PIN FUNCTION	GPIO1	GPO1	GPI1	GPI2
—	—	GPIO1_CFG	GPO1_CFG	GPI1_CFG	GPI2_CFG
—	—	P0_R33[7:4]	P0_R34[7:4]	P0_R43[6:4]	P0_R43[2:0]
A	Pin disabled	S(1)	S (default)	S (default)	S (default)
B	General-purpose output (GPO)	S	S	NS(2)	NS
C	Interrupt output (IRQ)	S (default)	S	NS	NS
D	Power-down for all record channels	S	NS	S	S
E	PDM clock output (PDMCLK)	S	S	NS	NS
F	MiCBIAS on/off input (BIASEN)	S	NS	NS	NS
G	General-purpose input (GPI)	S	NS	S	S
H	Master clock input (MCLK)	S	NS	S	S
I	ASI daisy-chain input (SDIN)	S	NS	S	S
J	PDM data input 1 (PDMDIN1)	S	NS	S	S
K	PDM data input 2 (PDMDIN2)	S	NS	S	S

(1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.
(2) NS means the feature mentioned in this row is *not supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPOx_DRV[3:0] or GPIO1_DRV[3:0] register bits. Table 7-42 lists the drive configuration settings.

Table 7-42. GPIO or GPOx Pins Drive Configuration Settings

P0_R33_D[3:0] : GPIO1_DRV[3:0]	GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1
000	The GPIO1 pin is set to high impedance (floated)
001	The GPIO1 pin is set to be driven active low or active high
010 (default)	The GPIO1 pin is set to be driven active low or weak high (on-chip pullup)
011	The GPIO1 pin is set to be driven active low or Hi-Z (floated)
100	The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high
101	The GPIO1 pin is set to be driven Hi-Z (floated) or active high
110 and 111	Reserved (do not use these settings)

Similarly, the GPO1 pin can be configured using the GPO1_DRV (P0_R34) register bits.

When configured as a general-purpose output (GPO), the GPIO1 or GPOx pin values can be driven by writing the GPIO_VAL or GPOx_VAL (P0_R41) registers. The GPIO_MON (P0_R42) register can be used to readback the status of the GPIO1 pin when configured as a general-purpose input (GPI). Similarly, the GPI_MON (P0_R47) register can be used to readback the status of the GPIx pins when configured as a general-purpose input (GPI).

7.4 Device Functional Modes

7.4.1 Sleep Mode or Software Shutdown

In sleep mode or software shutdown mode, the device consumes very low quiescent current from the AVDD supply and, at the same time, allows the I^{2}C communication to wake the device for active operation.

The device enters sleep mode when the host device sets the SLEEP_ENZ (P0_R2_D0) bit to 1'b0. If the SLEEP_ENZ bit is asserted low when the device is in active mode, the device ramps down the volume on the record data, powers down the analog and digital blocks, and enters sleep mode. However, the device still continues to retain the last programmed value of the device configuration registers and programmable coefficients.

In sleep mode, do not perform any I^{2}C transactions, except for exiting sleep mode in order to enter active mode. After entering sleep mode, wait at least 10 ms before starting I^{2}C transactions to exit sleep mode.

When exiting sleep mode, the host device must configure the PCMD3140-Q1 to use either an external 1.8-V AREG supply (default setting) or an on-chip, regulator-generated AREG supply. To configure the AREG supply, write to AREG_SELECT (bit D7) in the same P0_R2 register.

7.4.2 Active Mode

If the host device exits sleep mode by setting the SLEEP_ENZ bit to 1'b1, the device enters active mode. In active mode, I^{2}C transactions can be done to configure and power-up the device for active operation. After entering active mode, wait at least 1 ms before starting any I^{2}C transactions to allow the device to complete the internal wake-up sequence.

Read and write operations to the programmable coefficient registers in page 2, page 3, and page 4 and to the channel configuration registers (CHx_CFG[1:4]) in page 0 must be done 10 ms after exiting sleep mode.

After configuring all other registers for the target application and system settings, configure the input and output channel enable registers, IN_CH_EN (P0_R115) and ASI_OUT_CH_EN (P0_R116), respectively. Lastly, configure the device power-up register, PWR_CFG (P0_R117). All programmable coefficient values must be written before powering up the respective channel.

In active mode, the power-up and power-down status of various blocks is monitored by reading the read-only device status bits located in the DEV_STS0 (P0_R117) and DEV_STS1 (P0_R118) registers.

7.4.3 Software Reset

A software reset can be done any time by asserting the SW_RESET (P0_R1_D0) bit, which is a self-clearing bit. This software reset immediately shuts down the device, and restores all device configuration registers and programmable coefficients to their default values.

7.5 Programming

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. These registers are called *device control registers* and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3, and page 4. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

7.5.1 Control Serial Interfaces

The device control registers can be accessed using I^{2}C communication to the device. The device operates with a fixed I^{2}C address and can be configured using this address.

7.5.1.1 I^{2}C Control Interface

The device supports the I^{2}C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. The I^{2}C control protocol requires a 7-bit target address. The 7-bit target address is fixed at 1001110 and cannot be changed. If the I2C_BRDCAST_EN (P0_R2_D2) bit is set to 1'b1, then the I^{2}C target address is fixed to 1001100 in order to allow simultaneous I^{2}C broadcast communication to multiple devices in the system including the PCMD3140-Q1 and PCMD3180-Q1. Table 7-43 lists the possible device addresses resulting from this configuration.

Table 7-43. I^{2}C Target Address Settings

I2C_BRDCAST_EN (P0_R2_D2)	I^{2}C TARGET ADDRESS
0 (default)	1001 110
1	1001 100

7.5.1.1.1 General I^{2}C Operation

The I^{2}C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 7-63 shows a generic data transfer sequence.

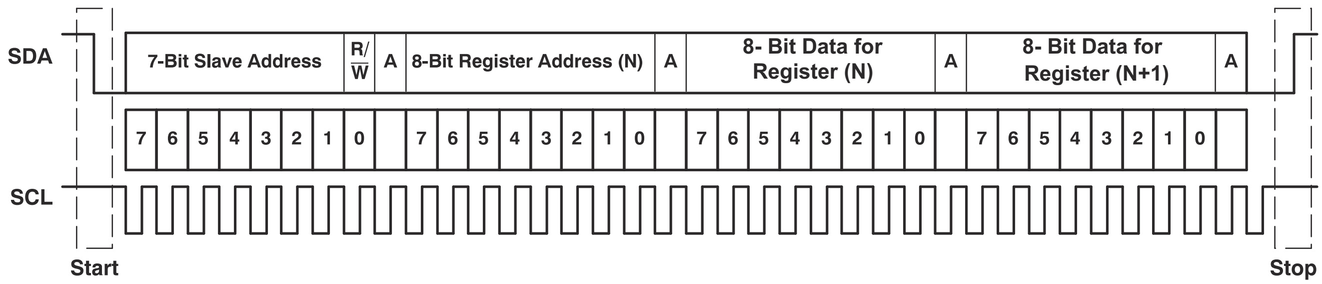


Figure 7-63. Typical I^{2}C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

7.5.1.1.2 I^{2}C Single-Byte and Multiple-Byte Transfers

The device I^{2}C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I^{2}C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I^{2}C write transaction takes place. For I^{2}C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

7.5.1.1.2.1 I^{2}C Single-Byte Write

As shown in Figure 7-64, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I^{2}C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.

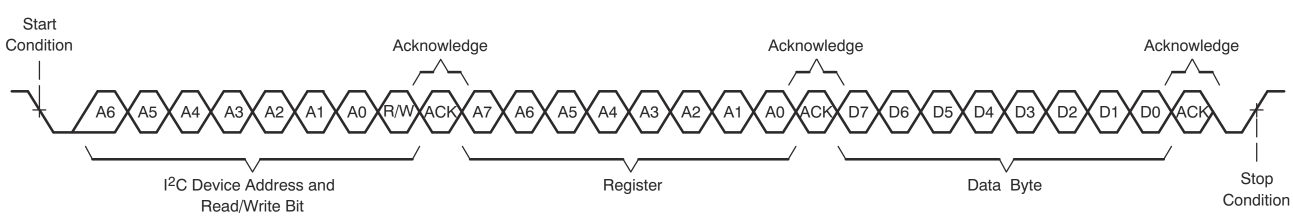


Figure 7-64. I^{2}C Single-Byte Write Transfer

7.5.1.1.2.2 I²C Multiple-Byte Write

As shown in Figure 7-65, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

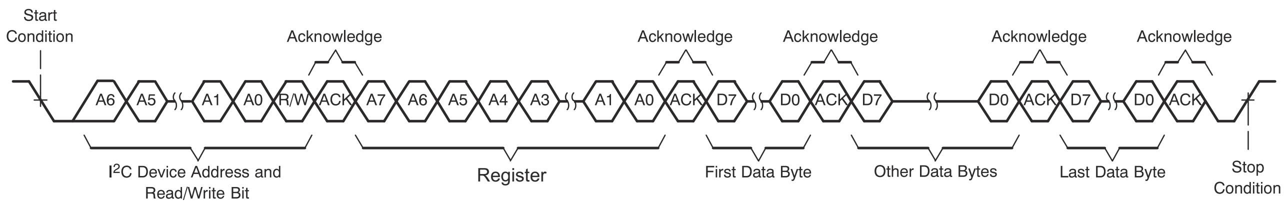


Figure 7-65. I²C Multiple-Byte Write Transfer

7.5.1.1.2.3 I²C Single-Byte Read

As shown in Figure 7-66, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I²C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.

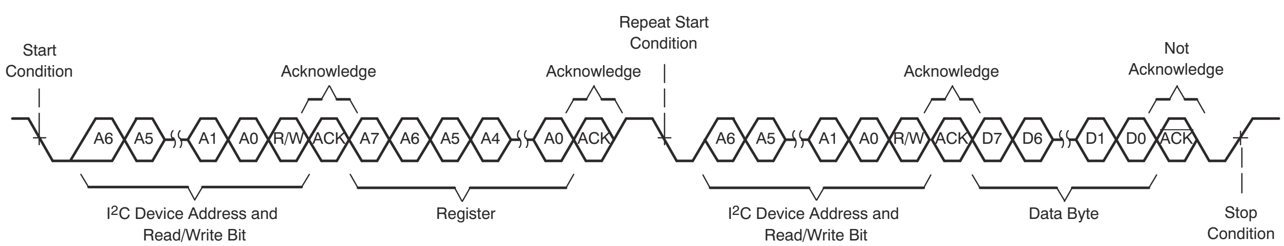


Figure 7-66. I²C Single-Byte Read Transfer

7.5.1.1.2.4 I²C Multiple-Byte Read

As shown in Figure 7-67, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.

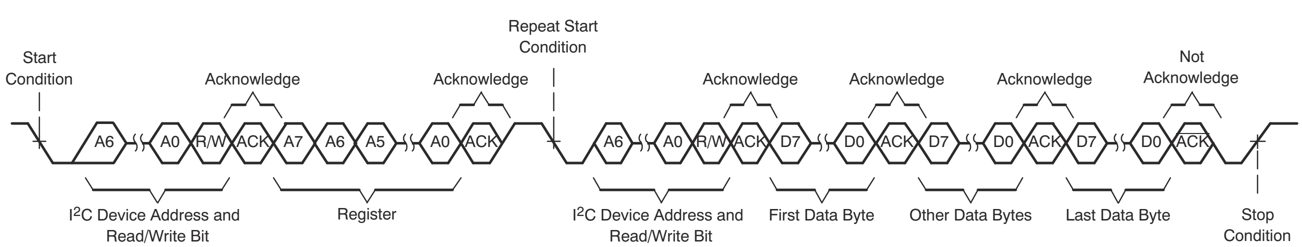


Figure 7-67. I²C Multiple-Byte Read Transfer

7.6 Register Maps

This section describes the control registers for the device in detail. All registers are eight bits in width and are allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using I^2C communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). All programmable coefficient registers are located in page 2, page 3, and page 4. The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

7.6.1 Page 0 Registers

Table 7-44 lists the memory-mapped registers for the Page 0 registers. All register offset addresses not listed in Table 7-44 should be considered as reserved locations and the register contents should not be modified.

Table 7-44. PAGE 0 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 7.6.1.1
0x1	SW_RESET	Software reset register	0x00	Section 7.6.1.2
0x2	SLEEP_CFG	Sleep mode register	0x00	Section 7.6.1.3
0x7	ASI_CFG0	ASI configuration register 0	0x30	Section 7.6.1.4
0x8	ASI_CFG1	ASI configuration register 1	0x00	Section 7.6.1.5
0x9	ASI_CFG2	ASI configuration register 2	0x00	Section 7.6.1.6
0xA	ASI_MIX_CFG	ASI input mixing configuration register	0x00	Section 7.6.1.7
0xB	ASI_CH1	Channel 1 ASI slot configuration register	0x00	Section 7.6.1.8
0xC	ASI_CH2	Channel 2 ASI slot configuration register	0x01	Section 7.6.1.9
0xD	ASI_CH3	Channel 3 ASI slot configuration register	0x02	Section 7.6.1.10
0xE	ASI_CH4	Channel 4 ASI slot configuration register	0x03	Section 7.6.1.11
0x13	MST_CFG0	ASI master mode configuration register 0	0x02	Section 7.6.1.12
0x14	MST_CFG1	ASI master mode configuration register 1	0x48	Section 7.6.1.13
0x15	ASI_STS	ASI bus clock monitor status register	0xFF	Section 7.6.1.14
0x16	CLK_SRC	Clock source configuration register 0	0x10	Section 7.6.1.15
0x1F	PDMCLK_CFG	PDM clock generation configuration register	0x40	Section 7.6.1.16
0x20	PDMIN_CFG	PDM DINx sampling edge register	0x00	Section 7.6.1.17
0x21	GPIO_CFG0	GPIO configuration register 0	0x22	Section 7.6.1.18
0x22	GPO_CFG0	GPO configuration register 0	0x00	Section 7.6.1.19
0x29	GPO_VAL	GPIO, GPO output value register	0x00	Section 7.6.1.20
0x2A	GPIO_MON	GPIO monitor value register	0x00	Section 7.6.1.21
0x2B	GPI_CFG0	GPI configuration register 0	0x00	Section 7.6.1.22
0x2F	GPI_MON	GPI monitor value register	0x00	Section 7.6.1.23
0x32	INT_CFG	Interrupt configuration register	0x00	Section 7.6.1.24
0x33	INT_MASK0	Interrupt mask register 0	0xFF	Section 7.6.1.25
0x36	INT_LTCH0	Latched interrupt readback register 0	0x00	Section 7.6.1.26
0x3B	BIAS_CFG	Bias and ADC configuration register	0x00	Section 7.6.1.27
0x3E	CH1_CFG2	Channel 1 configuration register 2	0xC9	Section 7.6.1.28
0x3F	CH1_CFG3	Channel 1 configuration register 3	0x80	Section 7.6.1.29
0x40	CH1_CFG4	Channel 1 configuration register 4	0x00	Section 7.6.1.30
0x41	CH2_CFG0	Channel 2 configuration register 0	0x00	Section 7.6.1.31
0x43	CH2_CFG2	Channel 2 configuration register 2	0xC9	Section 7.6.1.32
0x44	CH2_CFG3	Channel 2 configuration register 3	0x80	Section 7.6.1.33
0x45	CH2_CFG4	Channel 2 configuration register 4	0x00	Section 7.6.1.34
0x48	CH3_CFG2	Channel 3 configuration register 2	0xC9	Section 7.6.1.35
0x49	CH3_CFG3	Channel 3 configuration register 3	0x80	Section 7.6.1.36
0x4A	CH3_CFG4	Channel 3 configuration register 4	0x00	Section 7.6.1.37
0x4D	CH4_CFG2	Channel 4 configuration register 2	0xC9	Section 7.6.1.38
0x4E	CH4_CFG3	Channel 4 configuration register 3	0x80	Section 7.6.1.39
0x4F	CH4_CFG4	Channel 4 configuration register 4	0x00	Section 7.6.1.40
0x6B	DSP_CFG0	DSP configuration register 0	0x01	Section 7.6.1.41
0x6C	DSP_CFG1	DSP configuration register 1	0x40	Section 7.6.1.42

Table 7-44. PAGE 0 Registers (continued)

Address	Acronym	Register Name	Reset Value	Section
0x73	IN_CH_EN	Input channel enable configuration register	0xC0	Section 7.6.1.43
0x74	ASI_OUT_CH_EN	ASI output channel enable configuration register	0x00	Section 7.6.1.44
0x75	PWR_CFG	Power up configuration register	0x00	Section 7.6.1.45
0x76	DEV_STS0	Device status value register 0	0x00	Section 7.6.1.46
0x77	DEV_STS1	Device status value register 1	0x80	Section 7.6.1.47
0x7E	I2C_CKSUM	I^{2}C checksum register	0x00	Section 7.6.1.48

7.6.1.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in Figure 7-68 and described in Table 7-45.

Return to the Table 7-44.

The device memory map is divided into pages. This register sets the page.

Figure 7-68. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

Table 7-45. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

7.6.1.2 SW_RESET Register (Address = 0x1) [Reset = 0x00]

SW_RESET is shown in Figure 7-69 and described in Table 7-46.

Return to the Table 7-44.

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

Figure 7-69. SW_RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R-0000000b							R/W-0b

Table 7-46. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits; Write only reset value
0	SW_RESET	R/W	0b	Software reset. This bit is self clearing. 0d = Do not reset 1d = Reset all registers to their reset values

7.6.1.3 SLEEP_CFG Register (Address = 0x2) [Reset = 0x00]

SLEEP_CFG is shown in Figure 7-70 and described in Table 7-47.

Return to the Table 7-44.

This register configures the regulator, VREF quick charge, I²C broadcast and sleep mode.

Figure 7-70. SLEEP_CFG Register

7	6	5	4	3	2	1	0
AREG_SELECT	RESERVED		VREF_QCHG[1:0]		I2C_BRDCAST_EN	RESERVED	SLEEP_ENZ
R/W-0b	R/W-00b		R/W-00b		R/W-0b	R-0b	R/W-0b

Table 7-47. SLEEP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AREG_SELECT	R/W	0b	The analog supply selection from either the internal regulator supply or the external AREG supply. 0d = External 1.8-V AREG supply (use this setting when AVDD is 1.8 V and short AREG with AVDD) 1d = Internally generated 1.8-V AREG supply using an on-chip regulator (use this setting when AVDD is 3.3 V)
6-5	RESERVED	R/W	00b	Reserved bits; Write only reset values
4-3	VREF_QCHG[1:0]	R/W	00b	The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)
2	I2C_BRDCAST_EN	R/W	0b	I²C broadcast addressing setting. 0d = I²C broadcast mode disabled 1d = I²C broadcast mode enabled; the I²C target address is fixed at 1001 100
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	SLEEP_ENZ	R/W	0b	Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode

7.6.1.4 ASI_CFG0 Register (Address = 0x7) [Reset = 0x30]

ASI_CFG0 is shown in Figure 7-71 and described in Table 7-48.

Return to the Table 7-44.

This register is the ASI configuration register 0.

Figure 7-71. ASI_CFG0 Register

7	6	5	4	3	2	1	0
ASI_FORMAT[1:0]		ASI_WLEN[1:0]		FSYNC_POL	BCLK_POL	TX_EDGE	TX_FILL
R/W-00b		R/W-11b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-48. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_FORMAT[1:0]	R/W	00b	ASI protocol format. 0d = TDM mode 1d = I²S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use

Table 7-48. ASI_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	ASI_WLEN[1:0]	R/W	11b	ASI word or slot length. 0d = 16 bits (Recommended this setting to be used with 10-kΩ or 20-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	FSYNC_POL	R/W	0b	ASI FSYNC polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	BCLK_POL	R/W	0b	ASI BCLK polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	TX_EDGE	R/W	0b	ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
0	TX_FILL	R/W	0b	ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles

7.6.1.5 ASI_CFG1 Register (Address = 0x8) [Reset = 0x00]

ASI_CFG1 is shown in Figure 7-72 and described in Table 7-49.

Return to the Table 7-44.

This register is the ASI configuration register 1.

Figure 7-72. ASI_CFG1 Register

7	6	5	4	3	2	1	0
TX_LSB	TX_KEEPER[1:0]		TX_OFFSET[4:0]				
R/W-0b	R/W-00b		R/W-00000b				

Table 7-49. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_LSB	R/W	0b	ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
6-5	TX_KEEPER[1:0]	R/W	00b	ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles

Table 7-49. ASI_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TX_OFFSET[4:0]	R/W	00000b	ASI data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

7.6.1.6 ASI_CFG2 Register (Address = 0x9) [Reset = 0x00]

ASI_CFG2 is shown in Figure 7-73 and described in Table 7-50.

Return to the Table 7-44.

This register is the ASI configuration register 2.

Figure 7-73. ASI_CFG2 Register

7	6	5	4	3	2	1	0
ASI_DAISY	RESERVED	ASI_ERR	ASI_ERR_RCOV	RESERVED	RESERVED		
R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R-000b		

Table 7-50. ASI_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_DAISY	R/W	0b	ASI daisy chain connection. 0d = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus. This is supported only if ASI input mixing is disabled, refer register 10 for details on ASI input mixing feature.
6	RESERVED	R	0b	Reserved bit; Write only reset value
5	ASI_ERR	R/W	0b	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
4	ASI_ERR_RCOV	R/W	0b	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2-0	RESERVED	R	000b	Reserved bits; Write only reset value

7.6.1.7 ASI_MIX_CFG Register (Address = 0xA) [Reset = 0x00]

ASI_MIX_CFG is shown in Figure 7-74 and described in Table 7-51.

Return to the Table 7-44.

This register is the ASI input mixing configuration register.

Figure 7-74. ASI_MIX_CFG Register

7	6	5	4	3	2	1	0

Figure 7-74. ASI_MIX_CFG Register (continued)

ASI_MIX_SEL[1:0]		ASI_GAIN_SEL[1:0]		ASI_IN_INVERSE	RESERVED	RESERVED	RESERVED
R/W-00b		R/W-00b		R/W-0b	R-0b	R-0b	R-0b

Table 7-51. ASI_MIX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_MIX_SEL[1:0]	R/W	00b	ASI input (from GPIx or GPIO) mixing selection with channel data. 0d = No mixing 1d = Channel 1 and channel 2 output data mixed with ASI input data on channel 1 (slot 0) 2d = Channel 1 and channel 2 output data mixed with ASI input data on channel 2 (slot 1) 3d = Mixed both channel data with ASI input data independently. Mixed asi_in_ch_1 with channel 1 output data and similarly mix asi_in_ch_2 with channel 2 output data
5-4	ASI_GAIN_SEL[1:0]	R/W	00b	ASI input data gain selection before mixing to channel data. 0d = No gain 1d = Gain asi input data by -6dB 2d = Gain asi input data by -12dB 3d = Gain asi input data by -18dB
3	ASI_IN_INVERSE	R/W	0b	Invert ASI input data before mixing to channel data. 0d = No inversion done for ASI input data 1d = ASI input data inverted before mixing with channel data
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

7.6.1.8 ASI_CH1 Register (Address = 0xB) [Reset = 0x00]

ASI_CH1 is shown in Figure 7-75 and described in Table 7-52.

Return to the Table 7-44.

This register is the ASI slot configuration register for channel 1.

Figure 7-75. ASI_CH1 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_SLOT[5:0]					
R-00b		R/W-000000b					

Table 7-52. ASI_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH1_SLOT[5:0]	R/W	000000b	Channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

7.6.1.9 ASI_CH2 Register (Address = 0xC) [Reset = 0x01]

ASI_CH2 is shown in Figure 7-76 and described in Table 7-53.

Return to the Table 7-44.

This register is the ASI slot configuration register for channel 2.

Figure 7-76. ASI_CH2 Register

7	6	5	4	3	2	1	0
RESERVED		CH2_SLOT[5:0]					
R-00b		R/W-000001b					

Table 7-53. ASI_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH2_SLOT[5:0]	R/W	000001b	Channel 2 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

7.6.1.10 ASI_CH3 Register (Address = 0xD) [Reset = 0x02]

ASI_CH3 is shown in Figure 7-77 and described in Table 7-54.

Return to the Table 7-44.

This register is the ASI slot configuration register for channel 3.

Figure 7-77. ASI_CH3 Register

7	6	5	4	3	2	1	0
RESERVED		CH3_SLOT[5:0]					
R-00b		R/W-000010b					

Table 7-54. ASI_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH3_SLOT[5:0]	R/W	000010b	Channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

7.6.1.11 ASI_CH4 Register (Address = 0xE) [Reset = 0x03]

ASI_CH4 is shown in Figure 7-78 and described in Table 7-55.

Return to the Table 7-44.

This register is the ASI slot configuration register for channel 4.

Figure 7-78. ASI_CH4 Register

7	6	5	4	3	2	1	0
RESERVED		CH4_SLOT[5:0]					

Figure 7-78. ASI_CH4 Register (continued)

R-00b	R/W-000011b

Table 7-55. ASI_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH4_SLOT[5:0]	R/W	000011b	Channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

7.6.1.12 MST_CFG0 Register (Address = 0x13) [Reset = 0x02]

MST_CFG0 is shown in Figure 7-79 and described in Table 7-56.

Return to the Table 7-44.

This register is the ASI master mode configuration register 0.

Figure 7-79. MST_CFG0 Register

7	6	5	4	3	2	1	0
MST_SLV_CFG	AUTO_CLK_CFG	AUTO_MODE_PLL_DIS	BCLK_FSYNC_GATE	FS_MODE	MCLK_FREQ_SEL[2:0]		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-010b		

Table 7-56. MST_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MST_SLV_CFG	R/W	0b	ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device) 1d = Device is in master mode (both BCLK and FSYNC are generated from the device)
6	AUTO_CLK_CFG	R/W	0b	Automatic clock configuration setting. 0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived) 1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings)
5	AUTO_MODE_PLL_DIS	R/W	0b	Automatic mode PLL setting. 0d = PLL is enabled in auto clock configuration 1d = PLL is disabled in auto clock configuration
4	BCLK_FSYNC_GATE	R/W	0b	BCLK and FSYNC clock gate (valid when the device is in master mode). 0d = Do not gate BCLK and FSYNC 1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode
3	FS_MODE	R/W	0b	Sample rate setting (valid when the device is in master mode). 0d = f_S is a multiple (or submultiple) of 48 kHz 1d = f_S is a multiple (or submultiple) of 44.1 kHz

Table 7-56. MST_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MCLK_FREQ_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz

7.6.1.13 MST_CFG1 Register (Address = 0x14) [Reset = 0x48]

MST_CFG1 is shown in Figure 7-80 and described in Table 7-57.

Return to the Table 7-44.

This register is the ASI master mode configuration register 1.

Figure 7-80. MST_CFG1 Register

7	6	5	4	3	2	1	0
FS_RATE[3:0]				FS_BCLK_RATIO[3:0]			
R/W-0100b				R/W-1000b			

Table 7-57. MST_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE[3:0]	R/W	0100b	Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 15d = Reserved; Don't use
3-0	FS_BCLK_RATIO[3:0]	R/W	1000b	Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d to 15d = Reserved; Don't use

7.6.1.14 ASI_STS Register (Address = 0x15) [Reset = 0xFF]

ASI_STS is shown in Figure 7-81 and described in Table 7-58.

Return to the Table 7-44.

This register s the ASI bus clock monitor status register

Figure 7-81. ASI_STS Register

7	6	5	4	3	2	1	0
FS_RATE_STS[3:0]				FS_RATIO_STS[3:0]			
R-1111b				R-1111b			

Table 7-58. ASI_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE_STS[3:0]	R	1111b	Detected sample rate of the ASI bus. 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 14d = Reserved status 15d = Invalid sample rate
3-0	FS_RATIO_STS[3:0]	R	1111b	Detected BCLK to FSYNC frequency ratio of the ASI bus. 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d to 14d = Reserved status 15d = Invalid ratio

7.6.1.15 CLK_SRC Register (Address = 0x16) [Reset = 0x10]

CLK_SRC is shown in Figure 7-82 and described in Table 7-59.

Return to the Table 7-44.

This register is the clock source configuration register.

Figure 7-82. CLK_SRC Register

7	6	5	4	3	2	1	0
DIS_PLL_SLV_CLK_SRC	MCLK_FREQ_SEL_MODE	MCLK_RATIO_SEL[2:0]			RESERVED	INV_BCLK_FOR_FSYNC	RESERVED
R/W-0b	R/W-0b	R/W-010b			R/W-0b	R/W-0b	R/W-0b

Table 7-59. CLK_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_PLL_SLV_CLK_SRC	R/W	0b	Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1). 0d = BCLK is used as the audio root clock source 1d = MCLK (GPIO or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting)
6	MCLK_FREQ_SEL_MODE	R/W	0b	Master mode MCLK (GPIO or GPIx) frequency selection mode (valid when the device is in auto clock configuration). 0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R19) configuration 1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R22) configuration
5-3	MCLK_RATIO_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIO or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode. 0d = Ratio of 64 1d = Ratio of 256 2d = Ratio of 384 3d = Ratio of 512 4d = Ratio of 768 5d = Ratio of 1024 6d = Ratio of 1536 7d = Ratio of 2304
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	INV_BCLK_FOR_FSYNC	R/W	0b	Invert BCLK polarity only for FSYNC generation in master mode configuration. 0d = Do not invert BCLK polarity for FSYNC generation 1d = Invert BCLK polarity for FSYNC generation
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

7.6.1.16 PDMCLK_CFG Register (Address = 0x1F) [Reset = 0x40]

PDMCLK_CFG is shown in Figure 7-83 and described in Table 7-60.

Return to the Table 7-44.

This register is the PDM clock generation configuration register.

Figure 7-83. PDMCLK_CFG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED					PDMCLK_DIV[1:0]	
R/W-0b	R/W-10000b					R/W-00b	

Table 7-60. PDMCLK_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6-2	RESERVED	R/W	10000b	Reserved bits; Write only reset values
1-0	PDMCLK_DIV[1:0]	R/W	00b	PDMCLK divider value. 0d = PDMCLK is 2.8224 MHz or 3.072 MHz 1d = PDMCLK is 1.4112 MHz or 1.536 MHz 2d = PDMCLK is 705.6 kHz or 768 kHz 3d = PDMCLK is 5.6448 MHz or 6.144 MHz (applicable only for PDM channel 1 and 2)

7.6.1.17 PDMIN_CFG Register (Address = 0x20) [Reset = 0x00]

PDMIN_CFG is shown in Figure 7-84 and described in Table 7-61.

Return to the Table 7-44.

This register is the PDM DINx sampling edge configuration register.

Figure 7-84. PDMIN_CFG Register

7	6	5	4	3	2	1	0
PDMDIN1_EDGE	RESERVED	RESERVED					
R/W-0b	R/W-0b	R-000000b					

Table 7-61. PDMIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDMDIN1_EDGE	R/W	0b	PDMCLK latching edge used for channel 1 and channel 2 data. 0d = Channel 1 data are latched on the negative edge, channel 2 data are latched on the positive edge 1d = Channel 1 data are latched on the positive edge, channel 2 data are latched on the negative edge
6	RESERVED	R/W	0b	Reserved bit; Write only reset value
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

7.6.1.18 GPIO_CFG0 Register (Address = 0x21) [Reset = 0x22]

GPIO_CFG0 is shown in Figure 7-85 and described in Table 7-62.

Return to the Table 7-44.

This register is the GPIO configuration register 0.

Figure 7-85. GPIO_CFG0 Register

7	6	5	4	3	2	1	0
GPIO1_CFG[3:0]				RESERVED	GPIO1_DRV[2:0]		
R/W-0010b				R-0b	R/W-010b		

Table 7-62. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	R/W	0010b	GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = Reserved; Don't use 4d = GPIO1 is configured as a PDM clock output (PDMCLK) 5d = Reserved; Don't use 6d = Reserved; Don't use 7d = PD all ADC channels 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 12d = GPIO1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 13d = GPIO1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 14d to 15d = Reserved; Don't use
3	RESERVED	R	0b	Reserved bit; Write only reset value

Table 7-62. GPIO_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	GPIO1_DRV[2:0]	R/W	010b	GPIO1 output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

7.6.1.19 GPO_CFG0 Register (Address = 0x22) [Reset = 0x00]

GPO_CFG0 is shown in Figure 7-86 and described in Table 7-63.

Return to the Table 7-44.

This registeris the GPO configuration register 0.

Figure 7-86. GPO_CFG0 Register

7	6	5	4	3	2	1	0
GPO1_CFG[3:0]				RESERVED	GPO1_DRV[2:0]		
R/W-0000b				R-0b	R/W-000b		

Table 7-63. GPO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_CFG[3:0]	R/W	0000b	GPO1 configuration. 0d = GPO1 is disabled 1d = GPO1 is configured as a general-purpose output (GPO) 2d = GPO1 is configured as a device interrupt output (IRQ) 3d = Reserved; Don't use 4d = GPO1 is configured as a PDM clock output (PDMCLK) 5d to 15d = Reserved; Don't use
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPO1_DRV[2:0]	R/W	000b	IN2M_GPO1 (GPO1) output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Reserved; Don't use 3d = Drive active low and Hi-Z 4d = Reserved; Don't use 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

7.6.1.20 GPO_VAL Register (Address = 0x29) [Reset = 0x00]

GPO_VAL is shown in Figure 7-87 and described in Table 7-64.

Return to the Table 7-44.

This register is the GPIO and GPO output value register.

Figure 7-87. GPO_VAL Register

7	6	5	4	3	2	1	0
GPIO1_VAL	GPO1_VAL	RESERVED					
R/W-0b	R/W-0b	R-000000b					

Table 7-64. GPO_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_VAL	R/W	0b	GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
6	GPO1_VAL	R/W	0b	GPO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

7.6.1.21 GPIO_MON Register (Address = 0x2A) [Reset = 0x00]

GPIO_MON is shown in Figure 7-88 and described in Table 7-65.

Return to the Table 7-44.

This register is the GPIO monitor value register.

Figure 7-88. GPIO_MON Register

7	6	5	4	3	2	1	0
GPIO1_MON	RESERVED						
R-0b	R-0000000b						

Table 7-65. GPIO_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_MON	R	0b	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6-0	RESERVED	R	0000000b	Reserved bits; Write only reset value

7.6.1.22 GPI_CFG0 Register (Address = 0x2B) [Reset = 0x00]

GPI_CFG0 is shown in Figure 7-89 and described in Table 7-66.

Return to the Table 7-44.

This register is the GPI configuration register 0.

Figure 7-89. GPI_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED	GPI1_CFG[2:0]			RESERVED	GPI2_CFG[2:0]		
R-0b	R/W-000b			R-0b	R/W-000b		

Table 7-66. GPI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6-4	GPI1_CFG[2:0]	R/W	000b	GPI1 (GPI1) configuration. 0d = GPI1 is disabled 1d = GPI1 is configured as a general-purpose input (GPI) 2d = GPI1 is configured as a master clock input (MCLK) 3d = GPI1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 4d = GPI1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 5d = GPI1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 6d = Reserved; Don't use 7d = PD all ADC channels

Table 7-66. GPI_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPI2_CFG[2:0]	R/W	000b	MICBIAS_GPI2 as GPI2 configuration. 0d = GPI2 is disabled 1d = GPI2 is configured as a general-purpose input (GPI) 2d = GPI2 is configured as a master clock input (MCLK) 3d = GPI2 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 4d = GPI2 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 5d = GPI2 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 6d = Reserved; Don't use 7d = PD all ADC channels

7.6.1.23 GPI_MON Register (Address = 0x2F) [Reset = 0x00]

GPI_MON is shown in Figure 7-90 and described in Table 7-67.

Return to the Table 7-44.

This regiser is the GPI monitor value register.

Figure 7-90. GPI_MON Register

7	6	5	4	3	2	1	0
GPI1_MON	GPI2_MON	RESERVED					
R-0b	R-0b	R-000000b					

Table 7-67. GPI_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI1_MON	R	0b	GPI1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6	GPI2_MON	R	0b	GPI2 monitor value when MICBIAS_GPI2 is configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

7.6.1.24 INT_CFG Register (Address = 0x32) [Reset = 0x00]

INT_CFG is shown in Figure 7-91 and described in Table 7-68.

Return to the Table 7-44.

This regiser is the interrupt configuration register.

Figure 7-91. INT_CFG Register

7	6	5	4	3	2	1	0
INT_POL	INT_EVENT[1:0]		RESERVED		LTCH_READ_CFG	RESERVED	
R/W-0b	R/W-00b		R-00b		R/W-0b	R-00b	

Table 7-68. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	R/W	0b	Interrupt polarity. 0d = Active low (IRQZ) 1d = Active high (IRQ)

Table 7-68. INT_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	INT_EVENT[1:0]	R/W	00b	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event Dont use 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	RESERVED	R	00b	Reserved bits; Write only reset value
2	LTCH_READ_CFG	R/W	0b	Interrupt latch registers readback configuration. 0d = All interrupts can be read through the LTCH registers 1d = Only unmasked interrupts can be read through the LTCH registers
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

7.6.1.25 INT_MASK0 Register (Address = 0x33) [Reset = 0xFF]

INT_MASK0 is shown in Figure 7-92 and described in Table 7-69.

Return to the Table 7-44.

This register is the interrupt masks register 0.

Figure 7-92. INT_MASK0 Register

7	6	5	4	3	2	1	0
INT_MASK0	INT_MASK0	INT_MASK0	INT_MASK0	INT_MASK0	RESERVED	RESERVED	RESERVED
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 7-69. INT_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0	R/W	1b	ASI clock error mask. 0d = Do not mask 1d = Mask
6	INT_MASK0	R/W	1b	PLL Lock interrupt mask. 0d = Do not mask 1d = Mask
5	INT_MASK0	R/W	1b	ASI input mixing saturation alert mask. 0d = Do not mask 1d = Mask
4	INT_MASK0	R/W	1b	VAD Power up detect interrupt mask. 0d = Do not mask 1d = Mask
3	INT_MASK0	R/W	1b	VAD Power down detect interrupt mask. 0d = Do not mask 1d = Mask
2	RESERVED	R/W	1b	Reserved bit; Write only reset value
1	RESERVED	R/W	1b	Reserved bit; Write only reset value
0	RESERVED	R/W	1b	Reserved bit; Write only reset value

7.6.1.26 INT_LTCH0 Register (Address = 0x36) [Reset = 0x00]

INT_LTCH0 is shown in Figure 7-93 and described in Table 7-70.

Return to the Table 7-44.

This register is the latched Interrupt readback register 0.

Figure 7-93. INT_LTCH0 Register

7	6	5	4	3	2	1	0
INT_LTCH0	INT_LTCH0	INT_LTCH0	INT_LTCH0	INT_LTCH0	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-70. INT_LTCH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0	R	0b	Interrupt caused by an ASI bus clock error (self-clearing bit). 0d = No interrupt 1d = Interrupt
6	INT_LTCH0	R	0b	Interrupt caused by PLL LOCK (self-clearing bit). 0d = No interrupt 1d = Interrupt
5	INT_LTCH0	R	0b	Interrupt caused by ASI input mixing channel saturation alert (self clearing bit). 0d = No interrupt 1d = Interrupt
4	INT_LTCH0	R	0b	Interrupt caused by VAD power up detect (self clearing bit). 0d = No interrupt 1d = Interrupt
3	INT_LTCH0	R	0b	Interrupt caused by VAD power down detect (self clearing bit). 0d = No interrupt 1d = Interrupt
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

7.6.1.27 BIAS_CFG Register (Address = 0x3B) [Reset = 0x00]

BIAS_CFG is shown in Figure 7-94 and described in Table 7-71.

Return to the Table 7-44.

This register is the bias and ADC configuration register

Figure 7-94. BIAS_CFG Register

7	6	5	4	3	2	1	0
RESERVED	MBIAS_VAL[2:0]			RESERVED		RESERVED	
R-0b	R/W-000b			R-00b		R/W-00b	

Table 7-71. BIAS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6-4	MBIAS_VAL[2:0]	R/W	000b	MICBIAS value. 0d = Microphone bias is set to VREF (2.750 V, 2.500 V, or 1.375 V) 1d = Microphone bias is set to VREF x 1.096 (3.014 V, 2.740 V, or 1.507 V) Dont use Dont use Dont use Dont use 6d = Microphone bias is set to AVDD 7d = MICBIAS configured as GPI2
3-2	RESERVED	R	00b	Reserved bits; Write only reset value
1-0	RESERVED	R/W	00b	Reserved bits; Write only reset values

7.6.1.28 CH1_CFG2 Register (Address = 0x3E) [Reset = 0xC9]

CH1_CFG2 is shown in Figure 7-95 and described in Table 7-72.

Return to the Table 7-44.

This register is configuration register 2 for channel 1.

Figure 7-95. CH1_CFG2 Register

7	6	5	4	3	2	1	0
CH1_DVOL[7:0]							
R/W-11001001b							

Table 7-72. CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_DVOL[7:0]	R/W	11001001b	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

7.6.1.29 CH1_CFG3 Register (Address = 0x3F) [Reset = 0x80]

CH1_CFG3 is shown in Figure 7-96 and described in Table 7-73.

Return to the Table 7-44.

This register is configuration register 3 for channel 1.

Figure 7-96. CH1_CFG3 Register

7	6	5	4	3	2	1	0
CH1_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 7-73. CH1_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH1_GCAL[3:0]	R/W	1000b	Channel 1 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.30 CH1_CFG4 Register (Address = 0x40) [Reset = 0x00]

CH1_CFG4 is shown in Figure 7-97 and described in Table 7-74.

Return to the Table 7-44.

This register is configuration register 4 for channel 1.

Figure 7-97. CH1_CFG4 Register

7	6	5	4	3	2	1	0
CH1_PCAL[7:0]							
R/W-00000000b							

Table 7-74. CH1_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PCAL[7:0]	R/W	00000000b	Channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

7.6.1.31 CH2_CFG0 Register (Address = 0x41) [Reset = 0x00]

CH2_CFG0 is shown in Figure 7-98 and described in Table 7-75.

Return to the Table 7-44.

This register is configuration register 0 for channel 2.

Figure 7-98. CH2_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED	CH2_INSRC[1:0]		RESERVED	RESERVED		RESERVED	RESERVED
R/W-0b	R/W-00b		R/W-0b	R/W-00b		R-0b	R/W-0b

Table 7-75. CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6-5	CH2_INSRC[1:0]	R/W	00b	Channel 2 input configuration. 0d = Input Source is not enabled Dont use 2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK) Dont use
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3-2	RESERVED	R/W	00b	Reserved bits; Write only reset values
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

7.6.1.32 CH2_CFG2 Register (Address = 0x43) [Reset = 0xC9]

CH2_CFG2 is shown in Figure 7-99 and described in Table 7-76.

Return to the Table 7-44.

This register is configuration register 2 for channel 2.

Figure 7-99. CH2_CFG2 Register

7	6	5	4	3	2	1	0
CH2_DVOL[7:0]							
R/W-11001001b							

Figure 7-99. CH2_CFG2 Register (continued)

Table 7-76. CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_DVOL[7:0]	R/W	11001001b	Channel 2 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

7.6.1.33 CH2_CFG3 Register (Address = 0x44) [Reset = 0x80]

CH2_CFG3 is shown in Figure 7-100 and described in Table 7-77.

Return to the Table 7-44.

This register is configuration register 3 for channel 2.

Figure 7-100. CH2_CFG3 Register

7	6	5	4	3	2	1	0
CH2_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 7-77. CH2_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH2_GCAL[3:0]	R/W	1000b	Channel 2 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.34 CH2_CFG4 Register (Address = 0x45) [Reset = 0x00]

CH2_CFG4 is shown in Figure 7-101 and described in Table 7-78.

Return to the Table 7-44.

This register is configuration register 4 for channel 2.

Figure 7-101. CH2_CFG4 Register

7	6	5	4	3	2	1	0
CH2_PCAL[7:0]							
R/W-00000000b							

Table 7-78. CH2_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PCAL[7:0]	R/W	00000000b	Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

7.6.1.35 CH3_CFG2 Register (Address = 0x48) [Reset = 0xC9]

CH3_CFG2 is shown in Figure 7-102 and described in Table 7-79.

Return to the Table 7-44.

This register is configuration register 2 for channel 3.

Figure 7-102. CH3_CFG2 Register

7	6	5	4	3	2	1	0
CH3_DVOL[7:0]							
R/W-11001001b							

Table 7-79. CH3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_DVOL[7:0]	R/W	11001001b	Channel 3 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

7.6.1.36 CH3_CFG3 Register (Address = 0x49) [Reset = 0x80]

CH3_CFG3 is shown in Figure 7-103 and described in Table 7-80.

Return to the Table 7-44.

This register is configuration register 3 for channel 3.

Figure 7-103. CH3_CFG3 Register

7	6	5	4	3	2	1	0
CH3_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 7-80. CH3_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH3_GCAL[3:0]	R/W	1000b	Channel 3 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.37 CH3_CFG4 Register (Address = 0x4A) [Reset = 0x00]

CH3_CFG4 is shown in Figure 7-104 and described in Table 7-81.

Return to the Table 7-44.

This register is configuration register 4 for channel 3.

Figure 7-104. CH3_CFG4 Register

7	6	5	4	3	2	1	0
CH3_PCAL[7:0]							
R/W-00000000b							

Table 7-81. CH3_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_PCAL[7:0]	R/W	00000000b	Channel 3 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

7.6.1.38 CH4_CFG2 Register (Address = 0x4D) [Reset = 0xC9]

CH4_CFG2 is shown in Figure 7-105 and described in Table 7-82.

Return to the Table 7-44.

This register is configuration register 2 for channel 4.

Figure 7-105. CH4_CFG2 Register

7	6	5	4	3	2	1	0
CH4_DVOL[7:0]							
R/W-11001001b							

Table 7-82. CH4_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_DVOL[7:0]	R/W	11001001b	Channel 4 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

7.6.1.39 CH4_CFG3 Register (Address = 0x4E) [Reset = 0x80]

CH4_CFG3 is shown in Figure 7-106 and described in Table 7-83.

Return to the Table 7-44.

This register is configuration register 3 for channel 4.

Figure 7-106. CH4_CFG3 Register

7	6	5	4	3	2	1	0
CH4_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 7-83. CH4_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH4_GCAL[3:0]	R/W	1000b	Channel 4 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.40 CH4_CFG4 Register (Address = 0x4F) [Reset = 0x00]

CH4_CFG4 is shown in Figure 7-107 and described in Table 7-84.

Return to the Table 7-44.

This register is configuration register 4 for channel 4.

Figure 7-107. CH4_CFG4 Register

7	6	5	4	3	2	1	0
CH4_PCAL[7:0]							
R/W-00000000b							

Table 7-84. CH4_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_PCAL[7:0]	R/W	00000000b	Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

7.6.1.41 DSP_CFG0 Register (Address = 0x6B) [Reset = 0x01]

DSP_CFG0 is shown in Figure 7-108 and described in Table 7-85.

Return to the Table 7-44.

This register is the digital signal processor (DSP) configuration register 0.

Figure 7-108. DSP_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DECI_FILT[1:0]		CH_SUM[1:0]		HPF_SEL[1:0]	
R/W-0b	R/W-0b	R/W-00b		R/W-00b		R/W-01b	

Table 7-85. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6	RESERVED	R/W	0b	Reserved bit; Write only reset value
5-4	DECI_FILT[1:0]	R/W	00b	Decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use
3-2	CH_SUM[1:0]	R/W	00b	Channel summation mode for higher SNR 0d = Channel summation mode is disabled 1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 output 2d = Reserved; Don't use 3d = Reserved; Don't use
1-0	HPF_SEL[1:0]	R/W	01b	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 x f_S (384 Hz at f_S = 48 kHz) is selected

7.6.1.42 DSP_CFG1 Register (Address = 0x6C) [Reset = 0x40]

DSP_CFG1 is shown in Figure 7-109 and described in Table 7-86.

Return to the Table 7-44.

This register is the digital signal processor (DSP) configuration register 1.

Figure 7-109. DSP_CFG1 Register

7	6	5	4	3	2	1	0

Figure 7-109. DSP_CFG1 Register (continued)

DVOL_GANG	BIQUAD_CFG[1:0]	DISABLE_SOFT_STEP	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-10b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-86. DSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DVOL_GANG	R/W	0b	DVOL control ganged across channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not
6-5	BIQUAD_CFG[1:0]	R/W	10b	Number of biquads per channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
4	DISABLE_SOFT_STEP	R/W	0b	Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

7.6.1.43 IN_CH_EN Register (Address = 0x73) [Reset = 0xC0]

IN_CH_EN is shown in Figure 7-110 and described in Table 7-87.

Return to the Table 7-44.

This register is the input channel enable configuration register.

Figure 7-110. IN_CH_EN Register

7	6	5	4	3	2	1	0
IN_CH1_EN	IN_CH2_EN	IN_CH3_EN	IN_CH4_EN	RESERVED			
R/W-1b	R/W-1b	R/W-0b	R/W-0b	R-0000b			

Table 7-87. IN_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_EN	R/W	1b	Input channel 1 enable setting. 0d = Channel 1 is disabled 1d = Channel 1 is enabled
6	IN_CH2_EN	R/W	1b	Input channel 2 enable setting. 0d = Channel 2 is disabled 1d = Channel 2 is enabled
5	IN_CH3_EN	R/W	0b	Input channel 3 (PDM only) enable setting. 0d = Channel 3 is disabled 1d = Channel 3 is enabled
4	IN_CH4_EN	R/W	0b	Input channel 4 (PDM only) enable setting. 0d = Channel 4 is disabled 1d = Channel 4 is enabled
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.44 ASI_OUT_CH_EN Register (Address = 0x74) [Reset = 0x00]

ASI_OUT_CH_EN is shown in Figure 7-111 and described in Table 7-88.

Return to the Table 7-44.

This register is the ASI output channel enable configuration register.

Figure 7-111. ASI_OUT_CH_EN Register

7	6	5	4	3	2	1	0
ASI_OUT_CH1_EN	ASI_OUT_CH2_EN	ASI_OUT_CH3_EN	ASI_OUT_CH4_EN	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

Table 7-88. ASI_OUT_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_OUT_CH1_EN	R/W	0b	ASI output channel 1 enable setting. 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled
6	ASI_OUT_CH2_EN	R/W	0b	ASI output channel 2 enable setting. 0d = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled
5	ASI_OUT_CH3_EN	R/W	0b	ASI output channel 3 enable setting. 0d = Channel 3 output slot is in a tri-state condition 1d = Channel 3 output slot is enabled
4	ASI_OUT_CH4_EN	R/W	0b	ASI output channel 4 enable setting. 0d = Channel 4 output slot is in a tri-state condition 1d = Channel 4 output slot is enabled
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

7.6.1.45 PWR_CFG Register (Address = 0x75) [Reset = 0x00]

PWR_CFG is shown in Figure 7-112 and described in Table 7-89.

Return to the Table 7-44.

This register is the power-up configuration register.

Figure 7-112. PWR_CFG Register

7	6	5	4	3	2	1	0
MICBIAS_PDZ	ADC_PDZ	PLL_PDZ	DYN_CH_PUPD_EN	DYN_MAXCH_SEL[1:0]		RESERVED	VAD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b

Table 7-89. PWR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_PDZ	R/W	0b	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS
6	ADC_PDZ	R/W	0b	Power control for PDM channels. 0d = Power down all PDM channels 1d = Power up all enabled PDM channels
5	PLL_PDZ	R/W	0b	Power control for the PLL. 0d = Power down the PLL 1d = Power up the PLL

Table 7-89. PWR_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DYN_CH_PUPD_EN	R/W	0b	Dynamic channel power-up, power-down enable. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on
3-2	DYN_MAXCH_SEL[1:0]	R/W	00b	Dynamic mode maximum channel select configuration. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled 2d = Reserved; Don't use 3d = Reserved; Don't use
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	VAD_EN	R/W	0b	Enable voice activity detection (VAD) algorithm. 0d = VAD is disabled 1d = VAD is enabled

7.6.1.46 DEV_STS0 Register (Address = 0x76) [Reset = 0x00]

DEV_STS0 is shown in Figure 7-113 and described in Table 7-90.

Return to the Table 7-44.

This register is the device status value register 0.

Figure 7-113. DEV_STS0 Register

7	6	5	4	3	2	1	0
CH1_STATUS	CH2_STATUS	RESERVED					
R-0b	R-0b	R-000000b					

Table 7-90. DEV_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_STATUS	R	0b	PDM channel 1 power status. 0d = PDM channel is powered down 1d = PDM channel is powered up
6	CH2_STATUS	R	0b	PDM channel 2 power status. 0d = PDM channel is powered down 1d = PDM channel is powered up
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

7.6.1.47 DEV_STS1 Register (Address = 0x77) [Reset = 0x80]

DEV_STS1 is shown in Figure 7-114 and described in Table 7-91.

Return to the Table 7-44.

This register is the device status value register 1.

Figure 7-114. DEV_STS1 Register

7	6	5	4	3	2	1	0
MODE_STS[2:0]			RESERVED				
R-100b			R-00000b				

Table 7-91. DEV_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MODE_STS[2:0]	R	100b	Device mode status. 4d = Device is in sleep mode or software shutdown mode 6d = Device is in active mode with all PDM channels turned off 7d = Device is in active mode with at least one PDM channel turned on
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

7.6.1.48 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C_CKSUM is shown in Figure 7-115 and described in Table 7-92.

Return to the Table 7-44.

This register returns the I^2C transactions checksum value.

Figure 7-115. I2C_CKSUM Register

7	6	5	4	3	2	1	0
I2C_CKSUM[7:0]							
R/W-00000000b							

Table 7-92. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	00000000b	These bits return the I^2C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages.

7.6.2 Page 1 Registers

Table 7-93 lists the memory-mapped registers for the Page 1 registers. All register offset addresses not listed in Table 7-93 should be considered as reserved locations and the register contents should not be modified.

Table 7-93. PAGE 1 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 7.6.2.1
0x1E	VAD_CFG1	Voice activity detection configuration register 1	0x20	Section 7.6.2.2
0x1F	VAD_CFG2	Voice activity detection configuration register 2	0x08	Section 7.6.2.3

7.6.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x0]

PAGE_CFG is shown in Figure 7-116 and described in Table 7-94.

Return to the Table 7-93.

The device memory map is divided into pages. This register sets the page.

Figure 7-116. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

Table 7-94. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

7.6.2.2 VAD_CFG1 Register (Address = 0x1E) [Reset = 0x20]

VAD_CFG1 is shown in Figure 7-117 and described in Table 7-95.

Return to the Table 7-93.

This register is configuration register 1 for voice activity detection.

Figure 7-117. VAD_CFG1 Register

7	6	5	4	3	2	1	0
VAD_MODE[1:0]		VAD_CH_SEL[1:0]		VAD_CLK_CFG[1:0]		VAD_EXT_CLK_CFG[1:0]	
R/W-00b		R/W-10b		R/W-00b		R/W-00b	

Table 7-95. VAD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VAD_MODE[1:0]	R/W	00b	Auto ADC power up / power down configuration selection. 0d = User initiated ADC power-up and ADC power-down 1d = VAD interrupt based ADC power up and ADC power down 2d = VAD interrupt based ADC power up but user initiated ADC power down 3d = User initiated ADC power-up but VAD interrupt based ADC power down

Table 7-95. VAD_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VAD_CH_SEL[1:0]	R/W	10b	VAD channel select. 0d = Channel 1 is monitored for VAD activity 1d = Channel 2 is monitored for VAD activity 2d = Channel 3 is monitored for VAD activity 3d = Channel 4 is monitored for VAD activity
3-2	VAD_CLK_CFG[1:0]	R/W	00b	Clock select for VAD 0d = VAD processing using internal oscillator clock 1d = VAD processing using external clock on BCLK input 2d = VAD processing using external clock on MCLK input 3d = Custom clock configuration based on MST_CFG, CLK_SRC and CLKGEN_CFG registers in page 0
1-0	VAD_EXT_CLK_CFG[1:0]	R/W	00b	Clock configuration using external clock for VAD. 0d = External clock is 3.072 MHz 1d = External clock is 6.144 MHz 2d = External clock is 12.288 MHz 3d = External clock is 18.432 MHz

7.6.2.3 VAD_CFG2 Register (Address = 0x1F) [Reset = 0x8]

VAD_CFG2 is shown in Figure 7-118 and described in Table 7-96.

Return to the Table 7-93.

This register is configuration register 2 for voice activity detection.

Figure 7-118. VAD_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED	SDOUT_INT_CFG	RESERVED	RESERVED	VAD_PD_DET_EN	RESERVED		
R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-1b	R-000b		

Table 7-96. VAD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6	SDOUT_INT_CFG	R/W	0b	SDOUT interrupt configuration. 0d = SDOUT pin is not enabled for interrupt function 1d = SDOUT pin is enabled to support interrupt output when channel data in not being recorded
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	VAD_PD_DET_EN	R/W	1b	Enable ASI output data during VAD activity. 0d = VAD processing is not enabled during ADC recording 1d = VAD processing is enabled during ADC recording and VAD interrupts are generated as configured
2-0	RESERVED	R	000b	Reserved bits; Write only reset values

7.6.3 Programmable Coefficient Registers

7.6.3.1 Programmable Coefficient Registers: Page 2

This register page (shown in Table 7-97) consists of the programmable coefficients for the biquad 1 to biquad 6 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

Table 7-97. Page 2 Programmable Coefficient Registers

Address	Acronym	Register Name	Reset Value
0x00	PAGE[7:0]	Device page register	0x00
0x08	BQ1_N0_BYT1[7:0]	Programmable biquad 1, N0 coefficient byte[31:24]	0x7F
0x09	BQ1_N0_BYT2[7:0]	Programmable biquad 1, N0 coefficient byte[23:16]	0xFF
0x0A	BQ1_N0_BYT3[7:0]	Programmable biquad 1, N0 coefficient byte[15:8]	0xFF
0x0B	BQ1_N0_BYT4[7:0]	Programmable biquad 1, N0 coefficient byte[7:0]	0xFF
0x0C	BQ1_N1_BYT1[7:0]	Programmable biquad 1, N1 coefficient byte[31:24]	0x00
0x0D	BQ1_N1_BYT2[7:0]	Programmable biquad 1, N1 coefficient byte[23:16]	0x00
0x0E	BQ1_N1_BYT3[7:0]	Programmable biquad 1, N1 coefficient byte[15:8]	0x00
0x0F	BQ1_N1_BYT4[7:0]	Programmable biquad 1, N1 coefficient byte[7:0]	0x00
0x10	BQ1_N2_BYT1[7:0]	Programmable biquad 1, N2 coefficient byte[31:24]	0x00
0x11	BQ1_N2_BYT2[7:0]	Programmable biquad 1, N2 coefficient byte[23:16]	0x00
0x12	BQ1_N2_BYT3[7:0]	Programmable biquad 1, N2 coefficient byte[15:8]	0x00
0x13	BQ1_N2_BYT4[7:0]	Programmable biquad 1, N2 coefficient byte[7:0]	0x00
0x14	BQ1_D1_BYT1[7:0]	Programmable biquad 1, D1 coefficient byte[31:24]	0x00
0x15	BQ1_D1_BYT2[7:0]	Programmable biquad 1, D1 coefficient byte[23:16]	0x00
0x16	BQ1_D1_BYT3[7:0]	Programmable biquad 1, D1 coefficient byte[15:8]	0x00
0x17	BQ1_D1_BYT4[7:0]	Programmable biquad 1, D1 coefficient byte[7:0]	0x00
0x18	BQ1_D2_BYT1[7:0]	Programmable biquad 1, D2 coefficient byte[31:24]	0x00
0x19	BQ1_D2_BYT2[7:0]	Programmable biquad 1, D2 coefficient byte[23:16]	0x00
0x1A	BQ1_D2_BYT3[7:0]	Programmable biquad 1, D2 coefficient byte[15:8]	0x00
0x1B	BQ1_D2_BYT4[7:0]	Programmable biquad 1, D2 coefficient byte[7:0]	0x00
0x1C	BQ2_N0_BYT1[7:0]	Programmable biquad 2, N0 coefficient byte[31:24]	0x7F
0x1D	BQ2_N0_BYT2[7:0]	Programmable biquad 2, N0 coefficient byte[23:16]	0xFF
0x1E	BQ2_N0_BYT3[7:0]	Programmable biquad 2, N0 coefficient byte[15:8]	0xFF
0x1F	BQ2_N0_BYT4[7:0]	Programmable biquad 2, N0 coefficient byte[7:0]	0xFF
0x20	BQ2_N1_BYT1[7:0]	Programmable biquad 2, N1 coefficient byte[31:24]	0x00
0x21	BQ2_N1_BYT2[7:0]	Programmable biquad 2, N1 coefficient byte[23:16]	0x00
0x22	BQ2_N1_BYT3[7:0]	Programmable biquad 2, N1 coefficient byte[15:8]	0x00
0x23	BQ2_N1_BYT4[7:0]	Programmable biquad 2, N1 coefficient byte[7:0]	0x00
0x24	BQ2_N2_BYT1[7:0]	Programmable biquad 2, N2 coefficient byte[31:24]	0x00
0x25	BQ2_N2_BYT2[7:0]	Programmable biquad 2, N2 coefficient byte[23:16]	0x00
0x26	BQ2_N2_BYT3[7:0]	Programmable biquad 2, N2 coefficient byte[15:8]	0x00
0x27	BQ2_N2_BYT4[7:0]	Programmable biquad 2, N2 coefficient byte[7:0]	0x00
0x28	BQ2_D1_BYT1[7:0]	Programmable biquad 2, D1 coefficient byte[31:24]	0x00
0x29	BQ2_D1_BYT2[7:0]	Programmable biquad 2, D1 coefficient byte[23:16]	0x00
0x2A	BQ2_D1_BYT3[7:0]	Programmable biquad 2, D1 coefficient byte[15:8]	0x00
0x2B	BQ2_D1_BYT4[7:0]	Programmable biquad 2, D1 coefficient byte[7:0]	0x00
0x2C	BQ2_D2_BYT1[7:0]	Programmable biquad 2, D2 coefficient byte[31:24]	0x00
0x2D	BQ2_D2_BYT2[7:0]	Programmable biquad 2, D2 coefficient byte[23:16]	0x00
0x2E	BQ2_D2_BYT3[7:0]	Programmable biquad 2, D2 coefficient byte[15:8]	0x00
0x2F	BQ2_D2_BYT4[7:0]	Programmable biquad 2, D2 coefficient byte[7:0]	0x00
0x30	BQ3_N0_BYT1[7:0]	Programmable biquad 3, N0 coefficient byte[31:24]	0x7F
0x31	BQ3_N0_BYT2[7:0]	Programmable biquad 3, N0 coefficient byte[23:16]	0xFF

Table 7-97. Page 2 Programmable Coefficient Registers (continued)

Address	Acronym	Register Name	Reset Value
0x32	BQ3_N0_BYT3[7:0]	Programmable biquad 3, N0 coefficient byte[15:8]	0xFF
0x33	BQ3_N0_BYT4[7:0]	Programmable biquad 3, N0 coefficient byte[7:0]	0xFF
0x34	BQ3_N1_BYT1[7:0]	Programmable biquad 3, N1 coefficient byte[31:24]	0x00
0x35	BQ3_N1_BYT2[7:0]	Programmable biquad 3, N1 coefficient byte[23:16]	0x00
0x36	BQ3_N1_BYT3[7:0]	Programmable biquad 3, N1 coefficient byte[15:8]	0x00
0x37	BQ3_N1_BYT4[7:0]	Programmable biquad 3, N1 coefficient byte[7:0]	0x00
0x38	BQ3_N2_BYT1[7:0]	Programmable biquad 3, N2 coefficient byte[31:24]	0x00
0x39	BQ3_N2_BYT2[7:0]	Programmable biquad 3, N2 coefficient byte[23:16]	0x00
0x3A	BQ3_N2_BYT3[7:0]	Programmable biquad 3, N2 coefficient byte[15:8]	0x00
0x3B	BQ3_N2_BYT4[7:0]	Programmable biquad 3, N2 coefficient byte[7:0]	0x00
0x3C	BQ3_D1_BYT1[7:0]	Programmable biquad 3, D1 coefficient byte[31:24]	0x00
0x3D	BQ3_D1_BYT2[7:0]	Programmable biquad 3, D1 coefficient byte[23:16]	0x00
0x3E	BQ3_D1_BYT3[7:0]	Programmable biquad 3, D1 coefficient byte[15:8]	0x00
0x3F	BQ3_D1_BYT4[7:0]	Programmable biquad 3, D1 coefficient byte[7:0]	0x00
0x40	BQ3_D2_BYT1[7:0]	Programmable biquad 3, D2 coefficient byte[31:24]	0x00
0x41	BQ3_D2_BYT2[7:0]	Programmable biquad 3, D2 coefficient byte[23:16]	0x00
0x42	BQ3_D2_BYT3[7:0]	Programmable biquad 3, D2 coefficient byte[15:8]	0x00
0x43	BQ3_D2_BYT4[7:0]	Programmable biquad 3, D2 coefficient byte[7:0]	0x00
0x44	BQ4_N0_BYT1[7:0]	Programmable biquad 4, N0 coefficient byte[31:24]	0x7F
0x45	BQ4_N0_BYT2[7:0]	Programmable biquad 4, N0 coefficient byte[23:16]	0xFF
0x46	BQ4_N0_BYT3[7:0]	Programmable biquad 4, N0 coefficient byte[15:8]	0xFF
0x47	BQ4_N0_BYT4[7:0]	Programmable biquad 4, N0 coefficient byte[7:0]	0xFF
0x48	BQ4_N1_BYT1[7:0]	Programmable biquad 4, N1 coefficient byte[31:24]	0x00
0x49	BQ4_N1_BYT2[7:0]	Programmable biquad 4, N1 coefficient byte[23:16]	0x00
0x4A	BQ4_N1_BYT3[7:0]	Programmable biquad 4, N1 coefficient byte[15:8]	0x00
0x4B	BQ4_N1_BYT4[7:0]	Programmable biquad 4, N1 coefficient byte[7:0]	0x00
0x4C	BQ4_N2_BYT1[7:0]	Programmable biquad 4, N2 coefficient byte[31:24]	0x00
0x4D	BQ4_N2_BYT2[7:0]	Programmable biquad 4, N2 coefficient byte[23:16]	0x00
0x4E	BQ4_N2_BYT3[7:0]	Programmable biquad 4, N2 coefficient byte[15:8]	0x00
0x4F	BQ4_N2_BYT4[7:0]	Programmable biquad 4, N2 coefficient byte[7:0]	0x00
0x50	BQ4_D1_BYT1[7:0]	Programmable biquad 4, D1 coefficient byte[31:24]	0x00
0x51	BQ4_D1_BYT2[7:0]	Programmable biquad 4, D1 coefficient byte[23:16]	0x00
0x52	BQ4_D1_BYT3[7:0]	Programmable biquad 4, D1 coefficient byte[15:8]	0x00
0x53	BQ4_D1_BYT4[7:0]	Programmable biquad 4, D1 coefficient byte[7:0]	0x00
0x54	BQ4_D2_BYT1[7:0]	Programmable biquad 4, D2 coefficient byte[31:24]	0x00
0x55	BQ4_D2_BYT2[7:0]	Programmable biquad 4, D2 coefficient byte[23:16]	0x00
0x56	BQ4_D2_BYT3[7:0]	Programmable biquad 4, D2 coefficient byte[15:8]	0x00
0x57	BQ4_D2_BYT4[7:0]	Programmable biquad 4, D2 coefficient byte[7:0]	0x00
0x58	BQ5_N0_BYT1[7:0]	Programmable biquad 5, N0 coefficient byte[31:24]	0x7F
0x59	BQ5_N0_BYT2[7:0]	Programmable biquad 5, N0 coefficient byte[23:16]	0xFF
0x5A	BQ5_N0_BYT3[7:0]	Programmable biquad 5, N0 coefficient byte[15:8]	0xFF
0x5B	BQ5_N0_BYT4[7:0]	Programmable biquad 5, N0 coefficient byte[7:0]	0xFF
0x5C	BQ5_N1_BYT1[7:0]	Programmable biquad 5, N1 coefficient byte[31:24]	0x00
0x5D	BQ5_N1_BYT2[7:0]	Programmable biquad 5, N1 coefficient byte[23:16]	0x00
0x5E	BQ5_N1_BYT3[7:0]	Programmable biquad 5, N1 coefficient byte[15:8]	0x00
0x5F	BQ5_N1_BYT4[7:0]	Programmable biquad 5, N1 coefficient byte[7:0]	0x00
0x60	BQ5_N2_BYT1[7:0]	Programmable biquad 5, N2 coefficient byte[31:24]	0x00
0x61	BQ5_N2_BYT2[7:0]	Programmable biquad 5, N2 coefficient byte[23:16]	0x00
0x62	BQ5_N2_BYT3[7:0]	Programmable biquad 5, N2 coefficient byte[15:8]	0x00
0x63	BQ5_N2_BYT4[7:0]	Programmable biquad 5, N2 coefficient byte[7:0]	0x00

Table 7-97. Page 2 Programmable Coefficient Registers (continued)

Address	Acronym	Register Name	Reset Value
0x64	BQ5_D1_BYT1[7:0]	Programmable biquad 5, D1 coefficient byte[31:24]	0x00
0x65	BQ5_D1_BYT2[7:0]	Programmable biquad 5, D1 coefficient byte[23:16]	0x00
0x66	BQ5_D1_BYT3[7:0]	Programmable biquad 5, D1 coefficient byte[15:8]	0x00
0x67	BQ5_D1_BYT4[7:0]	Programmable biquad 5, D1 coefficient byte[7:0]	0x00
0x68	BQ5_D2_BYT1[7:0]	Programmable biquad 5, D2 coefficient byte[31:24]	0x00
0x69	BQ5_D2_BYT2[7:0]	Programmable biquad 5, D2 coefficient byte[23:16]	0x00
0x6A	BQ5_D2_BYT3[7:0]	Programmable biquad 5, D2 coefficient byte[15:8]	0x00
0x6B	BQ5_D2_BYT4[7:0]	Programmable biquad 5, D2 coefficient byte[7:0]	0x00
0x6C	BQ6_N0_BYT1[7:0]	Programmable biquad 6, N0 coefficient byte[31:24]	0x7F
0x6D	BQ6_N0_BYT2[7:0]	Programmable biquad 6, N0 coefficient byte[23:16]	0xFF
0x6E	BQ6_N0_BYT3[7:0]	Programmable biquad 6, N0 coefficient byte[15:8]	0xFF
0x6F	BQ6_N0_BYT4[7:0]	Programmable biquad 6, N0 coefficient byte[7:0]	0xFF
0x70	BQ6_N1_BYT1[7:0]	Programmable biquad 6, N1 coefficient byte[31:24]	0x00
0x71	BQ6_N1_BYT2[7:0]	Programmable biquad 6, N1 coefficient byte[23:16]	0x00
0x72	BQ6_N1_BYT3[7:0]	Programmable biquad 6, N1 coefficient byte[15:8]	0x00
0x73	BQ6_N1_BYT4[7:0]	Programmable biquad 6, N1 coefficient byte[7:0]	0x00
0x74	BQ6_N2_BYT1[7:0]	Programmable biquad 6, N2 coefficient byte[31:24]	0x00
0x75	BQ6_N2_BYT2[7:0]	Programmable biquad 6, N2 coefficient byte[23:16]	0x00
0x76	BQ6_N2_BYT3[7:0]	Programmable biquad 6, N2 coefficient byte[15:8]	0x00
0x77	BQ6_N2_BYT4[7:0]	Programmable biquad 6, N2 coefficient byte[7:0]	0x00
0x78	BQ6_D1_BYT1[7:0]	Programmable biquad 6, D1 coefficient byte[31:24]	0x00
0x79	BQ6_D1_BYT2[7:0]	Programmable biquad 6, D1 coefficient byte[23:16]	0x00
0x7A	BQ6_D1_BYT3[7:0]	Programmable biquad 6, D1 coefficient byte[15:8]	0x00
0x7B	BQ6_D1_BYT4[7:0]	Programmable biquad 6, D1 coefficient byte[7:0]	0x00
0x7C	BQ6_D2_BYT1[7:0]	Programmable biquad 6, D2 coefficient byte[31:24]	0x00
0x7D	BQ6_D2_BYT2[7:0]	Programmable biquad 6, D2 coefficient byte[23:16]	0x00
0x7E	BQ6_D2_BYT3[7:0]	Programmable biquad 6, D2 coefficient byte[15:8]	0x00
0x7F	BQ6_D2_BYT4[7:0]	Programmable biquad 6, D2 coefficient byte[7:0]	0x00

7.6.3.2 Programmable Coefficient Registers: Page 3

This register page (shown in Table 7-98) consists of the programmable coefficients for the biquad 7 to biquad 12 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I²C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

Table 7-98. Page 3 Programmable Coefficient Registers

ADDR	REGISTER	RESET	DESCRIPTION
0x00	PAGE[7:0]	0x00	Device page register
0x08	BQ7_N0_BYT1[7:0]	0x7F	Programmable biquad 7, N0 coefficient byte[31:24]
0x09	BQ7_N0_BYT2[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[23:16]
0x0A	BQ7_N0_BYT3[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[15:8]
0x0B	BQ7_N0_BYT4[7:0]	0xFF	Programmable biquad 7, N0 coefficient byte[7:0]
0x0C	BQ7_N1_BYT1[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[31:24]
0x0D	BQ7_N1_BYT2[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[23:16]
0x0E	BQ7_N1_BYT3[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[15:8]
0x0F	BQ7_N1_BYT4[7:0]	0x00	Programmable biquad 7, N1 coefficient byte[7:0]
0x10	BQ7_N2_BYT1[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[31:24]
0x11	BQ7_N2_BYT2[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[23:16]
0x12	BQ7_N2_BYT3[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[15:8]
0x13	BQ7_N2_BYT4[7:0]	0x00	Programmable biquad 7, N2 coefficient byte[7:0]
0x14	BQ7_D1_BYT1[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[31:24]
0x15	BQ7_D1_BYT2[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[23:16]
0x16	BQ7_D1_BYT3[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[15:8]
0x17	BQ7_D1_BYT4[7:0]	0x00	Programmable biquad 7, D1 coefficient byte[7:0]
0x18	BQ7_D2_BYT1[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[31:24]
0x19	BQ7_D2_BYT2[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[23:16]
0x1A	BQ7_D2_BYT3[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[15:8]
0x1B	BQ7_D2_BYT4[7:0]	0x00	Programmable biquad 7, D2 coefficient byte[7:0]
0x1C	BQ8_N0_BYT1[7:0]	0x7F	Programmable biquad 8, N0 coefficient byte[31:24]
0x1D	BQ8_N0_BYT2[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[23:16]
0x1E	BQ8_N0_BYT3[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[15:8]
0x1F	BQ8_N0_BYT4[7:0]	0xFF	Programmable biquad 8, N0 coefficient byte[7:0]
0x20	BQ8_N1_BYT1[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[31:24]
0x21	BQ8_N1_BYT2[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[23:16]
0x22	BQ8_N1_BYT3[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[15:8]
0x23	BQ8_N1_BYT4[7:0]	0x00	Programmable biquad 8, N1 coefficient byte[7:0]
0x24	BQ8_N2_BYT1[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[31:24]
0x25	BQ8_N2_BYT2[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[23:16]
0x26	BQ8_N2_BYT3[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[15:8]
0x27	BQ8_N2_BYT4[7:0]	0x00	Programmable biquad 8, N2 coefficient byte[7:0]
0x28	BQ8_D1_BYT1[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[31:24]
0x29	BQ8_D1_BYT2[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[23:16]
0x2A	BQ8_D1_BYT3[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[15:8]
0x2B	BQ8_D1_BYT4[7:0]	0x00	Programmable biquad 8, D1 coefficient byte[7:0]
0x2C	BQ8_D2_BYT1[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[31:24]
0x2D	BQ8_D2_BYT2[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[23:16]
0x2E	BQ8_D2_BYT3[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[15:8]
0x2F	BQ8_D2_BYT4[7:0]	0x00	Programmable biquad 8, D2 coefficient byte[7:0]
0x30	BQ9_N0_BYT1[7:0]	0x7F	Programmable biquad 9, N0 coefficient byte[31:24]
0x31	BQ9_N0_BYT2[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[23:16]
0x32	BQ9_N0_BYT3[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[15:8]

Table 7-98. Page 3 Programmable Coefficient Registers (continued)

ADDR	REGISTER	RESET	DESCRIPTION
0x33	BQ9_N0_BYT4[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[7:0]
0x34	BQ9_N1_BYT1[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[31:24]
0x35	BQ9_N1_BYT2[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[23:16]
0x36	BQ9_N1_BYT3[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[15:8]
0x37	BQ9_N1_BYT4[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[7:0]
0x38	BQ9_N2_BYT1[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[31:24]
0x39	BQ9_N2_BYT2[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[23:16]
0x3A	BQ9_N2_BYT3[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[15:8]
0x3B	BQ9_N2_BYT4[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[7:0]
0x3C	BQ9_D1_BYT1[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[31:24]
0x3D	BQ9_D1_BYT2[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[23:16]
0x3E	BQ9_D1_BYT3[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[15:8]
0x3F	BQ9_D1_BYT4[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[7:0]
0x40	BQ9_D2_BYT1[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[31:24]
0x41	BQ9_D2_BYT2[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[23:16]
0x42	BQ9_D2_BYT3[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[15:8]
0x43	BQ9_D2_BYT4[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[7:0]
0x44	BQ10_N0_BYT1[7:0]	0x7F	Programmable biquad 10, N0 coefficient byte[31:24]
0x45	BQ10_N0_BYT2[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[23:16]
0x46	BQ10_N0_BYT3[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[15:8]
0x47	BQ10_N0_BYT4[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[7:0]
0x48	BQ10_N1_BYT1[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[31:24]
0x49	BQ10_N1_BYT2[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[23:16]
0x4A	BQ10_N1_BYT3[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[15:8]
0x4B	BQ10_N1_BYT4[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[7:0]
0x4C	BQ10_N2_BYT1[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[31:24]
0x4D	BQ10_N2_BYT2[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[23:16]
0x4E	BQ10_N2_BYT3[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[15:8]
0x4F	BQ10_N2_BYT4[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[7:0]
0x50	BQ10_D1_BYT1[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[31:24]
0x51	BQ10_D1_BYT2[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[23:16]
0x52	BQ10_D1_BYT3[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[15:8]
0x53	BQ10_D1_BYT4[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[7:0]
0x54	BQ10_D2_BYT1[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[31:24]
0x55	BQ10_D2_BYT2[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[23:16]
0x56	BQ10_D2_BYT3[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[15:8]
0x57	BQ10_D2_BYT4[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[7:0]
0x58	BQ11_N0_BYT1[7:0]	0x7F	Programmable biquad 11, N0 coefficient byte[31:24]
0x59	BQ11_N0_BYT2[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[23:16]
0x5A	BQ11_N0_BYT3[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[15:8]
0x5B	BQ11_N0_BYT4[7:0]	0xFF	Programmable biquad 11, N0 coefficient byte[7:0]
0x5C	BQ11_N1_BYT1[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[31:24]
0x5D	BQ11_N1_BYT2[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[23:16]
0x5E	BQ11_N1_BYT3[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[15:8]
0x5F	BQ11_N1_BYT4[7:0]	0x00	Programmable biquad 11, N1 coefficient byte[7:0]
0x60	BQ11_N2_BYT1[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[31:24]
0x61	BQ11_N2_BYT2[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[23:16]
0x62	BQ11_N2_BYT3[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[15:8]
0x63	BQ11_N2_BYT4[7:0]	0x00	Programmable biquad 11, N2 coefficient byte[7:0]
0x64	BQ11_D1_BYT1[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[31:24]

Table 7-98. Page 3 Programmable Coefficient Registers (continued)

ADDR	REGISTER	RESET	DESCRIPTION
0x65	BQ11_D1_BYT2[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[23:16]
0x66	BQ11_D1_BYT3[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[15:8]
0x67	BQ11_D1_BYT4[7:0]	0x00	Programmable biquad 11, D1 coefficient byte[7:0]
0x68	BQ11_D2_BYT1[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[31:24]
0x69	BQ11_D2_BYT2[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[23:16]
0x6A	BQ11_D2_BYT3[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[15:8]
0x6B	BQ11_D2_BYT4[7:0]	0x00	Programmable biquad 11, D2 coefficient byte[7:0]
0x6C	BQ12_N0_BYT1[7:0]	0x7F	Programmable biquad 12, N0 coefficient byte[31:24]
0x6D	BQ12_N0_BYT2[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[23:16]
0x6E	BQ12_N0_BYT3[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[15:8]
0x6F	BQ12_N0_BYT4[7:0]	0xFF	Programmable biquad 12, N0 coefficient byte[7:0]
0x70	BQ12_N1_BYT1[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[31:24]
0x71	BQ12_N1_BYT2[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[23:16]
0x72	BQ12_N1_BYT3[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[15:8]
0x73	BQ12_N1_BYT4[7:0]	0x00	Programmable biquad 12, N1 coefficient byte[7:0]
0x74	BQ12_N2_BYT1[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[31:24]
0x75	BQ12_N2_BYT2[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[23:16]
0x76	BQ12_N2_BYT3[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[15:8]
0x77	BQ12_N2_BYT4[7:0]	0x00	Programmable biquad 12, N2 coefficient byte[7:0]
0x78	BQ12_D1_BYT1[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[31:24]
0x79	BQ12_D1_BYT2[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[23:16]
0x7A	BQ12_D1_BYT3[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[15:8]
0x7B	BQ12_D1_BYT4[7:0]	0x00	Programmable biquad 12, D1 coefficient byte[7:0]
0x7C	BQ12_D2_BYT1[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[31:24]
0x7D	BQ12_D2_BYT2[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[23:16]
0x7E	BQ12_D2_BYT3[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[15:8]
0x7F	BQ12_D2_BYT4[7:0]	0x00	Programmable biquad 12, D2 coefficient byte[7:0]

7.6.3.3 Programmable Coefficient Registers: Page 4

This register page (shown in Table 7-99) consists of the programmable coefficients for mixer 1 to mixer 4 and the first-order IIR filter.

$$\text{hex2dec (value)} / 2^{31} \quad (4)$$

Table 7-99. Page 4 Programmable Coefficient Registers

ADDR	REGISTER	RESET	DESCRIPTION
0x00	PAGE[7:0]	0x00	Device page register
0x08	MIX1_CH1_BYT1[7:0]	0x7F	Digital mixer 1, channel 1 coefficient byte[31:24]
0x09	MIX1_CH1_BYT2[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[23:16]
0x0A	MIX1_CH1_BYT3[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[15:8]
0x0B	MIX1_CH1_BYT4[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[7:0]
0x0C	MIX1_CH2_BYT1[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[31:24]
0x0D	MIX1_CH2_BYT2[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[23:16]
0x0E	MIX1_CH2_BYT3[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[15:8]
0x0F	MIX1_CH2_BYT4[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[7:0]
0x10	MIX1_CH3_BYT1[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[31:24]
0x11	MIX1_CH3_BYT2[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[23:16]
0x12	MIX1_CH3_BYT3[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[15:8]
0x13	MIX1_CH3_BYT4[7:0]	0x00	Digital mixer 1, channel 3 coefficient byte[7:0]
0x14	MIX1_CH4_BYT1[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[31:24]
0x15	MIX1_CH4_BYT2[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[23:16]
0x16	MIX1_CH4_BYT3[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[15:8]
0x17	MIX1_CH4_BYT4[7:0]	0x00	Digital mixer 1, channel 4 coefficient byte[7:0]
0x18	MIX2_CH1_BYT1[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[31:24]
0x19	MIX2_CH1_BYT2[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[23:16]
0x1A	MIX2_CH1_BYT3[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[15:8]
0x1B	MIX2_CH1_BYT4[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[7:0]
0x1C	MIX2_CH2_BYT1[7:0]	0x7F	Digital mixer 2, channel 2 coefficient byte[31:24]
0x1D	MIX2_CH2_BYT2[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[23:16]
0x1E	MIX2_CH2_BYT3[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[15:8]
0x1F	MIX2_CH2_BYT4[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[7:0]
0x20	MIX2_CH3_BYT1[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[31:24]
0x21	MIX2_CH3_BYT2[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[23:16]
0x22	MIX2_CH3_BYT3[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[15:8]
0x23	MIX2_CH3_BYT4[7:0]	0x00	Digital mixer 2, channel 3 coefficient byte[7:0]
0x24	MIX2_CH4_BYT1[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[31:24]
0x25	MIX2_CH4_BYT2[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[23:16]
0x26	MIX2_CH4_BYT3[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[15:8]
0x27	MIX2_CH4_BYT4[7:0]	0x00	Digital mixer 2, channel 4 coefficient byte[7:0]
0x28	MIX3_CH1_BYT1[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[31:24]
0x29	MIX3_CH1_BYT2[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[23:16]
0x2A	MIX3_CH1_BYT3[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[15:8]
0x2B	MIX3_CH1_BYT4[7:0]	0x00	Digital mixer 3, channel 1 coefficient byte[7:0]
0x2C	MIX3_CH2_BYT1[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[31:24]
0x2D	MIX3_CH2_BYT2[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[23:16]
0x2E	MIX3_CH2_BYT3[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[15:8]
0x2F	MIX3_CH2_BYT4[7:0]	0x00	Digital mixer 3, channel 2 coefficient byte[7:0]
0x30	MIX3_CH3_BYT1[7:0]	0x7F	Digital mixer 3, channel 3 coefficient byte[31:24]
0x31	MIX3_CH3_BYT2[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[23:16]
0x32	MIX3_CH3_BYT3[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[15:8]

Table 7-99. Page 4 Programmable Coefficient Registers (continued)

ADDR	REGISTER	RESET	DESCRIPTION
0x33	MIX3_CH3_BYT4[7:0]	0xFF	Digital mixer 3, channel 3 coefficient byte[7:0]
0x34	MIX3_CH4_BYT1[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[31:24]
0x35	MIX3_CH4_BYT2[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[23:16]
0x36	MIX3_CH4_BYT3[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[15:8]
0x37	MIX3_CH4_BYT4[7:0]	0x00	Digital mixer 3, channel 4 coefficient byte[7:0]
0x38	MIX4_CH1_BYT1[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[31:24]
0x39	MIX4_CH1_BYT2[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[23:16]
0x3A	MIX4_CH1_BYT3[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[15:8]
0x3B	MIX4_CH1_BYT4[7:0]	0x00	Digital mixer 4, channel 1 coefficient byte[7:0]
0x3C	MIX4_CH2_BYT1[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[31:24]
0x3D	MIX4_CH2_BYT2[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[23:16]
0x3E	MIX4_CH2_BYT3[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[15:8]
0x3F	MIX4_CH2_BYT4[7:0]	0x00	Digital mixer 4, channel 2 coefficient byte[7:0]
0x40	MIX4_CH3_BYT1[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[31:24]
0x41	MIX4_CH3_BYT2[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[23:16]
0x42	MIX4_CH3_BYT3[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[15:8]
0x43	MIX4_CH3_BYT4[7:0]	0x00	Digital mixer 4, channel 3 coefficient byte[7:0]
0x44	MIX4_CH4_BYT1[7:0]	0x7F	Digital mixer 4, channel 4 coefficient byte[31:24]
0x45	MIX4_CH4_BYT2[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[23:16]
0x46	MIX4_CH4_BYT3[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[15:8]
0x47	MIX4_CH4_BYT4[7:0]	0xFF	Digital mixer 4, channel 4 coefficient byte[7:0]
0x48	IIR_N0_BYT1[7:0]	0x7F	Programmable first-order IIR, N0 coefficient byte[31:24]
0x49	IIR_N0_BYT2[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[23:16]
0x4A	IIR_N0_BYT3[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[15:8]
0x4B	IIR_N0_BYT4[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[7:0]
0x4C	IIR_N1_BYT1[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[31:24]
0x4D	IIR_N1_BYT2[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[23:16]
0x4E	IIR_N1_BYT3[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[15:8]
0x4F	IIR_N1_BYT4[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[7:0]
0x50	IIR_D1_BYT1[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[31:24]
0x51	IIR_D1_BYT2[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[23:16]
0x52	IIR_D1_BYT3[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[15:8]
0x53	IIR_D1_BYT4[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[7:0]

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The PCMD3140-Q1 is a multichannel, pulse-density-modulation (PDM) input to time-division multiplexing (TDM) or I²S audio output converter that supports output sample rates of up to 768 kHz. The device supports up to four digital pulse density modulation (PDM) microphones for simultaneous recording applications.

Communication to the PCMD3140-Q1 for configuration of the control registers is supported using an I²C interface. The device supports a highly flexible, audio serial interface (TDM, I²S, and LJ) to transmit audio data seamlessly in the system across devices.

8.2 Typical Application

8.2.1 Four-Channel Digital PDM Microphone Recording

Figure 8-1 shows a typical configuration of the PCMD3140-Q1 for an application using four digital PDM MEMS microphones with simultaneous recording operation using an I²C control interface and the TDM audio data slave interface. If the MICBIAS output is not used in the system then the 1-µF capacitor for the MICBIAS pin is not used.

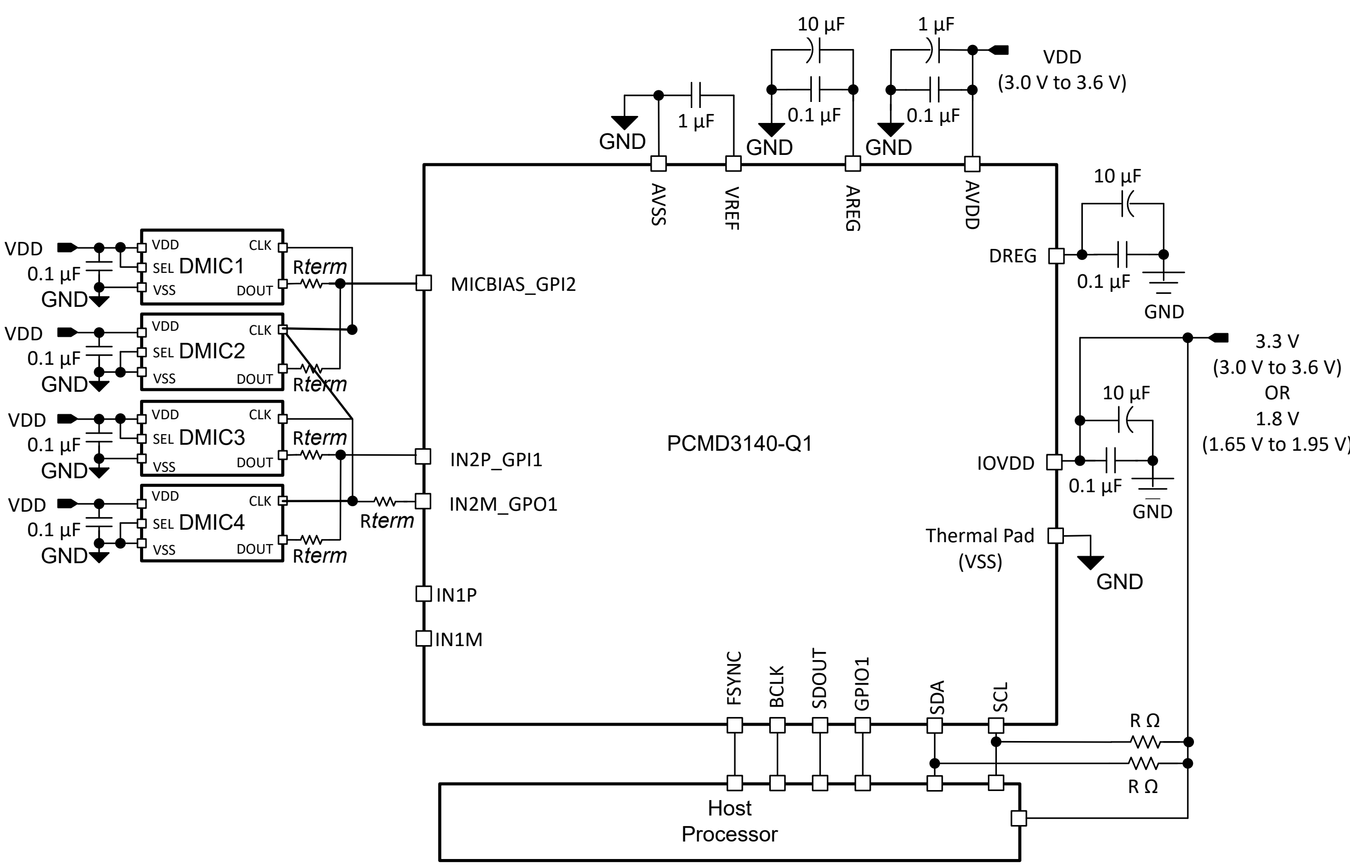


Figure 8-1. Four-Channel Digital PDM Microphone Recording Diagram

8.2.1.1 Design Requirements

The supply decoupling capacitors used must be ceramic with low ESR. Table 8-1 lists the design parameters for this application.

Table 8-1. Design Parameters

KEY PARAMETER	SPECIFICATION
AVDD	3.3 V
AVDD supply current consumption	10 mA (PLL on, four-channel recording, f_S = 48 kHz, PDMCLKx = 64 × f_S)
IOVDD	1.8 V or 3.3 V

8.2.1.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCMD3140-Q1 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power-up the IOVDD and AVDD power supplies
   b. Wait for at least 1 ms to allow the device to initialize the internal registers initialization
   c. The device now goes into sleep shutdown mode (low-power mode < 10 µA)
2. Transition from sleep mode to active mode whenever required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
   d. Configure channel 1 to channel 2 (CHx_INSRC) for the digital microphone as the input source for recording
   e. Configure GPO1 (GPO1_CFG) and GPIO1 (GPIO1_CFG) as the PDMCLK output
   f. Configure GPIx (GPI1x_CFG) as PDMDINx
   g. Enable all desired input channels by writing to P0_R115
   h. Enable all desired audio serial interface output channels by writing to P0_R116
   i. Power-up the PDM converter and PLL by writing to P0_R117
   j. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a.

      See the *Section 7.3.2* section for supported sample rates and the BCLK to FSYNC ratio.
   k. The device recording data is now sent to the host processor using the TDM audio serial data bus
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
   a. Enter sleep mode by writing to P0_R2 to enable sleep mode
   b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
   c. Read P0_R119 to check the device shutdown and sleep mode status
   d. If the device P0_R119_D7 status bit is 1'b1 then stop FSYNC and BCLK in the system
   e. The device now goes into sleep mode (low-power mode < 10 µA) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
   d. The device recording data are now sent to the host processor using the TDM audio serial data bus
5. Repeat step 3 and step 4 as required for mode transitions and step 2 to step 4 for configuration changes.

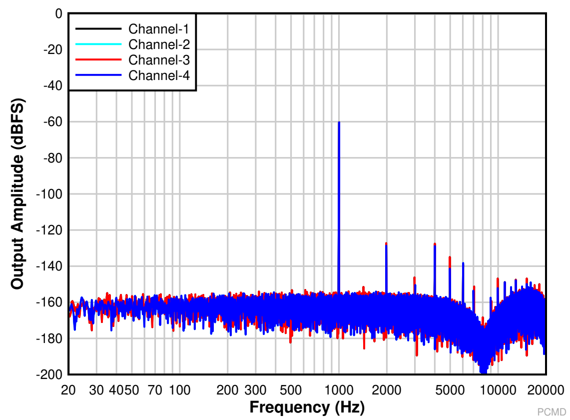
8.2.1.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I^{2}C register control script that shows how to set up the PCMD3140-Q1 in a 4-channel digital PDM microphone recording mode.

```
# Key: w 9C XX YY ==> write to I2C address 0x9C, to register 0xXX, data 0xYY
#                # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the PCMD3140EVM user guide for jumper settings and audio connections.
#
# PDM 8-channel : PDMDIN1 - Ch1 and Ch2, PDMDIN2 - Ch3 and Ch4,
#                 PDMDIN3 - Ch5 and Ch6, PDMDIN4 - Ch7 and Ch8
# PDMCLKx = 2.8224 MHz (PDMCLKx/FSYNC = 64)
# FSYNC = 44.1 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#################################################################
#
#
# Power up IOVDD and AVDD power supplies
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Wait for 1ms.
#
# Wake-up device by I2C write into P0_R2 using internal AREG
w 9C 02 81
#
# Configure CH2_INSRC as Digital PDM Input by I2C write into P0_R65
w 9C 41 40
#
# Configure MICBIAS_GPI2 as Digital PDM Input by I2C write into P0_R59
w 9C 3B 70
#
# Configure GPO1 as PDMCLK by I2C write into P0_R34
w 9C 22 41
#
# Configure GPI1 and GPI2 as PDMDIN1 and PDMDIN2 by I2C write into P0_R43
w 9C 2B 45
#
# Enable Input Ch-1 to Ch-4 by I2C write into P0_R115
w 9C 73 F0
#
# Enable ASI Output Ch-1 to Ch-4 slots by I2C write into P0_R116
w 9C 74 F0
#
# Power-up ADC and PLL by I2C write into P0_R117
w 9C 75 60
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data by host on ASI bus with TDM protocol 32-bits channel wordlength
```

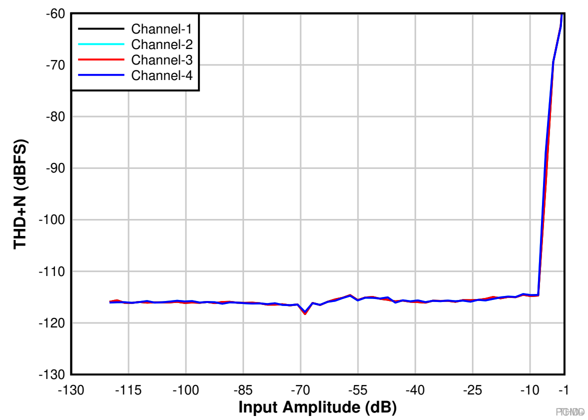
8.2.1.3 Application Curves

Measurements are done on the EVM by feeding the device PDM digital input signal using audio precision. In the system application, the device performance is expected to be limited by the single-bit PDM modulator digital microphone output performance.



4th-order PDM modulator with PDMCLKx = 2.8224 MHz

Figure 8-2. FFT With a –60-dBr Input



4th-order PDM modulator with PDMCLKx = 2.8224 MHz

Figure 8-3. THD+N vs Input Amplitude

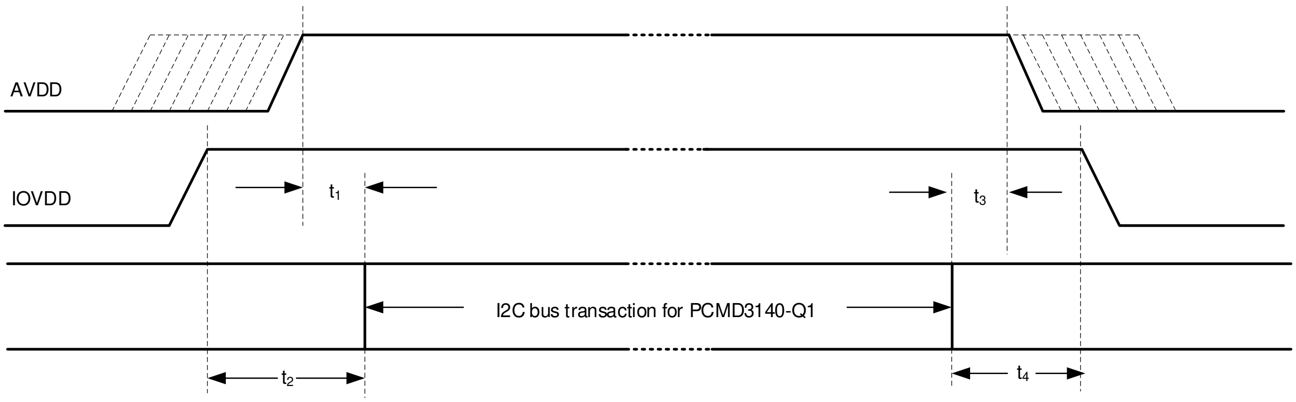
8.3 What to Do and What Not to Do

In the VAD mode of operation, there are some limitations on interrupt generation when auto wake up is enabled. For details about these limitations, see the *Using the Voice Activity Detector (VAD) in the TLV320ADC5120 and TLV320ADC6120* application report.

9 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, only initiate the I^{2}C transactions after all supplies are stable to initialize the device.

For the supply power-up requirement, t_1 and t_2 must be at least 2 ms to allow the device to initialize the internal registers. See the *Section 7.4* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_3 and t_4 must be at least 10 ms. This timing (as shown in Figure 9-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.


AVDD
IOVDD
t1
t3
I2C bus transaction for PCMD3140-Q1
t2
t4

Make sure that the supply ramp rate is slower than 1 V/µs and that the wait time between a power-down and a power-up event is at least 100 ms. For a supply ramp rate slower than 0.1 V/ms, the host device must apply a software reset as the first transaction before configuring the device. Make sure that all digital input pins are at valid input levels and not toggling during supply sequencing.

The PCMD3140-Q1 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG. However, if the AVDD voltage is less than 1.98 V in the system, then short the AREG and AVDD pins onboard and do not enable the internal AREG by keeping the AREG_SELECT bit to 1b'0 (default value) of P0_R2. If the AVDD supply used in the system is higher than 2.7 V, then the host device can set AREG_SELECT to 1'b1 when exiting sleep mode to allow the device internal regulator to generate the AREG supply.

10 Layout

10.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- The supply decoupling capacitors must be used ceramic type with low ESR.
- Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

10.2 Layout Example

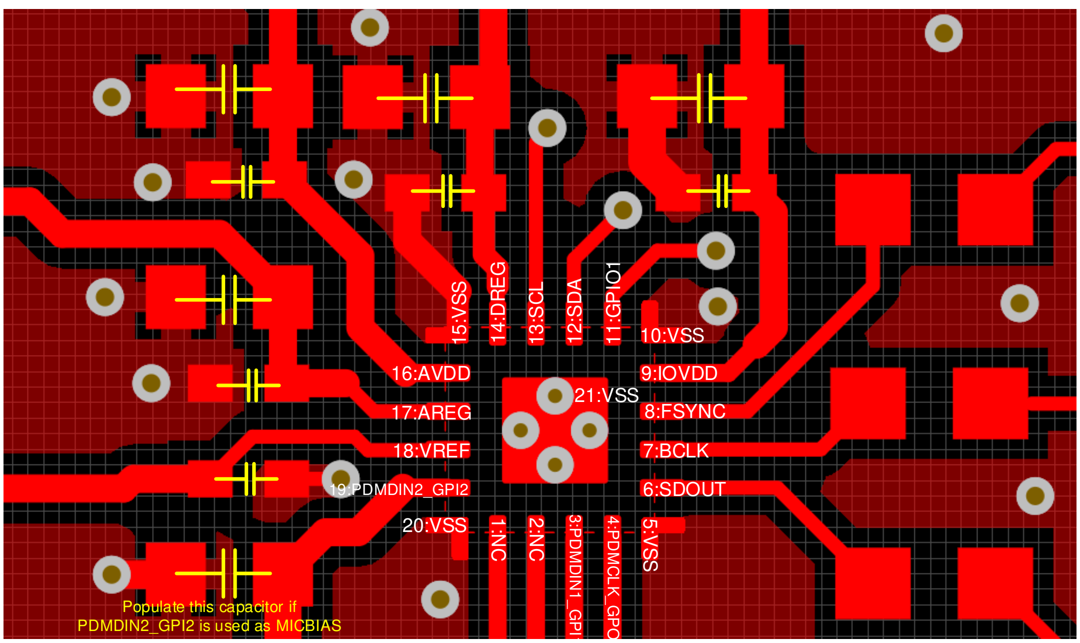


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Multiple TLV320ADCx140 Devices With Shared TDM and I²C Bus* application report
- Texas Instruments, *Configuring and Operating TLV320ADCx120 as an Audio Bus Master* application report
- Texas Instruments, *TLV320ADCx140 Sampling Rates and Programmable Processing Blocks Supported* application report
- Texas Instruments, *TLV320ADCx140 Programmable Biquad Filter Configuration and Applications* application report
- Texas Instruments, *TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios* application report
- Texas Instruments, *Using the Voice Activity Detector (VAD) in the TLV320ADC5120 and TLV320ADC6120* application report
- Texas Instruments, *ADCx120EVM-PDK Evaluation module* user's guide
- Texas Instruments, PurePath™ Console Graphical Development Suite for Audio System Design and Development

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PurePath™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

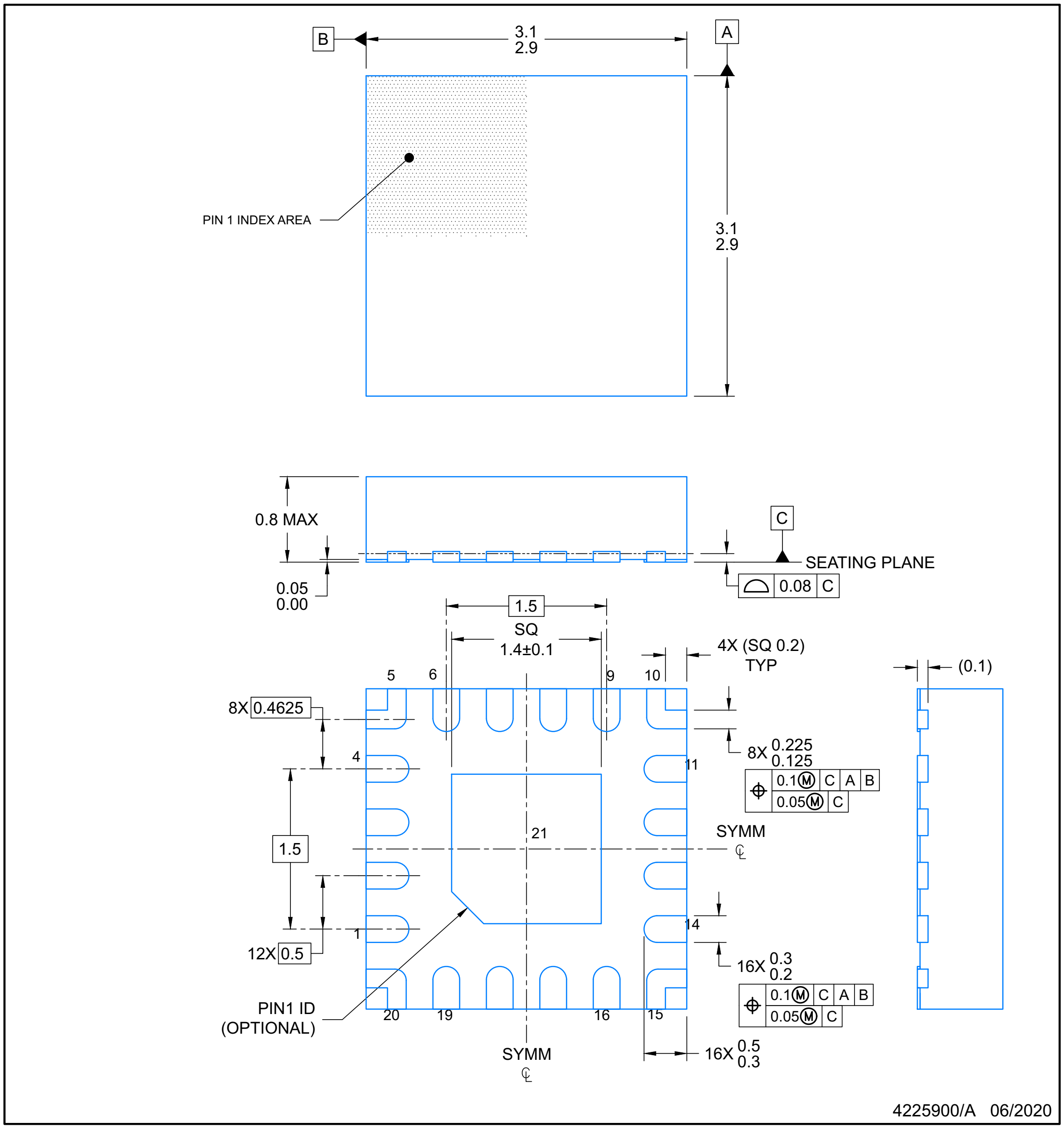
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

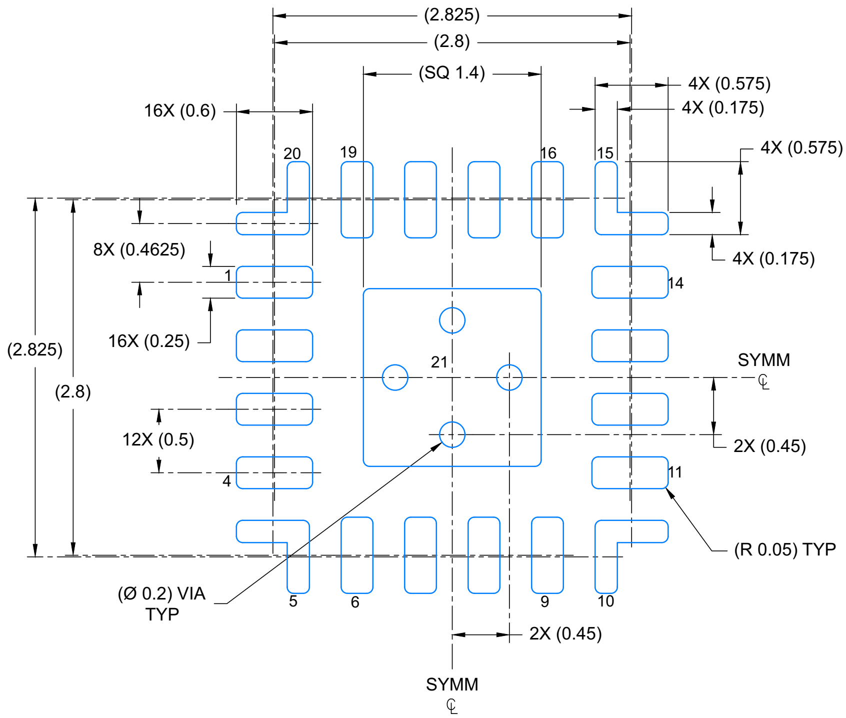
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

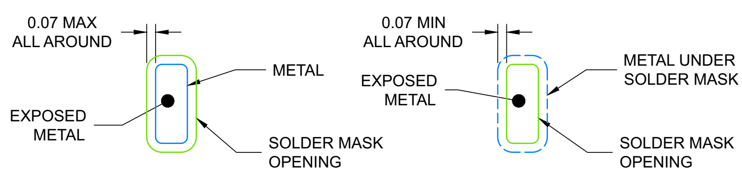
RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

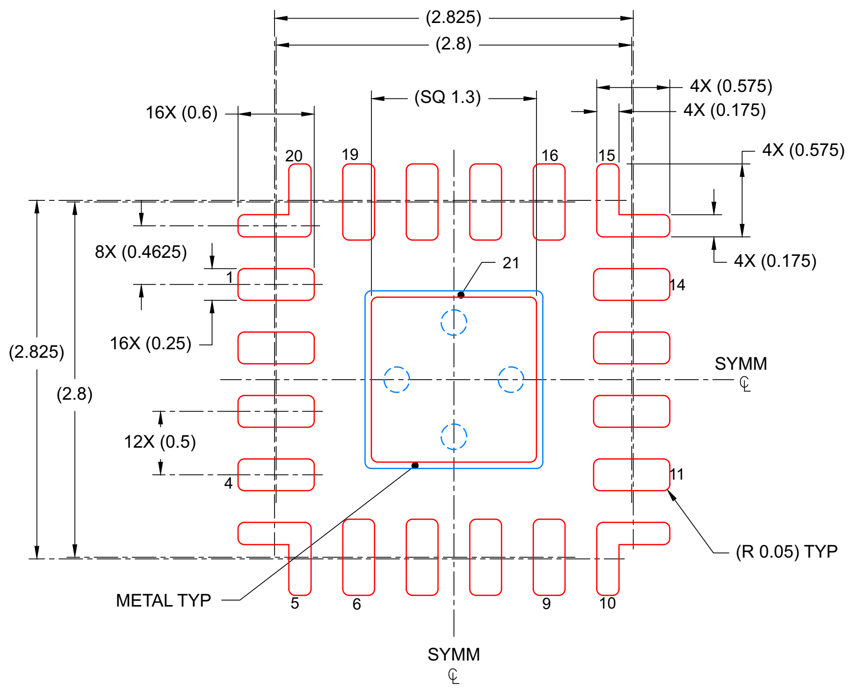
www.ti.com

EXAMPLE STENCIL DESIGN

RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCMD3140QRTERQ1	Active	Production	WQFN (RTE) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D3140Q
PCMD3140QRTERQ1.A	Active	Production	WQFN (RTE) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D3140Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCMD3140-Q1 :

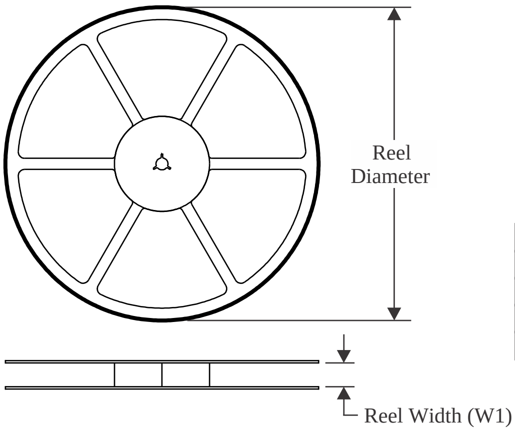
- Catalog : PCMD3140

NOTE: Qualified Version Definitions:

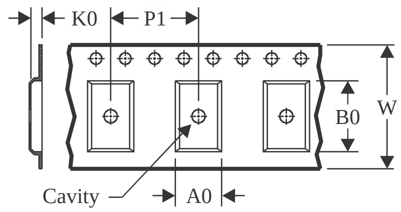
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

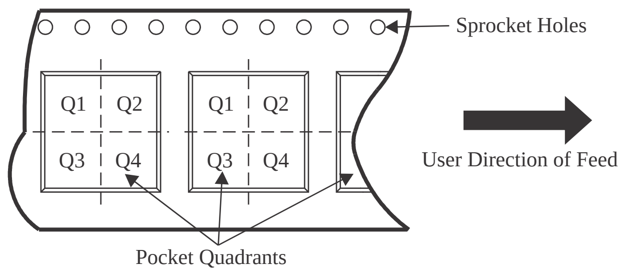


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

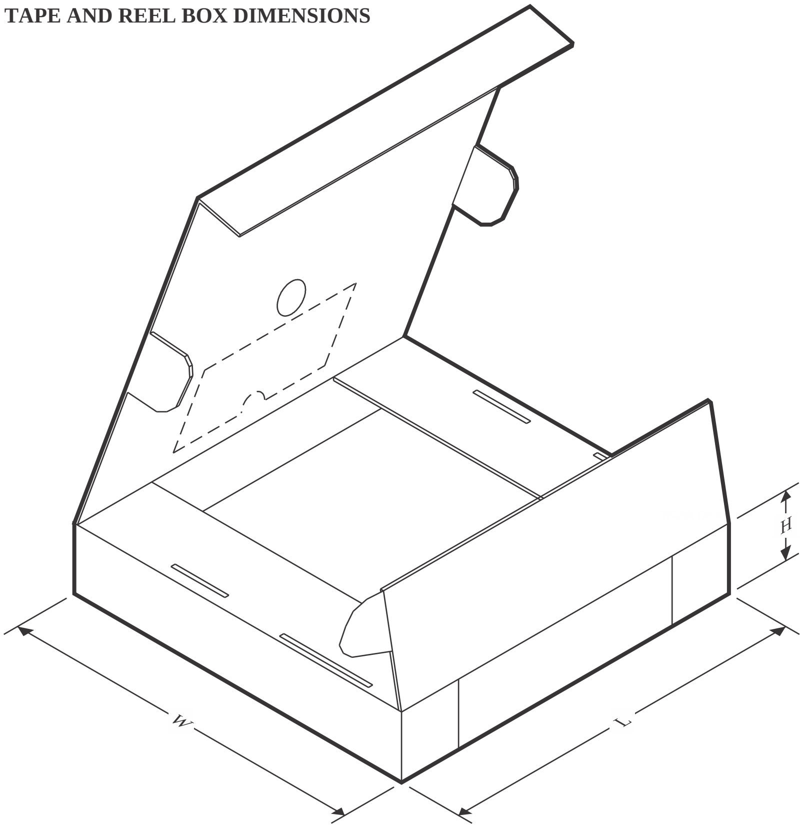
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

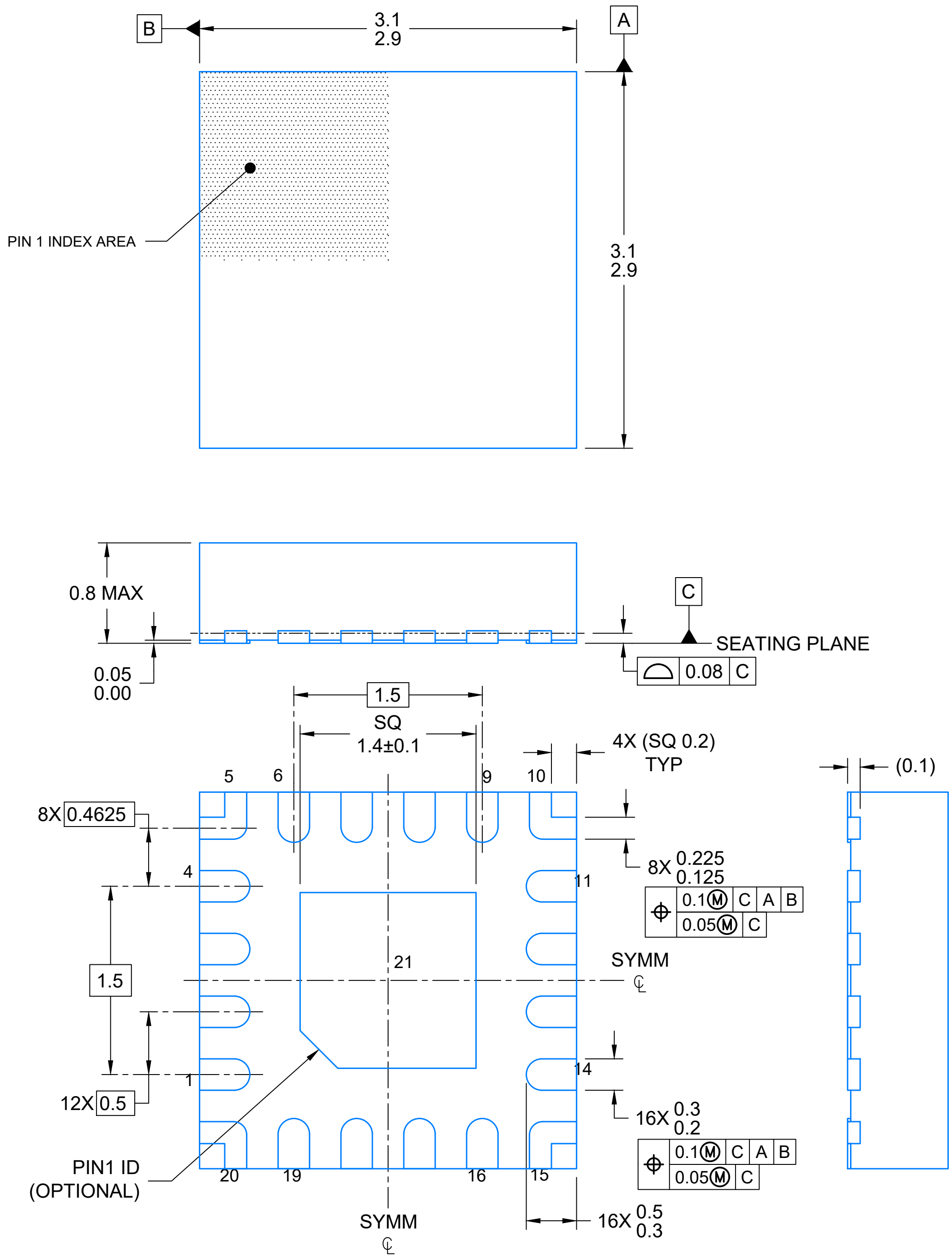
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCMD3140QRTERQ1	WQFN	RTE	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCMD3140QRTERQ1	WQFN	RTE	20	3000	367.0	367.0	35.0



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NOTES:

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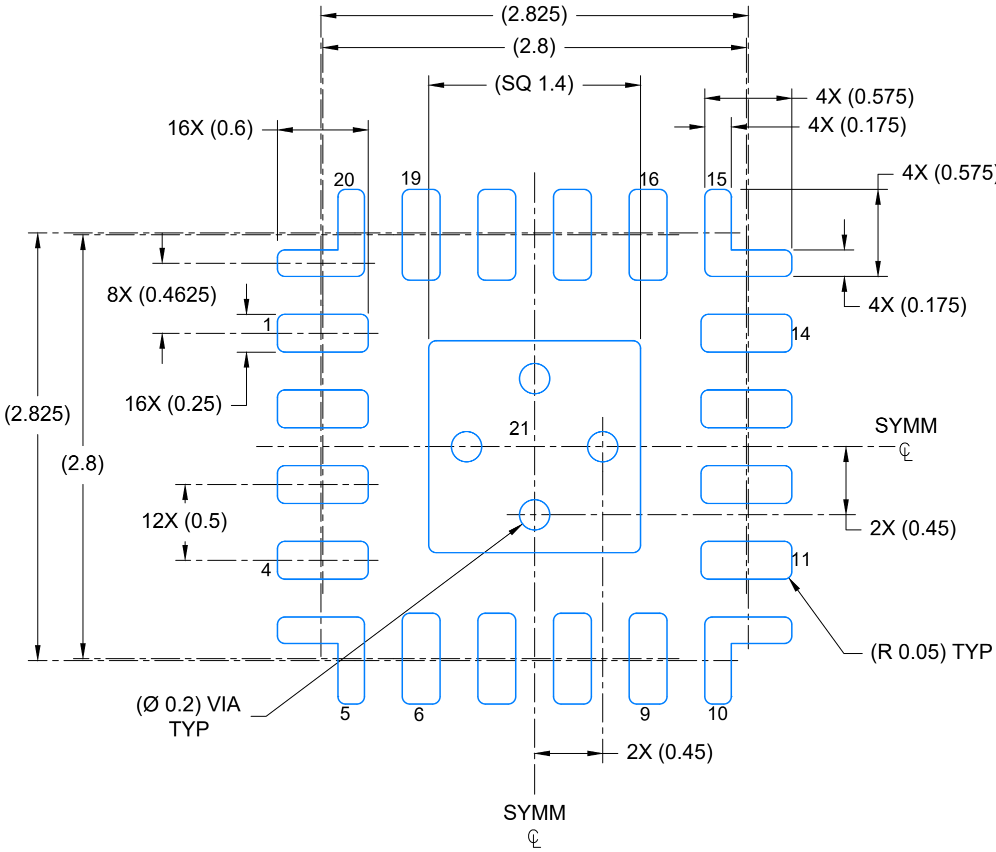
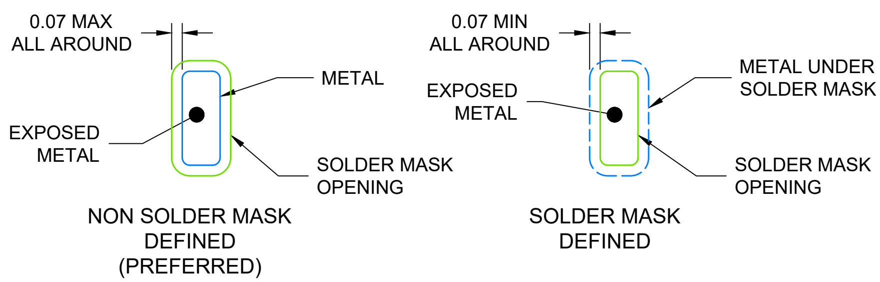


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

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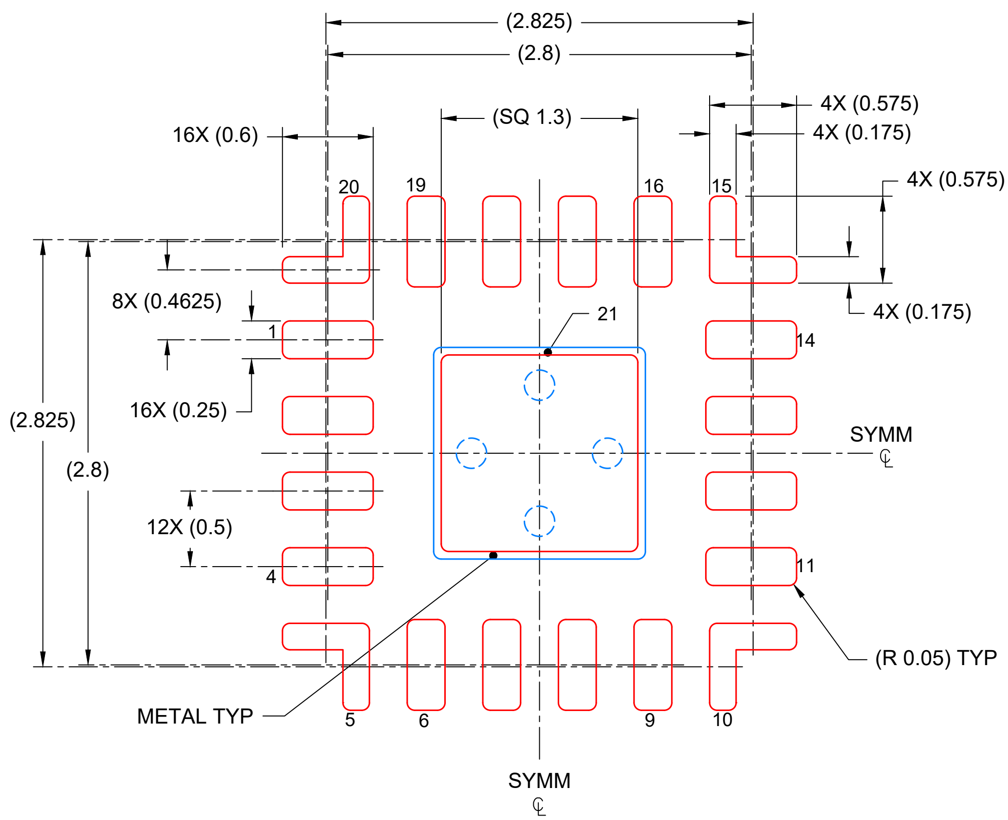
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 20X

4225900/A 06/2020

NOTES: (continued)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265