2-V_{RMS} DirectPath™, 112/106/100-dB Audio Stereo DAC With 32-Bit, 384-kHz PCM Interface

Check for Samples: PCM5100-Q1 (Preliminary), PCM5101-Q1 (Preliminary), PCM5102-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Market-Leading Low Out-of-Band Noise
- Selectable Digital-Filter Latency and Performance
- No DC Blocking Capacitors Required
- Integrated Negative Charge Pump
- Internal Pop-Free Control For Sample-Rate Changes or Clock Halts
- Intelligent Muting System; Soft Up/Down Ramp and Analog Mute For 120-dB Mute SNR With Popless Operation.
- Integrated High-Performance Audio PLL With BCK Reference to Generate SCK Internally
- Small 20-pin TSSOP Package

Typical Performance (3.3-V Power Supply)

Parameter	PCM5102-Q1 / PCM5101-Q1 / PCM5100-Q1
SNR	112 / 106 / 100 dB
Dynamic range	112 / 106 / 100 dB
THD+N at –1 dBFS	–93 / –92 / –90 dB
Full-scale output	2.1V_{RMS} (GND center)
Normal 8× oversampling digital-filter latency: 22 / f_S	
Low-latency 8× oversampling digital-filter latency: 3.5 / f_S	
Sampling frequency	8 kHz to 384 kHz
System clock multiples (f_{SCK}): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	

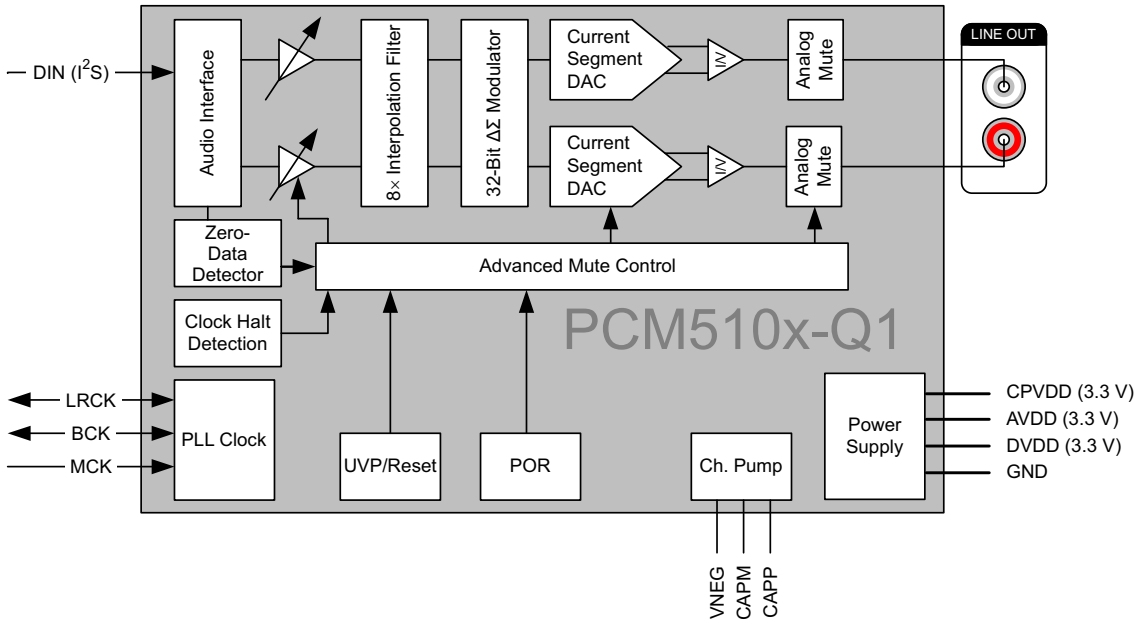


Figure 1. PCM510x-Q1 Functional Block Diagram

OTHER KEY FEATURES

- **Accepts 16-, 24-, and 32-Bit Audio Data**
- **PCM Data Formats: I²S, Left-Justified**
- **Automatic Power-Save Mode When LRCK And BCK Are Deactivated**
- **3.3-V Failsafe LVCMOS Digital Inputs**
- **Hardware Configuration**
- **Single-Supply Operation:**
  - **3.3-V Analog, 3.3-V Digital**
- **Integrated Power-On Reset**

APPLICATIONS

- **A/V Receivers**
- **DVD, BD Players**
- **HDTV Receivers**
- **Applications Requiring 2-V_{RMS} Audio Output**

DESCRIPTION

The PCM510x-Q1 family is a series of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM510x-Q1 uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

The PCM510x-Q1 provides 2.1-V_{RMS} ground-centered outputs, allowing designers to eliminate not only dc blocking capacitors on the output, but also external muting circuits traditionally associated with single-supply line drivers.

The integrated line driver surpasses all other charge-pump-based line drivers by supporting loads down to 1 kΩ. By supporting loads down to 1 kΩ, the PCM510x-Q1 can essentially drive up to 10 products in parallel (LCD TV, DVDR, AV receivers, and so on).

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock). This allows a three-wire I²S connection, along with reduced system EMI.

Intelligent clock error and PowerSense undervoltage protection uses a two-level mute system for pop-free performance. On clock error or system power failure, the device digitally attenuates the data (or last known-good data), then mutes the analog circuit

Compared with existing DAC technology, the PCM510x-Q1 offers up to 20-dB lower out-of-band (OBN) noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100-kHz OBN measurements all the way to 3 MHz)

The PCM510x-Q1 accepts industry-standard audio data formats with 16- to 32-bit data and supports sSample rates up to 384 kHz.

Table 1. Ordering Information

Part Number	T_A	Top-Side Symbol
PCM5100TPWRQ1 (Preview)	–40°C to 105°C	PCM5100Q
PCM5101TPWRQ1 (Preview)	–40°C to 105°C	PCM5101Q
PCM5102TPWRQ1	–40°C to 105°C	PCM5102Q

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage	AVDD, CPVDD, DVDD	–0.3 to 3.9	V
Digital input voltage		–0.3 to 3.9	
Analog input voltage		–0.3 to 3.9	
Operating temperature range		–40 to 105	°C
Storage temperature range		–65 to 150	
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750	V

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Theta JA	High K		91.2		ºC/W
ψ_{JT}	Psi JT			1		
ψ_{JB}	Psi JB			41.5		
θ_{JC}	Theta JC	Top		25.3		
θ_{JB}	Theta JB			42		

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Power-Supply Requirements						
DV_{DD}	Digital supply voltage	Target DV_{DD} = 3.3 V	3	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3	3.3	3.6	VDC
CPV_{DD}	Charge-pump supply voltage		3	3.3	3.6	VDC
I_{DD}	DV_{DD} supply current at 3.3 V(1)	f_S = 48 kHz		7	12	mA
		f_S = 96 kHz		8		
		f_S = 192 kHz		9		
I_{DD}	DV_{DD} supply current at 3.3 V(2)	f_S = 48 kHz		8	13	mA
		f_S = 96 kHz		9		
		f_S = 192 kHz		10		
I_{DD}	DV_{DD} supply current at 3.3 V(3)			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} supply current(1)	f_S = 48 kHz		11	16	mA
		f_S = 96 kHz		11		
		f_S = 192 kHz		11		

(1) Input is bipolar-zero data.
(2) Input is 1-kHz, –1-dBFS data.
(3) Power-down mode

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Power-Supply Requirements						
I_{CC}	AV_{DD} / CPV_{DD} supply current(2)	f_S = 48 kHz		22	32	mA
		f_S = 96 kHz		22		
		f_S = 192 kHz		22		
I_{CC}	AV_{DD} / CPV_{DD} supply current(3)	f_S = N/A		0.2	0.4	mA
	Power dissipation, DV_{DD} = 3.3 V(1)	f_S = 48 kHz		59.4	92.4	mW
		f_S = 96 kHz		62.7		
		f_S = 192 kHz		66		
	Power dissipation, DV_{DD} = 3.3 V(2)	f_S = 48 kHz		99	148.5	mW
		f_S = 96 kHz		102.3		
		f_S = 192 kHz		105.6		
	Power dissipation, DV_{DD} = 3.3 V(3)	f_S = N/A (power-down mode)		2.3	4	mW

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
Data Format (PCM Mode)						
	Audio data interface format		I^2S, left justified			
	Audio data bit length		16, 24, 32-bit acceptable			
	Audio data format		MSB-first, 2s complement			
f_S	Sampling frequency		8		384	kHz
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f_{SCK}, up to 50 Mhz			
Digital Input/Output						
	Logic family: 3.3-V LVCMOS compatible					
V_{IH}	Input logic level		0.7 × DV_{DD}			V
V_{IL}					0.3 × DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –4 mA	0.8 × DV_{DD}			V
V_{OL}		I_{OL} = 4 mA			0.22 × DV_{DD}	
Dynamic Performance (PCM Mode)(1)(2) (Values shown for three devices PCM5102-Q1/PCM5101-Q1/PCM5100-Q1)						
	THD+N at –1 dBFS(2)	f_S = 48 kHz		–93/–92/–90	–83/–82/–80	dB
		f_S = 96 kHz		–93/–92/–90		
		f_S = 192 kHz		–93/–92/–90		
	Dynamic range(2)	EIAJ, A-weighted, f_S = 48 kHz	106/100/95	112/106/100		
		EIAJ, A-weighted, f_S = 96 kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192 kHz		112/106/100		
	Signal-to-noise ratio(2)	EIAJ, A-weighted, f_S = 48 kHz		112/106/100		
		EIAJ, A-weighted, f_S = 96 kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192 kHz		112/106/100		
	Signal-to-noise ratio with analog mute(2)(3)	EIAJ, A-weighted, f_S = 48 kHz	113	123		
		EIAJ, A-weighted, f_S = 96 kHz		123		
		EIAJ, A-weighted, f_S = 192 kHz		123		
	Channel separation	f_S = 48 kHz	100/95/90	109/103/97		
		f_S = 96 kHz		109/103/97		
		f_S = 192 kHz		109/103/97		
Analog Output						
	Output voltage			2.1		V_{RMS}
	Gain error		–6	±2	6	% of FSR
	Gain mismatch, channel-to-channel		–6	±2	6	% of FSR
	Bipolar-zero error	At bipolar zero	–5	±1	5	mV
	Load impedance		1			kΩ
Filter Characteristics–1: Normal						

(1) Filter condition: THD+N: 20-Hz HPF, 20-kHz AES17 LPF; dynamic range: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted channel separation: 20-Hz HPF, 20-kHz AES17 LPF; using the System Two Cascade™ audio measurement system by Audio Precision™ in the rms mode to measure analog performance specifications.
(2) Output load is 10 kΩ, with 470-Ω output resistor and a 2.2-nF shunt capacitor (see recommended output filter).
(3) Both L-ch and R-ch are BPZ with XSMT de-asserted

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Pass band				0.45 f_S	
	Stop band		0.55 f_S			
	Stop-band attenuation		–60			dB
	Pass-band ripple				±0.02	
	Delay time			22 / f_S		s
Filter Characteristics–2: Low Latency						
	Pass band				0.47 f_S	
	Stop band		0.55 f_S			
	Stop-band attenuation		–52			dB
	Pass-band ripple				±0.0001	
	Delay time			3.5 / f_S		s

DEVICE INFORMATION

TERMINAL FUNCTIONS, PCM510x-Q1

PW Package
20 Pins
(Top View)

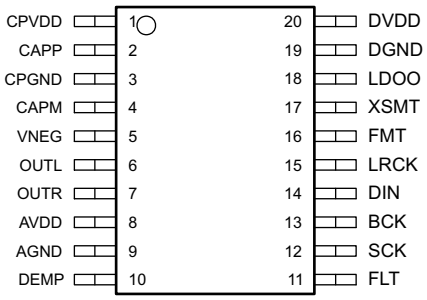


Table 2. PIN FUNCTIONS, PCM510x-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog ground
AVDD	8	-—	Analog power supply, 3.3 V
BCK	13	I	Audio-data bit-clock input(1)
CAPM	4	O	Charge-pump flying-capacitor terminal for negative rail
CAPP	2	O	Charge-pump flying-capacitor terminal for positive rail
CPGND	3	—	Charge-pump ground
CPVDD	1	—	Charge-pump power supply, 3.3 V
DEMP	10	I	De-emphasis control for 44.1-kHz sampling rate(1): Off (Low), On (High)
DGND	19	—	Digital ground
DIN	14	I	Audio-data input(1)
DVDD	20	—	Digital power supply, 3.3 V
FLT	11	I	Filter select : Normal latency (Low) or Low latency (High)
FMT	16	I	Audio format selection : I^2S (Low) or Left-justified (High)

(1) Failsafe LVCMOS Schmitt-trigger input

Table 2. PIN FUNCTIONS, PCM510x-Q1 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
LDOO	18	—	Internal-logic supply-rail terminal for decoupling
LRCK	15	I	Audio-data word-clock input(1)
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
SCK	12	I	System clock input(1)
VNEG	5	O	Negative charge-pump rail terminal for decoupling, –3.3 V
XSMT	17	I	Soft-mute control(1): Soft mute (Low), Soft un-mute (High)

TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data unless otherwise noted.

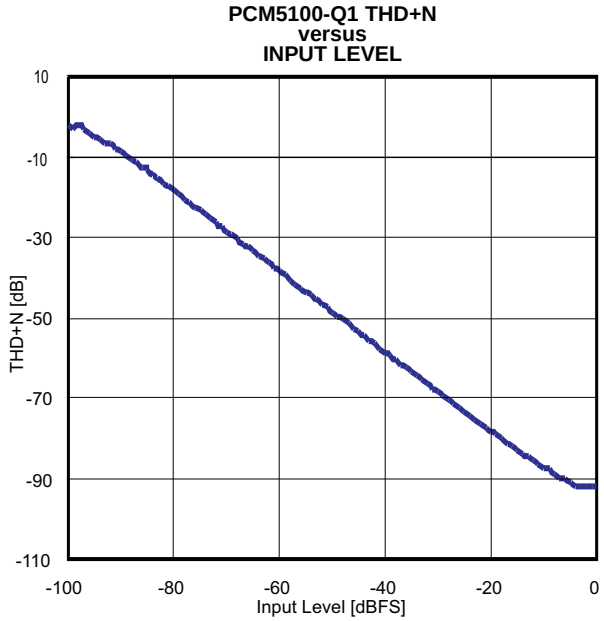


Figure 2.

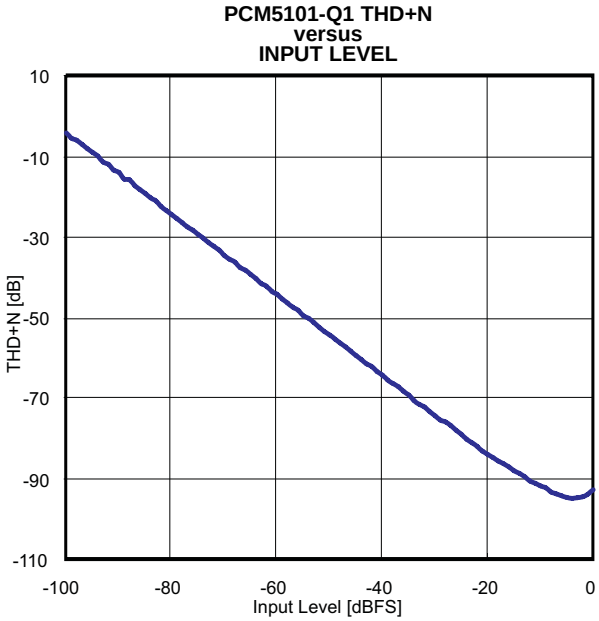


Figure 3.

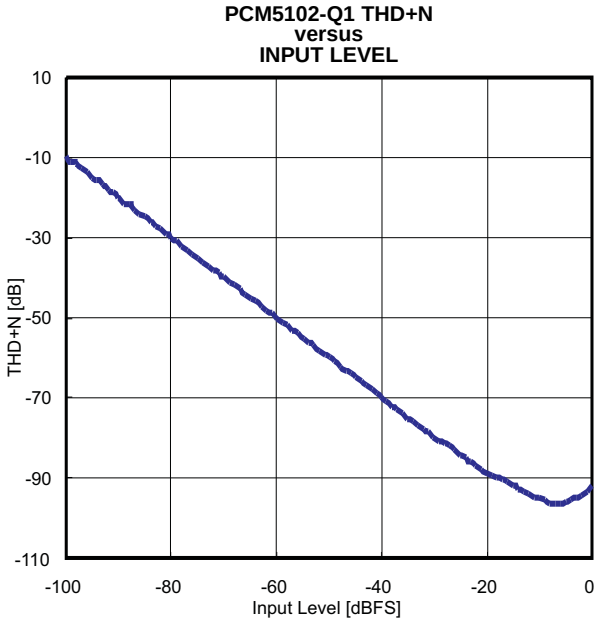


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data unless otherwise noted.

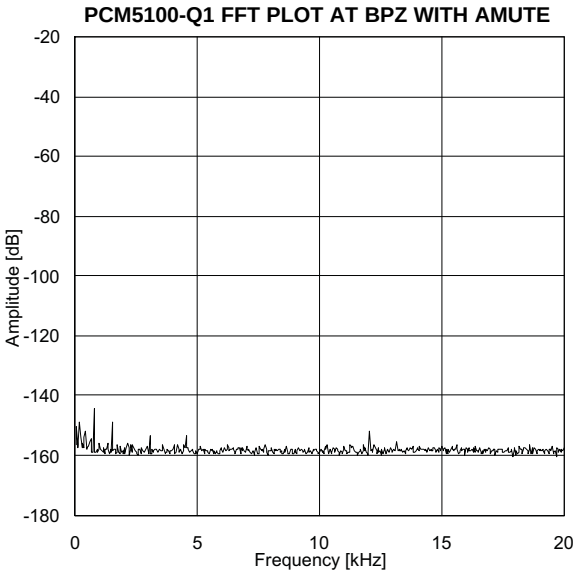


Figure 5.

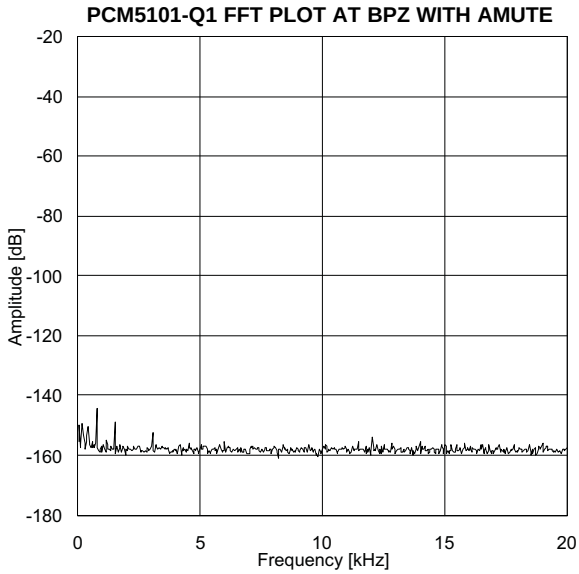


Figure 6.

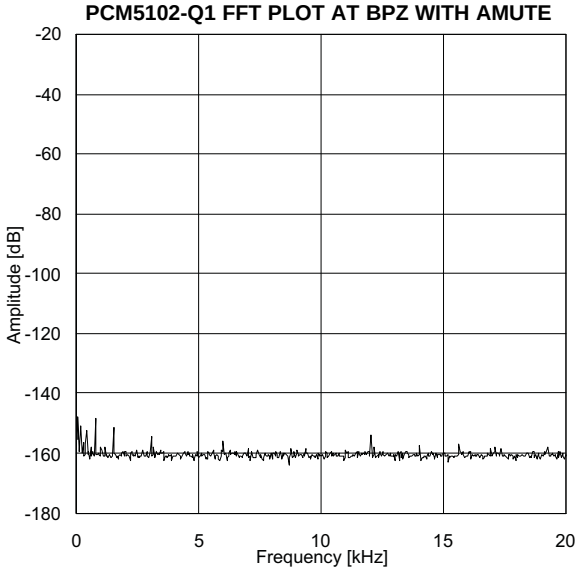


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data unless otherwise noted.

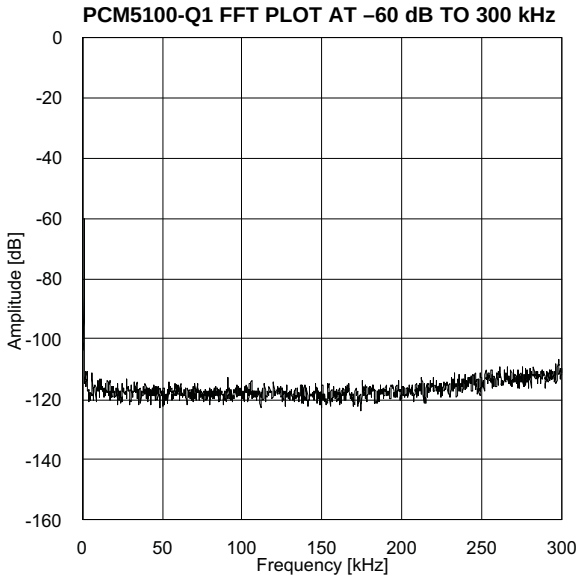


Figure 8.

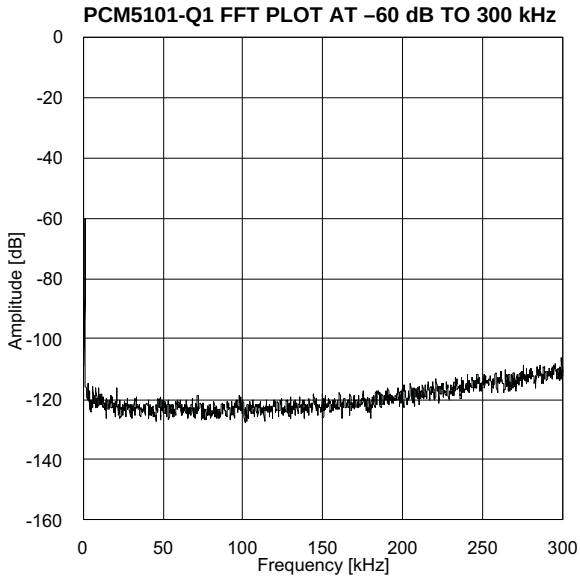


Figure 9.

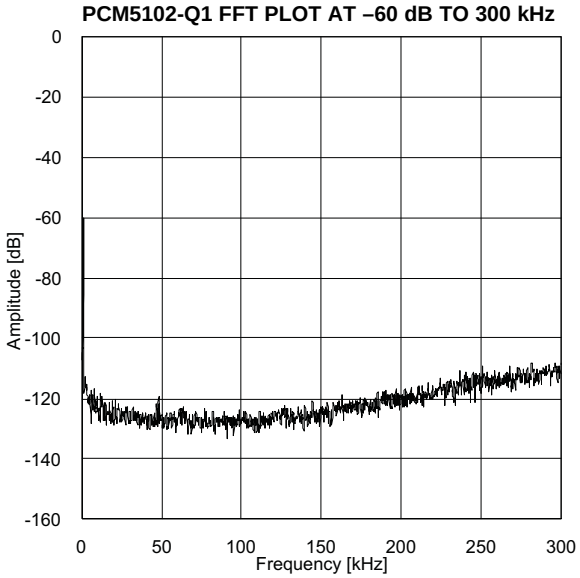


Figure 10.

APPLICATION INFORMATION

Reset and System Clock Functions

Power-On Reset Function

The PCM510x-Q1 includes a power-on-reset function shown in Figure 11. Having V_{DD} > 2.8 V enables the power-on reset function. After the initialization period, the PCM510x-Q1 enters its default reset state.

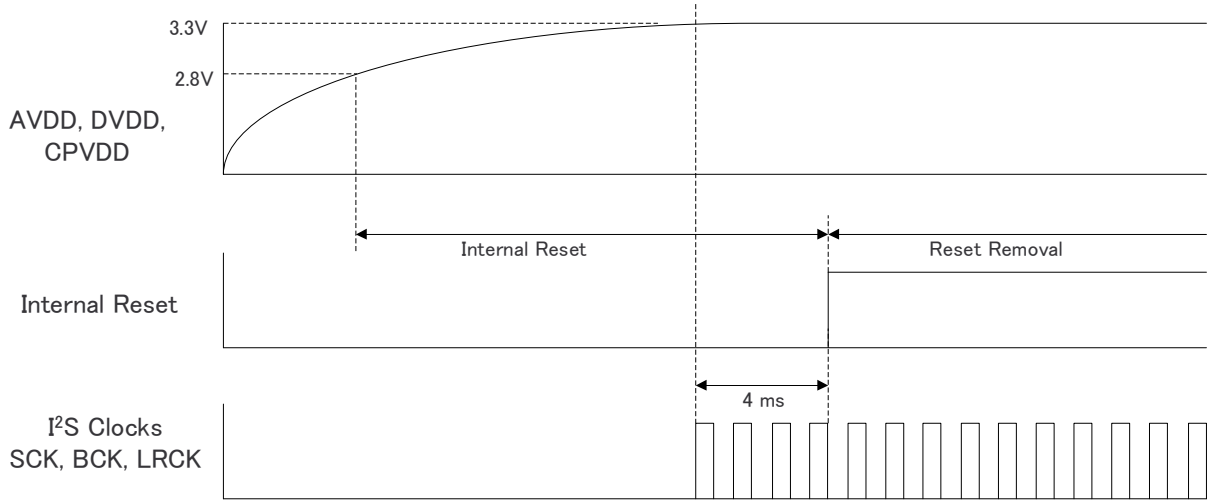


Figure 11. Power-On Reset Timing, DVDD = 3.3 V

System-Clock Input

The PCM510x-Q1 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock, applied at the SCK input (pin 12), supports up to 50 MHz. The PCM510x-Q1 has a system-clock detection circuit that automatically senses the system-clock frequency. The device supports common audio sampling frequencies of 8 kHz, 16 kHz, 32 kHz–44.1 kHz and 48 kHz, 88.2 kHz-96 kHz, 176.4 kHz-192 kHz, and 384 kHz with ±4% tolerance. The sampling-frequency detector sets the clock for the digital filter, delta-sigma modulator (DSM), and the negative charge pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

NOTE

The sampling frequency detector only detects six sampling-frequency options. Any sampling frequency between the range of 32 kHz–44.1 kHz (or if it is 48 kHz) is one option. The same case applies for the ranges from 88.2 kHz–96 kHz and 176.4 kHz–192 kHz.

The device supports SCK rates between 1 MHz and 50 MHz that are not common to standard audio clocks by configuring various PLL and clock-divider registers. This allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example. using 12 MHz to generate 44.1 kHz (LRCK) and 2.8224 MHz (BCK)).

Figure 12 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 3. System Master Clock Inputs for Audio-Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	–(1)	1.0240(2)	1.5360(2)	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	–(1)	2.0480(2)	3.0720(2)	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	–(1)	4.0960(2)	6.1440(2)	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	–(1)	–(1)
44.1 kHz	–(1)	5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)
48 kHz	–(1)	6.1440(2)	9.2160(2)	12.2880	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)
88.2 kHz	–(1)	11.2896(2)	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
96 kHz	–(1)	12.2880(2)	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
176.4 kHz	–(1)	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
192 kHz	–(1)	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
384 kHz	24.5760	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)

(1) The device does not support this system clock rate for the given sampling frequency.
(2) PLL mode supports this system clock rate.

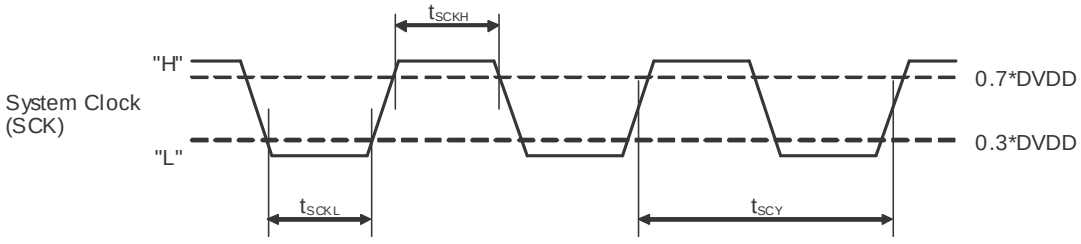


Figure 12. Timing Requirements for SCK Input

Table 4. Timing Requirements for SCK Input

	Parameters	Min	Max	Unit
t_{SCY}	System clock-pulse cycle time	20	1000	ns
t_{SCKH}	System clock-pulse duration, High	9		ns
t_{SCKL}	System clock-pulse duration, Low	9		ns

System Clock PLL Mode

The system clock PLL mode allows designers to use a simple three-wire I^2S audio source when driving the DAC, thereby reducing the need for a high-frequency SCK, making PCB layout easier, and reducing high-frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. In the PCM510x-Q1, supplying an external SCK disables the internal PLL; the device requires specific BCK rates to generate an appropriate master clock. Table 5 describes the minimum and maximum BCK per LRCK for the integrated PLL to generate an internal SCK automatically.

Table 5. BCK Rates (MHz) by LRCK Sample Rate for PCM510x-Q1 PLL Operation

	BCK (f_S)	
Sample f (kHz)	32	64
8	–	–
16	–	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

Audio Data Interface

Audio Serial Interface

The audio interface port is a three-wire serial port. It includes LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, and it clocks the serial data present on DIN into the serial shift register of the audio interface. Clocking of serial data into the PCM510x-Q1 occurs on the rising edge of BCK. LRCK is the serial audio left/right word clock.

Table 6. PCM510x-Q1 Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f_S]	SCK RATE [× f_S]	BCK RATE [× f_S]
Hardware control	I^2S or LJ	32, 24, 20, 16	Up to 192 kHz	128–3072 (≤50 MHz)	64, 48, 32
			384 kHz	64, 128	64, 48, 32

The PCM510x-Q1 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and the system clock.

If the relationship between LRCK and BCK is invalid for more than 4 LRCK periods, the device initializes internal operation within one sample period and forces analog outputs to the bipolar-zero level until the completion of resynchronization between LRCK and BCK.

PCM Audio Data Formats and Timing

The PCM510x-Q1 supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected using the FMT (pin 16), Low for I^2S, and High for left-justified.

All formats require binary 2s-complement, MSB-first audio data. Figure 13 shows a detailed timing diagram for the serial audio interface.

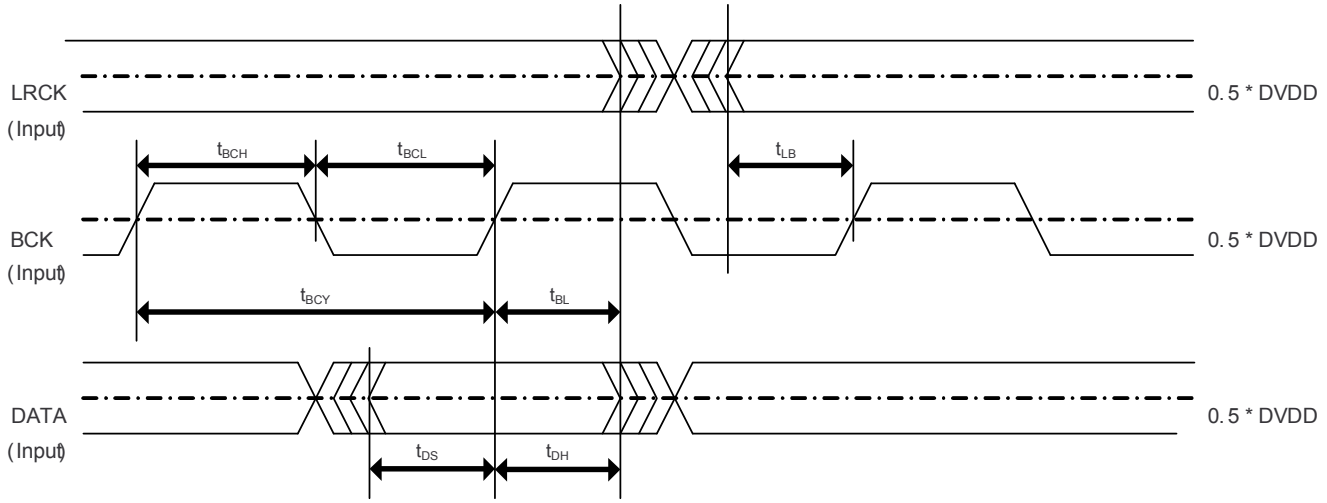
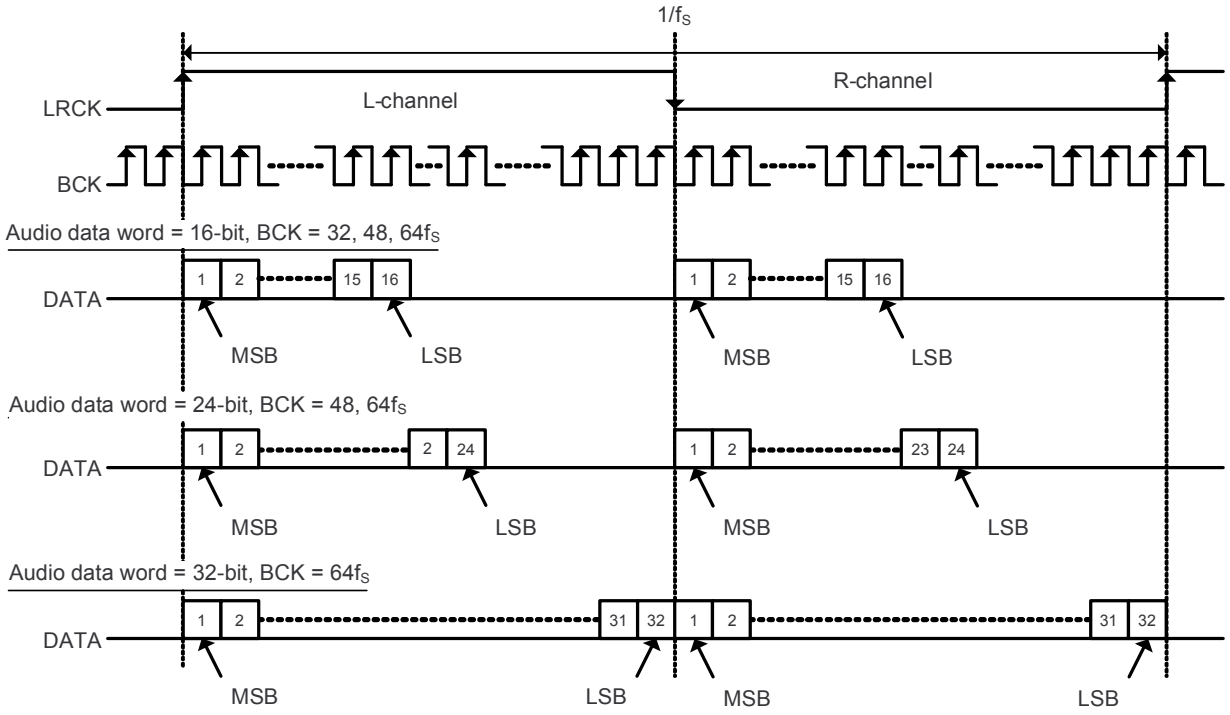


Figure 13. PCM510x-Q1 Serial Audio Timing - Slave

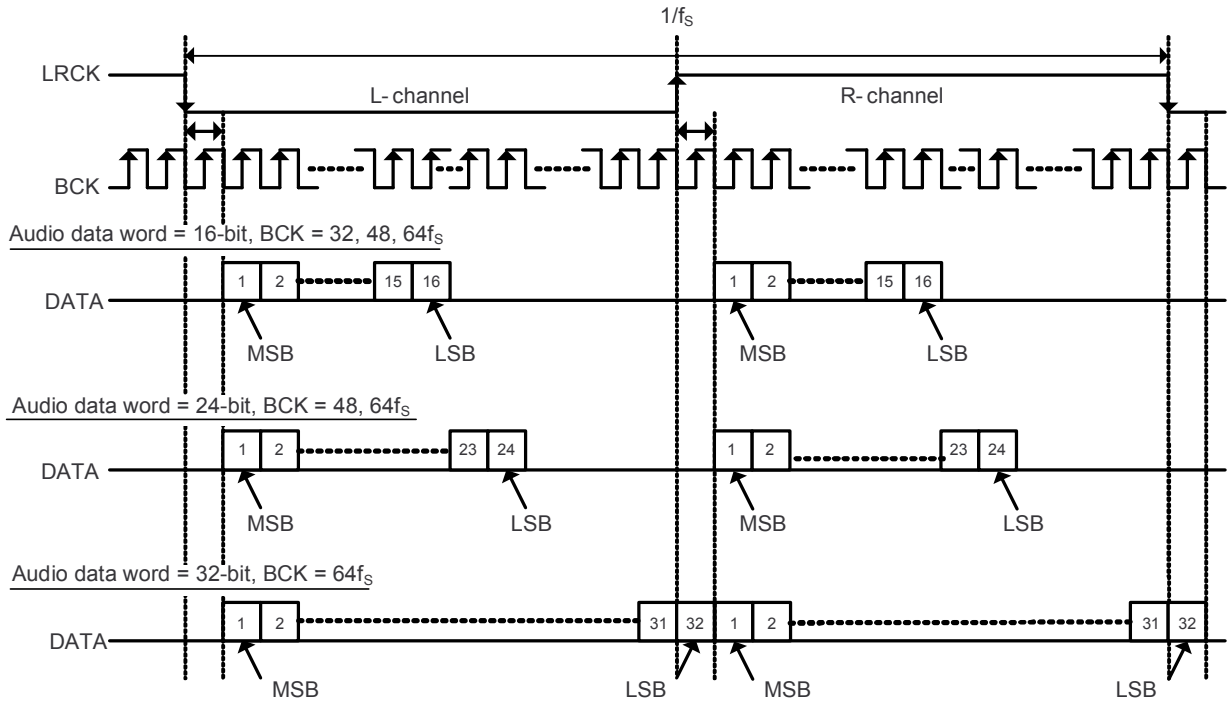
Table 7. Audio Interface Slave Timing

	Parameters	Min	Max	Unit
t_{BCY}	BCK pulse cycle time	40		ns
t_{BCL}	BCK pulse duration, LOW	16		ns
t_{BCH}	BCK pulse duration, HIGH	16		ns
t_{BL}	BCK rising edge to LRCK edge	8		ns
t_{LB}	LRCK edge to BCK rising edge	8		ns
t_{DS}	DATA setup time	8		ns
t_{DH}	DATA hold time	8		ns
f_{BCK}	BCK frequency at DVDD = 3.3 V		24.576	MHz



Left-justified data format; L-channel = HIGH, R-channel = LOW

Figure 14. Left-Justified Audio Data Format



I^2S Data Format; L-channel = LOW, R-channel = HIGH

Figure 15. I^2S Audio Data Format

Function Descriptions

Interpolation Filter

The PCM510x-Q1 provides two types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11).

Table 8. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR normal ×8, ×4, ×2, and ×1 interpolation filters
1	IIR low-latency ×8, ×4, ×2, and ×1 interpolation filters

The normal ×8, ×4, ×2, or ×1 (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) for from 8 kHz to 384 kHz.

Table 9. Normal ×8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	0–0.45 f_S		±0.02	dB
Filter-gain stop band	0.55 f_S–7.455 f_S	–60		dB
Filter-group delay		22 / f_S		s

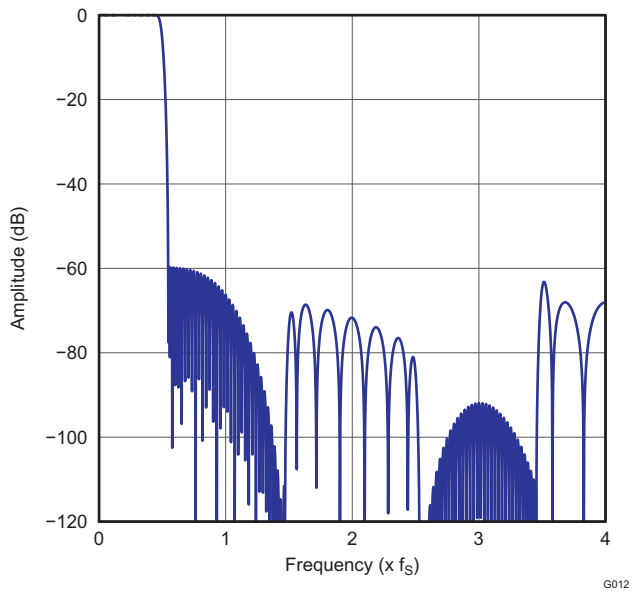


Figure 16. Normal ×8 Interpolation-Filter Frequency Response

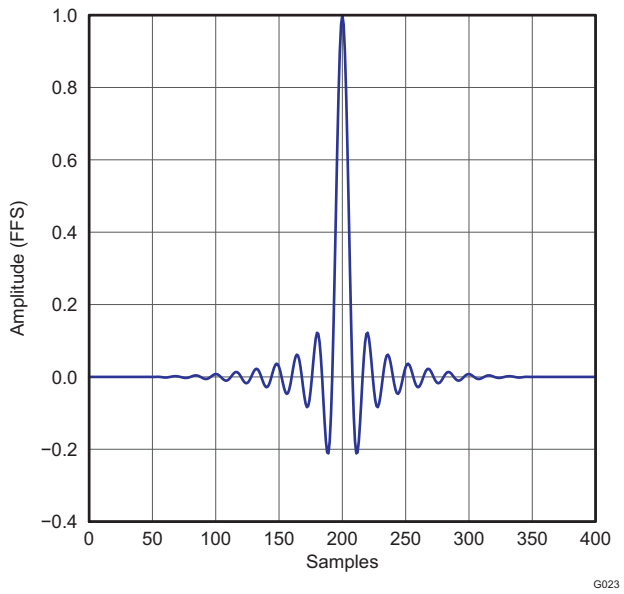


Figure 17. Normal ×8 Interpolation-Filter Impulse Response

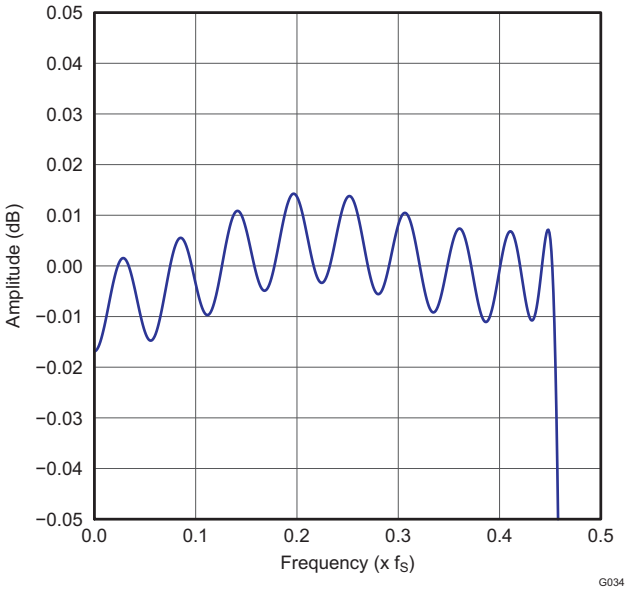


Figure 18. Normal ×8 Interpolation-Filter Pass-Band Ripple

The normal ×4, ×2, or ×1 (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) from 8 kHz to 384 kHz.

Table 10. Normal ×4 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	0–0.45 f_S		±0.02	dB
Filter-gain stop band	0.55 f_S–7.455 f_S	–60		dB
Filter-group delay		22 / f_S		s

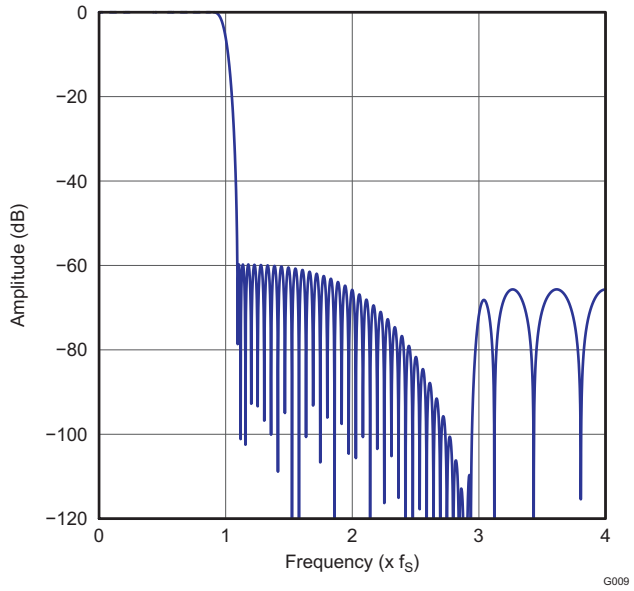


Figure 19. Normal ×4 Interpolation-Filter Frequency Response

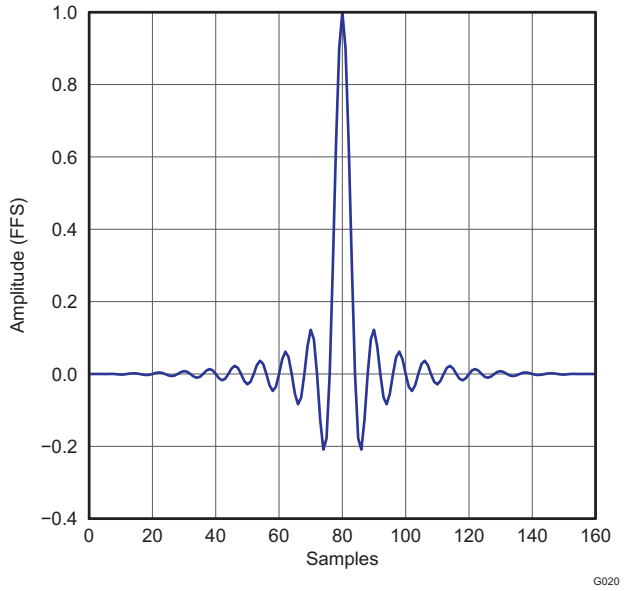


Figure 20. Normal ×4 Interpolation-Filter Impulse Response

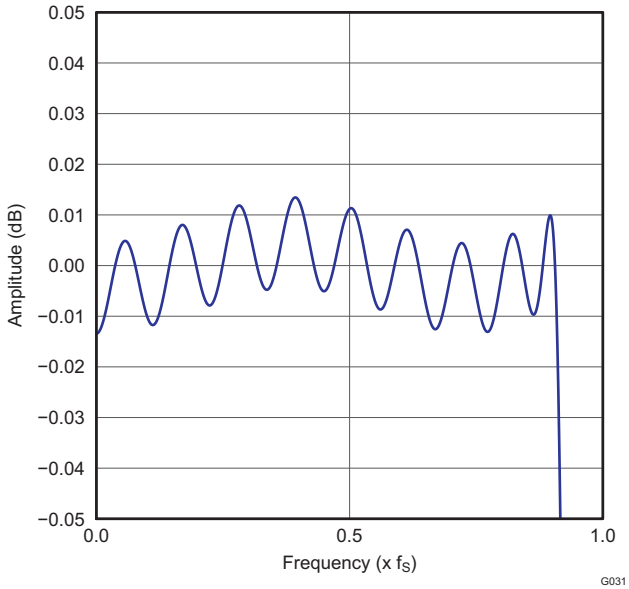


Figure 21. Normal ×4 Interpolation-Filter Pass-Band Ripple

Normal ×2 or ×1 (bypass) interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) from 8 kHz to 384 kHz.

Table 11. Normal ×2 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Unit
Filter-gain pass band	0–0.45 f_S		±0.02	dB
Filter-gain stop band	0.55 f_S–7.455 f_S	–60		dB
Filter-group delay		22 / f_S		s

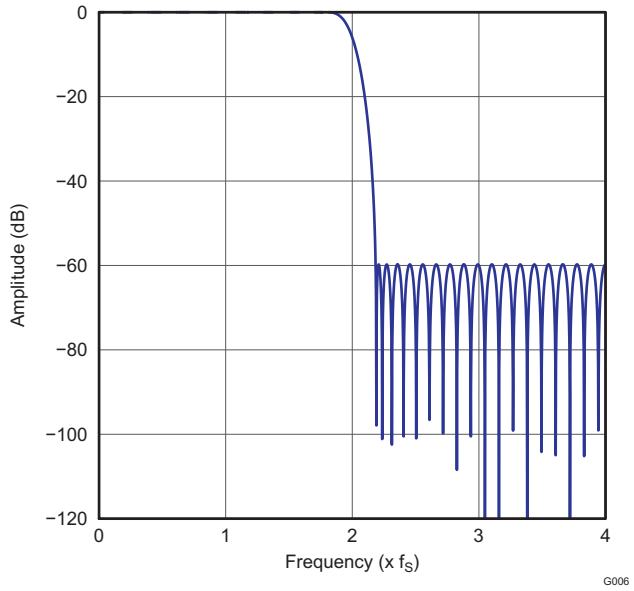


Figure 22. Normal ×2 Interpolation-Filter Frequency Response

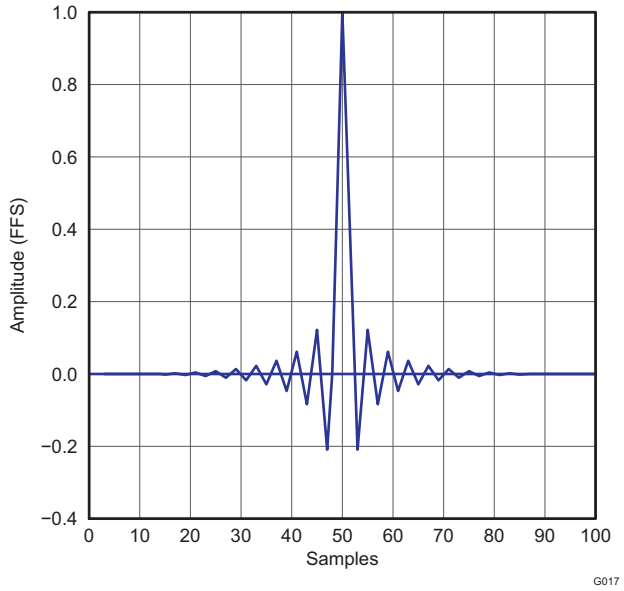


Figure 23. Normal ×2 Interpolation-Filter Impulse Response

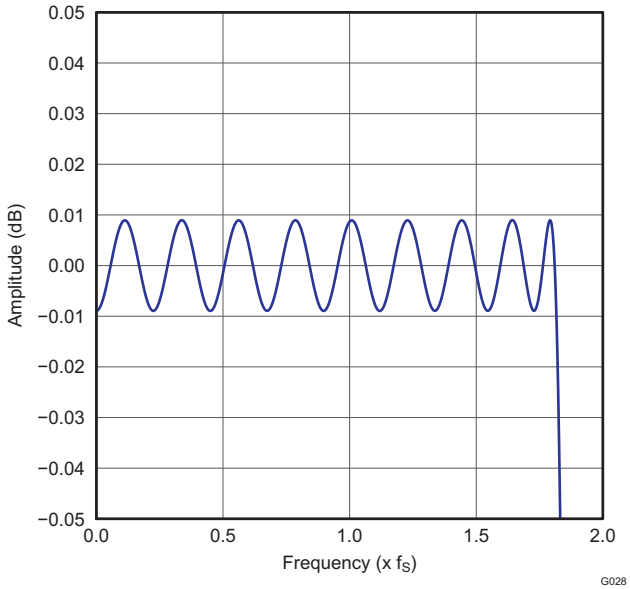


Figure 24. Normal ×2 Interpolation-Filter Pass-Band Ripple

The low-latency ×8, ×4, ×2, or ×1 (bypass) interpolation filter is programmed in 256 cycles in 1 f_S from 8 kHz to 384 kHz.

Table 12. Low-Latency ×8 Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	0–0.45 f_S	±0.0001	dB
Filter-gain stop band	0.55 f_S–7.455 f_S	–52	dB
Filter-group delay		3.5 / f_S	s

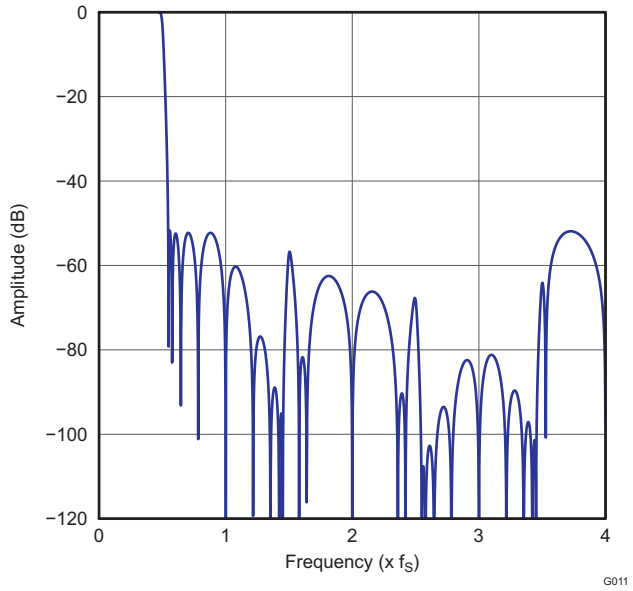


Figure 25. ×8 Interpolation-Filter Frequency Response

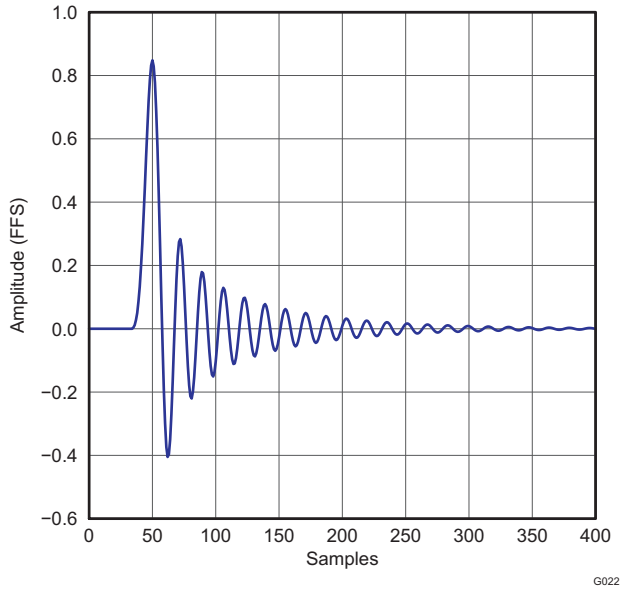


Figure 26. Low-Latency ×8 Interpolation-Filter Impulse Response

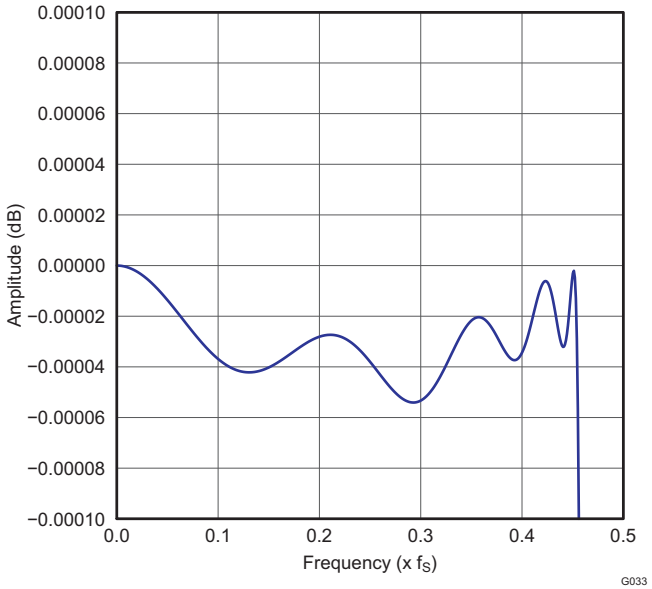


Figure 27. Low-Latency ×8 Interpolation-Filter Pass-Band Ripple

Table 13. Low-Latency ×4 Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	0–0.45 f_S	±0.0001	dB
Filter-gain stop band	0.55 f_S–3.455 f_S	–52	dB
Filter-group delay		3.5 / f_S	s

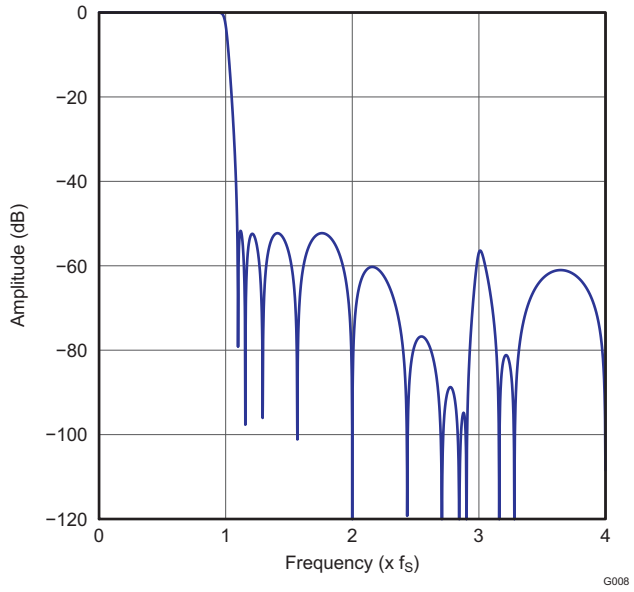


Figure 28. Low-Latency ×4 Interpolation-Filter Frequency Response

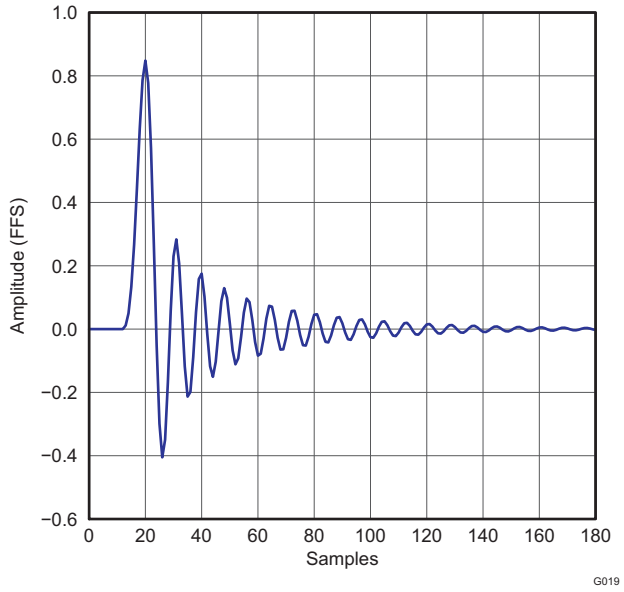


Figure 29. Low-Latency ×4 Interpolation-Filter Impulse Response

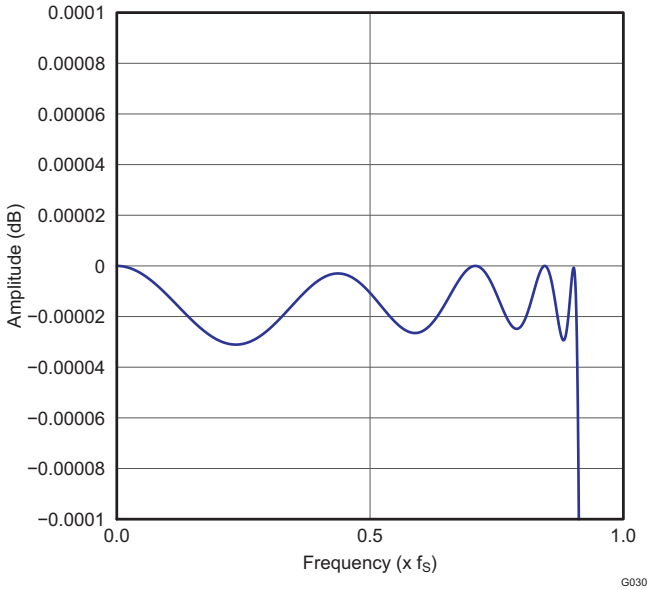


Figure 30. Low latency ×4 Interpolation-Filter Pass-Band Ripple

Table 14. Low-Latency ×2 Interpolation Filter

Parameter	Condition	Value (Typ)	Unit
Filter-gain pass band	0–0.45 f_S	±0.0001	dB
Filter-gain stop band	0.55 f_S–1.455 f_S	–52	dB
Filter-group delay		3.5 / f_S	s

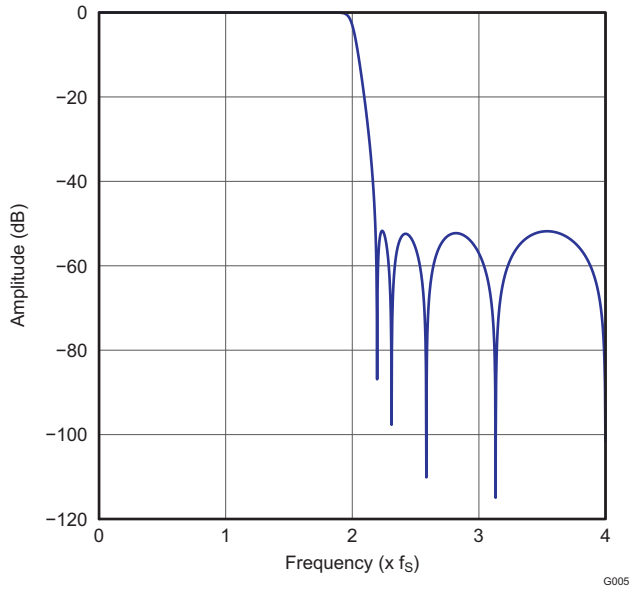


Figure 31. Low-Latency ×2 Interpolation-Filter Frequency Response

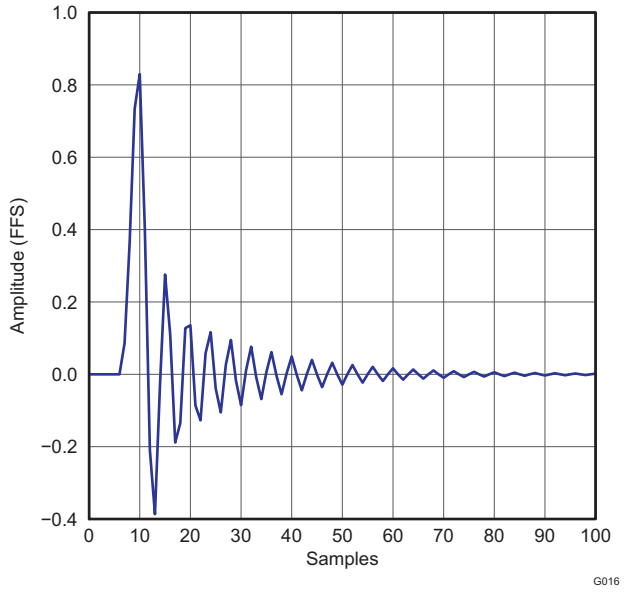


Figure 32. Low-Latency ×2 Interpolation-Filter Impulse Response

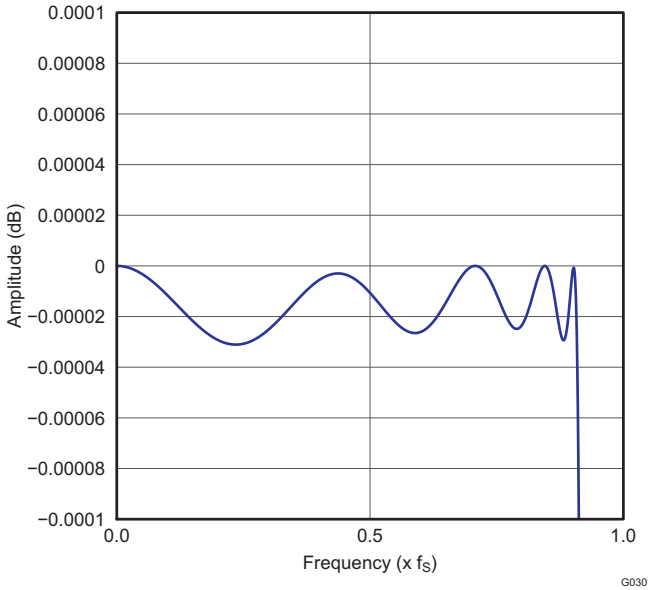


Figure 33. Low-Latency ×2 Interpolation-Filter Pass-Band Ripple

Zero-Data Detect

The PCM510x-Q1 has a zero-data detect function. When the device detects continuous zero data, it enters a full analog-mute condition.

The PCM510x-Q1 counts zero data over 1024 LRCKs (21 ms at 48 kHz) before setting analog mute.

Power-Save Mode

On detection of any kind of clock error (SCK, BCK, and LRCK) or clock halt, the PCM510x-Q1 enters standby mode automatically and powers down the current-segment DAC and line driver.

When BCK and LRCK halt to a low level for more than 1 second, the PCM510x-Q1 enters the power-down mode automatically. Power-down mode includes the negative charge pump and reference circuit power-down in addition to standby.

On application of expected audio clocks (SCK, BCK, LRCK) to the PCM510x-Q1, the device starts its power-up sequence automatically.

XSMT Pin (Soft Mute and Soft Un-Mute)

For external digital control of the PCM510x-Q1, an external digital host must drive the XSMT pin with a specific minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM510x-Q1 requires t_r and t_f times of less than 20 ns. In the majority of applications, this should not be a problem; however, traces with high capacitance may have issues.

When shifting the XSMT pin from high to low (3.3 V to 0 V), a soft digital attenuation ramp starts. Gain steps of –1 dB occur every 1 / f_S from 0 dBFS to –∞. This takes 104 sample periods.

Shifting the XSMT pin from low to high (0 V to 3.3V) starts a soft digital un-mute. Gain steps of 1 dB occur every 1 / f_S from –∞ to 0 dBFS. This takes 104 sample periods.

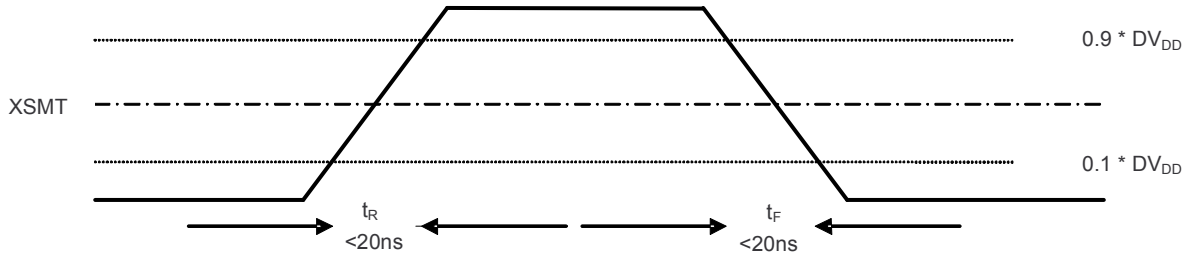


Figure 34. XSMT Timing for Soft Mute and Soft Un-Mute

Table 15. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time (t_r)		20	ns
Fall time (t_F)		20	ns

External Power Sense Undervoltage Protection mode

The XSMT pin can alternatively monitor a system voltage, such as the 24-VDC LCD TV backlight, or 12-VDC system supply, using a potential divider created with two resistors. (See Figure 35.)

- If the XSMT pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage-protection mode. This mode uses two trigger levels.
- When the XSMT pin level reaches 2 V, the soft-mute process begins.
- When the XSMT pin level reaches 1.2 V, analog mute engages, regardless of digital audio level, and analog shutdown begins (for example, DAC circuitry powers down, and so forth).

Figure 36 is a timing diagram that shows this.

NOTE

The XSMT input-pin voltage range is from –0.3 V to DVDD + 0.3 V. Consider the ratio of external resistors within this input range. Any increase in power supply (such as power-supply positive noise or ripple) can pull the XSMT pin higher than DVDD + 0.3 V.

For example, if the PCM510x-Q1 monitors a 12-V input that a voltage divider has divided by 4, then the voltage at XSMT during ideal power supply conditions is 3 V. If the voltage spikes any higher than 14.4 V, then the voltage on XSMT exceeeds 3.6 V (DVDD + 0.3), potentially damaging the device.

Appropriate setting of the divider allows monitoring of any dc voltage.

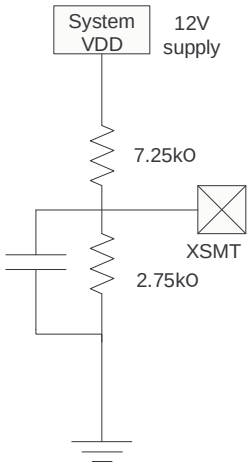


Figure 35. XSMT in External UVP Mode

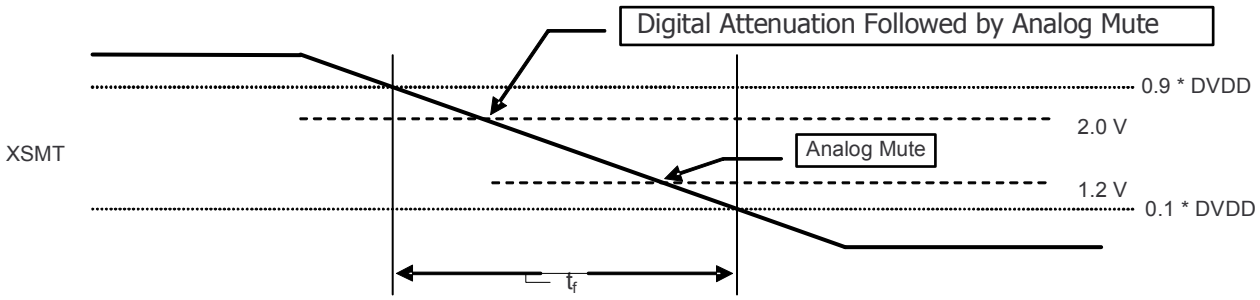


Figure 36. XSMT Timing for Undervoltage Protection

Typical Application Circuits

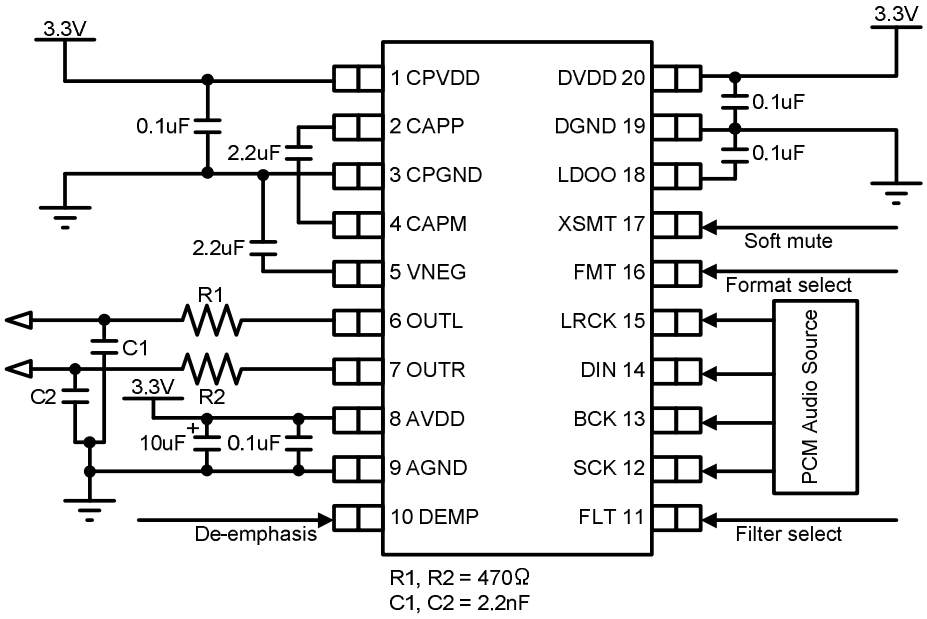


Figure 37. PCM510x-Q1 Standard PCM Audio Operation, 3.3 V

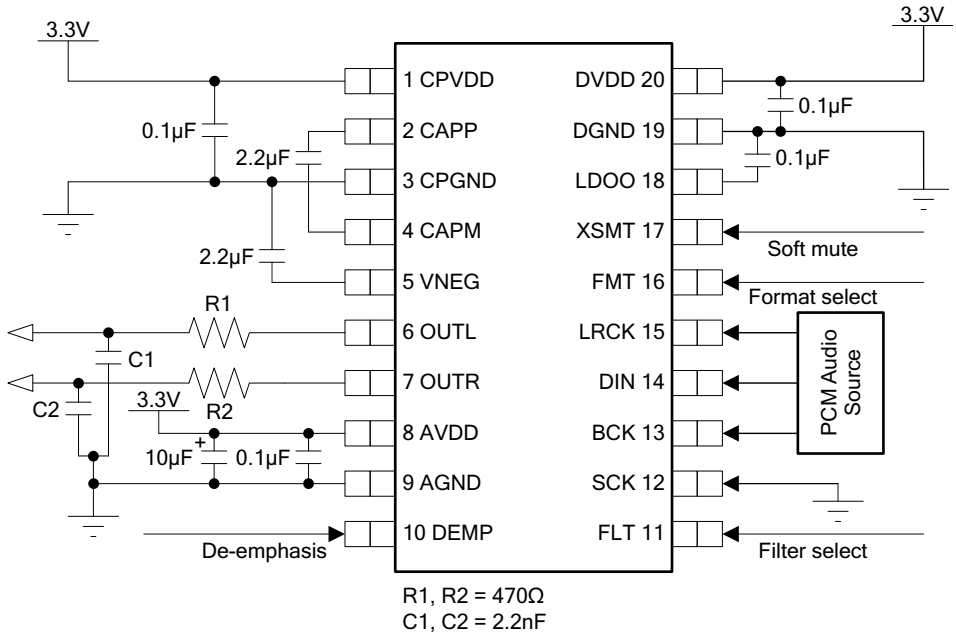


Figure 38. PCM510x-Q1 PLL Operation

Recommended Output Filter for the PCM510x-Q1

The diagram in Figure 39 shows the recommended output filter for the PCM510x-Q1. The new PCM510x-Q1 next-generation current-segment architecture offers excellent out-of-band noise, making a traditional 20-kHz low-pass filter a thing of the past.

The RC settings below offer a –3-dB filter point at 153 kHz (approximately), giving the DAC the ability to reproduce virtually all frequencies through to its maximum sampling rate of 384 kHz.

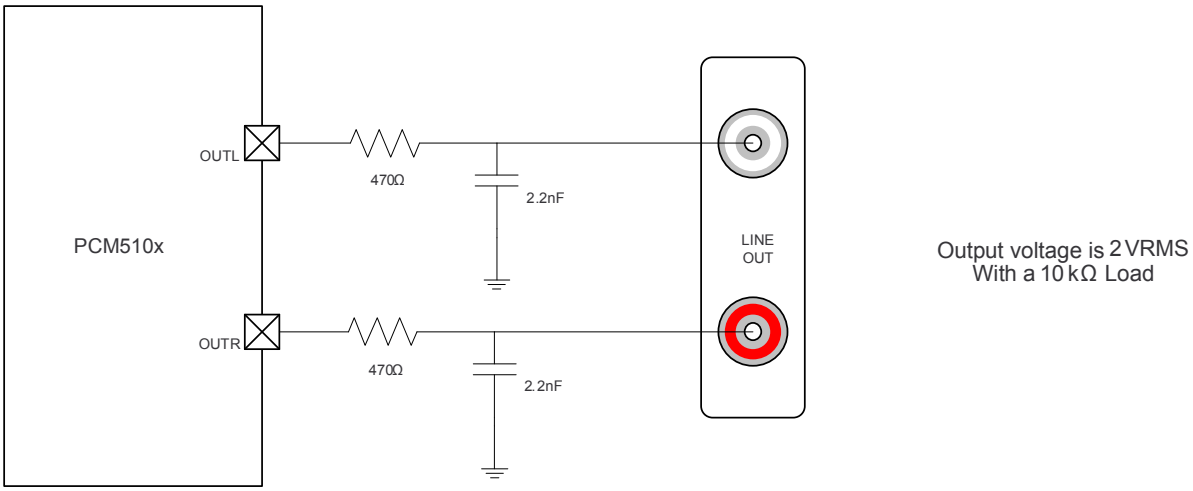


Figure 39. Recommended Low-Pass Output Filter for 10-kΩ Operation

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM5102TPWRQ1	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	PCM5102Q
PCM5102TPWRQ1.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	PCM5102Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF PCM5102-Q1 :

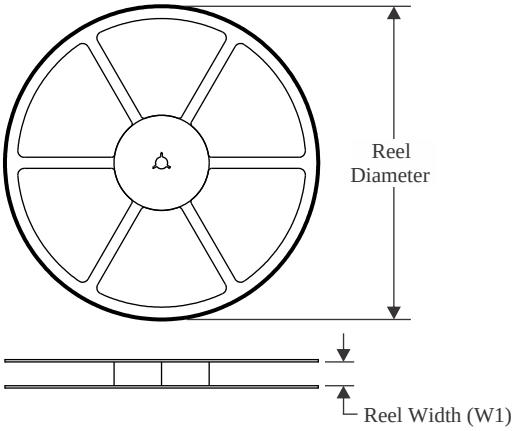
- Catalog : PCM5102

NOTE: Qualified Version Definitions:

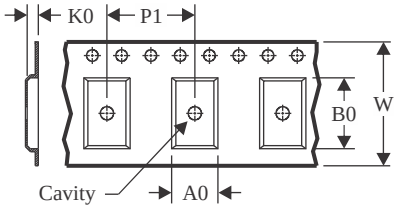
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

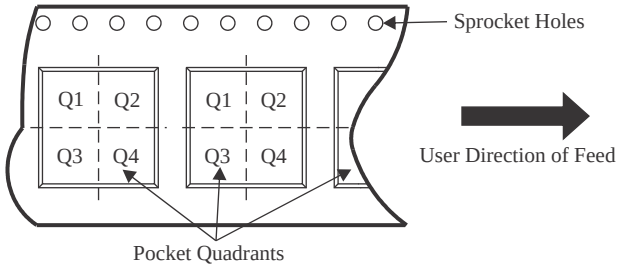


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

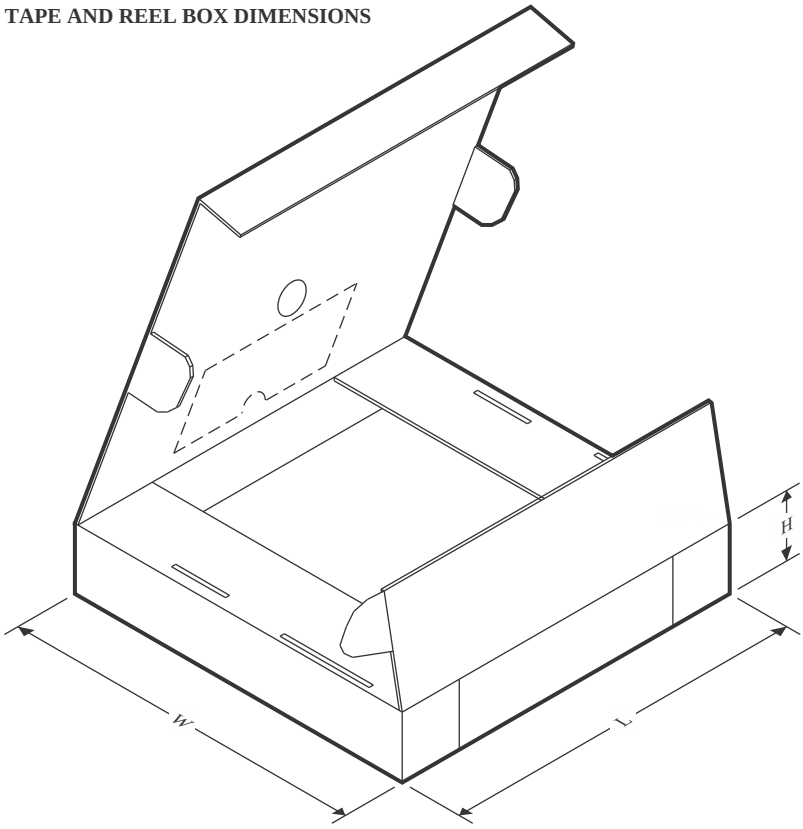
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5102TPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

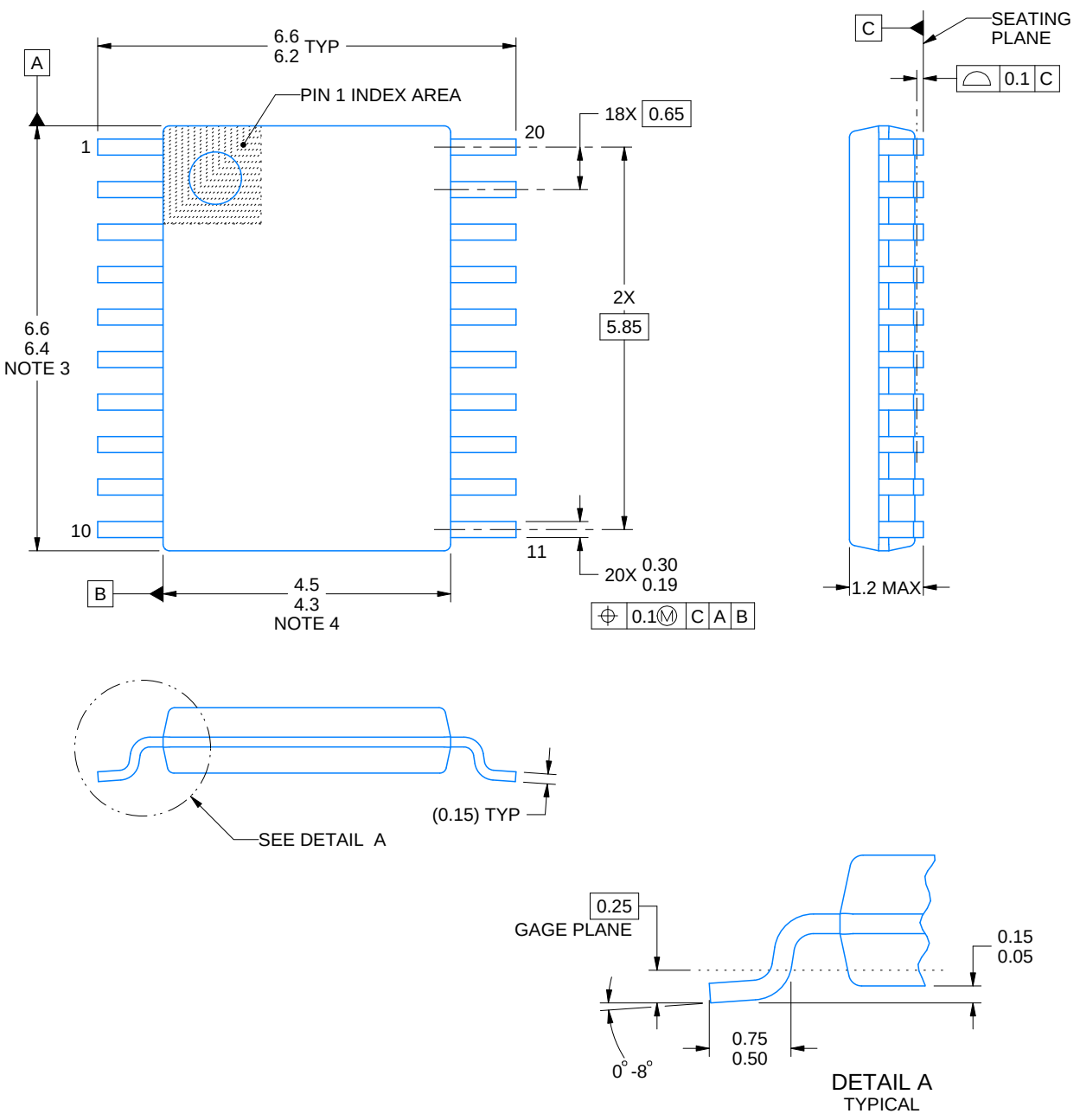
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5102TPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0020A

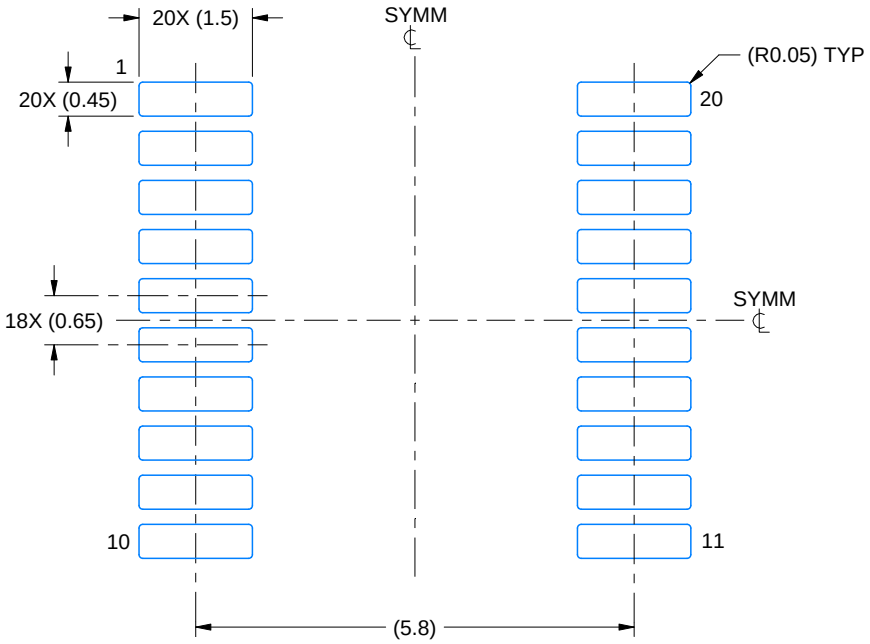
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



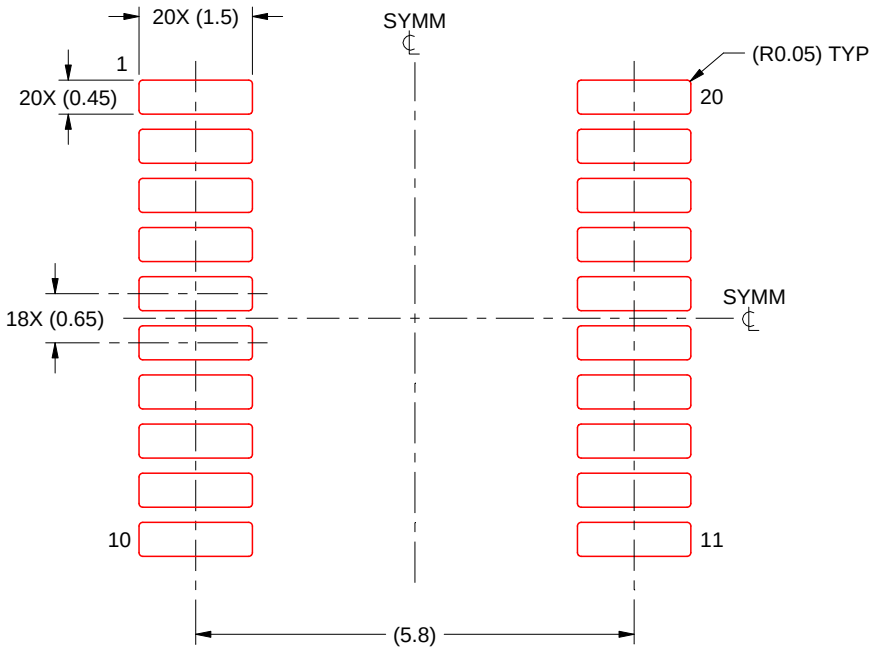
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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