TEXAS INSTRUMENTS

PCA9515B

SCPS232B –MARCH 2012–REVISED MARCH 2016

PCA9515B Dual Bidirectional I^{2}C Bus and SMBus Repeater

1 Features

- Two-Channel Bidirectional Buffers
- I^{2}C Bus and SMBus Compatible
- Support for I^{2}C Standard Mode (100-kHz) and Fast Mode (400-kHz)
- Active-High Repeater-Enable Input
- Open-Drain I^{2}C Input and Output
- 5.5-V Tolerant I^{2}C Input and Output and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode, Fast Mode I^{2}C Devices, and Multiple Masters
- Supports Arbitration and Clock Stretching Across Repeater
- Powered-Off High-Impedance I^{2}C Pins
- Latch-Up Performance Exceeds 100-mA Per JESD 78, Class I
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products with Many I^{2}C Slaves and Long PCB Traces

3 Description

The PCA9515B is a BiCMOS dual bidirectional buffer integrated circuit intended for I^{2}C bus and SMBus applications. The device contains two identical bidirectional open-drain buffer circuits that enables I^{2}C and similar bus systems to be extended (or add slaves) without degrading system performance. The dual bidirectional I^{2}C buffer is operational at 2.3 V to 3.6 V V$_{CC}$.

The PCA9515B buffers both the serial data (SDA) and serial clock (SCL) signals on the I^{2}C bus, while retaining all the operating modes and features of the I^{2}C system. The device allows two buses, of 400-pF bus capacitance, to be connected in an I^{2}C application.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9515B	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
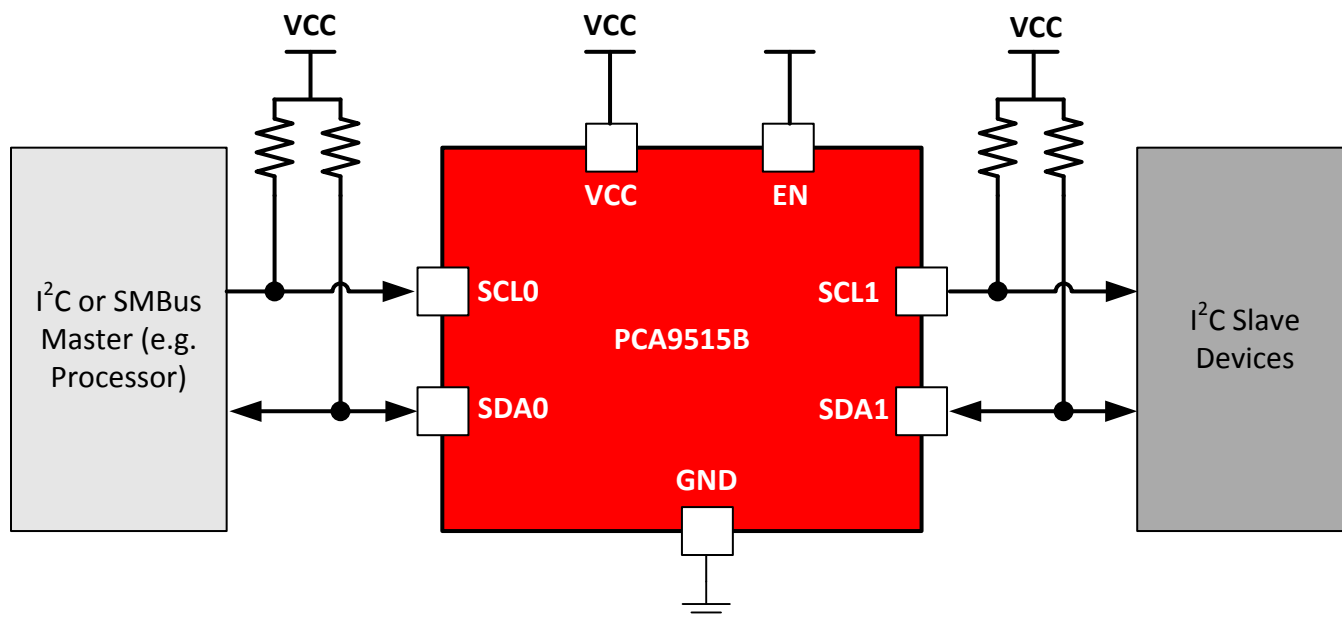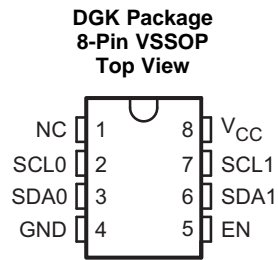
Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B   **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted the ordering information. See POA at the end of the datasheet. 1

Changes from Original (March 2012) to Revision A   **Page**

- Updated the V_{OL} and V_{OL} - V_{ILC} specifications. 5

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View

```
      NC [ 1    8 ] V_CC
    SCL0 [ 2    7 ] SCL1
    SDA0 [ 3    6 ] SDA1
     GND [ 4    5 ] EN
```

NC - No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	No internal connection
2	SCL0	I/O	Serial clock bus 0
3	SDA0	I/O	Serial data bus 0
4	GND	—	Supply ground
5	EN	I	Active-high repeater enable input
6	SDA1	I/O	Serial data bus 1
7	SCL1	I/O	Serial clock bus 1
8	V_{CC}	—	Supply power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Enable input voltage [2]		–0.5	7	V
$V_{I/O}$	I²C bus voltage [2]		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	SDA and SCL inputs	$0.7 \times V_{CC}$	5.5	V
		EN input	2	5.5	
V_{IL} [1]	Low-level input voltage	SDA and SCL inputs	–0.5	$0.3 \times V_{CC}$	V
		EN input	–0.5	0.8	
V_{ILc} [1]	SDA and SCL low-level input voltage contention		–0.5	0.4	V
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V		6	mA
		$V_{CC} = 3$ V		6	
T_A	Operating free-air temperature		–40	85	°C

(1) V_{IL} specification is for the EN input and the first low level seen by the SDAx and SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx and SCLx lines. V_{ILc} must be at least 70 mV below V_{OL}.

6.4 Thermal Information

	THERMAL METRIC[1]	PCA9515B DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	170.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Links: *PCA9515B*

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA		2.3 V to 3.6 V	−1.2			V
V_{OL}	Low-level output voltage	SDAx, SCLx	$I_{OL} = 20$ µA or 6 mA	2.3 V to 3.6 V	0.47	0.52	0.6	V
$V_{OL} - V_{ILc}$	Low-level input voltage below low-level output voltage	SDAx, SCLx	guaranteed by design	2.3 V to 3.6 V		120		mV
I_{CC}	Quiescent supply current		Both channels high, SDAx = SCLx = V_{CC}	2.7 V		0.5	3	mA
				3.6 V		0.5	3	
			Both channels low, SDA0 = SCL0 = GND and SDA1 = SCL1 = open; or SDA0 = SCL0 = open and SDA1 = SCL1 = GND	2.7 V		1	4	
				3.6 V		1	4	
			In contention, SDAx = SCLx = GND	2.7 V		1	4	
				3.6 V		1	4	
I_I	Input current	SDAx, SCLx	$V_I = 3.6$ V	2.3 V to 3.6 V			±1	µA
			$V_I = 0.2$ V				3	
		EN	$V_I = V_{CC}$				±1	
			$V_I = 0.2$ V			−10	−20	
I_{off}	Leakage current	SDAx, SCLx	$V_I = 3.6$ V	EN = L or H	0 V			0.5	µA
			$V_I = $ GND					0.5	
$I_{I(ramp)}$	Leakage current during power up	SDAx, SCLx	$V_I = 3.6$ V	EN = L or H	0 V to 2.3 V			1	µA
C_{in}	Input capacitance	EN	$V_I = 3$ V or GND		3.3 V		7	9	pF
		SDAx, SCLx		EN = H	3.3 V		7	9	

(1) All typical values are at nominal supply voltage ($V_{CC} = 2.5$ V or 3.3 V) and $T_A = 25$°C.

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

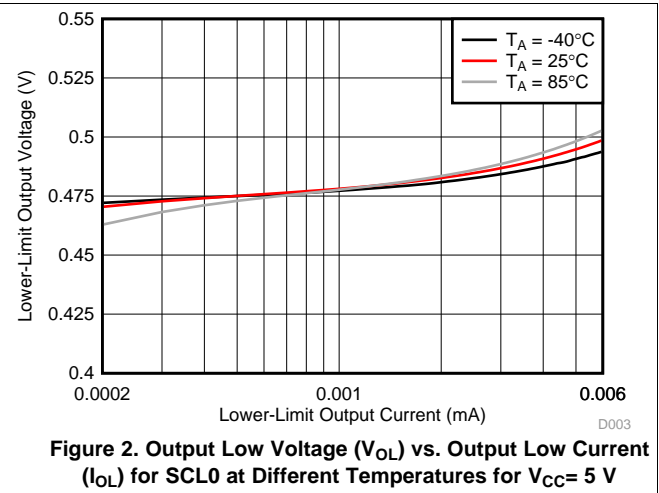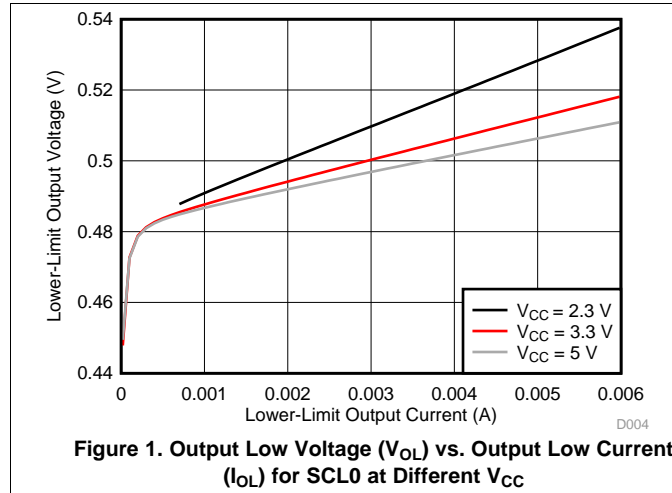|		V_{CC}	MIN	MAX	UNIT
t_{su}	Setup time, EN↑ before Start condition	2.5 V ± 0.2 V	100		ns
		3.3 V ± 0.3 V	100		
t_h	Hold time, EN↓ after Stop condition	2.5 V ± 0.2 V	130		ns
		3.3 V ± 0.3 V	100		

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L ≤ 100$ pF (unless otherwise noted)

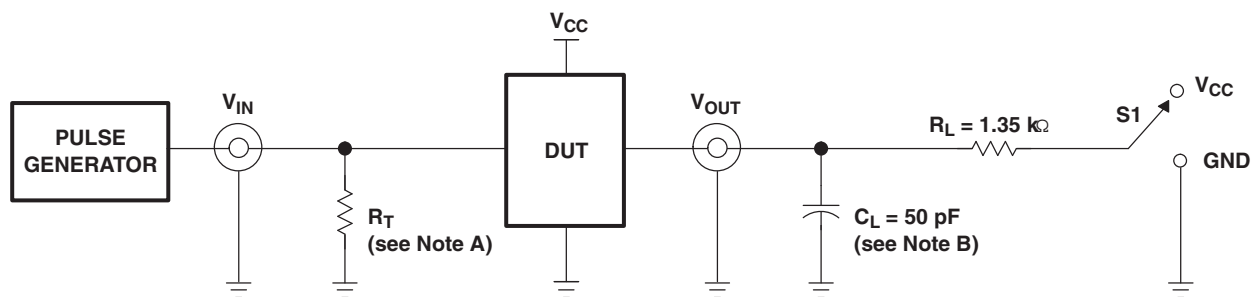| PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP[1]	MAX	UNIT
t_{PZL}	Propagation delay time[2]	SDA0, SCL0 or SDA1, SCL1	SDA1, SCL1 or SDA0, SCL0	2.5 V ± 0.2 V	45	82	130	ns
				3.3 V ± 0.3 V	45	68	120	
t_{PLZ}				2.5 V ± 0.2 V	33	113	190	
				3.3 V ± 0.3 V	33	102	180	
t_{tHL}	Output transition time[2] (SDAx, SCLx)	80%	20%	2.5 V ± 0.2 V		57		ns
				3.3 V ± 0.3 V		58		
t_{tLH}		20%	80%	2.5 V ± 0.2 V		148		
				3.3 V ± 0.3 V		147		

(1) All typical values are at nominal supply voltage ($V_{CC} = 2.5$ V or 3.3 V) and $T_A = 25$°C.
(2) Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
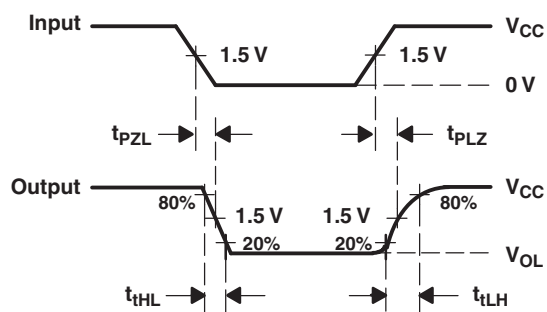
6.8 Typical Characteristics

Figure 1. Output Low Voltage (V_{OL}) vs. Output Low Current (I_{OL}) for SCL0 at Different V_{CC}

Figure 2. Output Low Voltage (V_{OL}) vs. Output Low Current (I_{OL}) for SCL0 at Different Temperatures for V_{CC}= 5 V

Product Folder Links: *PCA9515B*

7 Parameter Measurement Information

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 3. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The PCA9515B is a BiCMOS dual bidirectional buffer integrated circuit intended for I^{2}C bus and SMBus applications. The device contains two identical bidirectional open-drain buffer circuits that enables I^{2}C and similar bus systems to be extended without degrading system performance. This device enables I^{2}C and similar bus systems to be extended (and add more slaves) without degradation of performance. The dual bidirectional I^{2}C buffer is operational at 2.3 V to 3.6 V V$_{CC}$.

The PCA9515B buffers both the serial data (SDA) and serial clock (SCL) signals on the I^{2}C bus, while retaining all the operating modes and features of the I^{2}C system. The device allows two buses, of 400-pF bus capacitance, to be connected in an I^{2}C application.

The I^{2}C bus capacitance limit of 400 pF restricts the number of slave devices and bus length. Using the PCA9515B, a system designer can capacitively isolate two halves of a bus, thus accommodating more I^{2}C devices and longer trace lengths.

The PCA9515B has an active-high enable (EN) input with an internal pull-up. This allows users to select when the repeater is active and isolate malfunctioning slaves on power-up reset. States should never be changed during an I^{2}C operation. Disabling during a bus operation will hang the bus and enabling part way through a bus cycle may confuse the I^{2}C parts being enabled. The EN input should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

The PCA9515B can also be used to operate two buses, one at 5 V interface levels and the other at 3.3 V interface levels. The buses may also function at 400-kHz or 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated if the operation of the 400-kHz bus is required. If the master is running at 400-kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

The low level outputs for each internal buffer are approximately 0.5 V; however, the input voltage of each internal buffer must be 70 mV or more below the low level output when the output is driven low internally. This prevents a lockup condition from occurring when the input low condition is released.

Two or more PCA9515B devices cannot be used in series. Since there is no direction pin, different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low, applied at the input of a PCA9515B, is propagated as a buffered low with a higher value on the enabled outputs. When this buffered low is applied to another PCA9515B-type device in series, the second device does not recognize it as a valid low and does not propagate it as a buffered low.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until V$_{CC}$ is at a valid level (V$_{CC}$ = 2.3 V).

As with the standard I^{2}C system, pullup resistors are required to provide the logic high levels on the buffered bus. The PCA9515B has standard open-collector configuration of the I^{2}C bus. The size of the pullup resistors depend on the system; however, each side of the repeater must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I^{2}C devices in addition to SMBus devices. Standard Mode I^{2}C devices only specify a 3 mA termination current in a generic I^{2}C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.
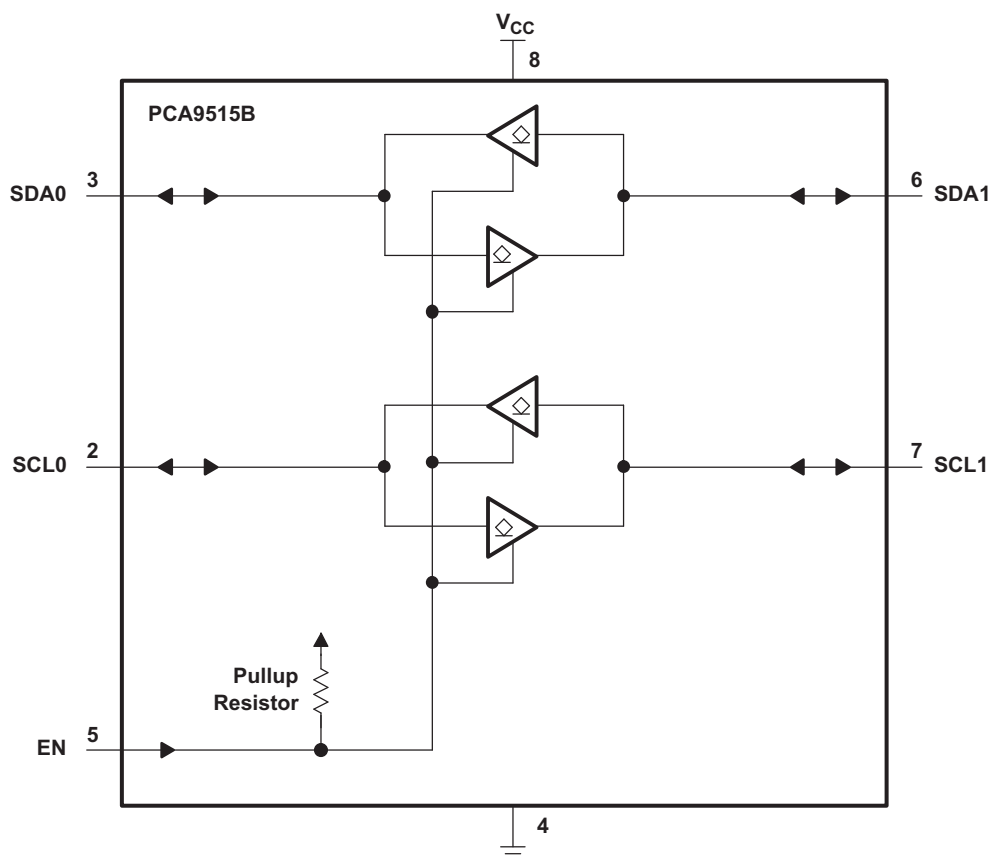
8.2 Functional Block Diagram

Figure 4. Logic Diagram (Poisitve Logic)

8.3 Feature Description

8.3.1 Two-Channel Bidirectional Buffer

The PCA9515B is a two-channel bidirectional buffer for open-drain applications like I^2C and SMBus.

8.3.2 Bidirectional Voltage-Level Translation

The PCA9515B allows bidirectional voltage-level translation (up-translation and down-translation) between low voltages (down to 2.3 V) and higher voltages (up to 5.5 V).

8.3.3 Active-High Enable Input

The PCA9515B has an active-high enable (EN) input with an internal pull-up to V_{CC}. The enable input needs to be pulled to GND to disable the PCA9515B and isolate the I^2C buses. Pulling-up the enable pin or floating the enable pin causes the PCA9515B to turn on and buffer the I^2C bus.

8.4 Device Functional Modes

The PCA9515B has an active-high enable (EN) input with an internal pull-up to V_{CC}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I^{2}C operation, because disabling during a bus operation my hang the bus, and enabling part way through the bus cycles could confuse the I^{2}C parts being enabled. The EN input should only change state when the global bus and repeater port are in the idle state to prevent system failures. Table 1 lists the PCA9515B functions.

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDA0 = SDA1, SCL0 = SCL1

Product Folder Links: *PCA9515B*

9   Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1   Application Information

The PCA9515B is typically used to buffer an I²C signal, isolating capacitance from two sides of the bus. This allows for longer traces and cables, and a more robust I²C communication. *Typical Application* section describes how the PCA9515B may be used to isolate a standard mode and fast mode I²C bus, to allow for faster communications when required, but maintaining compatibility with the slower standard mode slave device.

It is critical to keep the V_{OL} and V_{IL} requirements in mind when designing with buffers, especially when using multiple buffers/translators on the same node. Care must be taken to not violate the V_{IL} requirement of a buffer, otherwise I²C communication errors will occur. An example of this would be a buffer with a V_{OL} of ~0.5 V, and a device requires a V_{IL} of less than 0.4 V. Such a connection would result in the slave device being unable to recognize the output low signal as a valid low.

9.2   Typical Application

A typical application is shown in Figure 5. In this example, the system master is running on a 3.3 V I²C bus, while the slave is connected to a 5-V bus. Both buses run at 100 kHz, unless the slave bus is isolated. If the slave bus is isolated (by pulling the EN pin low), the master bus can run at 400 kHz. Master devices can be placed on either bus, the PCA9515B does not care which side the master is on. Decoupling capacitors are required, but are not shown in Figure 5 for simplicity.
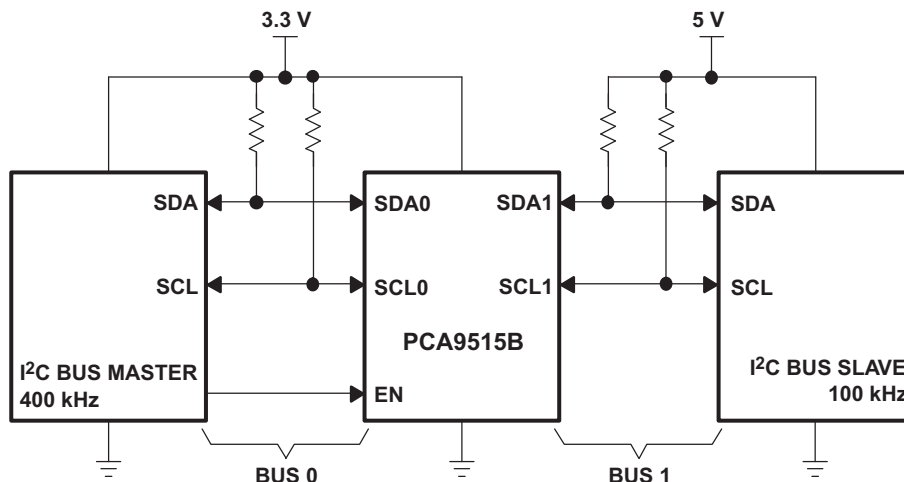

Figure 5. Typical Application

9.2.1   Design Requirements

Table 2 lists the design requirements.

Table 2. Design Requirements

PARAMETER	VALUE
Input-side I²C signal	3.3 V
Output-side I²C signal	5 V

Product Folder Links: *PCA9515B*

9.2.2 Detailed Design Procedure

The PCA9515B is 5.5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages. When one side of the PCA9515B is pulled low by a device on the I²C bus, a CMOS hysteresis-type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side also to go low. The side driven low by the PCA9515B typically is at V_{OL} = 0.5 V.

Figure 6 and Figure 7 show the waveforms that are seen in a typical application. If the bus master in Figure 5 writes to the slave through the PCA9515B, Bus 0 has the waveform shown in Figure 6. The waveform looks like a normal I²C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515B. Because the V_{OL} of the PCA9515B typically is around 0.5 V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

On the Bus 1 side of the PCA9515B, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PCA9515B. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in the example.
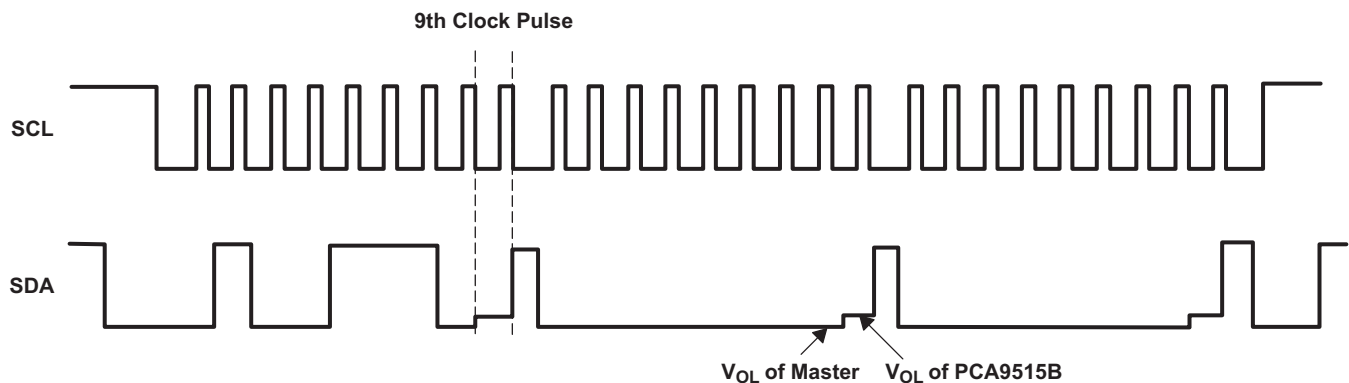
9.2.3 Application Curves

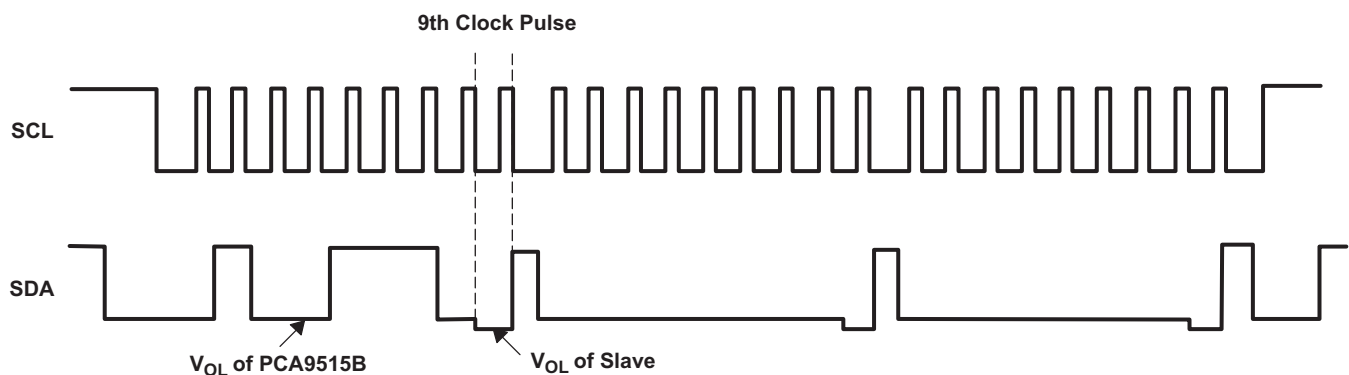**Figure 6. Bus 0 Waveforms**

Figure 7. Bus 1 Waveforms

10 Power Supply Recommendations

For V_{CC}, a 2.3 V to 3.6 V power supply is required. Standard decoupling capacitors are recommended. These capacitors typically range from 0.1 µF to 1 µF, but the ideal capacitance depends on the amount of noise from the power supply.

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCA9515B, common PCB layout practices should be followed. In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a small capacitor to filter out high-frequency ripple. These decoupling capacitors should be placed as close to the V_{CC} pin of PCA9515B as possible.

The layout example shown in Figure 8 shows a 4 layer board, which is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and one to power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer on the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board. This routing and via is not necessary if V_{CC} and GND are both full planes as opposed to the partial planes depicted.
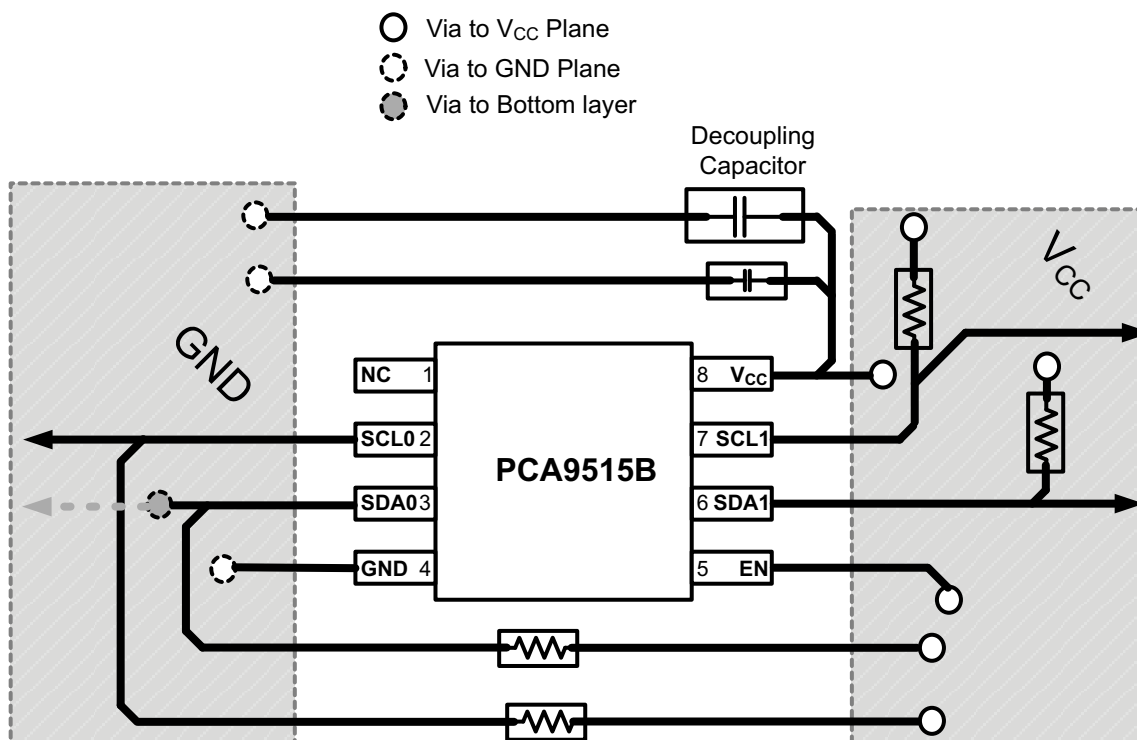
11.2 Layout Example

Figure 8. Layout Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- *I2C Bus Pullup Resistor Calculation*, SLVA689
- *Maximum Clock Frequency of I2C Bus Using Repeaters*, SLVA695
- *Introduction to Logic*, SLVA700
- *Understanding the I2C Bus*, SLVA704

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9515BDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7SE, 7SF)
PCA9515BDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7SE, 7SF)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9515BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9515BDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

5.05
4.75 TYP

PIN 1 INDEX AREA

A

1

4

3.1
2.9
NOTE 3

8

5

B

3.1
2.9
NOTE 4

6X ⌴0.65⌴

2X
⌴1.95⌴

8X 0.38
0.25

⊕ 0.13Ⓜ C A B

C

⌒ 0.1 C

SEATING
PLANE

0.23
0.13

SEE DETAIL A

0.25
GAGE PLANE

1.1 MAX

0°-8°

0.7
0.4

0.15
0.05

DETAIL A
TYPICAL

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PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

DGK0008A

SYMM

8X (1.4)

(R0.05) TYP

8X (0.45)   1

8

SYMM

6X (0.65)

4

5

SEE DETAILS

(4.4)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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