TEXAS INSTRUMENTS

SCPS139E – JANUARY 2006 – REVISED JUNE 2014

PCA6107 Remote 8-Bit I^{2}C and SMBus Low-power I/O Expander With Interrupt Output, Reset, and Configuration Registers

1 Features

- Low Standby Current Consumption of 1 μA Max
- I^{2}C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Active-Low Reset Input
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I^{2}C Bus
- Three Hardware Address Pins Allow for Use of up to Eight Devices on the I^{2}C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- High-Impedance Open Drain on P0
- Power Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 8-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL) and serial data (SDA)].

The PCA6107 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

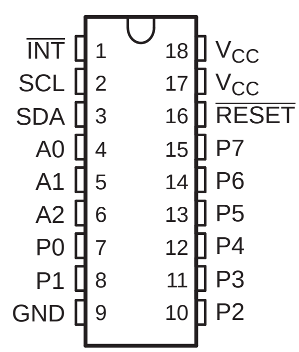
The system master can reset the PCA6107 in the event of a timeout or other improper operation by asserting a low in the active-low reset ($\overline{\text{RESET}}$) input. The power-on reset puts the registers in their default states and initializes the I^{2}C/SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset/initialization to occur without depowering the part.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA6424	SOIC (18)	11.50 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DW PACKAGE (TOP VIEW)



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3 Revision History

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• Added $\overline{\text{RESET}}$ Errata section.	16
• Added Interrupt Errata section.	17
• Power-On Reset Errata section.	25

4 Description (Continued)

The PCA6107 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

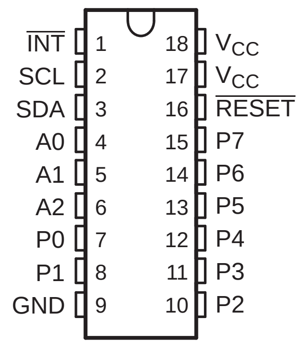
$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the PCA6107 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption and a high-impedance open-drain output pin, P0.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address, allowing up to eight devices to share the same I^2C bus or SMBus.

5 Pin Configuration And Functions

DW PACKAGE
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	$\overline{\text{INT}}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
3	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
4	A0	Address input. Connect directly to V_{CC} or ground.
5	A1	Address input. Connect directly to V_{CC} or ground.
6	A2	Address input. Connect directly to V_{CC} or ground.
7	P0	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
8	P1	P-port input/output. Push-pull design structure.
9	GND	Ground
10	P2	P-port input/output. Push-pull design structure.
11	P3	P-port input/output. Push-pull design structure.
12	P4	P-port input/output. Push-pull design structure.
13	P5	P-port input/output. Push-pull design structure.
14	P6	P-port input/output. Push-pull design structure.
15	P7	P-port input/output. Push-pull design structure.
16	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
17	V_{CC}	Supply voltage
18	V_{CC}	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range[2]		–0.5	6	V
V_O	Output voltage range[2]		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current, P7–P1	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance[3]			73	°C/W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P7–P0, $\overline{\text{RESET}}$	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A2–A0, P7–P0, $\overline{\text{RESET}}$	–0.5	0.8	
I_{OH}	High-level output current	P7-P1		–10	mA
I_{OL}	Low-level output current	P7-P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.65	2.1	V
V_{OH}	P-port high-level output voltage[(2)]	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	3			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.5			
			3 V	2.5			
			4.5 V	3			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3			mA
	P port[(3)]	V_{OL} = 0.5 V	2.3 V to 5.5 V	8	20		
		V_{OL} = 0.55 V		8	20		
		V_{OL} = 0.7 V		10	24		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3			
I_{OH}	P port, except for P0[(3)]	$V_{OH} = V_{CC}$ – 0.4 V	2.3 V to 5.5 V	–4			mA
	P0[(3)]	V_{OH} = 4.6 V	4.6 V to 5.5 V			1	μA
		V_{OH} = 3.3 V	3.3 V to 5.5 V			1	
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μA
	A2–A0, $\overline{RESET}$					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	μA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			1	μA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	5.5 V		19	25	μA
			3.6 V		12	22	
			2.7 V		8	20	
		$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 100 kHz	5.5 V		1.5	5	
			3.6 V		1	4	
			2.7 V		0.6	3	
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz	5.5 V		0.25	1	
			3.6 V		0.25	0.9	
			2.7 V		0.2	0.8	
ΔI_{CC}	Additional current in Standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			0.2	mA
		Every LED I/O at V_I = 4.3 V, f_{SCL} = 0 kHz	5.5 V			0.4	
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	6	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	8	pF
	P port				7.5	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P1) must be limited to a maximum current of 200 mA.
(3) The total current sourced by all I/Os must be limited to 85 mA per bit.

6.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 13)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}	I²C spike time		50		50	ns
t_{sds}	I²C serial data setup time	250		100		ns
t_{sdh}	I²C serial data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		µs
t_{sps}	I²C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		0.9	µs
C_b	I²C bus capacitive load		400		400	pF

(1) C_b = total capacitance of one bus line in pF

6.6 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 16)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_W	Reset pulse duration	16		16		ns
t_{REC}	Reset recovery time	0		0		ns
t_{RESET}	Time to reset (1)	400		400		ns

(1) The PCA6107 requires a minimum of 400 ns to be reset.

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 13)

PARAMETER		FROM	TO	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P0		250		250	ns
		SCL	P1–P7		200		200	
t_{ps}	Input data setup time	P port	SCL	0		0		ns
t_{ph}	Input data hold time	P port	SCL	200		200		ns

6.8 Typical Characteristics

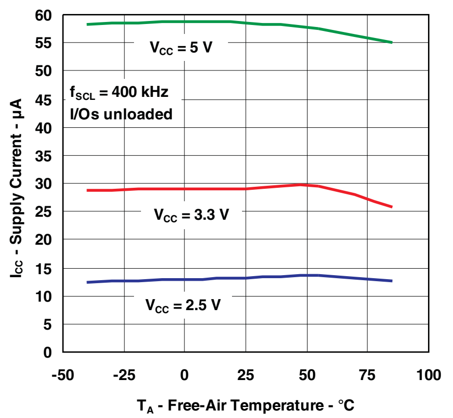


Figure 1. Supply Current vs Temperature

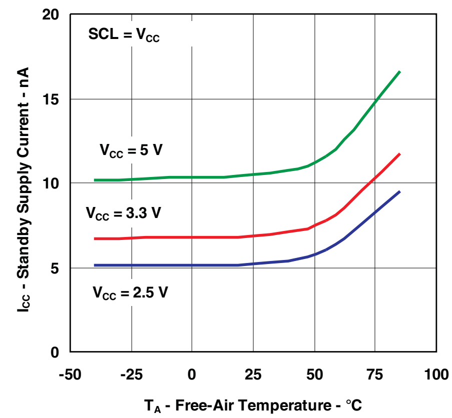


Figure 2. Standby Supply Current vs Temperature

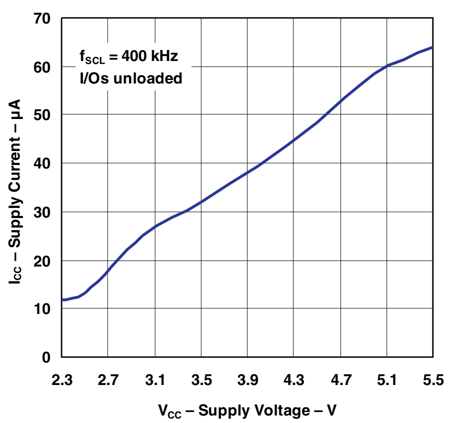


Figure 3. Supply Current vs Supply Voltage

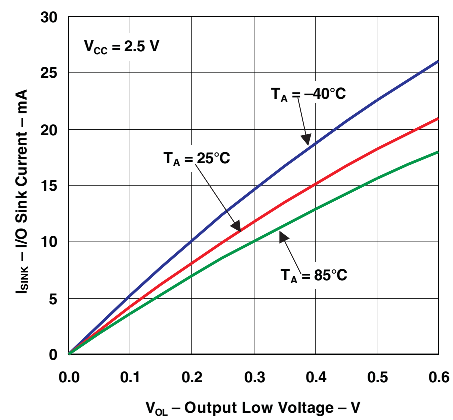


Figure 4. I/O Sink Current vs Output Low Voltage

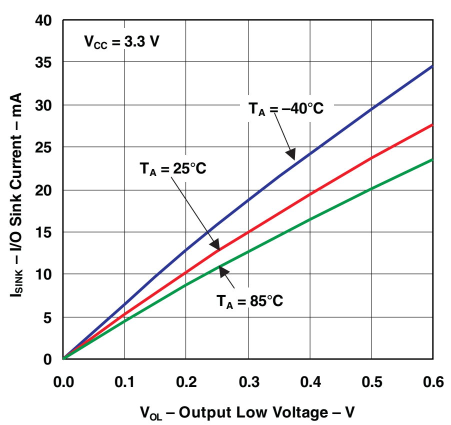


Figure 5. I/O Sink Current vs Output Low Voltage

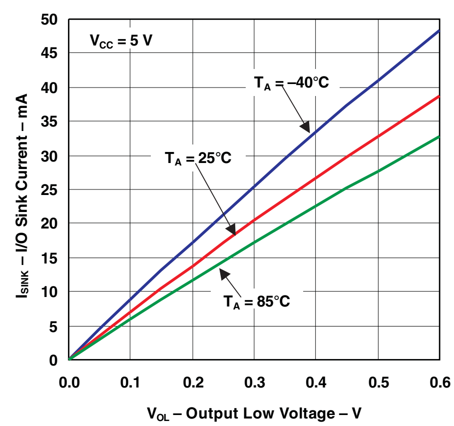


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

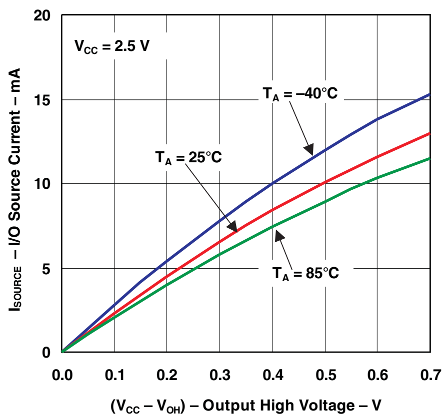


Figure 7. I/O Source Current vs Output High Voltage (P7–P1)

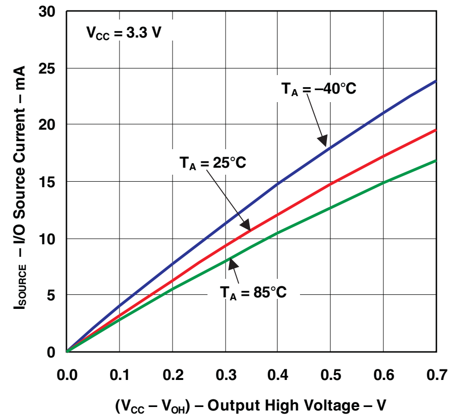


Figure 8. I/O Source Current vs Output High Voltage (P7–P1)

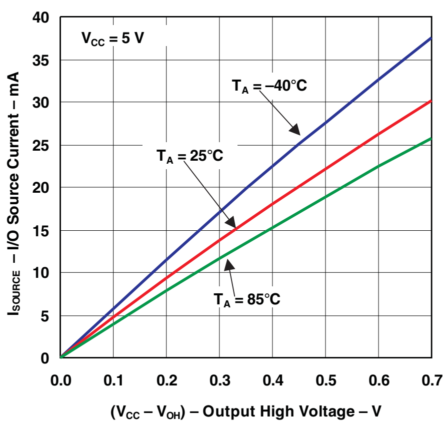


Figure 9. I/O Source Current vs Output High Voltage (P7–P1)

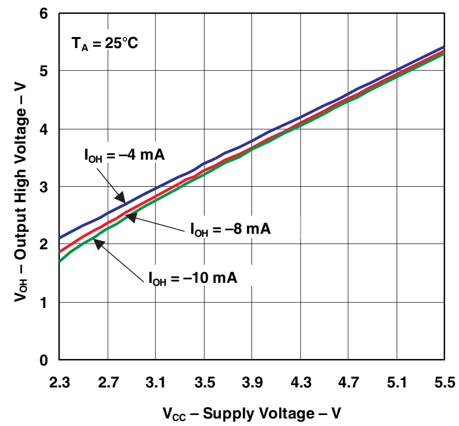


Figure 10. Output High Voltage vs Supply Voltage (P7–P1)

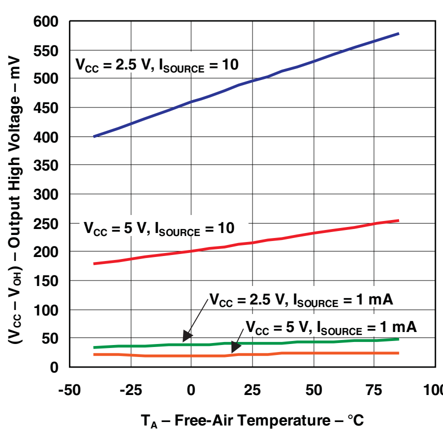


Figure 11. Output High Voltage vs Temperature (P7–P1)

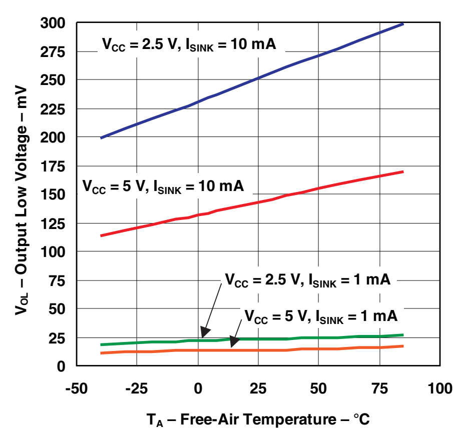
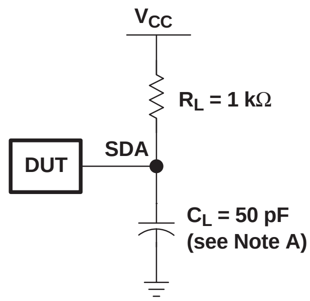
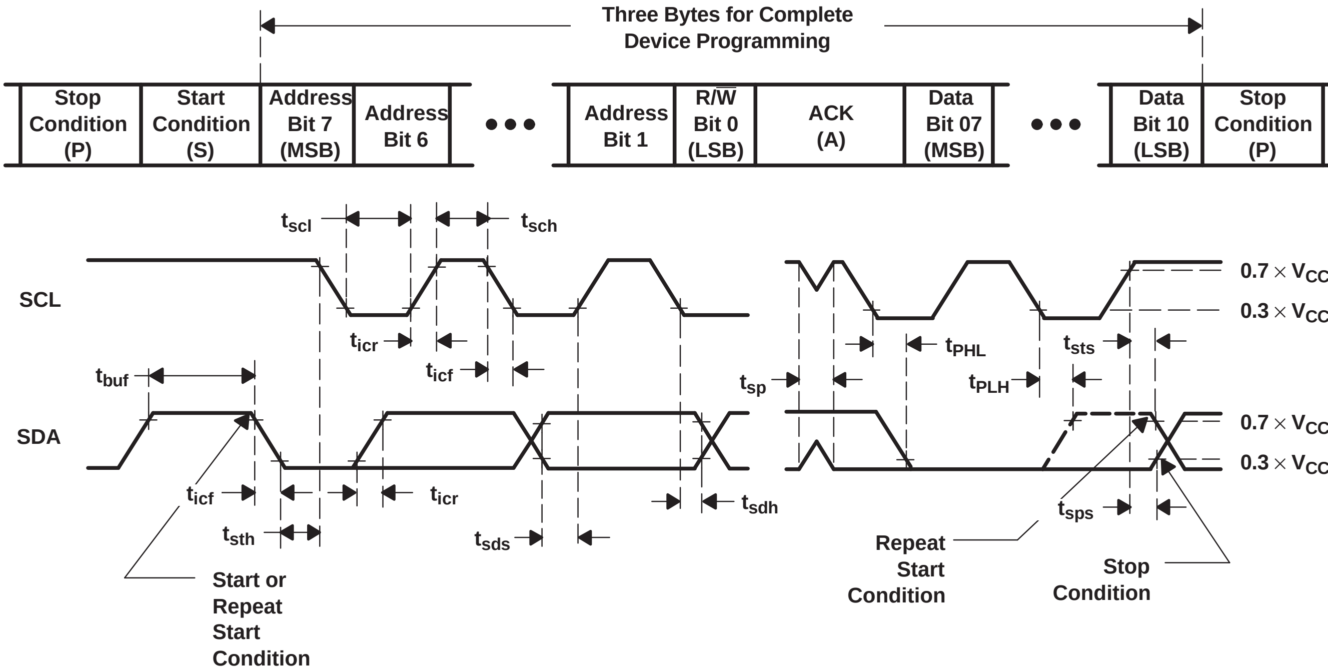


Figure 12. Output Low Voltage vs Temperature

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

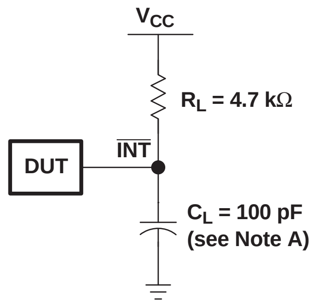
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

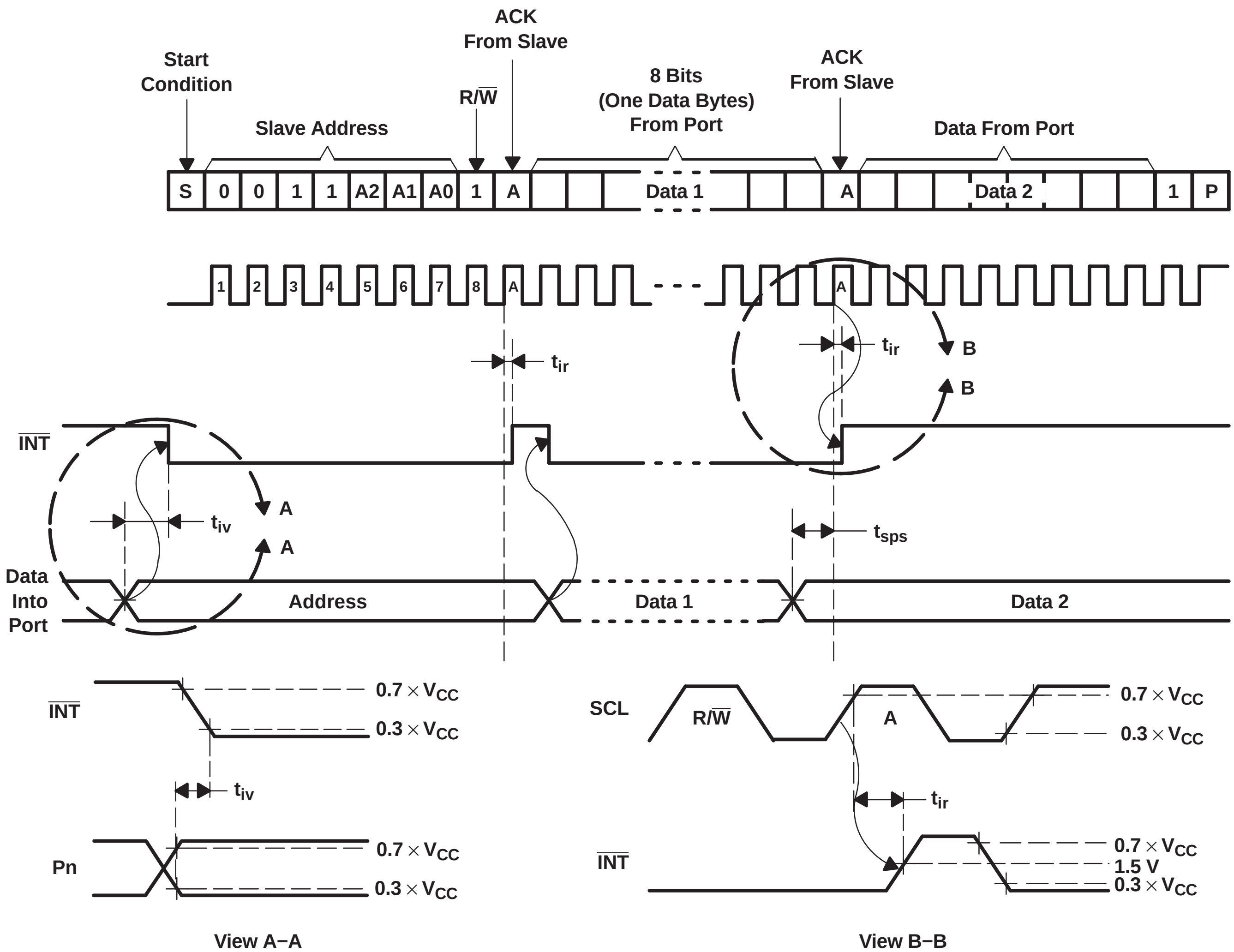
C. All parameters and waveforms are not applicable to all devices.

Figure 13. I^2C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



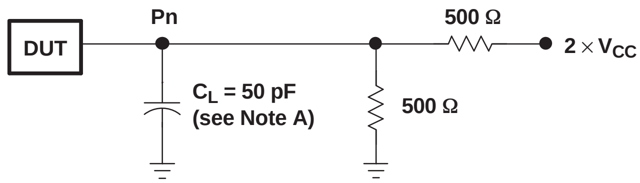
A. C_L includes probe and jig capacitance.

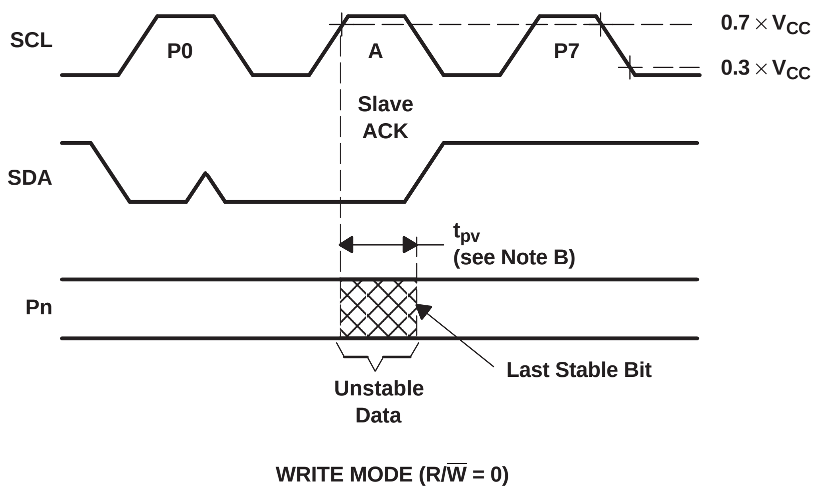
B. All inputs are supplied by generators having the following characteristics: PRR = 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

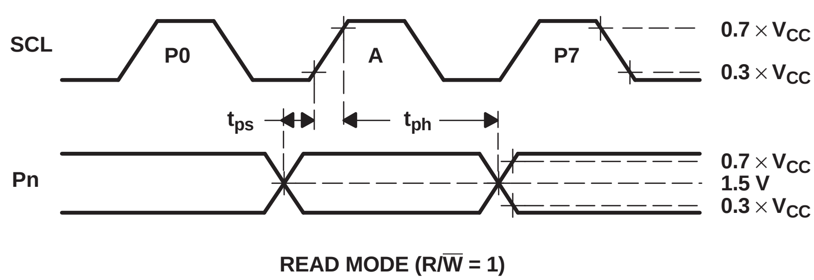
C. All parameters and waveforms are not applicable to all devices.

Figure 14. Interrupt Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)







A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (P_n) output.

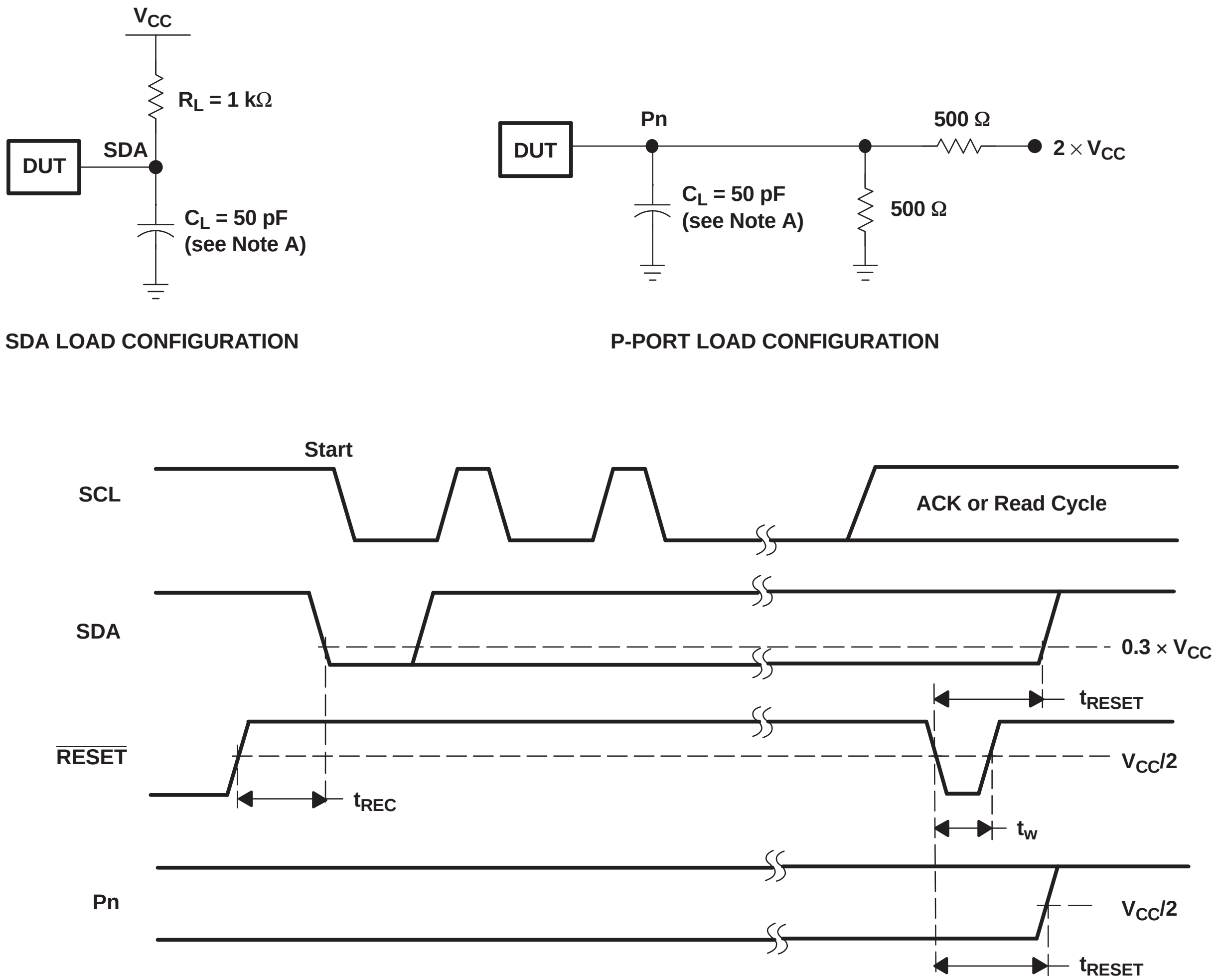
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 15. P-Port Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)

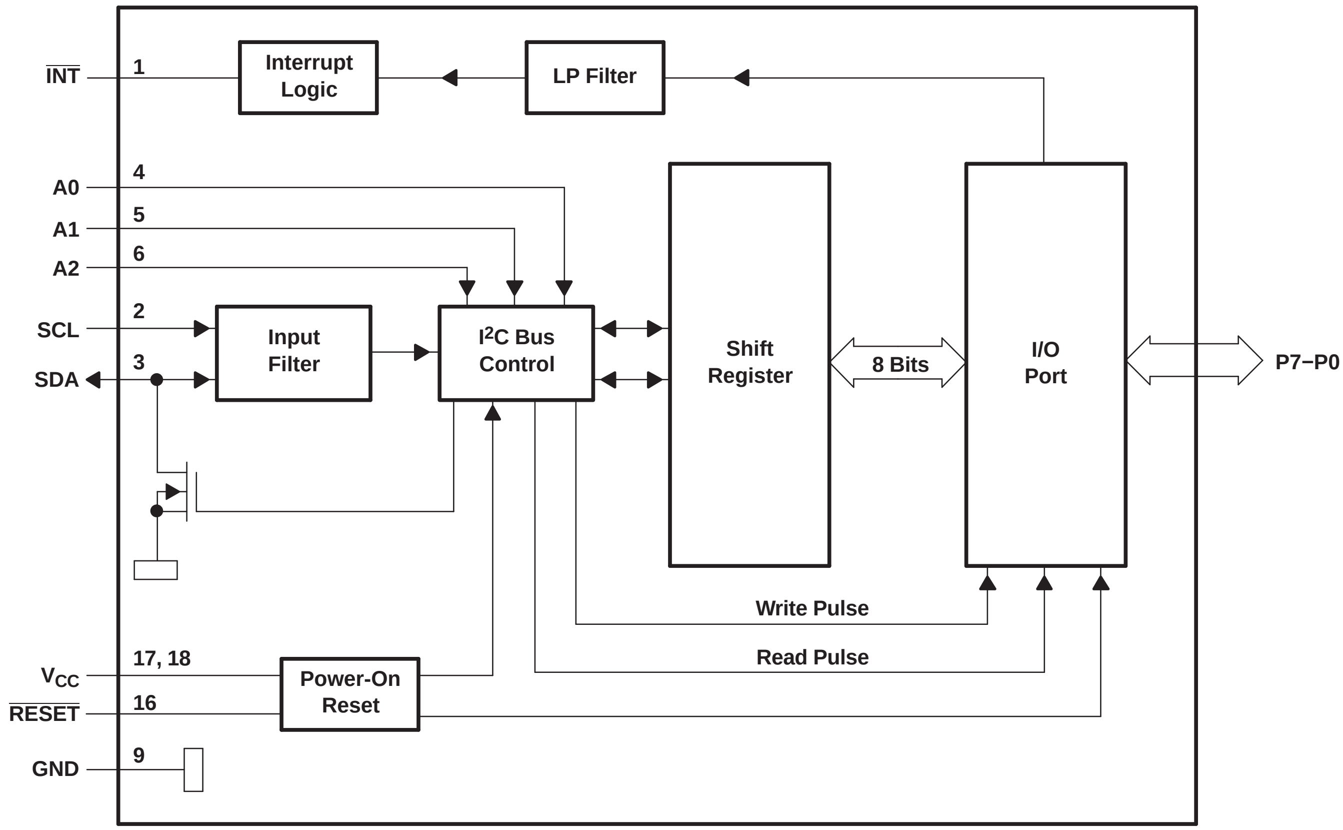


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. I/Os are configured as inputs.
D. All parameters and waveforms are not applicable to all devices.

Figure 16. Reset Load Circuits And Voltage Waveforms

8 Detailed Description

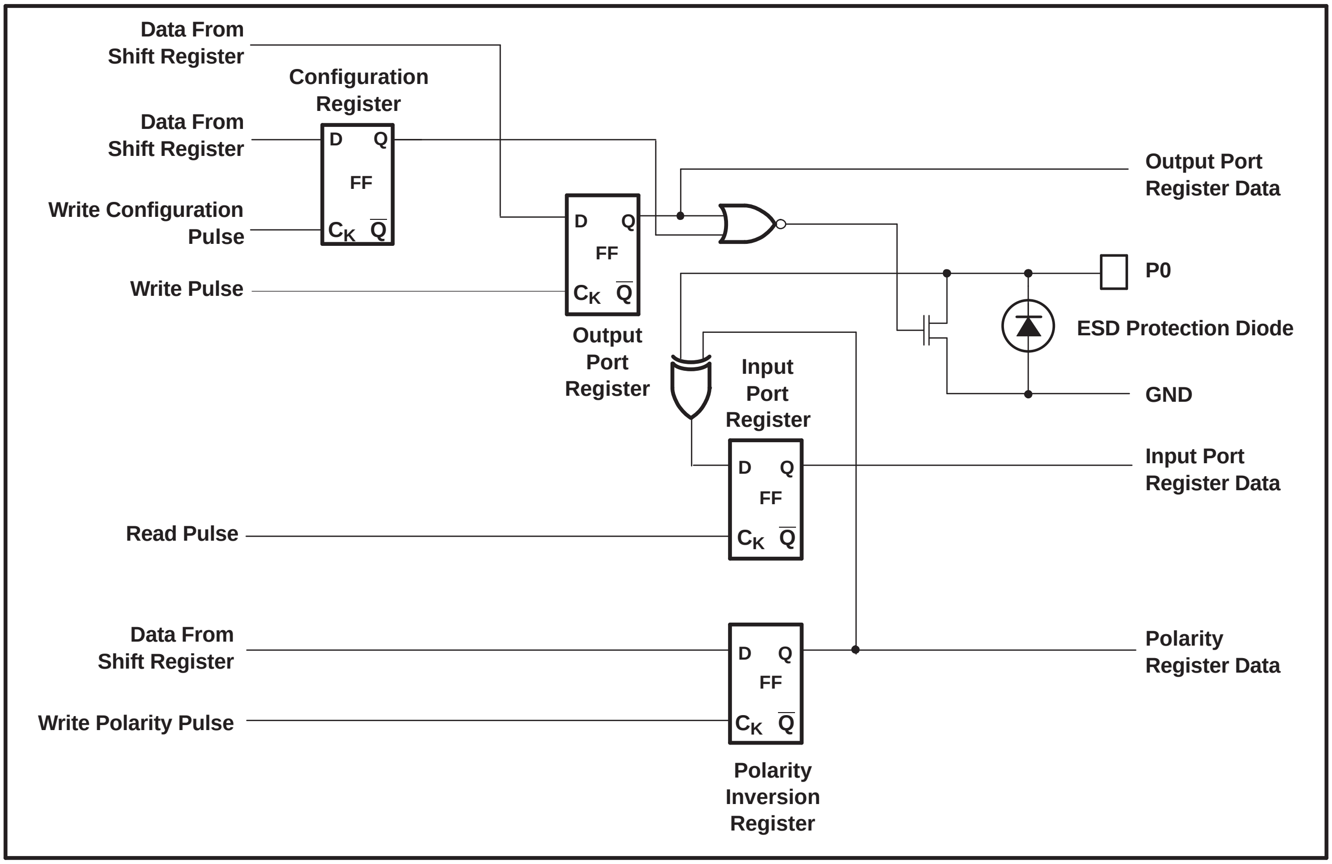
8.1 Functional Block Diagram



A. All I/Os are set to inputs at reset.

Figure 17. Logic Diagram (Positive Logic)

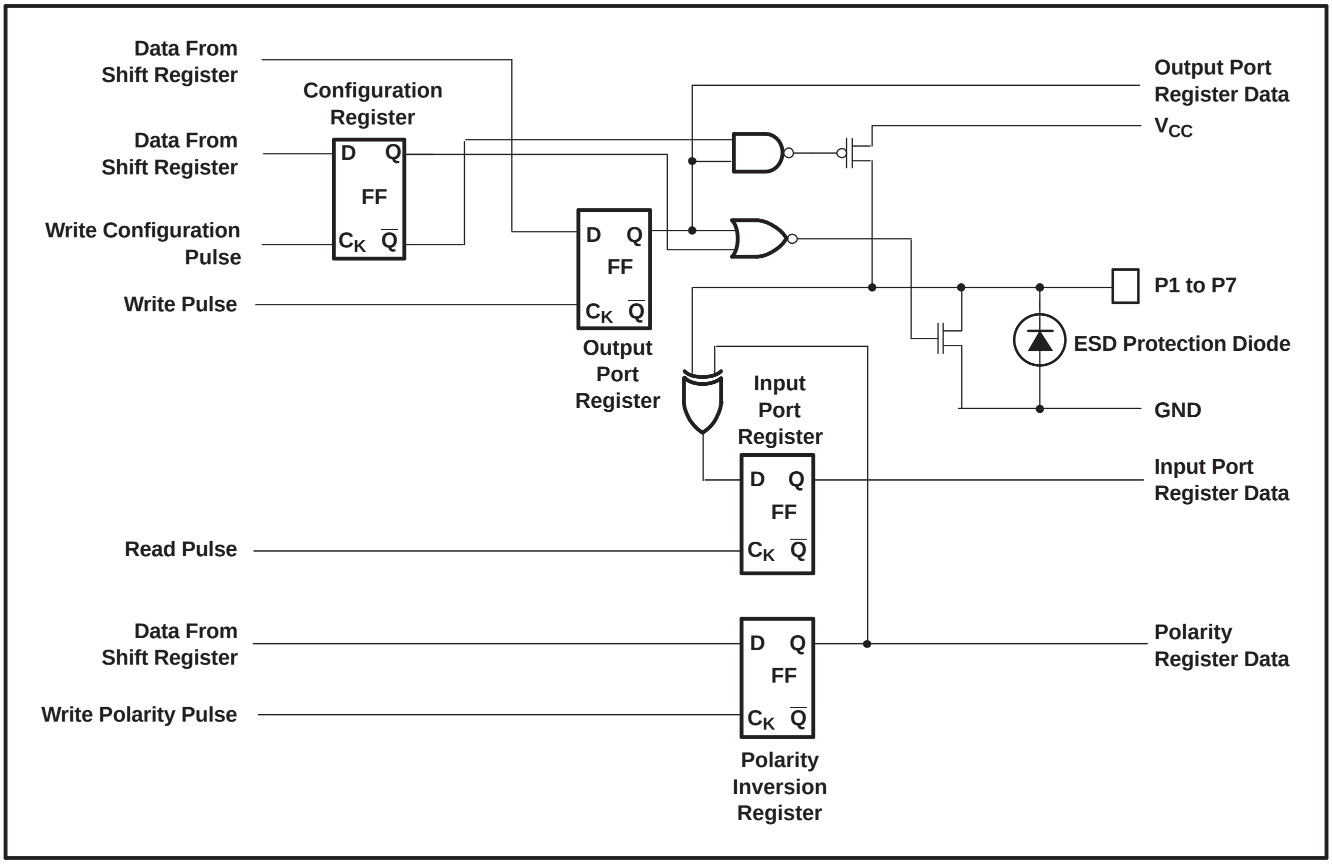
Functional Block Diagram (continued)



A. On power up or reset, all registers return to default values.

Figure 18. Simplified Schematic Of P0

Functional Block Diagram (continued)



A. On power up or reset, all registers return to default values.

Figure 19. Simplified Schematic Of P1 To P7

8.2 Device Functional Modes

8.2.1 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA6107 registers and I^2C/SMBus state machine are held in their default states until the $\overline{\text{RESET}}$ input is again high. This input requires a pullup resistor to V_{CC}, if no active connection is used.

8.2.1.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current will flow from $\overline{\text{RESET}}$ pin to VCC pin.

System Impact

VCC will be pulled above its regular voltage level

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC

8.2.2 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA6107 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the PCA6107 registers and I^2C/SMBus state machine initializes to their default states. After that, V_{CC} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle. The $\overline{\text{RESET}}$ input can be asserted to reset the system, while keeping the V_{CC} at its operating level.

Refer to the *Power-On Reset Errata* section.

8.2.3 Interrupt ($\overline{\text{INT}}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{\text{INT}}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

Device Functional Modes (continued)

8.2.3.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^{2}C command byte (register pointer) written to the device was 00h.

> **NOTE**
> This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^{2}C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA6107 device or before reading from another slave device.

> **NOTE**
> Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I^{2}C Interface

The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^{2}C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 20). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and the Stop conditions.

On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 21).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 20).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 22). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Programming (continued)

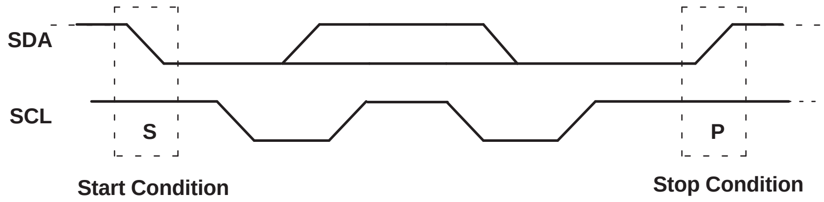


Figure 20. Definition Of Start And Stop Conditions

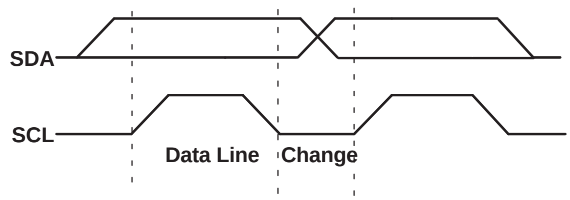


Figure 21. Bit Transfer

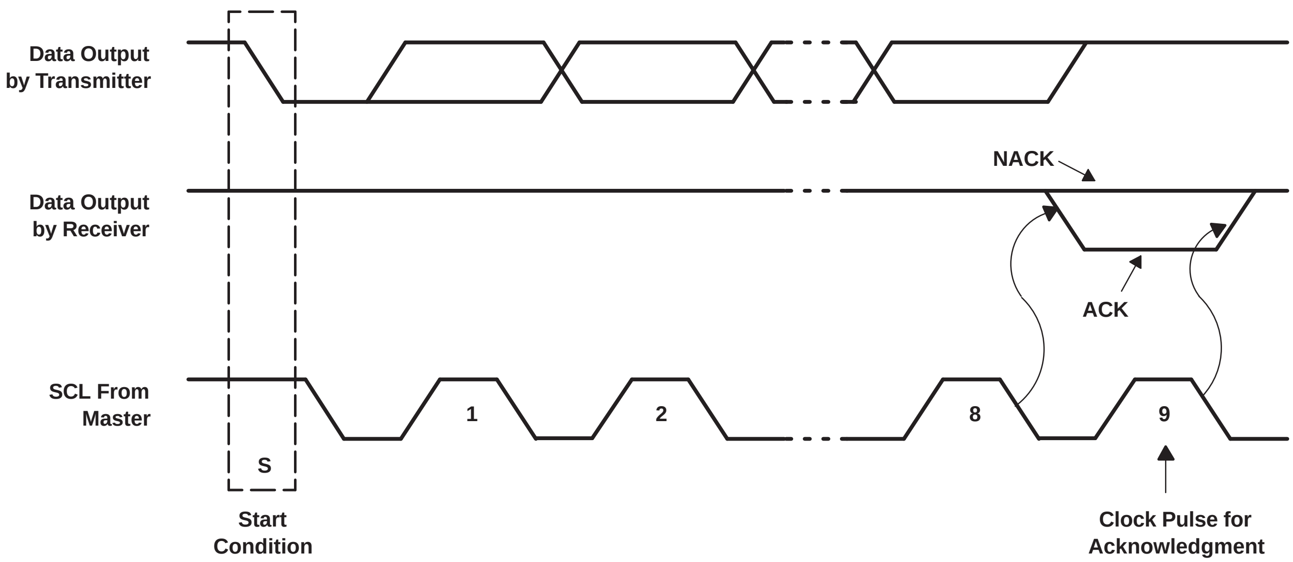


Figure 22. Acknowledgment On The I²C Bus

8.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	L	H	H	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.3.2.1 Device Address

The address of the PCA6107 is shown in Figure 23.

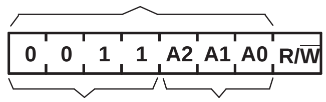


Figure 23. Pca6107 Address

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	24 (decimal), 18 (hexadecimal)
L	L	H	25 (decimal), 19 (hexadecimal)
L	H	L	26 (decimal), 1A (hexadecimal)
L	H	H	27 (decimal), 1B (hexadecimal)
H	L	L	28 (decimal), 1C (hexadecimal)
H	L	H	29 (decimal), 1D (hexadecimal)
H	H	L	30 (decimal), 1E (hexadecimal)
H	H	H	31 (decimal), 1F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA6107. Two bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a new command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	0	B1	B0

Figure 24. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	0000 0000
1	0	0x02	Polarity Inversion	Read/write byte	1111 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

8.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It acts only on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I^{2}C device that the Input Port register will be accessed next.

Table 4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	0	0	0	0	0	0	0	0

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	1	1	1	1	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA6107 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the PCA6107 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 23 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

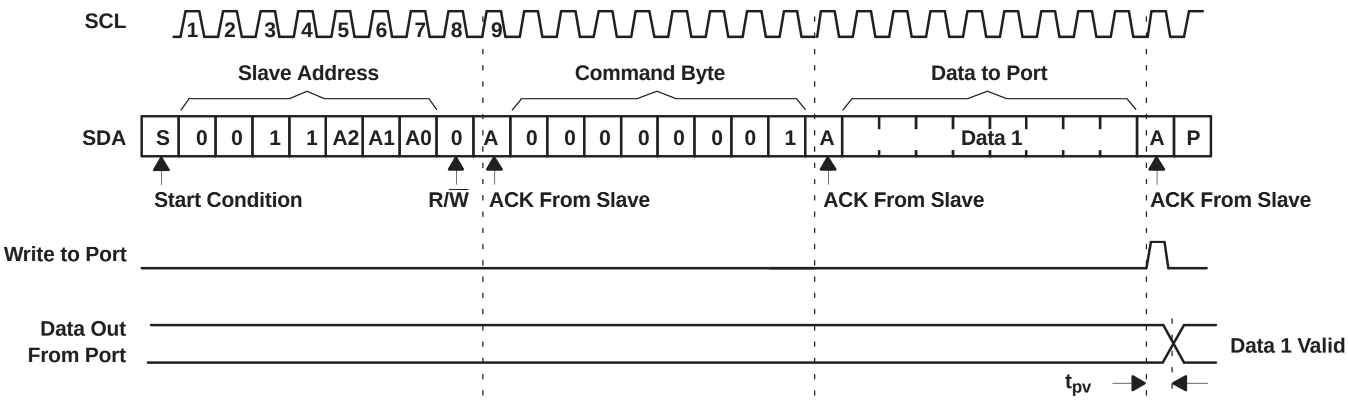


Figure 25. Write To Output Port Register

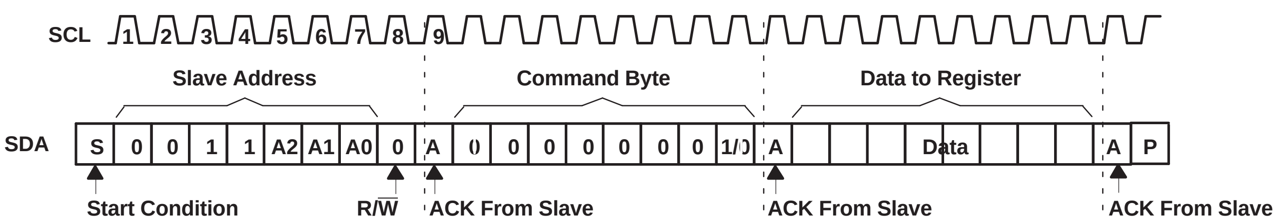


Figure 26. Write To Configuration Or Polarity Inversion Registers

8.3.2.4.2 Reads

The bus master first must send the PCA6107 address with the least-significant bit set to a logic 0 (see Figure 23 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA6107 (see Figure 27 and Figure 28). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

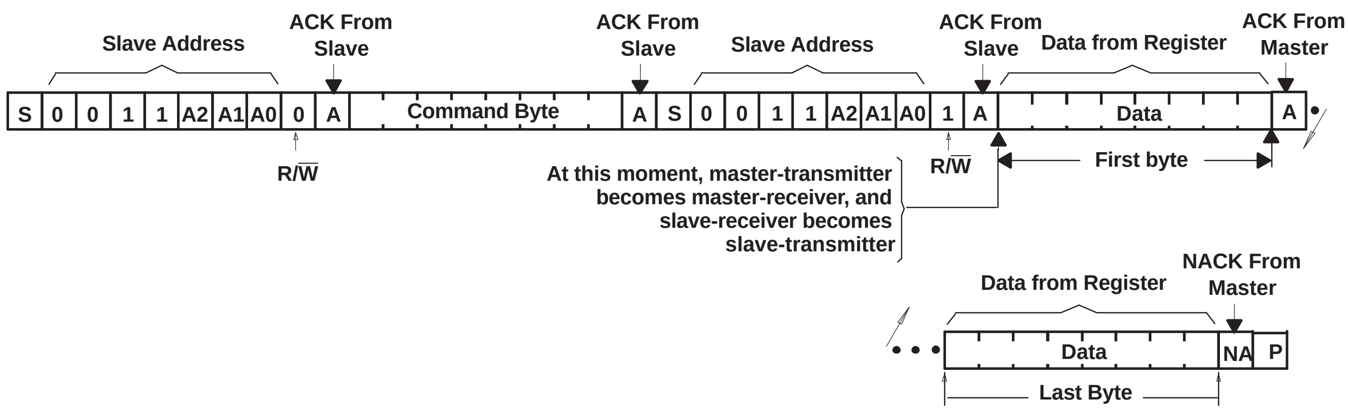
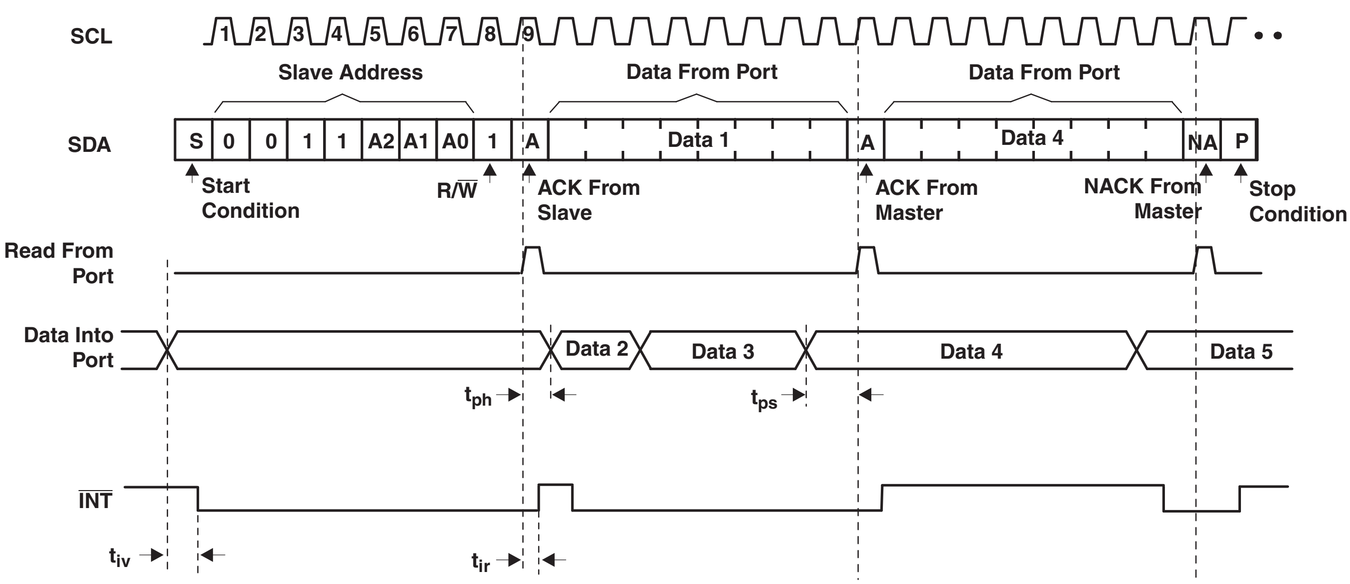


Figure 27. Read From Register



A. This figure assumes the command byte has been programmed previously with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

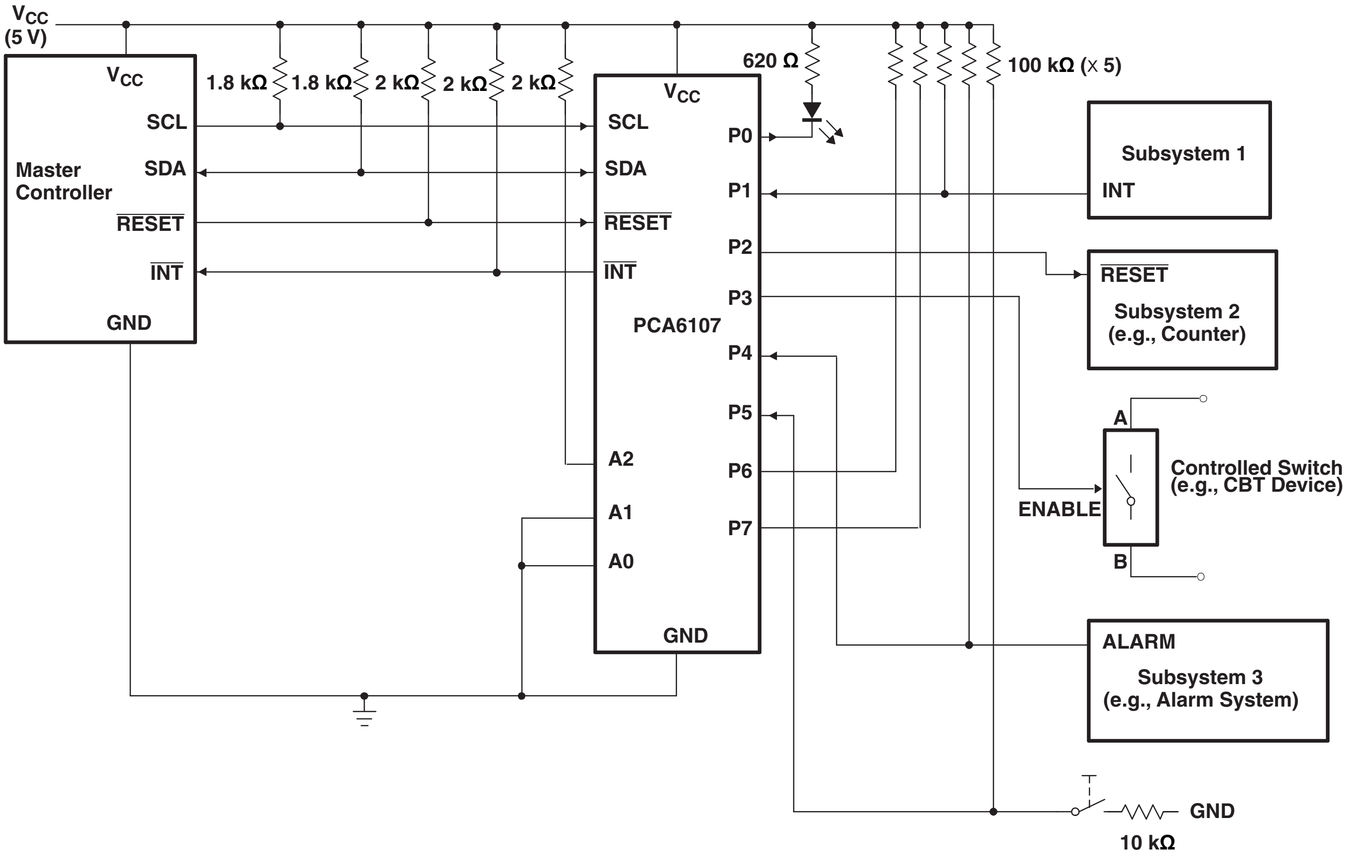
C. This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 27 for these details).

Figure 28. Read Input Port Register

9 Application And Implementation

9.1 Typical Application

Figure 29 shows an application where the PCA6107 can be used.



A. Device address is configured as 0011100 for this example.

B. P1, P4, and P5 are configured as inputs.

C. P0, P2, and P3 are configured as outputs.

D. P6 and P7 are not used and must be configured as outputs.

Figure 29. Typical Application

Typical Application (continued)

9.1.1 Detailed Design Procedure

9.1.1.1 Minimizing I_{CC} When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 29. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in *Electrical Characteristics* shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pin greater than or equal to V_{CC} when the LED is off.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

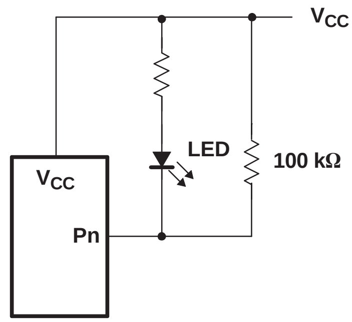


Figure 30. High-Value Resistor In Parallel With The Led

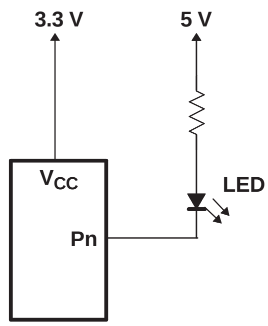
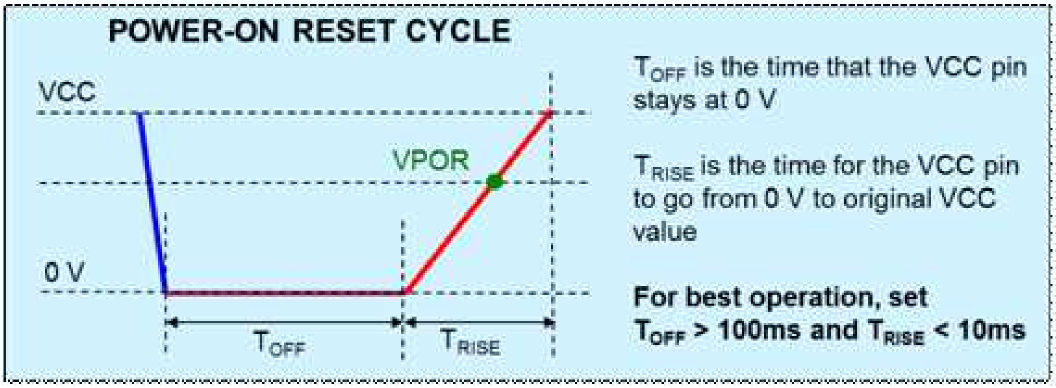


Figure 31. Device Supplied By A Low Voltage

10 Power Supply Recommendations

10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA6107DWR	Obsolete	Production	SOIC (DW) | 18	-	-	Call TI	Call TI	-40 to 85	PCA6107

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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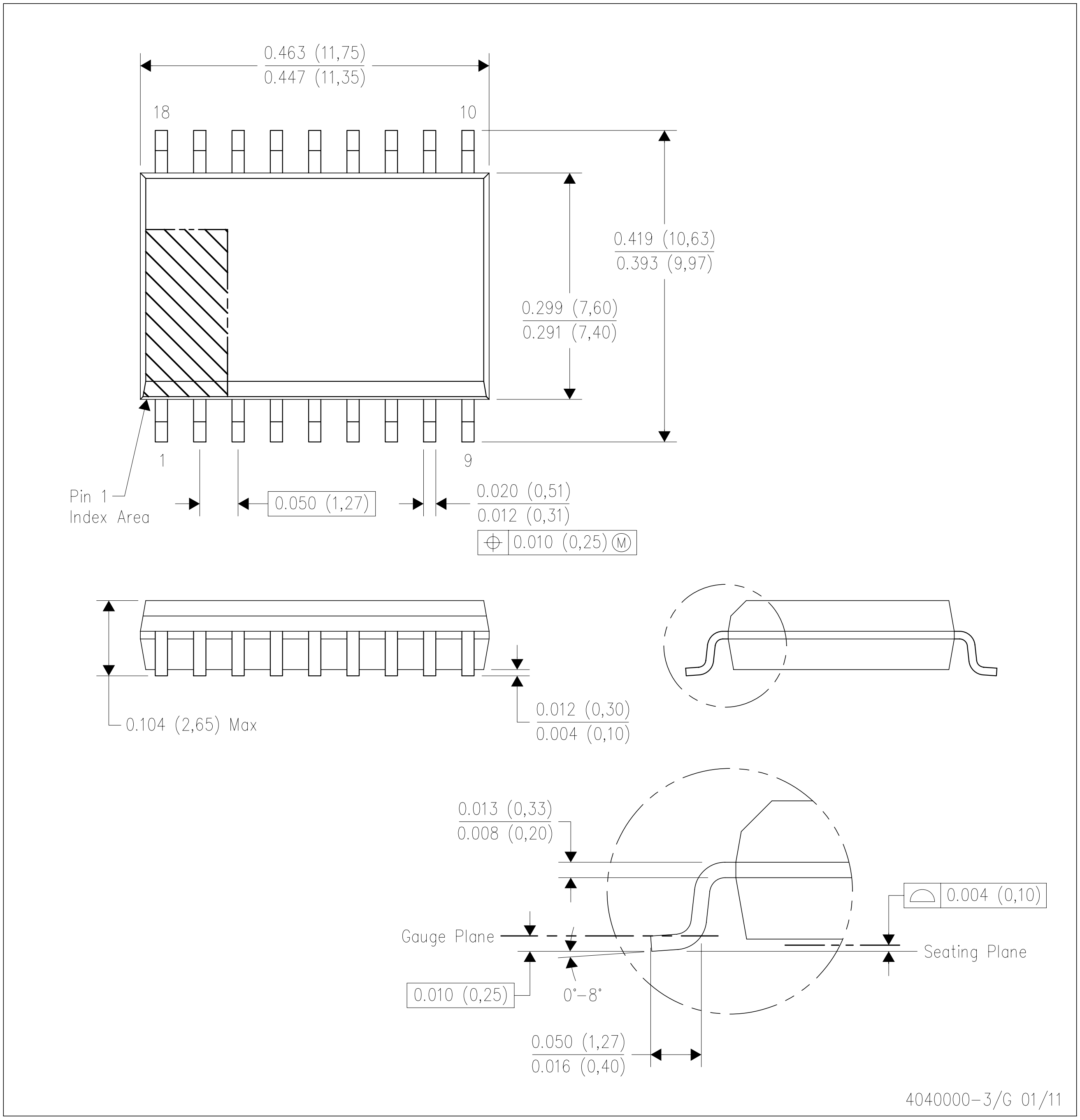
DW (R-PDSO-G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AB.

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