OPAx994-Q1 Automotive, 32V Rail-to-Rail Input and Output, 24MHz, 125mA Output Current Op Amp With Unlimited Capacitive Load Drive

1 Features

- Wide supply voltage: 2.7V to 32V
- Rail-to-rail input and output
- Wide bandwidth: 24MHz GBW, unity-gain stable
- Unlimited capacitive load drive capability
  - Phase margin of 50° when driving a load of 10µF and 1MΩ
- High output current drive: ±125mA
- Low offset voltage: ±350µV (typical)
- Low offset voltage drift: ±2.5µV/°C (typical)
- Low noise: 12nV/√Hz at 1kHz
- High common-mode rejection: 125dB
- High slew rate: 35V/µs
- Low quiescent current: 1.35mA per amplifier

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- HEV/EV inverter and motor control
- HEV/EV DC/DC converter
- On-board charger (OBC) and wireless charger
- AC charging (pile) station
- GFCI fault detection and test
- Software defined radio
- High-side and low-side current sensing

3 Description

The OPAx994-Q1 family (OPA994-Q1 and OPA2994-Q1) is a family of high voltage (32V) rail-to-rail input and output (RRIO) operational amplifiers. These devices offer excellent AC performance, including a wide unity gain bandwidth of 24MHz and a high slew rate of 35V/µs, while only requiring a quiescent current of 1.35mA per channel.

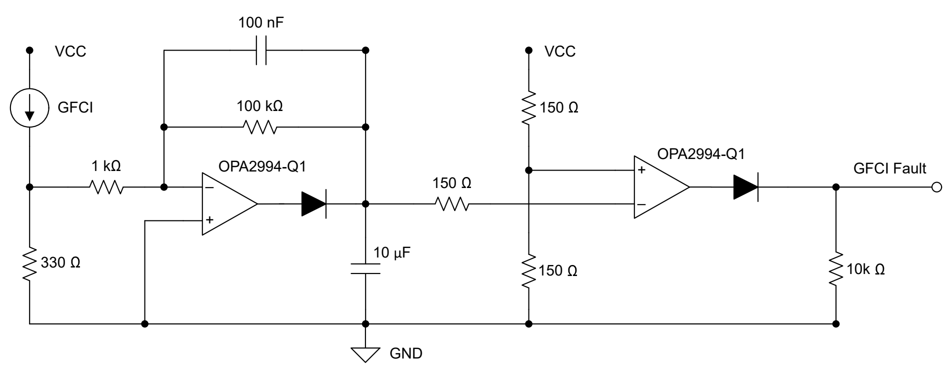
The OPAx994-Q1 family was designed to maintain stability across a wide range of capacitive loads. For example, OPAx994-Q1 is able to achieve a phase margin of 50 degrees when driving large capacitive loads of 10µF with a load resistance of 1MΩ. The OPAx994-Q1 is designed with compensation architectures that mitigate sustained ringing for large capacitive loads. This allows for reliable performance and ease of design for systems that have large, varying, or unknown capacitive loads.

These devices also offer excellent DC precision, including a high short-circuit output current of 125mA/channel, low offset voltage (±350µV, typical), low offset drift (±2.5µV/°C, typical), and high CMRR of 125dB for high voltage operation within the main input pair. This makes the OPAx994-Q1 a flexible, robust, and high-performance op amp for high-voltage automotive applications.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE	PACKAGE SIZE (3)
OPA994-Q1	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
OPA2994-Q1	Dual	D (SOIC, 8)	4.9mm × 6mm
		DGK (VSSOP, 8)(2)	3mm × 4.9mm

(1) For more information, see Section 10.
(2) This package is preview only.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



OPAx994-Q1 in Electric Vehicle Service Equipment (EVSE) Ground-Fault Circuit Interrupter (GFCI) Fault Detection and Test Circuit

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4 Pin Configuration and Functions

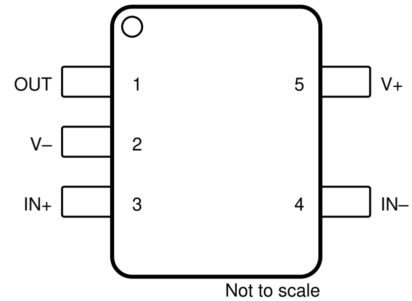


Figure 4-1. OPA994-Q1 DBV Package 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPA994-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

(1) I = input, O = output

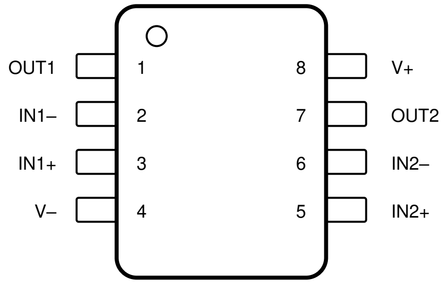


Figure 4-2. OPA2994-Q1 D and DGK(1) Packages: 8-Pin SOIC and VSSOP (Top View)

Table 4-2. Pin Functions: OPA2994-Q1

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) The DGK (VSSOP, 8) package is preview only.
(2) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	33	V
Signal input pins	Common-mode voltage[3]	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage[4]		±10	V
	Current[3]		±10	mA
Output short-circuit[2]		Continuous		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC-Q100-002[1]	±4000	V
		Charged-device model (CDM), per AEC-Q100-001	±1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDECE JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	32	V
V_I	Common mode voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC[(1)]		OPA994-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC[(1)]		OPA2994-Q1		Unit
		D (SOIC) 8 PINS	DGK (VSSOP) 8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	169.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.3	61.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	91.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	9.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.6	89.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.35	±2.3	mV
			T_A = –40°C to 125°C			±3.3	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±2.5		μV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 5V to 32V	T_A = –40°C to 125°C		±3.5	±22	μV/V
		V_{CM} = V–, V_S = 2.7V to 32V	T_A = –40°C to 125°C			±60(1)	μV/V
	DC channel separation				1		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±400	±1500	nA
I_{OS}	Input offset current				±7		nA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			1.8		$μV_{PP}$
					0.3		$μV_{RMS}$
e_N	Input voltage noise density	f = 1kHz			12		nV/√Hz
		f = 10kHz			11		
i_N	Input current noise density	f = 1kHz			1		pA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode input voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 32V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C	109	125		dB
		V_S = 5V, V– < V_{CM} < (V+) – 2V (Main Input Pair)(1)	T_A = –40°C to 125°C	93	111		
		V_S = 2.7V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C		114		
		V_S = 2.7 – 32V, (V+) – 1V < V_{CM} < V+ (Aux Input Pair)	T_A = –40°C to 125°C		77		
		(V+) – 2V < V_{CM} < (V+) – 1V	T_A = –40°C to 125°C	See Offset Voltage vs Common-Mode Voltage (Transition Region)			
INPUT IMPEDANCE							
Z_{ID}	Differential				0.2 || 1		MΩ || pF
Z_{ICM}	Common-mode				2 || 0.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 32V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V		80	87		dB
			T_A = –40°C to 125°C		87		
		V_S = 5V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		75	80		
			T_A = –40°C to 125°C		80		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		75	80		
			T_A = –40°C to 125°C		80		

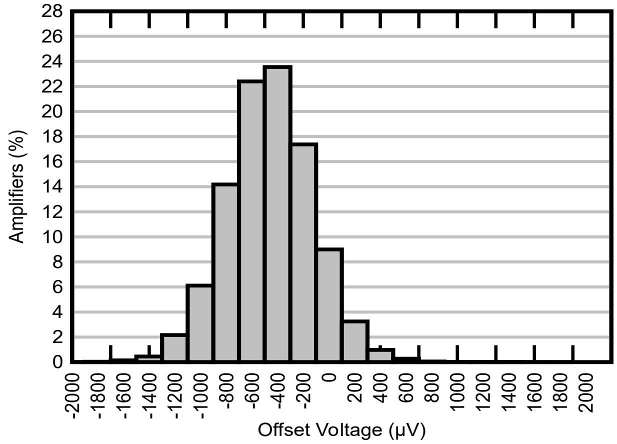
For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				24		MHz
SR	Slew rate	V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 20pF			35		V/µs
t_S	Settling time	To 0.1%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 50pF			0.43		µs
		To 0.1%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 500pF			0.45		
		To 0.01%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 50pF			0.77		
		To 0.01%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 500pF			0.85		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			50		°
	Overload recovery time	V_{IN} × gain > V_S			130		ns
THD+N	Total harmonic distortion + noise	V_S = 32V, V_O = $3V_{RMS}$, G = 1, f = 1kHz, R_L = 10kΩ			0.00022		%
					113		dB
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 32V, R_L = no load		20		mV
			V_S = 32V, R_L = 10kΩ		58	68	
			V_S = 32V, R_L = 2kΩ		117	137	
			V_S = 5V, R_L = no load		30		
			V_S = 5V, R_L = 10kΩ		45	52	
			V_S = 5V, R_L = 2kΩ		25	60	
			V_S = 2.7V, R_L = no load		25		
			V_S = 2.7V, R_L = 10kΩ		42	48	
			V_S = 2.7V, R_L = 2kΩ		45	54	
I_{SC}	Short-circuit current	V_S = 32V		±62	±125		mA
		V_S = 5V(1)		±50	±85		
		V_S = 2.7V(1)		±30	±60		
C_{LOAD}	Capacitive load drive			Unlimited; See Phase Margin vs Capacitive Load			pF
Z_O	Open-loop output impedance	I_O = 0A		See Open-Loop Output Impedance vs Frequency			Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V-, I_O = 0A			1.35	1.93	mA
			T_A = –40°C to 125°C			2.23	mA

(1) Specified by characterization only.

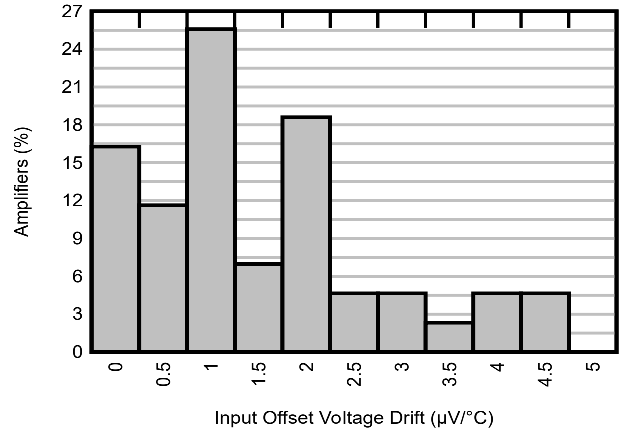
5.7 Typical Characteristics

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



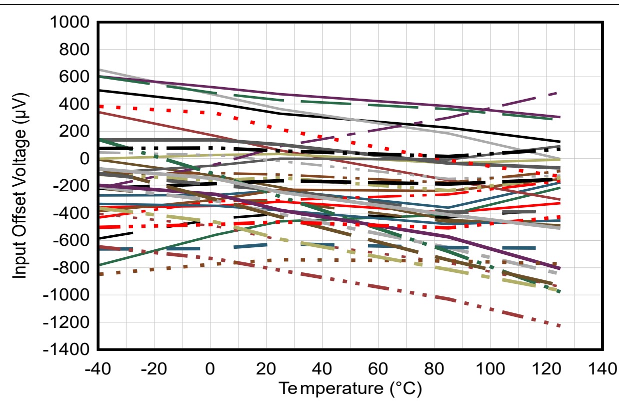
Distribution from 17,184 amplifiers

Figure 5-1. Offset Voltage Production Distribution



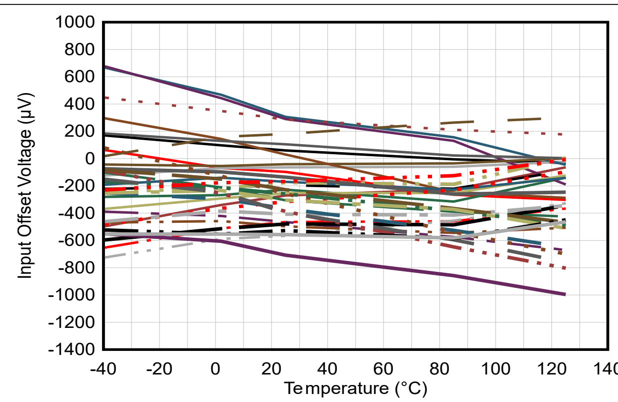
Distribution from 43 amplifiers
T_A = -40°C to 125°C

Figure 5-2. Offset Voltage Drift Distribution



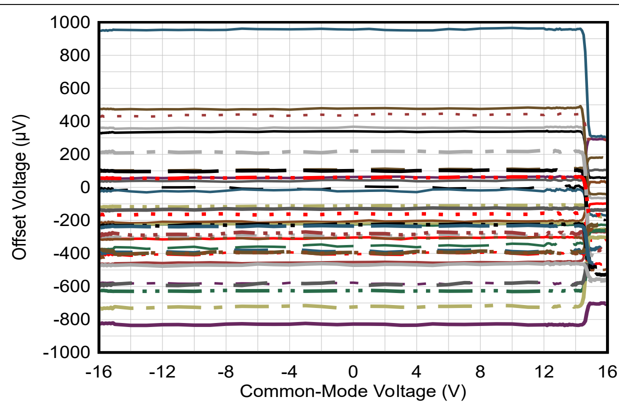
V_{CM} = V-
Each line represents one channel

Figure 5-3. Offset Voltage vs Temperature



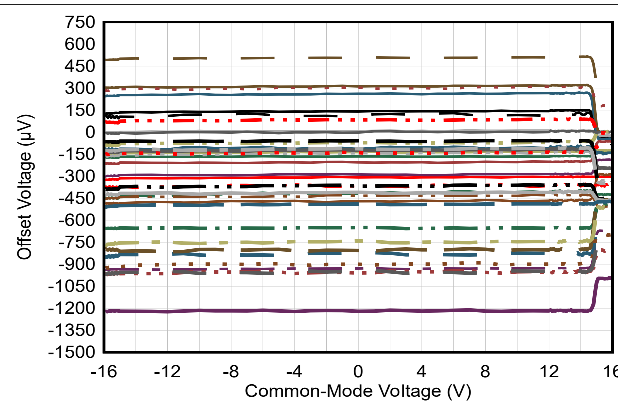
V_{CM} = V+
Each line represents one channel

Figure 5-4. Offset Voltage vs Temperature



Each line represents one channel
T_A = 25°C

Figure 5-5. Offset Voltage vs Common-Mode Voltage

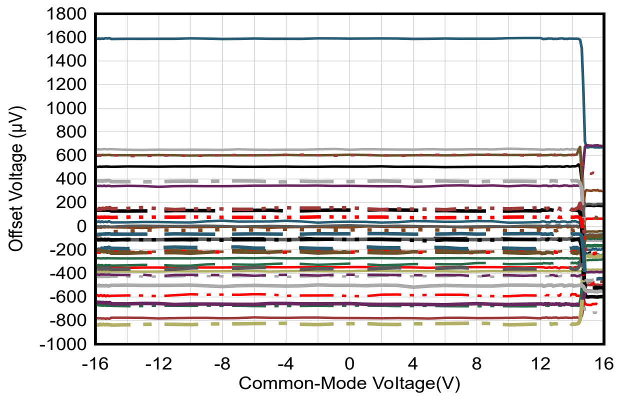


Each line represents one channel
T_A = 125°C

Figure 5-6. Offset Voltage vs Common-Mode Voltage

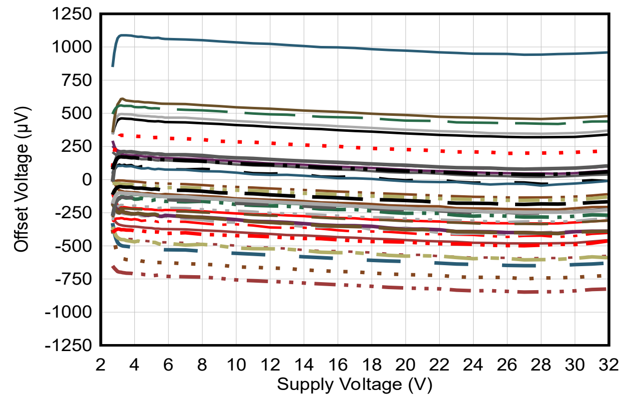
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



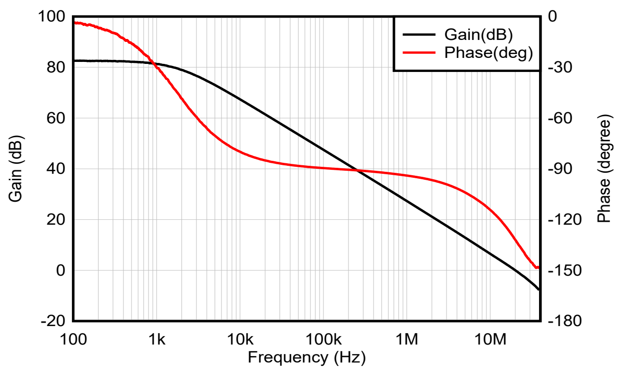
Each line represents one channel
T_A = -40°C

Figure 5-7. Offset Voltage vs Common-Mode Voltage



V_{CM} = V-

Figure 5-8. Offset Voltage vs Power Supply



C_L = 20 pF

Figure 5-9. Open-Loop Gain and Phase vs Frequency

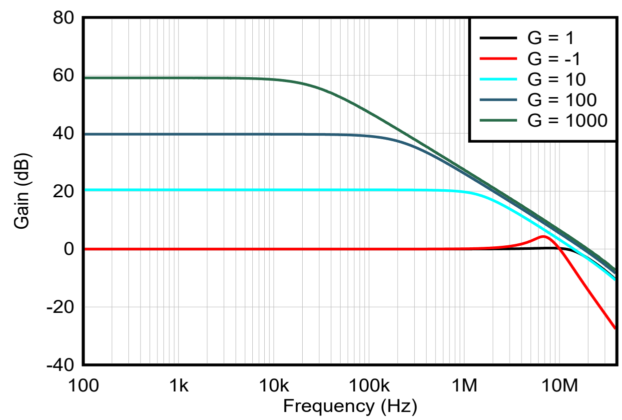


Figure 5-10. Closed-Loop Gain vs Frequency

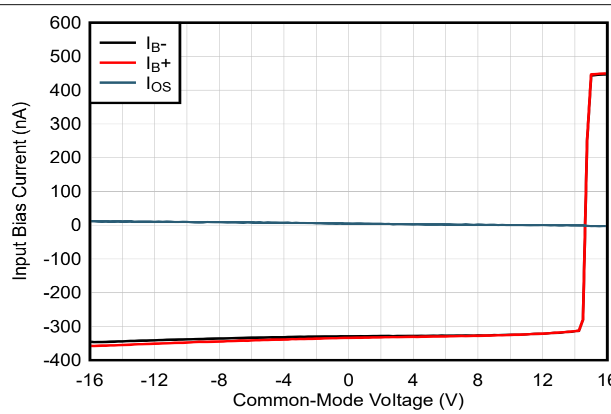


Figure 5-11. Input Bias Current and Offset Current vs Common-Mode Voltage

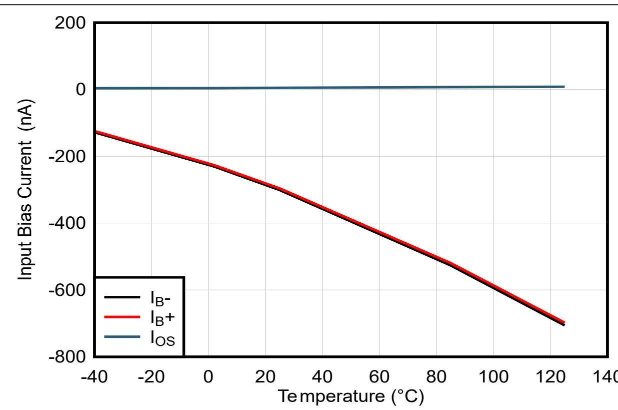
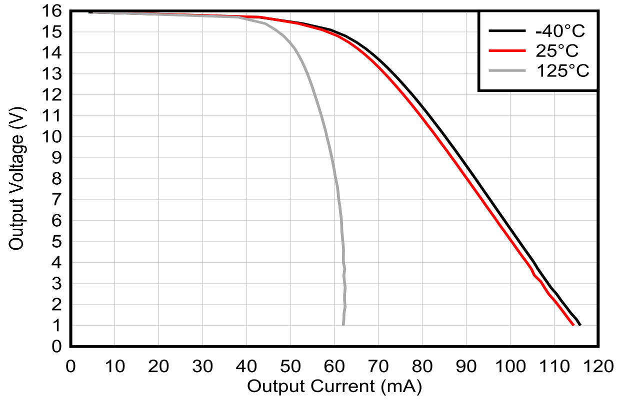


Figure 5-12. Input Bias Current and Offset Current vs Temperature

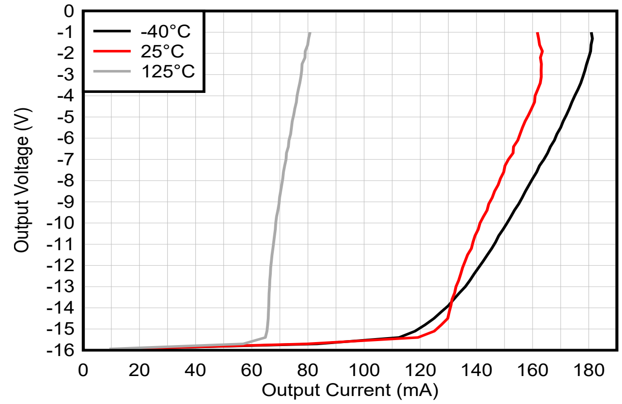
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



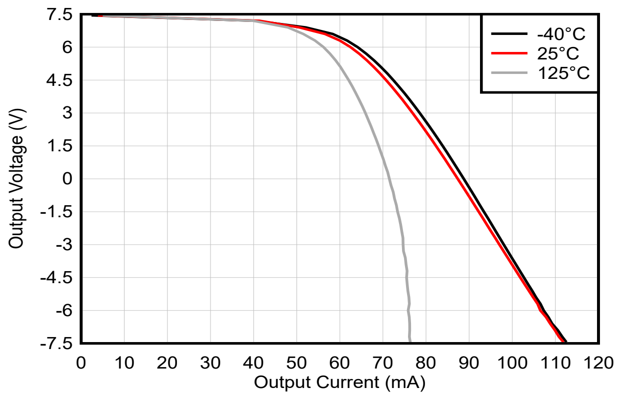
V_S = 32 V

Figure 5-13. Output Voltage Swing vs Output Current (Sourcing)



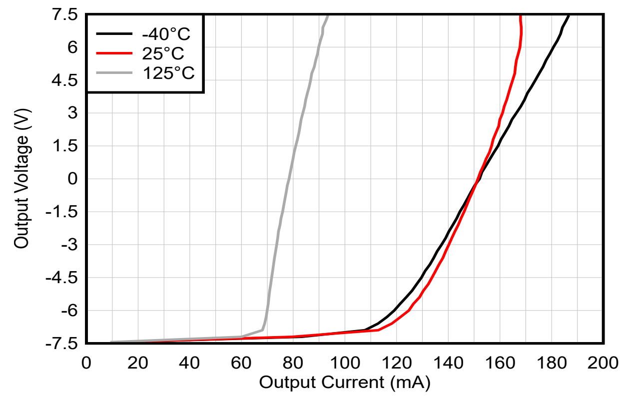
V_S = 32 V

Figure 5-14. Output Voltage Swing vs Output Current (Sinking)



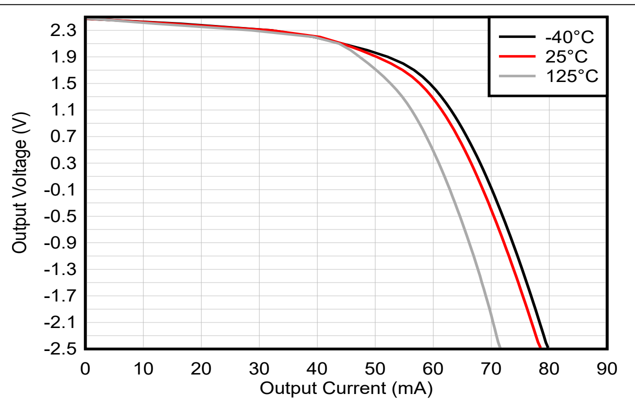
V_S = 15 V

Figure 5-15. Output Voltage Swing vs Output Current (Sourcing)



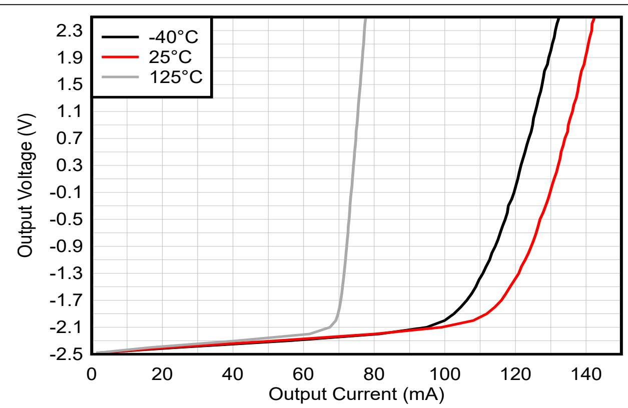
V_S = 15 V

Figure 5-16. Output Voltage Swing vs Output Current (Sinking)



V_S = 5 V

Figure 5-17. Output Voltage Swing vs Output Current (Sourcing)

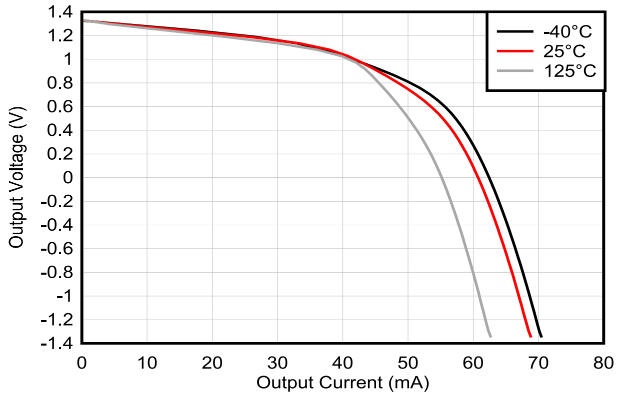


V_S = 5 V

Figure 5-18. Output Voltage Swing vs Output Current (Sinking)

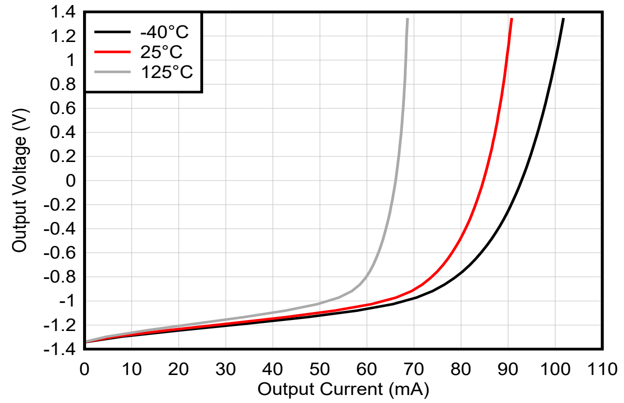
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



V_S = 2.7 V

Figure 5-19. Output Voltage Swing vs Output Current (Sourcing)



V_S = 2.7 V

Figure 5-20. Output Voltage Swing vs Output Current (Sinking)

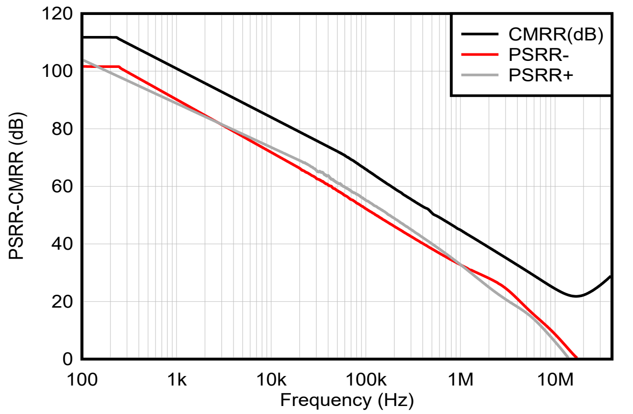
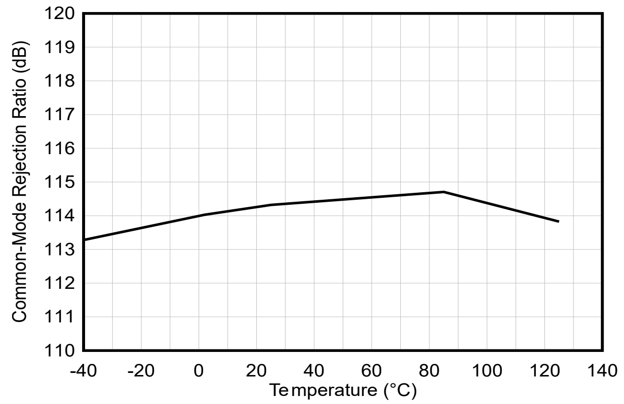
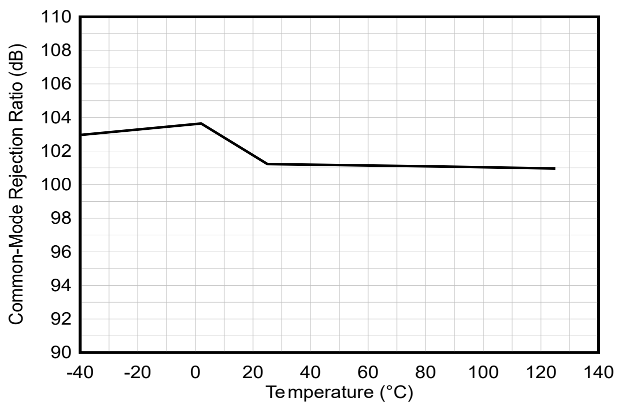


Figure 5-21. CMRR and PSRR vs Frequency



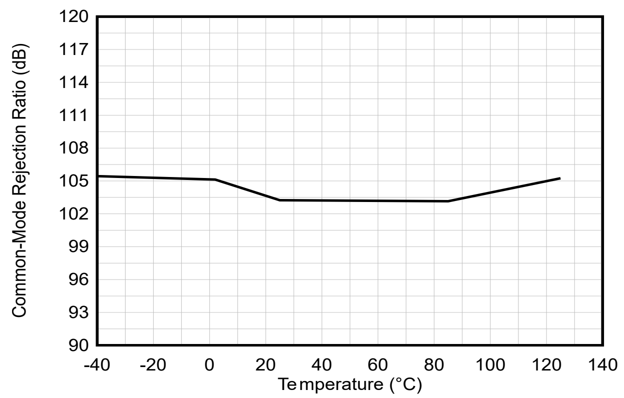
f = 0 Hz

Figure 5-22. CMRR vs Temperature



V_S = 5 V
f = 0 Hz

Figure 5-23. CMRR vs Temperature

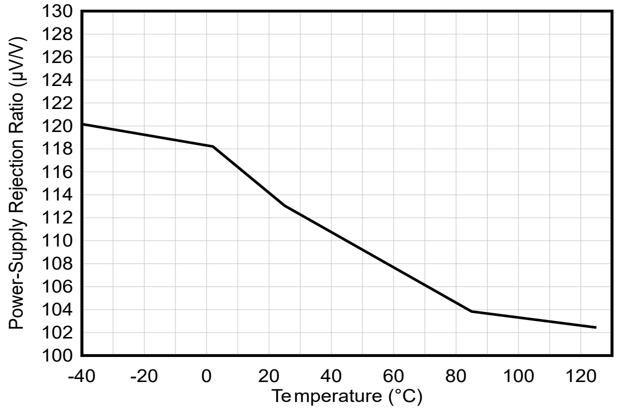


V_S = 2.7 V
f = 0 Hz

Figure 5-24. CMRR vs Temperature

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



f = 0 Hz

Figure 5-25. PSRR vs Temperature

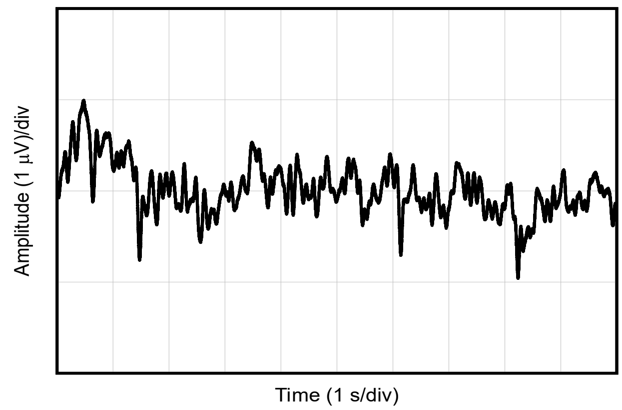


Figure 5-26. 0.1Hz to 10Hz Noise

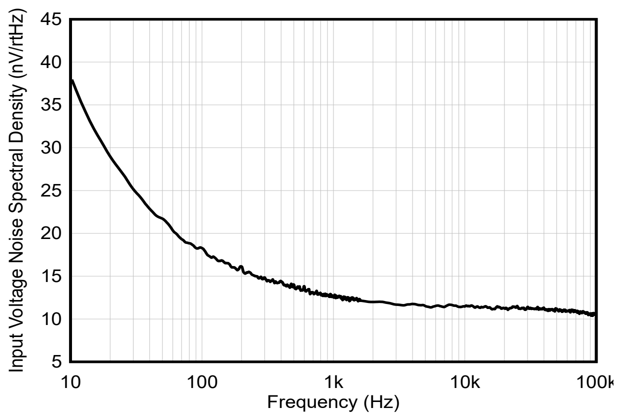
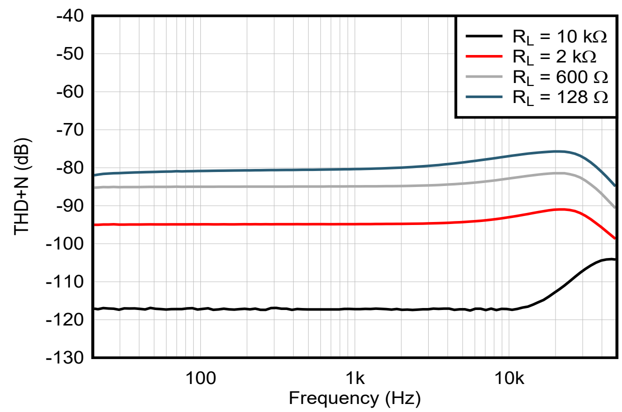
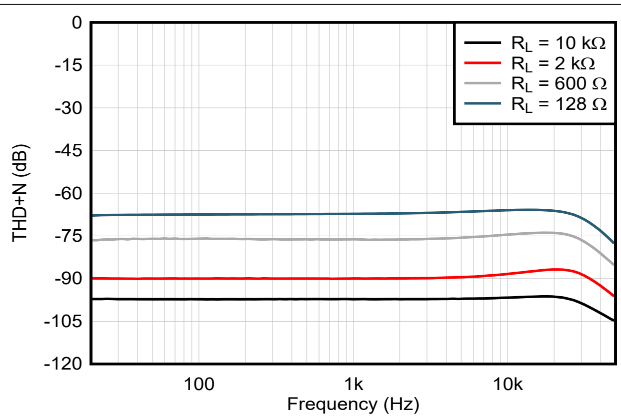


Figure 5-27. Input Voltage Noise Spectral Density vs Frequency



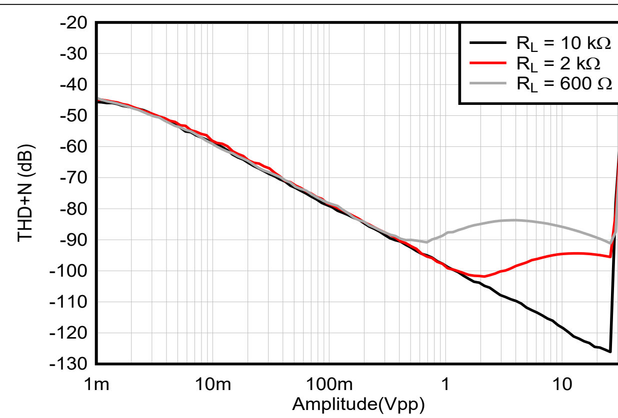
G = +1
V_{OUT} = 3 V_{RMS}
BW = 80 kHz

Figure 5-28. THD+N Ratio vs Frequency



G = -1
V_{OUT} = 3 V_{RMS}
BW = 80 kHz

Figure 5-29. THD+N Ratio vs Frequency

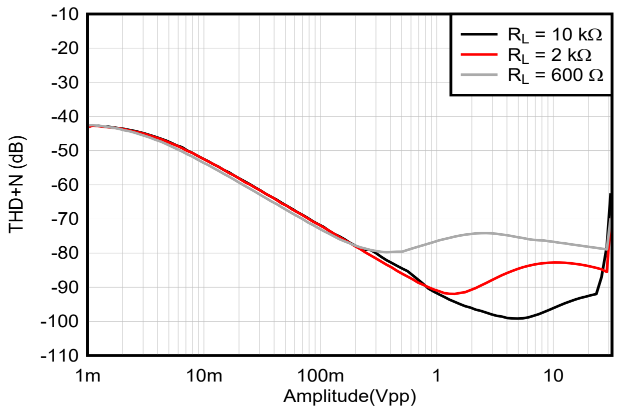


f = 1 kHz
BW = 80 kHz
G = +1

Figure 5-30. THD+N vs Output Amplitude

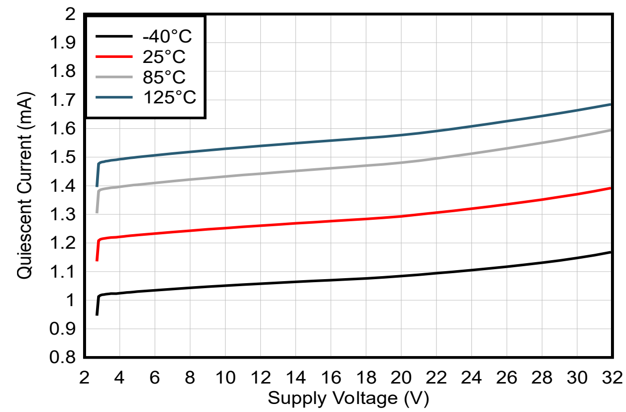
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



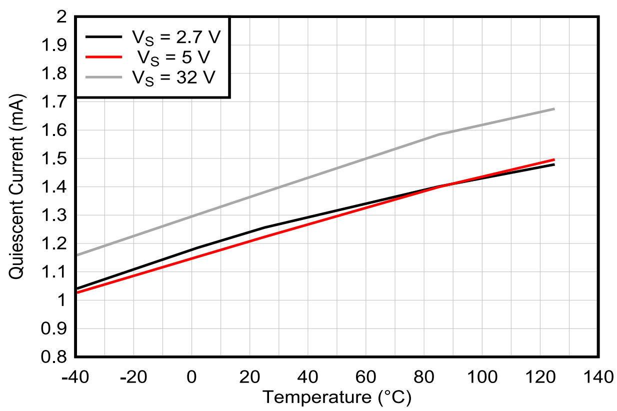
f = 1 kHz
BW = 80 kHz
G = -1

Figure 5-31. THD+N vs Output Amplitude



V_{CM} = V-

Figure 5-32. Quiescent Current vs Supply Voltage



V_{CM} = V-

Figure 5-33. Quiescent Current vs Temperature

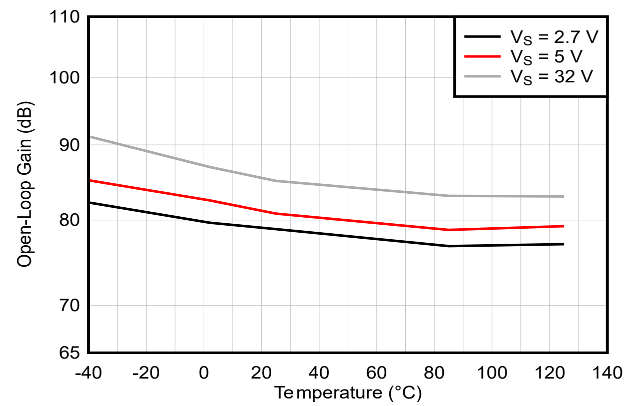


Figure 5-34. Open-Loop Voltage Gain vs Temperature (dB)

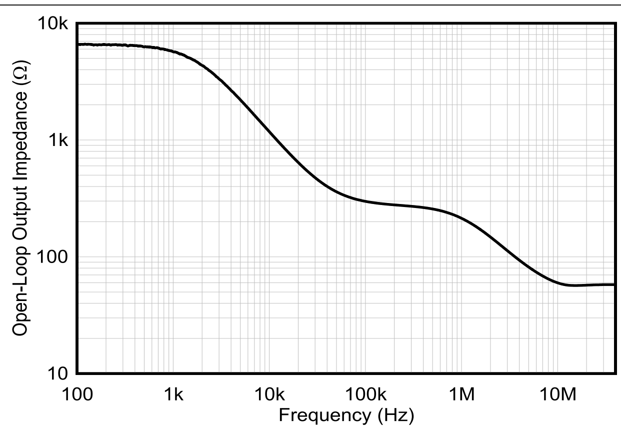
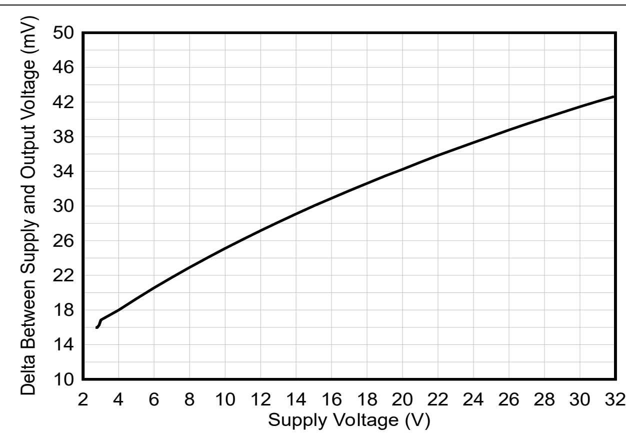


Figure 5-35. Open-Loop Output Impedance vs Frequency

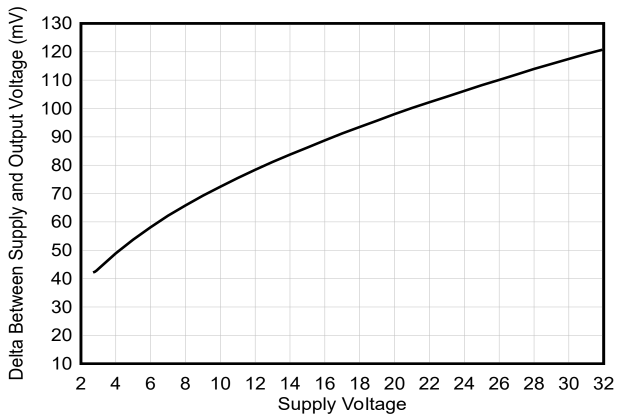


R_L = 10 kΩ

Figure 5-36. Output Swing vs Supply Voltage, Positive Swing

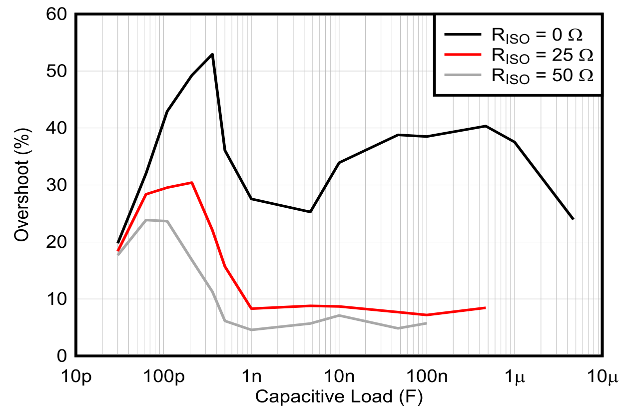
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



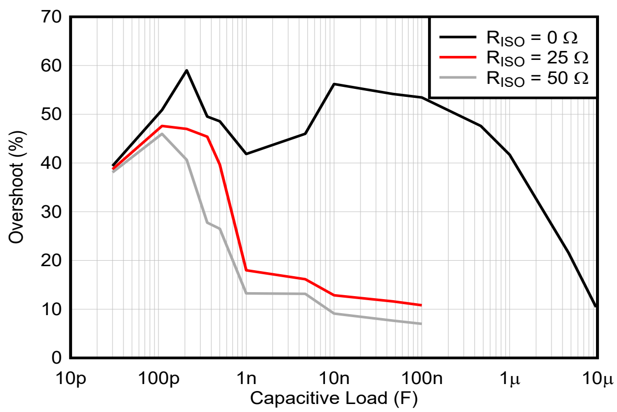
R_L = 2 kΩ

Figure 5-37. Output Swing vs Supply Voltage, Positive Swing



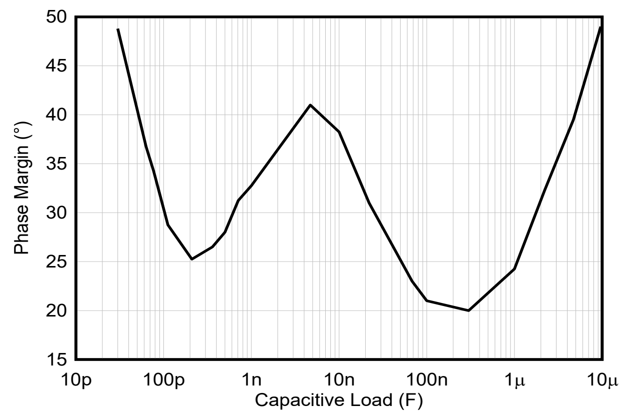
20 mV_{pp} Output Step
G = -1

Figure 5-38. Small-Signal Overshoot vs Capacitive Load



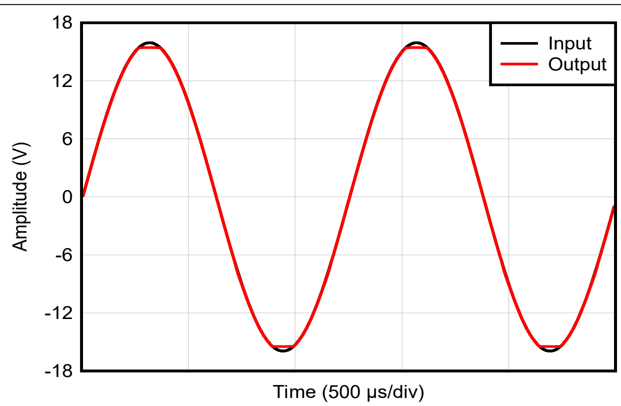
20 mV_{pp} Output Step
G = +1

Figure 5-39. Small-Signal Overshoot vs Capacitive Load



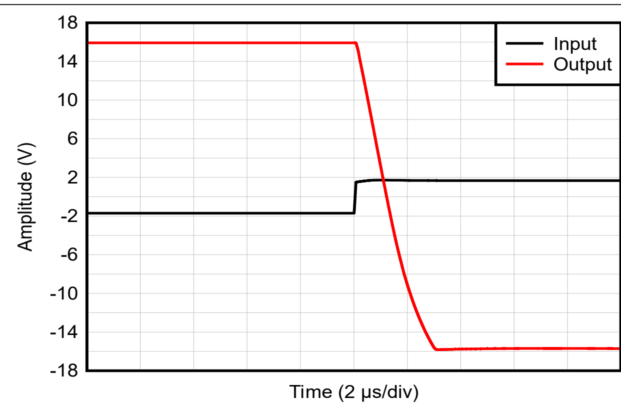
Gain = +1

Figure 5-40. Phase Margin vs Capacitive Load



G = 1
V_{IN} = ±16 V
V_S = V_{OUT} = ±15.5 V

Figure 5-41. No Phase Reversal

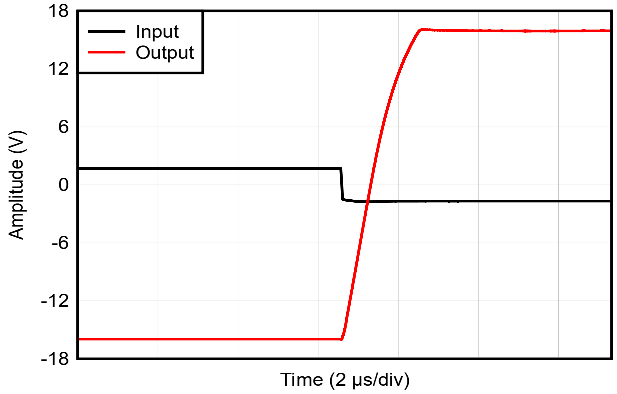


G = -10

Figure 5-42. Positive Overload Recovery

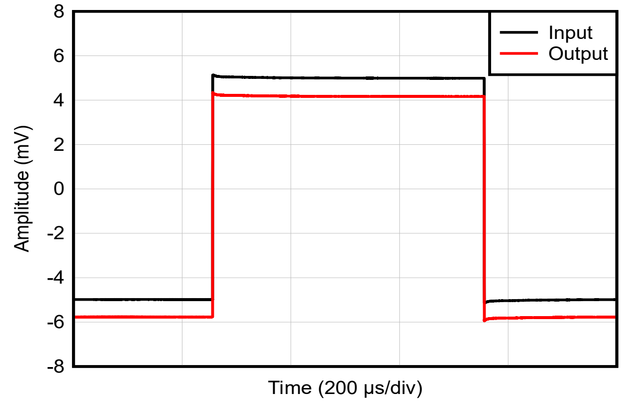
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



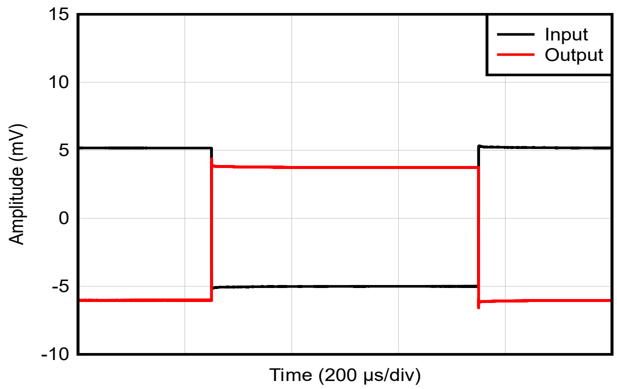
G = -10

Figure 5-43. Negative Overload Recovery



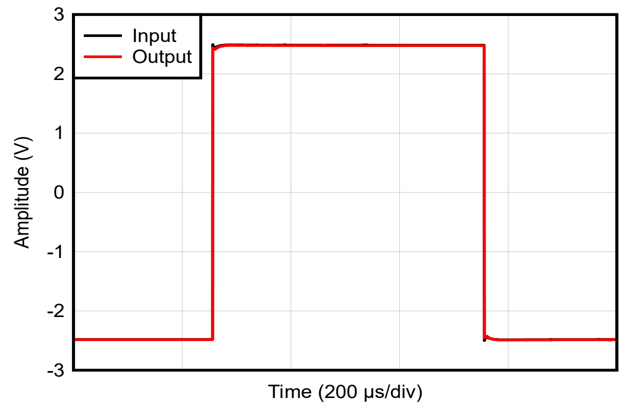
V_{IN} = 10 mV_{pp}
G = +1
C_L = 20 pF

Figure 5-44. Small-Signal Step Response



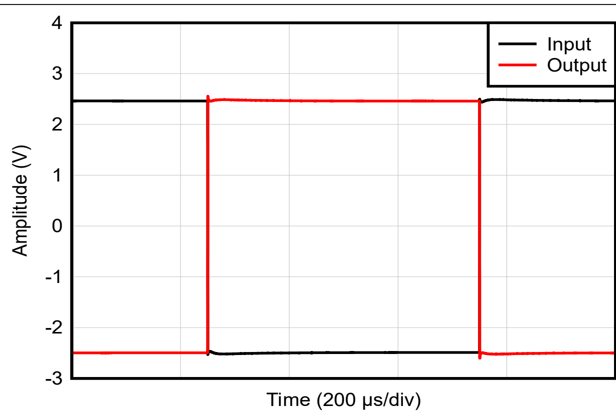
V_{IN} = 10 mV_{PP}
G = -1
C_L = 20 pF

Figure 5-45. Small-Signal Step Response



V_{IN} = 5 V_{pp}
G = +1
C_L = 20 pF

Figure 5-46. Large-Signal Step Response



V_{IN} = 5 V_{pp}
G = -1
C_L = 20 pF

Figure 5-47. Large-Signal Step Response

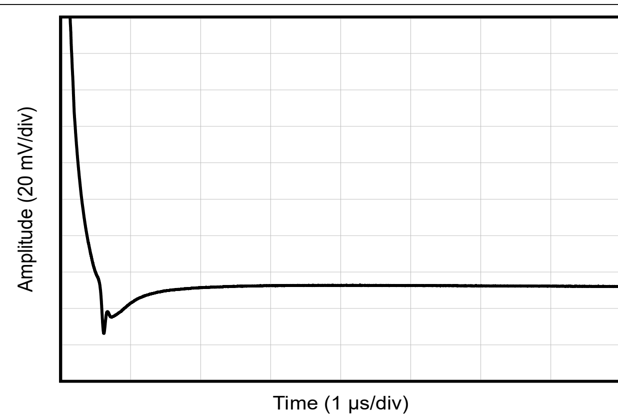


Figure 5-48. Settling Time

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

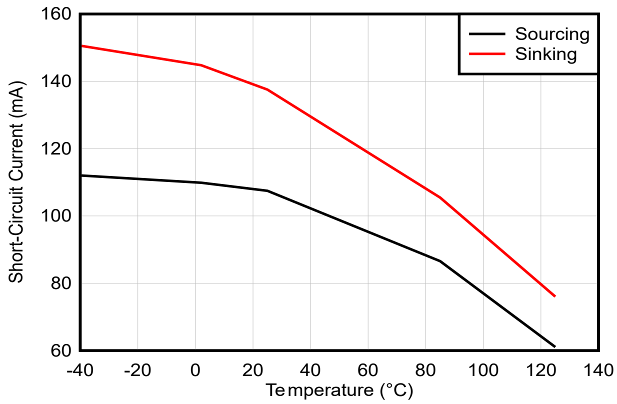


Figure 5-49. Short-Circuit Current vs Temperature

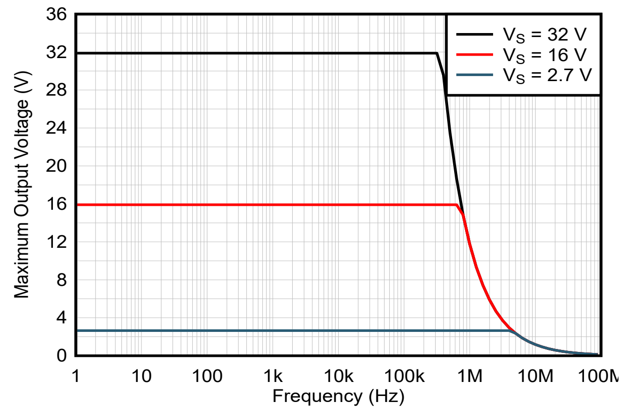


Figure 5-50. Maximum Output Voltage vs Frequency

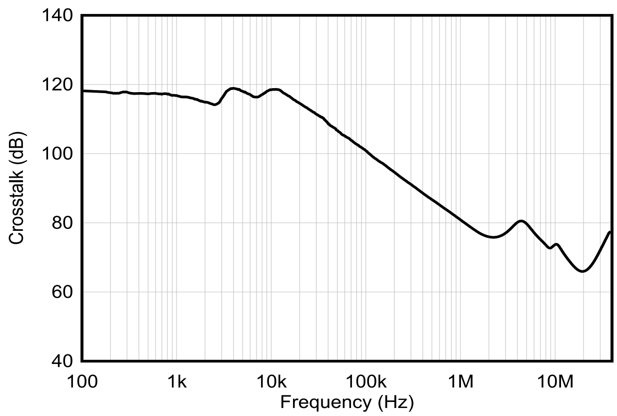


Figure 5-51. Channel Separation vs Frequency

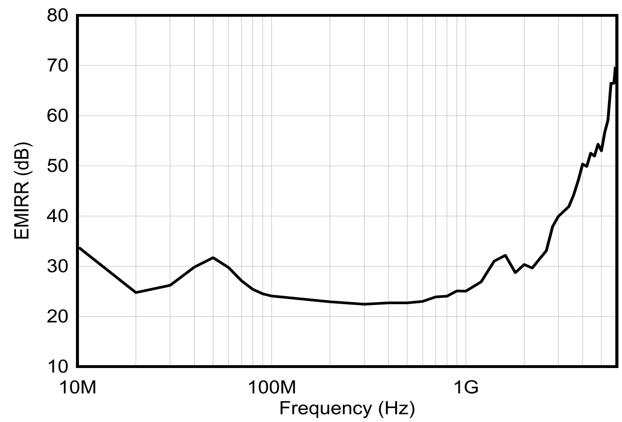


Figure 5-52. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

6.1 Overview

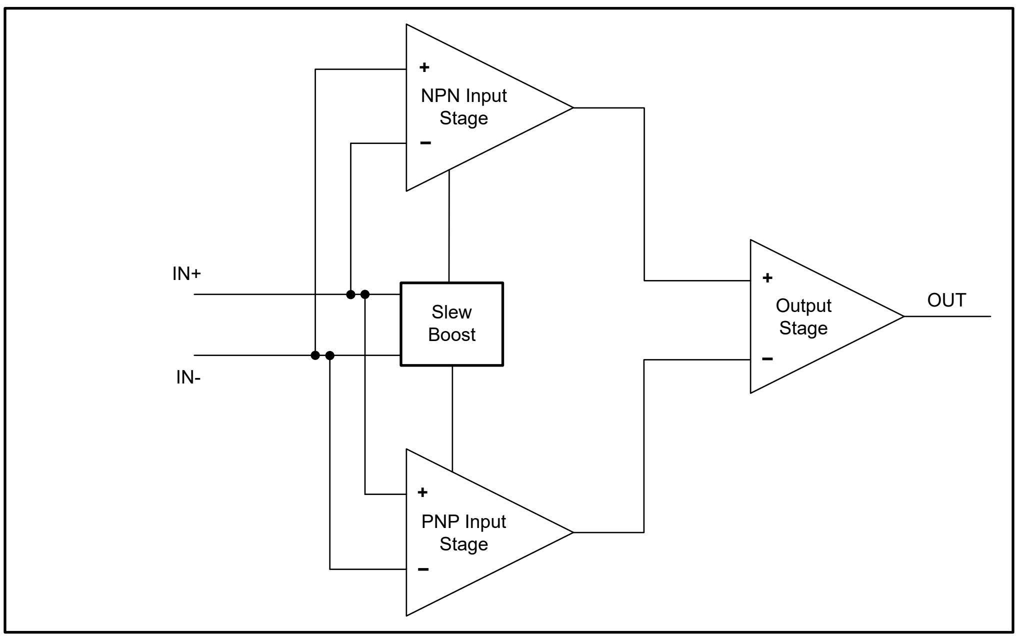
The OPAx994-Q1 family (OPA994-Q1 and OPA2994-Q1) is a family of high voltage (32V) general purpose operational amplifiers.

The OPAx994-Q1 family has a wide gain bandwidth of 24MHz when no capacitive load is present. These devices have unlimited capacitive load drive and are able to drive large capacitive loads without continuous oscillations.

These devices also offer excellent DC precision, including rail-to-rail input/output, low offset (±350μV, typical), and low offset drift (±2.5μV/°C, typical).

Special features such as unlimited capacitive load drive, high short-circuit current (±125mA, typical), and high slew rate (35V/μs, typical) make the OPAx994-Q1 an extremely flexible, robust, and high-performance operational amplifier for high-voltage automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unlimited Capacitive Load Drive

One of the challenges when designing an op-amp circuit is verifying that the op-amp is stable when driving capacitive loads. The OPAx994-Q1 has a unique architecture that features Unlimited Capacitive Load Drive (UCLD), which is used to prevent sustained oscillations on the output signals of an amplifier when driving large capacitive loads. This is achieved by maintaining an acceptable phase margin as the size of the capacitive load increases.

An op-amp circuit that is unstable can have an unpredictable or unexpected output with poor transient performance. This typically results in large overshoots and ringing when changes occur on the input or load, but can also result in sustained oscillations. One common cause of instability in op-amps can occur when connecting a load capacitor, CL, to the output of the amplifier. This instability is a result of the internal output resistance, Zo, of the op-amp that creates a secondary pole with CL.

The UCLD of the OPAx994-Q1 family has a proprietary output compensation structure that is able to sense the capacitance on the output and adjust internal pole and zero structures to achieve acceptable phase margins. This behavior is unique to UCLD devices and allows the op-amp to remain stable under larger capacitive loads compared to traditional amplifiers.

To keep an acceptable phase margin, UCLD devices lower the gain bandwidth product under larger capacitive loads. The OPAx994-Q1 is specified to have a gain bandwidth product of 24MHz without significant capacitive load, but this value will begin to decrease at the point where a traditional amplifier would begin to become unstable. This tradeoff is what extends the output drive capability. OPAx994-Q1 is designed with a wide gain bandwidth product to make sure there is headroom for many general-purpose applications with higher capacitive loads.

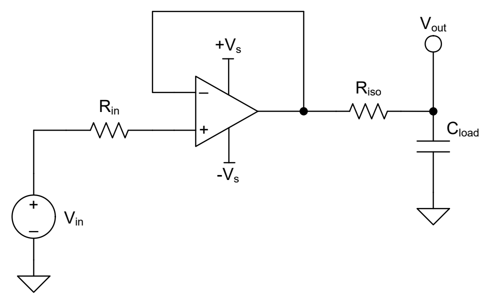


Figure 6-1. Extending Capacitive Load Drive With the OPAx994-Q1

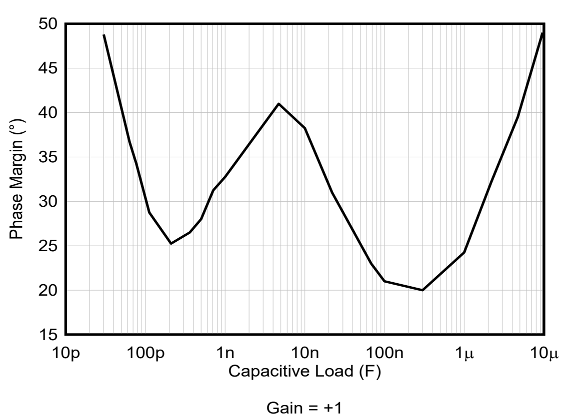


Figure 6-2. Phase Margin vs Capacitive Load

6.3.2 Common-Mode Voltage Range

The OPAx994-Q1 is a 32V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary PNP and NPN differential input pairs, as shown in Figure 6-3. The NPN pair is active for input voltages close to the positive rail, typically from (V+) – 1V to the positive supply. The PNP pair is active for inputs from the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region.

For more information on common-mode voltage range and complementary pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

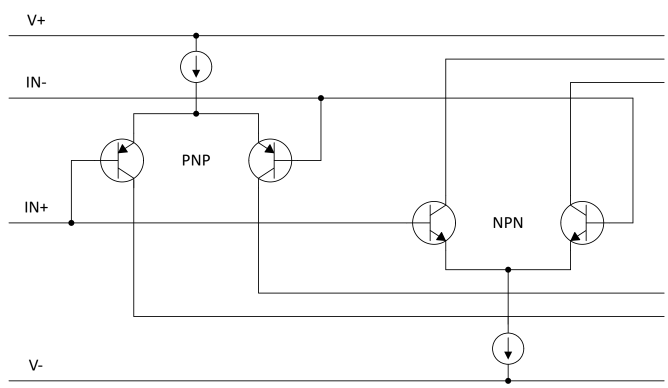


Figure 6-3. Rail-to-Rail Input Stage

6.3.3 Phase Reversal Protection

The OPAx994-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx994-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-4. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

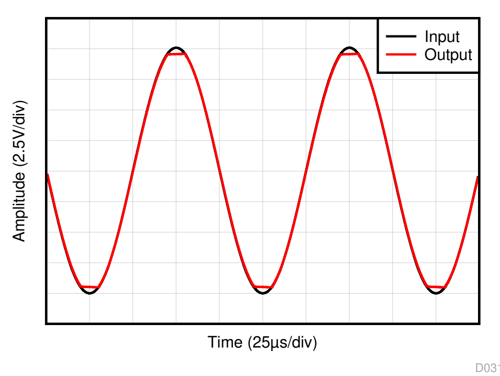


Figure 6-4. No Phase Reversal

6.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-5 shows an illustration of the ESD circuits contained in the OPAx994-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

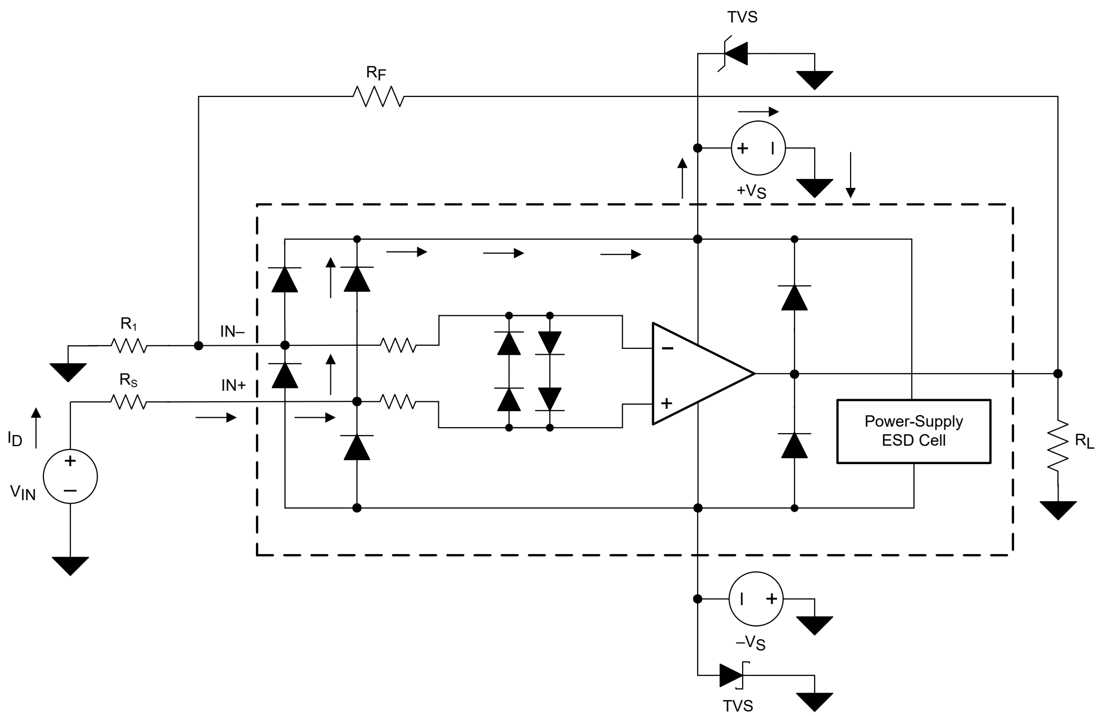


Figure 6-5. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx994-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 6-5), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 6-5 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals; see Figure 6-5. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx994-Q1 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 6-5. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx994-Q1. Figure 6-5 shows an example configuration that implements a current-limiting feedback resistor.

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx994-Q1 is approximately 130ns.

6.3.6 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier can exhibit some amount of deviation from the ideal value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

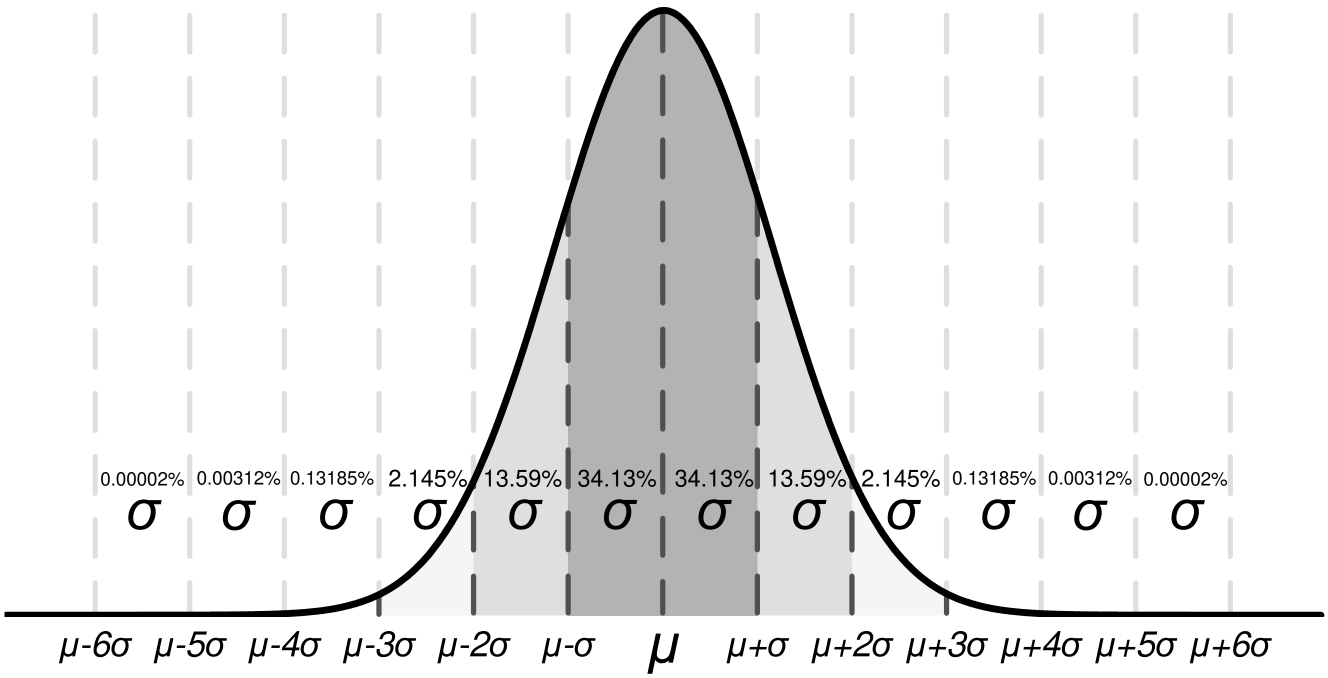


Figure 6-6. Ideal Gaussian Distribution

The Figure 6-6 figure shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Designers can use this chart to calculate approximate probability of a specification in a unit; for example, for OPAx994-Q1, the typical input voltage offset is 350μV. So 68.2% of all OPAx994-Q1 devices are expected to have an offset from –350μV to +350μV. At 4σ (±1400μV), 99.9937% of the distribution has an offset voltage less than ±1400μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are tested by TI, unless otherwise noted, and units outside these limits are removed from production material. For example, the OPAx994-Q1 family has a maximum offset voltage of 2.3mV at 25°C, and even though this corresponds to slightly less than 5σ (≈1 in 1.7 million units), which is extremely unlikely, units with larger offset than 2.3mV are removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the designers application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the OPAx994-Q1 family does not have a maximum or minimum for offset voltage drift. But based on the typical value of 2.5μV/°C in the *Electrical Characteristics* table, it can be calculated that the 6σ value for offset voltage drift is about 15μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.4 Device Functional Modes

The OPAx994-Q1 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the OPAx994-Q1 is 32V (±16V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx994-Q1 family offers excellent DC precision and AC performance. These devices operate up to 32V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 24MHz bandwidth and high output drive. These features make the OPAx994-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the OPA994-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

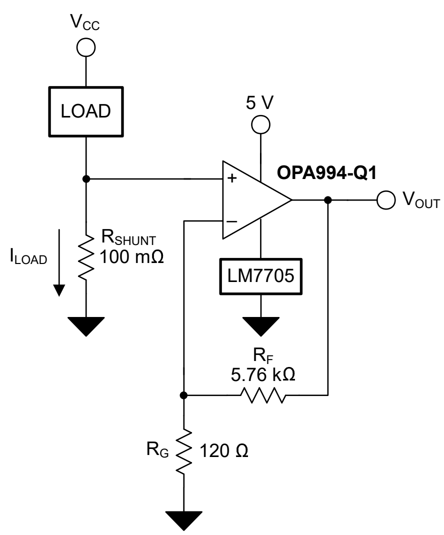


Figure 7-1. OPAx994-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are as follows:

- Load current: 0A to 1A
- Max output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA994-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the OPA994-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA994-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because these are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors can generate thermal noise that exceeds the intrinsic noise of the op amp. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curve

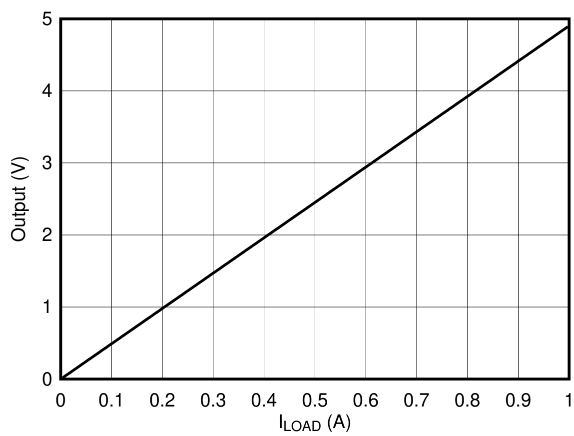


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The OPAx994-Q1 is specified for operation from 2.7V to 32V (±1.35V to ±32V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

> **CAUTION**
>
> Supply voltages larger than 33V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

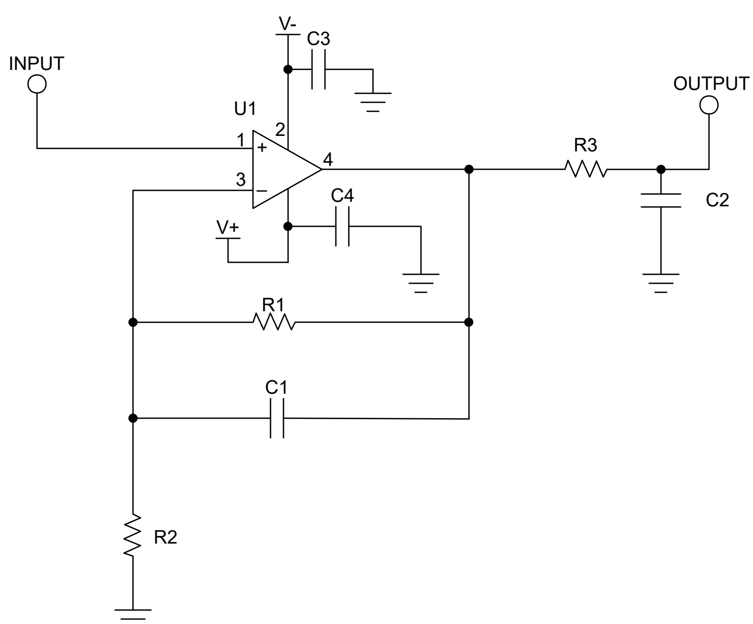


Figure 7-3. Schematic for Noninverting Configuration Layout Example

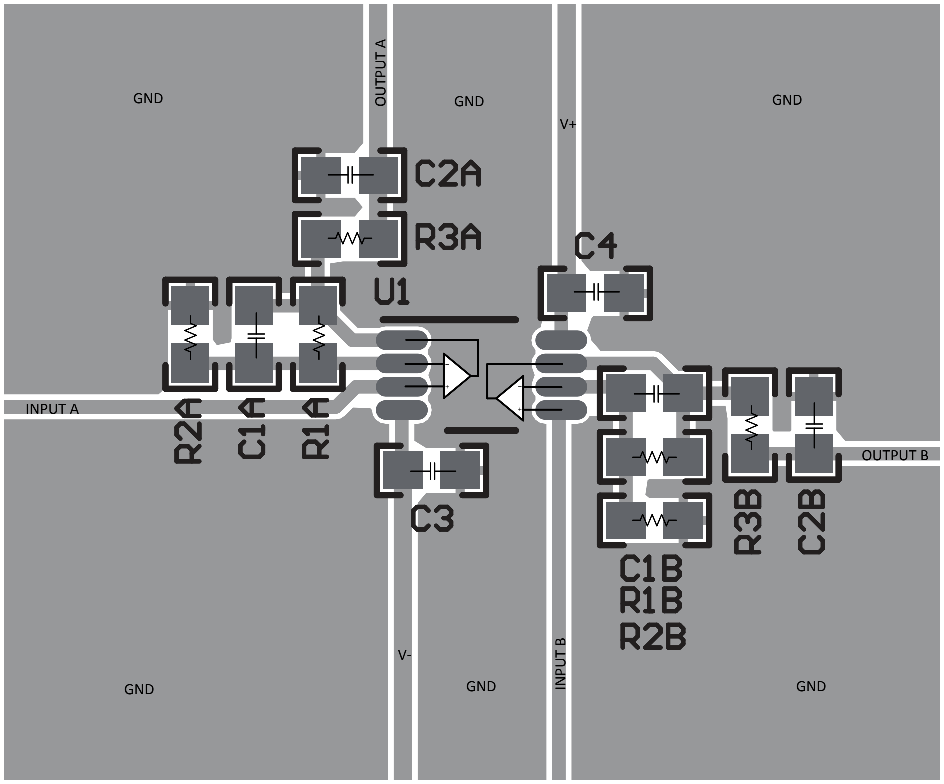


Figure 7-4. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note
- Texas Instruments, *0-1-A, Single-Supply, Low-Side, Current Sensing Solution* reference design (TIPD129)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2024) to Revision B (October 2024) **Page**

- Changed the data sheet status from *Production Mixed* to *Production Data* 1
- Removed the OPA994-Q1 preview note from the *Device Information* table... 1

Changes from Revision * (November 2023) to Revision A (October 2024) **Page**

- Change the data sheet status from Advanced Information to Production Mixed.. 1
- Updated the maximum recommended supply voltage from 24V to 32V throughout data sheet........................ 1
- Updated the typical gain bandwidth product from 25MHz to 24MHz throughout data sheet.............................. 1
- Updated the typical output short-circuit current from 150mA to 125mA throughout data sheet......................... 1
- Changed the status of OPA994QDBVRQ1 and OPA2994QDRQ1 from: *preview* to: *active* 1
- Added device typical characteristic curves in *Typical Characteristics* section.. 9

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2994QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2994Q
OPA2994QDRQ1.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2994Q
OPA994QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	QODBV
OPA994QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	QODBV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2994-Q1, OPA994-Q1 :

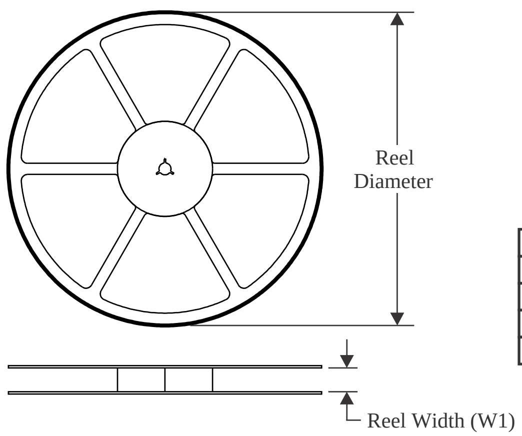
- Catalog : OPA2994, OPA994

NOTE: Qualified Version Definitions:

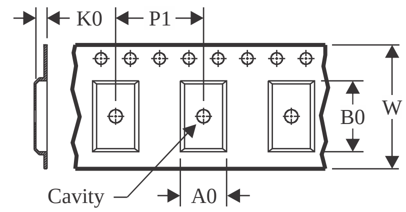
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

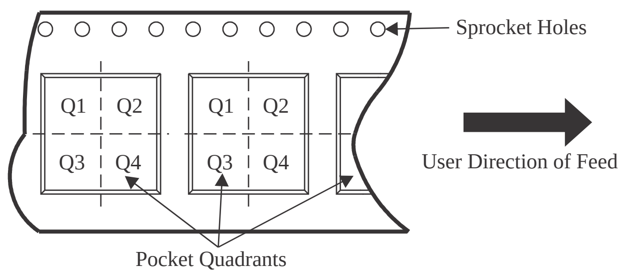


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

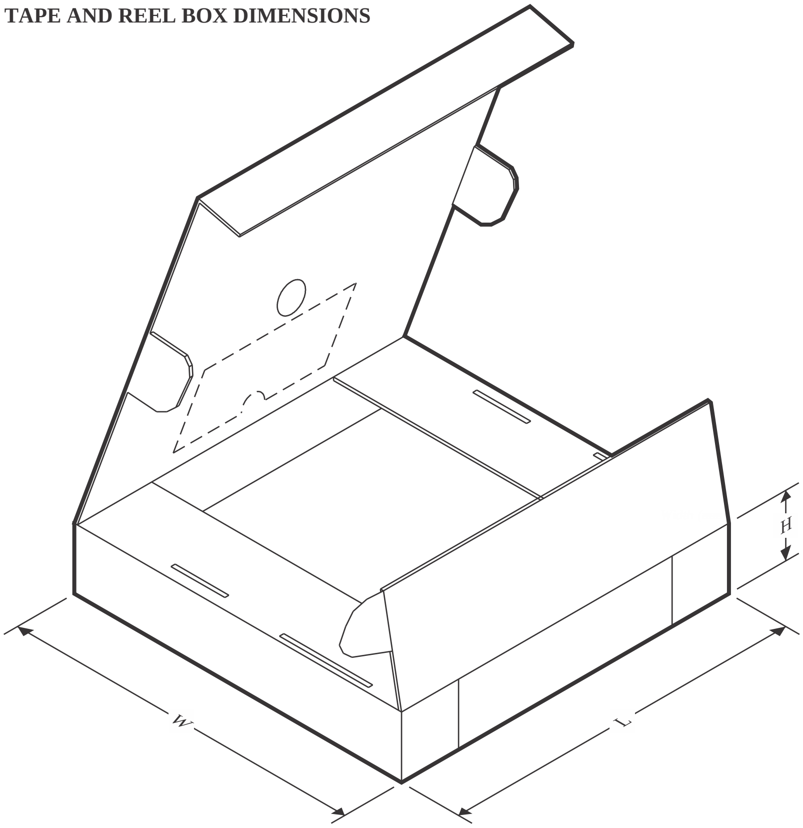
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

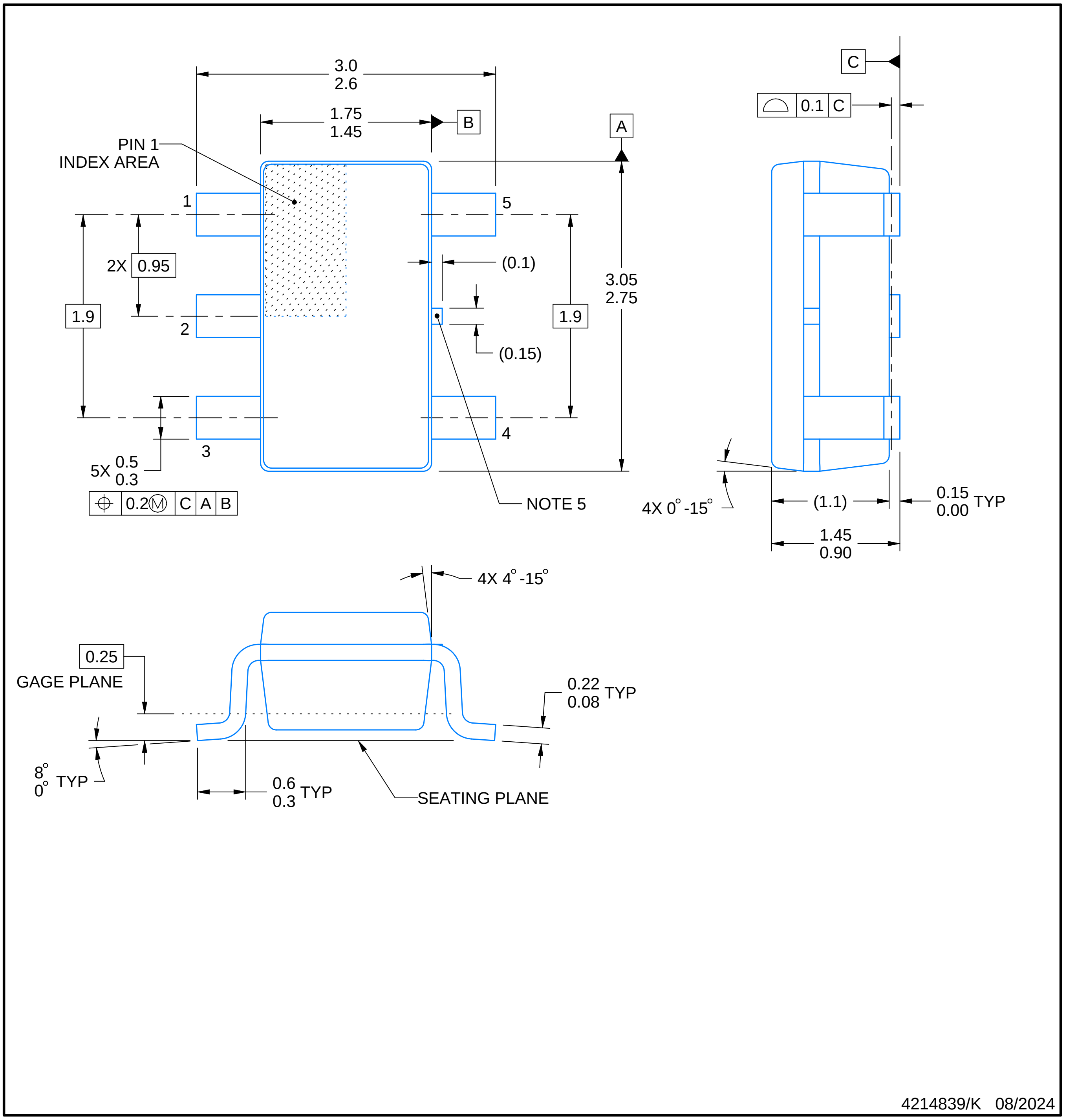
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2994QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA994QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



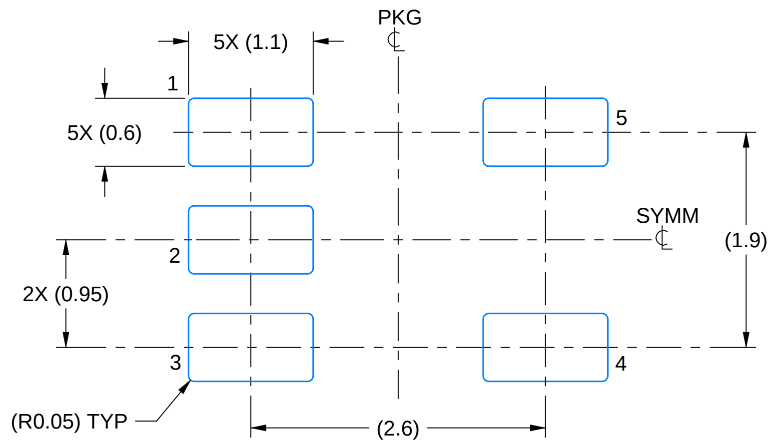
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2994QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
OPA994QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

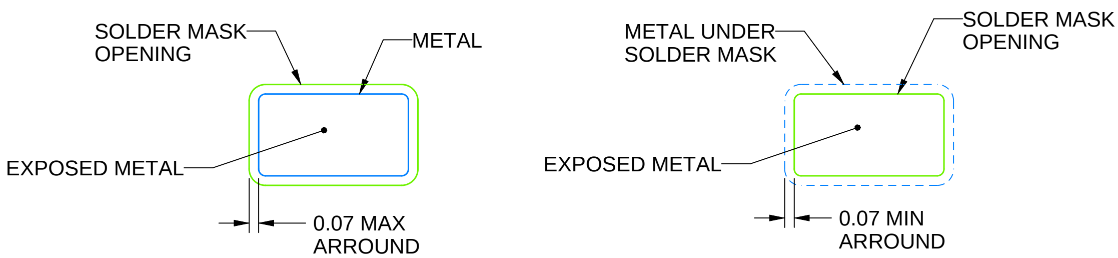


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

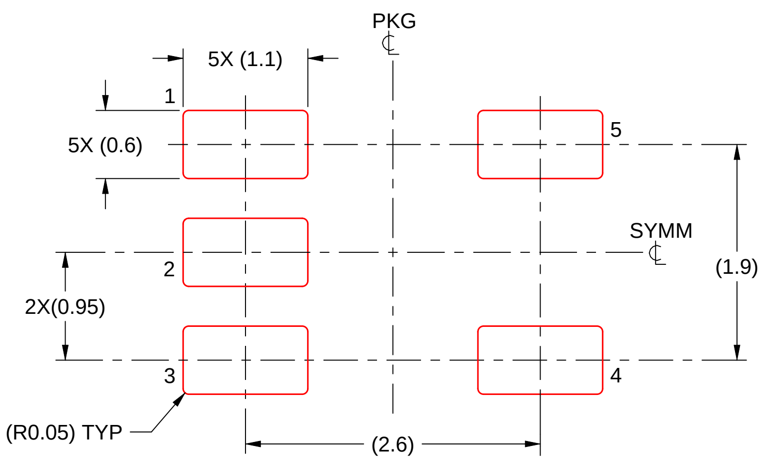
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

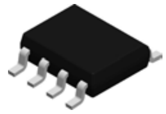


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

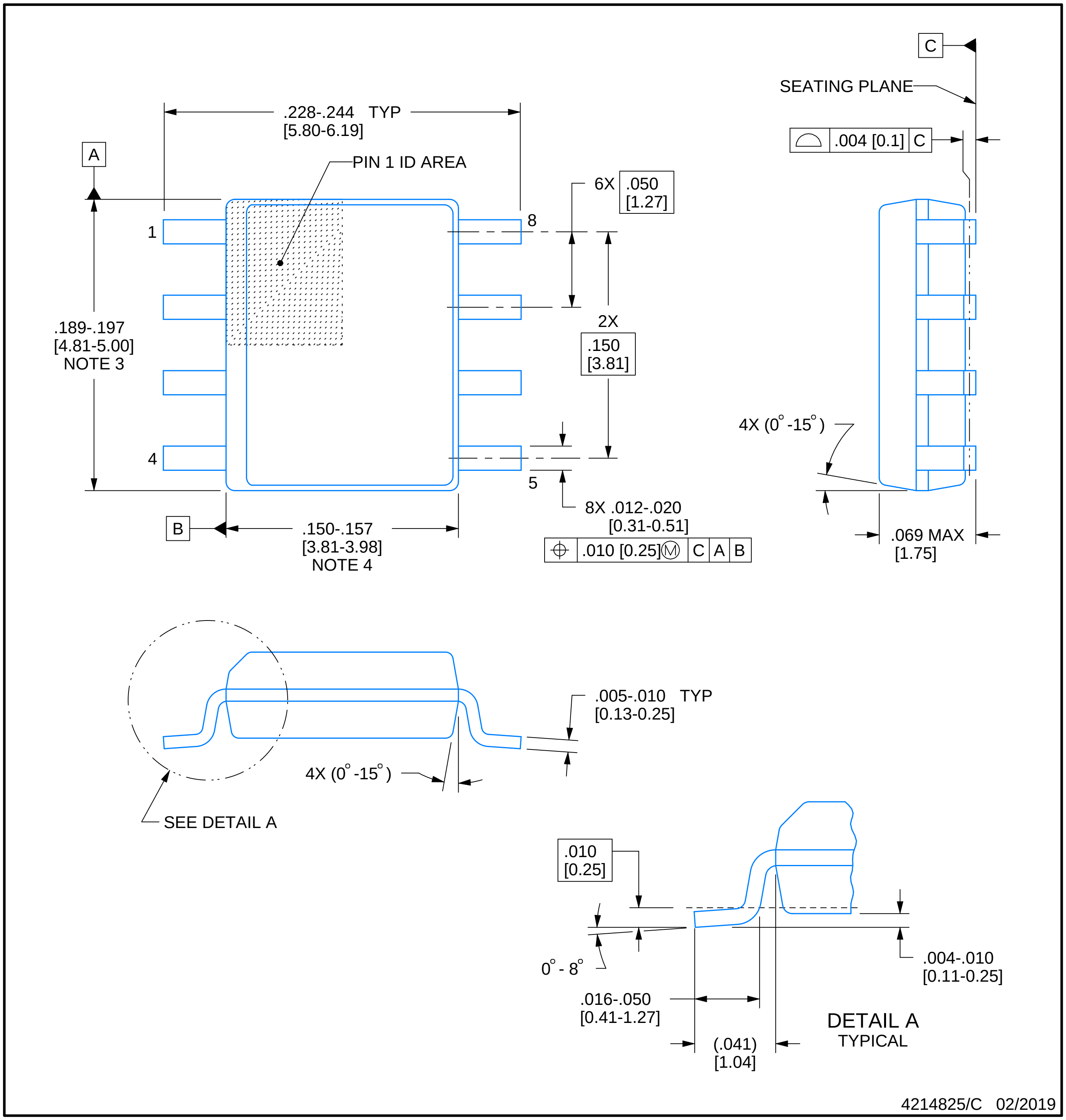


PACKAGE OUTLINE

D0008A

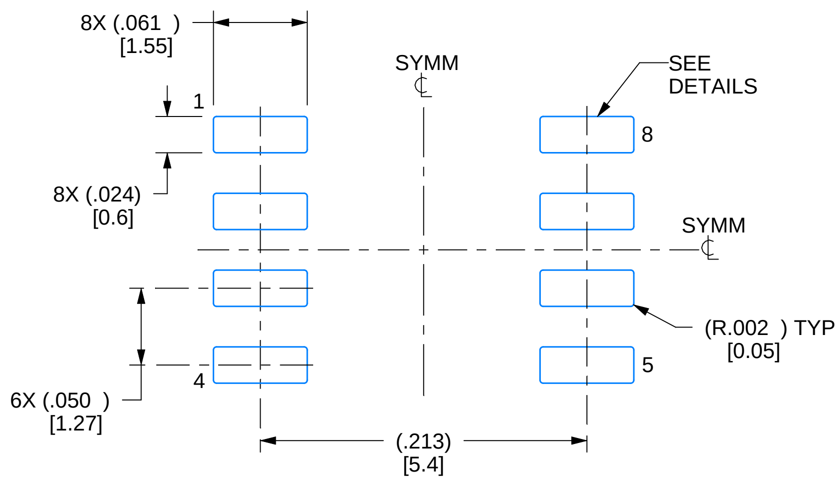
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

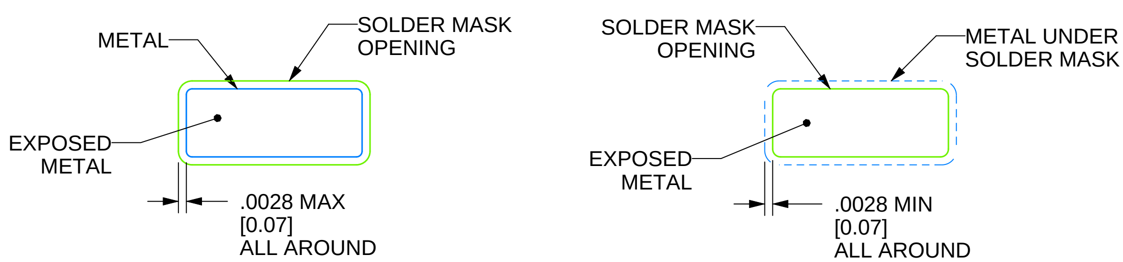


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

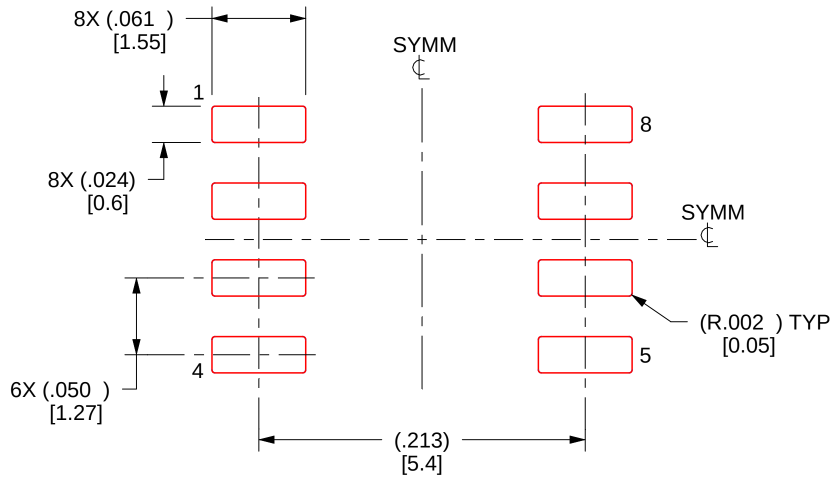
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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