

OPA838 1mA, 300MHz Gain Bandwidth, Voltage-Feedback Op Amp

1 Features

- Gain bandwidth product: 300MHz
- Very-low (trimmed) supply current: 950 μ A
- Bandwidth: 90MHz ($A_V = 6V/V$)
- High full-power bandwidth: 45MHz, 4V_{PP}
- Negative rail input, rail-to-rail output
- Single-supply operating range: 2.7V to 5.4V
- 25°C input offset: $\pm 125\mu V$ (maximum)
- Input offset voltage drift: $< \pm 1.6\mu V/^\circ C$ (maximum)
- Input voltage noise: 1.8nV/ \sqrt{Hz} ($> 200Hz$)
- Input current noise: 1pA/ \sqrt{Hz} ($> 2000Hz$)
- $< 1\mu A$ shutdown current for power savings

2 Applications

- Low-power transimpedance amplifier
- Low-noise high-gain stage
- 12-bit to 16-bit low-power SAR ADC driver
- High-gain active filter design
- Ultrasonic flow meter

3 Description

The OPA838 decompensated voltage-feedback operational amplifier provides a high, 300MHz gain bandwidth product with 1.8nV/ \sqrt{Hz} input noise voltage, requiring only a trimmed 0.95mA supply current. These features combine to provide an extremely power-efficient device for photodiode transimpedance designs and high-voltage gain stages, which require the lowest input voltage noise in signal receiver applications.

Operating at the minimum recommended noninverting gain of 6V/V results in a 90MHz, $-3dB$ bandwidth. Extremely low input noise and offset voltage make the OPA838 an excellent choice for high gains. Even at a dc-coupled gain of 1000V/V, a 300kHz signal bandwidth is available with a maximum output offset voltage of $\pm 125mV$.

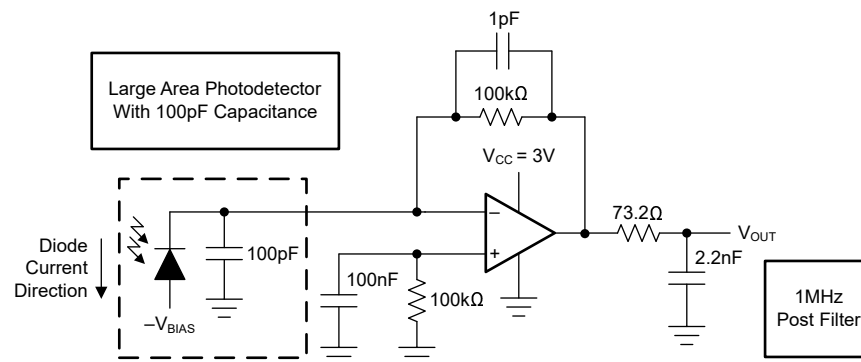
The single-channel OPA838 is available in 6-pin SOT-23, 6-pin SC70, and 8-pin X2QFN packages, all with a power shutdown feature. The OPA838 is also available in a 5-pin SC70 package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
OPA838	DBV (SOT-23, 6)	2.9mm \times 2.8mm
	DCK (SC70, 5)	2mm \times 1.25mm
	DCK (SC70, 6)	2mm \times 1.5mm
	DXB (X2QFN, 8)	1.4mm \times 1.2mm

(1) For more information, see [Section 11](#).

(2) The package size (length \times width) is a nominal value and includes pins, where applicable.



Single 3V Supply, $< 3mW$ Photodiode Amplifier With $< 1.1pA/\sqrt{Hz}$ Total Input-Referred Current Noise and 100k Ω Gain With Overall 1MHz SSBW



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4 Related Products

PART NUMBER ⁽¹⁾	GBP (MHz)	5V I_Q (mA, MAXIMUM 25°C)	INPUT NOISE VOLTAGE (nV/ $\sqrt{\text{Hz}}$)	2V _{PP} THD (dBc, 100kHz)	RAIL-TO-RAIL INPUT/OUTPUT	DUALS
OPA838	300	0.99	1.9	–110	Negative in/out	None
OPA837	50	0.625	4.7	–120	Negative in/out	OPA2837
OPA835	30	0.35	9.3	–100	Negative in/out	OPA2835
OPA836	110	1	4.8	–115	Negative in/out	OPA2836
LMP7717	88	1.4	5.8	—	Negative in/out	LMP7718
OPA830	100	4.7	9.5	–105	Negative in/out	OPA2830
THS4281	38	0.93	12.5	12.5	In/out	None

(1) For a complete selection of TI high-speed amplifiers, visit www.ti.com.

5 Pin Configuration and Functions

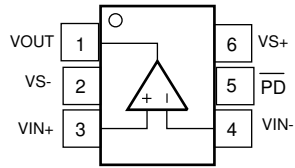


Figure 5-1. DBV Package, 6-Pin SOT-23 and DCK Package, 6-Pin SC70 (Top View)

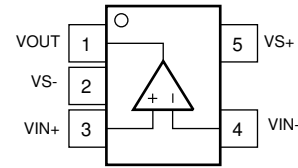


Figure 5-2. DCK Package, 5-Pin SC70 (Top View)

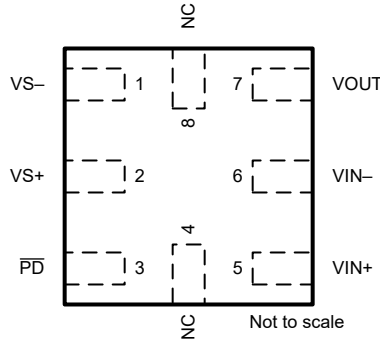


Figure 5-3. DXB Package, 8-Pin X2QFN (Top View)

Table 5-1. Pin Functions

NAME	PIN NO.			TYPE	DESCRIPTION
	DBV (SOT-23), DCK (SC70, 6)	DCK (SC70, 5)	DXB (X2QFN)		
NC	—	—	4, 8	NC	No connect pin. This pin is not internally connected.
$\overline{\text{PD}}$	5	—	3	Input/Output	Amplifier power down. Low = disabled, high = normal operation (pin must be driven).
VIN–	4	4	6	Input/Output	Inverting input pin
VIN+	3	3	5	Input/Output	Noninverting input pin
VOUT	1	1	7	Input/Output	Output pin
VS–	2	2	1	Power	Negative power-supply pin
VS+	6	5	2	Power	Positive power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		5.5	V
	Supply turn-on and turn-off maximum dV/dT ⁽²⁾		1	V/ μ s
V_I	Input voltage	$V_{S-} - 0.5$	$V_{S+} + 0.5$	V
V_{ID}	Differential input voltage		± 1	V
I_I	Continuous input current		± 10	mA
I_O	Continuous output current ⁽³⁾		± 20	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Stay below this \pm supply turn-on edge rate to prevent the edge-triggered ESD absorption device across the supply pins from turning on.
- (3) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply voltage	2.7	5	5.4	V
T_A	Ambient temperature	-40	25	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA838				UNIT
		DBV (SOT-23)	DCK (SC70)	DCKS (SC70)	DXB (X2SON)	
		6 PINS	5 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194	203	189	194	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	129	152	150	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39	76	79	109	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26	58	61	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39	76	79	109	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics $V_S = 5\text{ V}$

at $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL ⁽¹⁾
AC PERFORMANCE							
SSBW	Small-signal bandwidth	$V_{OUT} = 20\text{ mV}_{PP}$, $G = 6$, (peaking $< 4\text{ dB}$)	75	90		MHz	C
		$V_{OUT} = 20\text{ mV}_{PP}$, $G = 10$, $R_F = 1.6\text{ k}\Omega$		50			C
		$V_{OUT} = 20\text{ mV}_{PP}$, $G = 100$, $R_F = 16.9\text{ k}\Omega$		3			C
GBP	Gain-bandwidth product	$V_{OUT} = 20\text{ mV}_{PP}$, $G = 100$	240	300		MHz	C
LSBW	Large-signal bandwidth	$V_{OUT} = 2\text{ V}_{PP}$, $G = 6$		45		MHz	C
	Bandwidth for 0.1-dB flatness	$V_{OUT} = 200\text{ mV}_{PP}$, $G = 6$		10		MHz	C
SR	Slew rate	From LSBW ⁽²⁾	250	350		V/ μs	C
	Overshoot, undershoot	$V_{OUT} = 2\text{-V step}$, $G = 6$, input $t_R = 12\text{ ns}$		1%	2%		C
t_R , t_F	Rise, fall time	$V_{OUT} = 2\text{-V step}$, $G = 6$, $R_L = 2\text{ k}\Omega$, input $t_R = 12\text{ ns}$		12.5	13	ns	C
	Settling time to 0.1%	$V_{OUT} = 2\text{-V step}$, $G = 6$, input $t_R = 12\text{ ns}$		30		ns	C
	Settling time to 0.01%	$V_{OUT} = 2\text{-V step}$, $G = 6$, input $t_R = 12\text{ ns}$		40		ns	C
HD2	Second-order harmonic distortion	$f = 100\text{ kHz}$, $V_O = 4\text{ V}_{PP}$, $G = 6$ (see Figure 8-1)		-110		dBc	C
HD3	Third-order harmonic distortion	$f = 100\text{ kHz}$, $V_O = 4\text{ V}_{PP}$, $G = 6$ (see Figure 8-1)		-120		dBc	C
	Input voltage noise	$f > 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$	C
	Voltage noise 1/f corner frequency			100		Hz	C
	Input current noise	$f > 100\text{ kHz}$		1		pA/ $\sqrt{\text{Hz}}$	C
	Current noise 1/f corner frequency			7		kHz	C
	Overdrive recovery time	$G = 6$, 2 x output overdrive, dc-coupled		50		ns	C
	Closed-loop output impedance	$f = 1\text{ MHz}$, $G = 6$		0.3		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	$V_O = \pm 2\text{ V}$, $R_L = 2\text{ k}\Omega$	120	125		dB	A
	Input-referred offset voltage	$T_A \approx 25^\circ\text{C}$ (DXB package)	-150	± 15	150	μV	A
		$T_A \approx 25^\circ\text{C}$	-125	± 15	125		A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-165	± 15	200		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-230	± 15	220		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-230	± 15	285		B
	Input offset voltage drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$ ⁽⁴⁾	-1.6	± 0.4	1.6	$\mu\text{V}/^\circ\text{C}$	B
	Input bias current ⁽³⁾	$T_A \approx 25^\circ\text{C}$	0.7	1.5	2.8	μA	A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	0.2	1.5	3.5		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	0.2	1.5	3.7		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	0.2	1.5	4.4		B
	Input bias current drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	4.5	7.8	17	nA/ $^\circ\text{C}$	B
	Input offset current	$T_A \approx 25^\circ\text{C}$ (DXB package)	-100	± 20	100	nA	A
		$T_A \approx 25^\circ\text{C}$	-70	± 20	70		A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-83	± 20	93		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-105	± 20	100		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-105	± 20	120		B
	Input offset current drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-500	± 40	500	pA/ $^\circ\text{C}$	B

6.5 Electrical Characteristics $V_S = 5\text{ V}$ (continued)

at $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL ⁽¹⁾
INPUT							
	Common-mode input range, low	$T_A \approx 25^\circ\text{C}$, CMRR > 92 dB	$V_{S-} - 0.2$	$V_{S-} - 0$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, CMRR > 92 dB	$V_{S-} - 0$				B
	Common-mode input range, high	$T_A \approx 25^\circ\text{C}$, CMRR > 92 dB	$V_{S+} - 1.3$	$V_{S+} - 1.2$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, CMRR > 92 dB	$V_{S+} - 1.3$				B
CMRR	Common-mode rejection ratio		95	105		dB	A
	Input impedance common-mode			35 1		M Ω pF	C
	Input impedance differential mode			30 1.3		k Ω pF	C
OUTPUT							
V_{OL}	Output voltage, low	$T_A \approx 25^\circ\text{C}$, $G = 6$	$V_{S-} + 0.05$	$V_{S-} + 0.1$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 6$	$V_{S-} + 0.05$	$V_{S-} + 0.1$			B
V_{OH}	Output voltage, high	$T_A \approx 25^\circ\text{C}$, $G = 6$	$V_{S+} - 0.1$	$V_{S+} - 0.05$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 6$	$V_{S+} - 0.2$	$V_{S+} - 0.1$			B
	Max current into a resistive load	$T_A \approx 25^\circ\text{C}$, $\pm 1.53\text{ V}$ into $41.3\text{ }\Omega$, $V_{IO} < 2\text{ mV}$	± 35	± 40		mA	A
	Linear current into a resistive load	$T_A \approx 25^\circ\text{C}$, $\pm 1.81\text{ V}$ into $70.6\text{ }\Omega$, $A_{OL} > 80\text{ dB}$	± 25	± 28		mA	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $\pm 1.58\text{ V}$ into $70.6\text{ }\Omega$, $A_{OL} > 80\text{ dB}$	± 22	± 25			B
	DC output impedance	$G = 6$		0.02		Ω	C
POWER SUPPLY							
	Specified operating voltage		2.7	5	5.4	V	B
	Quiescent operating current	$T_A \approx 25^\circ\text{C}$ (DXB package) ⁽⁶⁾	900	960	1025	μA	A
		$T_A \approx 25^\circ\text{C}$ ⁽⁶⁾	913	960	1025		A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	700	960	1365		B
dlq/dT	Quiescent current temperature coefficient	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	2.6	3	3.4	$\mu\text{A}/^\circ\text{C}$	B
+PSRR	Positive power-supply rejection ratio		98	110		dB	A
-PSRR	Negative power-supply rejection ratio		93	105		dB	A
POWER DOWN (Pin Must be Driven, SOT23-6 and SC70-6)							
	Enable voltage threshold	Specified <i>on</i> above $V_{S+} + 1.5\text{ V}$	1.5			V	A
	Disable voltage threshold	Specified <i>off</i> below $V_{S+} + 0.55\text{ V}$			0.55	V	A
	Disable pin bias current	$\overline{\text{PD}} = V_{S-}$ to V_{S+}	-50	20	50	nA	A
	Power-down quiescent current	$\overline{\text{PD}} = 0.55\text{ V}$		0.1	1	μA	A
	Turn-on time delay	Time from $\overline{\text{PD}} = \text{high}$ to $V_{OUT} = 90\%$ of final value		1.7		μs	C
	Turn-off time delay	Time from $\overline{\text{PD}} = \text{low}$ to $V_{OUT} = 10\%$ of original value		100		ns	C

- (1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C , overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
- (2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(0.8 \times V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{-3dB}$ where this f_{-3dB} is the typical measured 4- V_{PP} bandwidth at gains of 6 V/V.
- (3) Current is considered positive out of the pin.
- (4) Input offset voltage drift, input bias current drift, and input offset current drift typical specifications are mean $\pm 1\sigma$ characterized by the full temperature range end-point data. Maximum drift specifications are set by the min, max packaged test range on the wafer-level screened drift. Drift is not specified by the final automated test equipment (ATE) or by QA sample testing.
- (5) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
- (6) The typical specification is at 25°C T_J . The minimum and maximum limits are expanded for the ATE to account for an ambient range from 22°C to 32°C with a $4\text{-}\mu\text{A}/^\circ\text{C}$ temperature coefficient on the supply current.

6.6 Electrical Characteristics $V_S = 3\text{ V}$

at $V_{S+} = 3\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL ⁽¹⁾
AC PERFORMANCE							
SSBW	Small-signal bandwidth	$V_{OUT} = 20\text{ mV}_{PP}$, $G = 6$ (peaking $< 4\text{ dB}$)	70	86		MHz	C
		$V_{OUT} = 20\text{ mV}_{PP}$, $G = 10$, $R_F = 1.6\text{ k}\Omega$		50			C
		$V_{OUT} = 20\text{ mV}_{PP}$, $G = 100$, $R_F = 16.9\text{ k}\Omega$		3			C
GBP	Gain-bandwidth product	$V_{OUT} = 20\text{ mV}_{PP}$, $G = 100$	240	300		MHz	C
LSBW	Large-signal bandwidth	$V_{OUT} = 2\text{ V}_{PP}$, $G = 6$		45		MHz	C
	Bandwidth for 0.1-dB flatness	$V_{OUT} = 200\text{ mV}_{PP}$, $G = 6$		9		MHz	C
SR	Slew rate	From LSBW ⁽²⁾	250	350		V/ μs	C
	Overshoot, undershoot	$V_{OUT} = 1\text{-V step}$, $G = 6$, input $t_R = 6\text{ ns}$		2%	4%		C
t_R , t_F	Rise, fall time	$V_{OUT} = 1\text{-V step}$, $G = 6$, input $t_R = 6\text{ ns}$		6.3	7	ns	C
	Settling time to 0.1%	$V_{OUT} = 1\text{-V step}$, $G = 6$, input $t_R = 6\text{ ns}$		30		ns	C
	Settling time to 0.01%	$V_{OUT} = 1\text{-V step}$, $G = 6$, input $t_R = 6\text{ ns}$		40		ns	C
HD2	Second-order harmonic distortion	$f = 100\text{ kHz}$, $V_O = 2\text{ V}_{PP}$, $G = 6$ (see Figure 8-1)		-108		dBc	C
HD3	Third-order harmonic distortion	$f = 100\text{ kHz}$, $V_O = 2\text{ V}_{PP}$, $G = 6$ (see Figure 8-1)		-125		dBc	C
		$f = 100\text{ kHz}$, $V_O = 2\text{ V}_{PP}$, $G = 6$ (DXB Package)		-110			
	Input voltage noise	$f > 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$	C
	Voltage noise 1/f corner frequency			100		Hz	C
	Input current noise	$f > 100\text{ kHz}$		1.0		pA/ $\sqrt{\text{Hz}}$	C
	Current noise 1/f corner frequency			7		kHz	C
	Overdrive recovery time	$G = 6$, 2 x output overdrive, dc-coupled		50		ns	C
	Closed-loop output impedance	$f = 1\text{ MHz}$, $G = 6$		0.3		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	$V_O = \pm 1\text{ V}$, $R_L = 2\text{ k}\Omega$	110	125		dB	A
	Input-referred offset voltage	$T_A \approx 25^\circ\text{C}$ (DXB package)	-150	± 15	150	μV	A
		$T_A \approx 25^\circ\text{C}$	-125	± 15	125		A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-165	± 15	200		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-230	± 15	220		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-230	± 15	285		B
	Input offset voltage drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$ ⁽⁴⁾	-1.6	± 0.4	1.6	$\mu\text{V}/^\circ\text{C}$	B
	Input bias current ⁽³⁾	$T_A \approx 25^\circ\text{C}$	0.7	1.5	2.8	μA	A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	0.2	1.5	3.5		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	0.2	1.5	3.7		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	0.2	1.5	4.4		B
	Input bias current drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	4.5	7.8	17	nA/ $^\circ\text{C}$	B
	Input offset current	$T_A \approx 25^\circ\text{C}$ (DXB package)	-100	± 20	100	nA	A
		$T_A \approx 25^\circ\text{C}$	-70	± 20	70		A
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$	-83	± 20	93		B
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-105	± 20	100		B
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-105	± 13	120		B
	Input offset current drift ⁽⁵⁾	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-500	± 20	500	pA/ $^\circ\text{C}$	B

6.6 Electrical Characteristics $V_S = 3\text{ V}$ (continued)

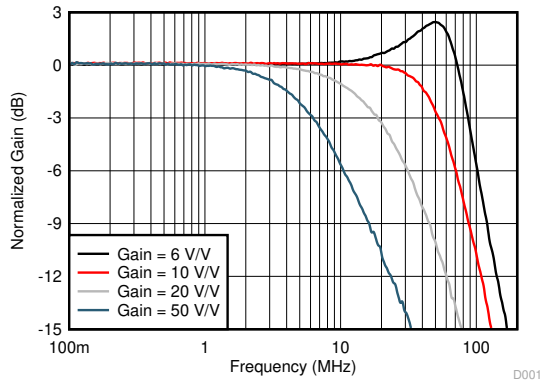
at $V_{S+} = 3\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL ⁽¹⁾
INPUT							
	Common-mode input range, low	$T_A \approx 25^\circ\text{C}$, CMRR > 92 dB	$V_{S-} - 0.2$	$V_{S-} - 0$		V	A
		$T_A = -40^\circ\text{C}$ to 125°C , CMRR > 92 dB	$V_{S-} - 0$			V	B
	Common-mode input range, high	$T_A \approx 25^\circ\text{C}$, CMRR > 92 dB	$V_{S+} - 1.3$	$V_{S+} - 1.2$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, CMRR > 92 dB	$V_{S+} - 1.3$			V	B
CMRR	Common-mode rejection ratio		95	105		dB	A
	Input impedance common-mode		55 1.1			M Ω pF	C
	Input impedance differential mode		30 1.3			k Ω pF	C
OUTPUT							
V_{OL}	Output voltage, low	$T_A \approx 25^\circ\text{C}$, $G = 6$	$V_{S-} + 0.05$	$V_{S-} + 0.1$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 6$	$V_{S-} + 0.1$	$V_{S-} + 0.2$		V	B
V_{OH}	Output voltage, high	$T_A \approx 25^\circ\text{C}$, $G = 6$	$V_{S+} - 0.1$	$V_{S+} - 0.05$		V	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 6$	$V_{S+} - 0.2$	$V_{S+} - 0.1$		V	B
	Max current into a resistive load	$T_A \approx 25^\circ\text{C}$, $\pm 0.77\text{ V}$ into $26.7\text{ }\Omega$, $V_{IO} < 2\text{ mV}$	± 28	± 30		mA	A
	Linear current into a resistive load	$T_A \approx 25^\circ\text{C}$, $\pm 0.88\text{ V}$ into $37\text{ }\Omega$, $A_{OL} > 70\text{ dB}$	± 23	± 25		mA	A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $\pm 0.76\text{ V}$ into $37\text{ }\Omega$, $A_{OL} > 70\text{ dB}$	± 20	± 23		mA	B
	DC output impedance	$G = 6$		0.02		Ω	C
POWER SUPPLY							
	Specified operating voltage		2.7	5	5.4	V	B
	Quiescent operating current	$T_A \approx 25^\circ\text{C}$ (DXB package) ⁽⁶⁾	875	930	970	μA	A
		$T_A \approx 25^\circ\text{C}$ ⁽⁶⁾	890	930	970		A
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	680	930	1350		B
dlq/dT	Quiescent current temperature coefficient	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	2.2	2.7	3.2	$\mu\text{A}/^\circ\text{C}$	B
+PSRR	Positive power-supply rejection ratio		95	110		dB	A
-PSRR	Negative power-supply rejection ratio		90	105		dB	A
POWER DOWN (Pin Must be Driven, SOT23-6 and SC70-6)							
	Enable voltage threshold	Specified <i>on</i> above $V_{S-} + 1.5\text{ V}$	1.5			V	A
	Disable voltage threshold	Specified <i>off</i> below $V_{S-} + 0.55\text{ V}$			0.55	V	A
	Disable pin bias current	$\overline{PD} = V_{S-}$ to V_{S+}	-50	20	50	nA	A
	Power-down quiescent current	$\overline{PD} = 0.55\text{ V}$		0.1	1	μA	A
	Turn-on time delay	Time from $\overline{PD} = \text{high}$ to $V_{OUT} = 90\%$ of final value		3.5		μs	C
	Turn-off time delay	Time from $\overline{PD} = \text{low}$ to $V_{OUT} = 10\%$ of original value		100		ns	C

- Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C , overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
- This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(0.8 \times V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{-3dB}$ where this f_{-3dB} is the typical measured 4-VPP bandwidth at gains of 6 V/V.
- Current is considered positive out of the pin.
- Input offset voltage drift, input bias current drift, and input offset current drift typical specifications are mean $\pm 1\sigma$ characterized by the full temperature range end-point data. Maximum drift specifications are set by the min, max packaged test range on the wafer-level screened drift. Drift is not specified by the final automated test equipment (ATE) or by QA sample testing.
- Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
- The typical specification is at 25°C T_J . The minimum and maximum limits are expanded for the ATE to account for an ambient range from 22°C to 32°C with a $4\text{-}\mu\text{A}/^\circ\text{C}$ temperature coefficient on the supply current.

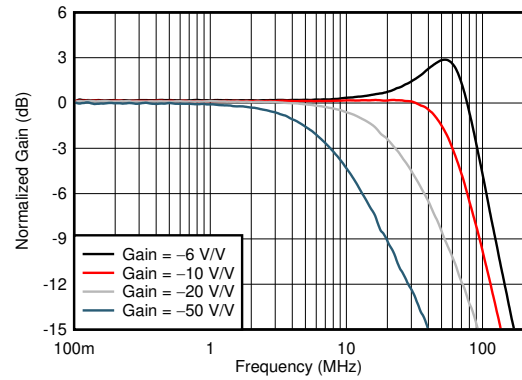
6.7 Typical Characteristics: $V_S = 5\text{ V}$

at $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$ (unless otherwise noted)



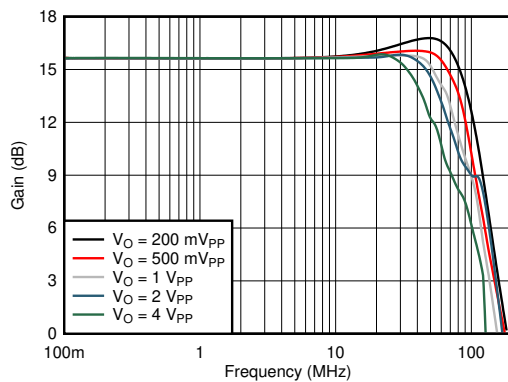
See Figure 8-1 and Table 8-1 ($V_O = 20\text{ mV}_{PP}$, $R_{LOAD} = 2\text{ k}\Omega$)

Figure 6-1. Noninverting Small-Signal Frequency Response vs Gain



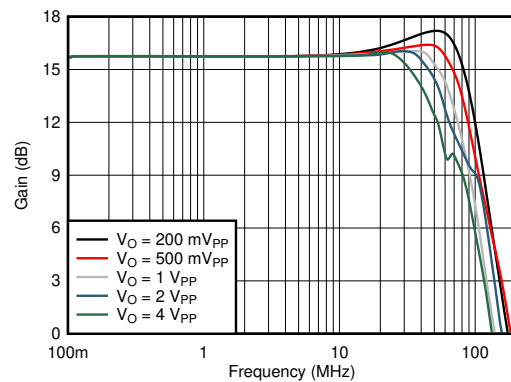
See Figure 8-2 and Table 8-2 ($V_O = 20\text{ mV}_{PP}$, $R_{LOAD} = 2\text{ k}\Omega$)

Figure 6-2. Inverting Small-Signal Frequency Response vs Gain



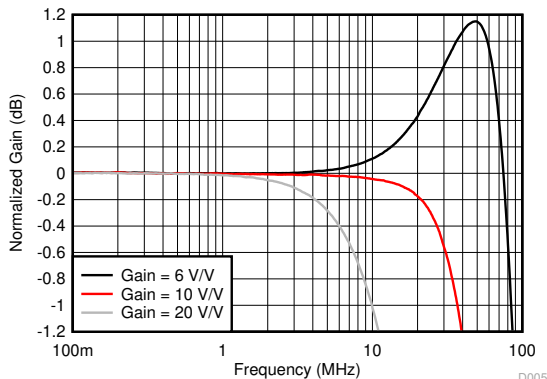
Gain = 6 V/V , $R_{LOAD} = 2\text{ k}\Omega$

Figure 6-3. Noninverting Large-Signal Bandwidth vs V_{OPP}



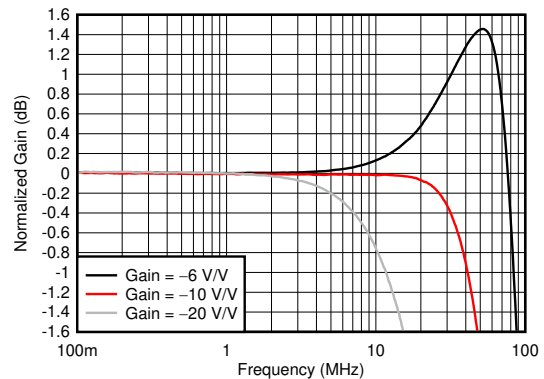
Gain = -6 V/V , $R_{LOAD} = 2\text{ k}\Omega$

Figure 6-4. Inverting Large-Signal Bandwidth vs V_{OPP}



See Figure 8-1 and Table 8-1 ($V_O = 200\text{ mV}_{PP}$, $R_{LOAD} = 2\text{ k}\Omega$)

Figure 6-5. Noninverting Response Flatness vs Gain

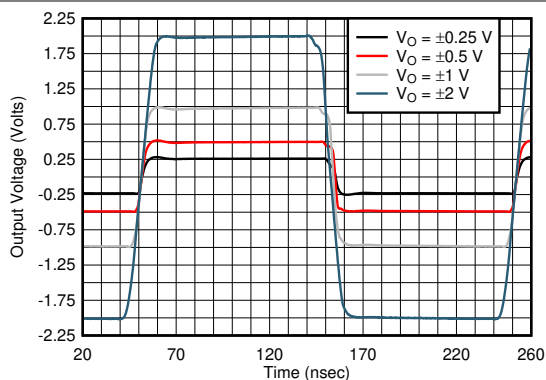


See Figure 8-2 and Table 8-2 ($V_O = 200\text{ mV}_{PP}$, $R_{LOAD} = 2\text{ k}\Omega$)

Figure 6-6. Inverting Response Flatness vs Gain

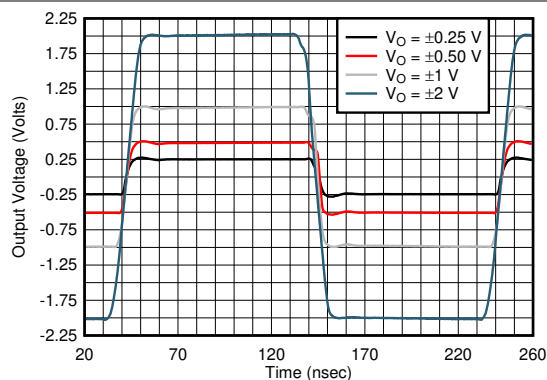
6.7 Typical Characteristics: $V_S = 5\text{ V}$ (continued)

at $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$ (unless otherwise noted)



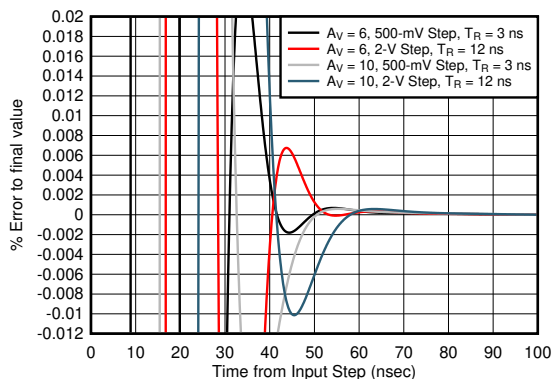
See Figure 8-1 (gain of 6 V/V)

Figure 6-7. Noninverting Step Response vs V_{OPP}



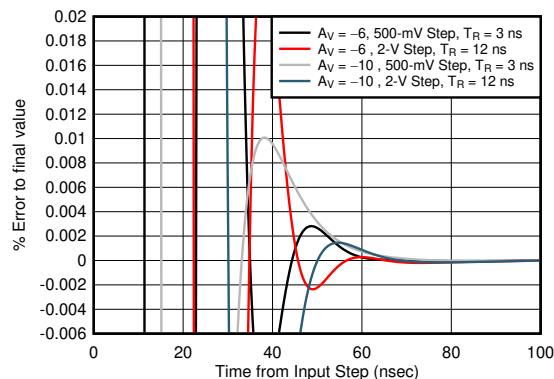
See Figure 8-2 (gain of -6 V/V)

Figure 6-8. Inverting Step Response vs V_{OPP}



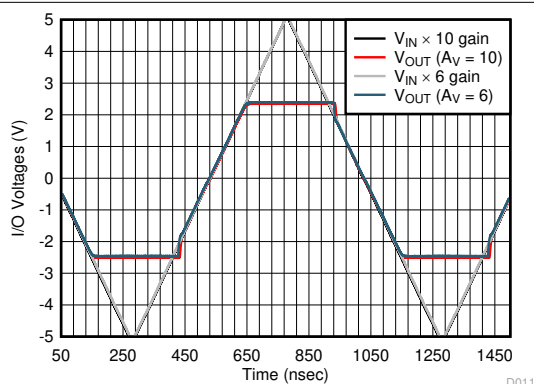
See Figure 8-1 and Table 8-1

Figure 6-9. Simulated Noninverting Settling Time



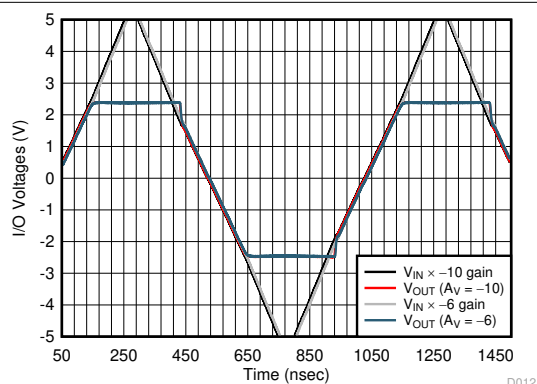
See Figure 8-2 and Table 8-2

Figure 6-10. Simulated Inverting Settling Time



See Figure 8-1 and Table 8-1

Figure 6-11. Noninverting Overdrive Recovery

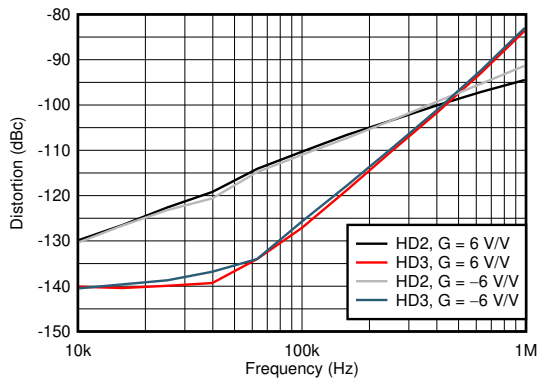


See Figure 8-2 and Table 8-2

Figure 6-12. Inverting Overdrive Recovery

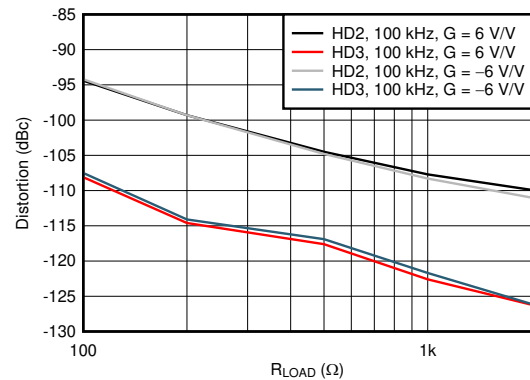
6.7 Typical Characteristics: $V_S = 5\text{ V}$ (continued)

at $V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A \approx 25^\circ\text{C}$ (unless otherwise noted)



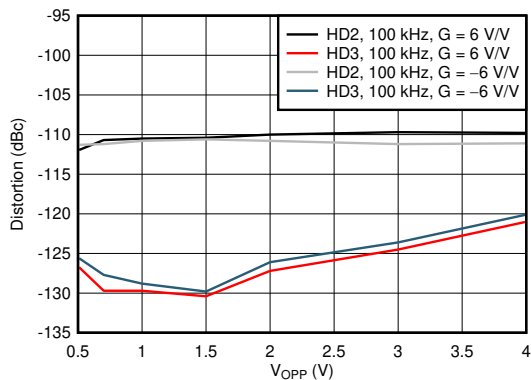
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2

Figure 6-13. Harmonic Distortion vs Frequency



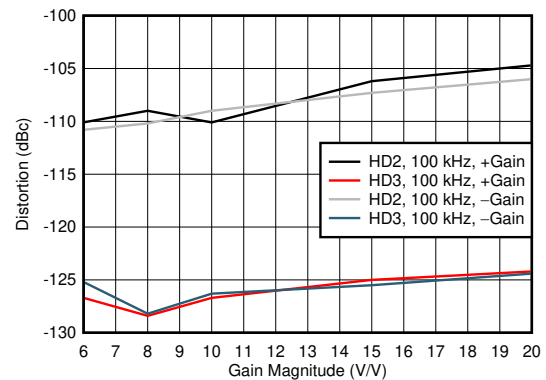
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2
 $V_O = 2\text{ V}_{PP}$, $f = 100\text{ kHz}$

Figure 6-14. Harmonic Distortion vs R_{LOAD}



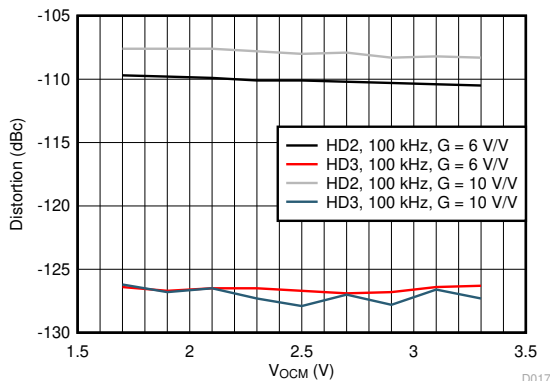
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2
 $f = 100\text{ kHz}$, $R_{LOAD} = 2\text{ k}\Omega$

Figure 6-15. Harmonic Distortion vs Output Swing



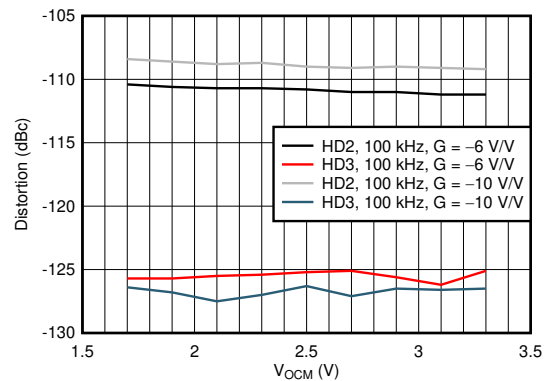
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2
 $V_O = 2\text{ V}_{PP}$, $R_{LOAD} = 2\text{ k}\Omega$, $f = 100\text{ kHz}$

Figure 6-16. Harmonic Distortion vs Gain



See Figure 8-1 and Table 8-1
 $V_O = 2\text{ V}_{PP}$, $f = 100\text{ kHz}$, $R_{LOAD} = 2\text{ k}\Omega$

Figure 6-17. Noninverting Distortion vs Output Common-Mode Voltage



See Figure 8-2 and Table 8-2
 $V_O = 2\text{ V}_{PP}$, $f = 100\text{ kHz}$, $R_{LOAD} = 2\text{ k}\Omega$

Figure 6-18. Inverting Distortion vs Output Common-Mode Voltage

6.8 Typical Characteristics: $V_S = 3\text{ V}$

at $V_{S+} = 3\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\ \Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

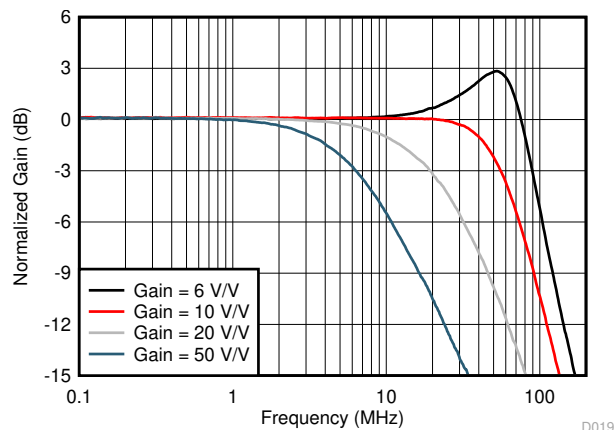


Figure 6-19. Noninverting Small-Signal Response vs Gain

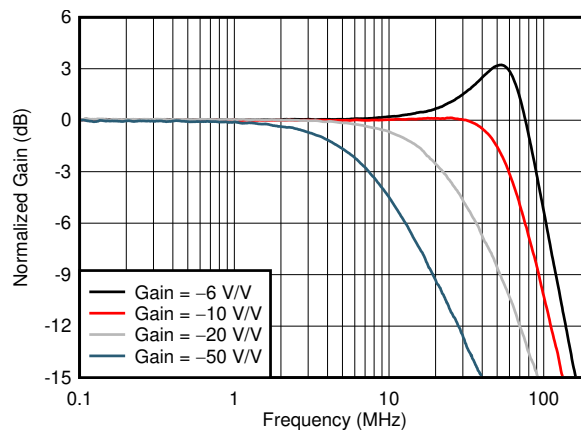


Figure 6-20. Inverting Small-Signal Response vs Gain

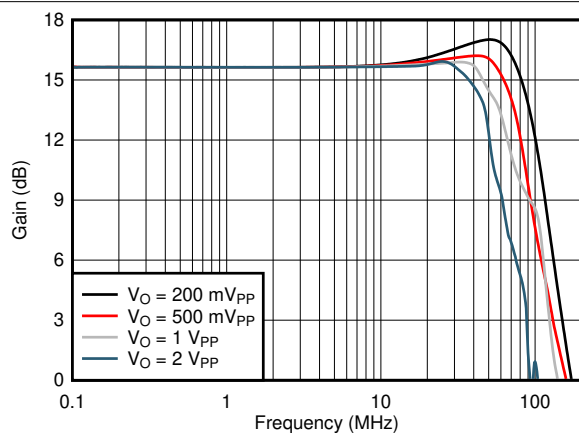


Figure 6-21. Noninverting Large-Signal Bandwidth vs V_{OPP}

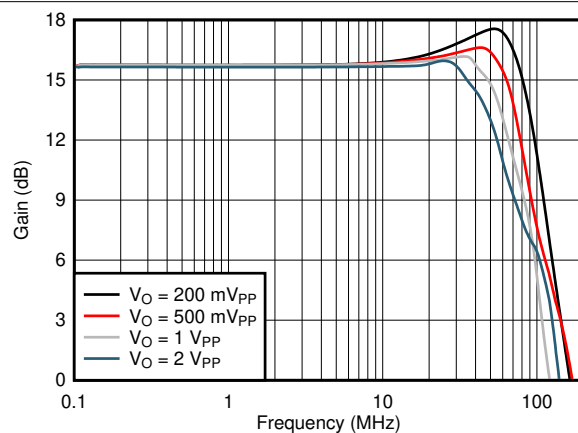


Figure 6-22. Inverting Large-Signal Bandwidth vs V_{OPP}

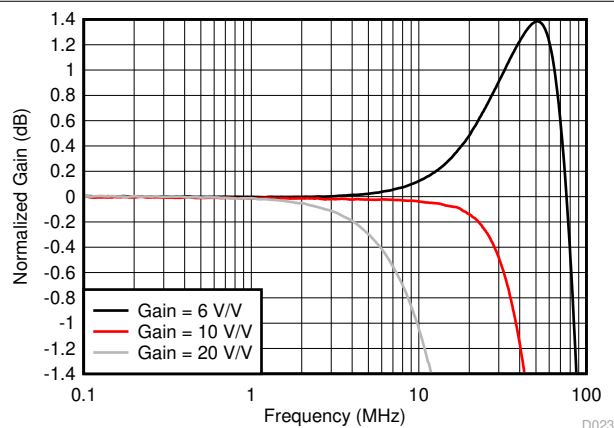


Figure 6-23. Noninverting Response Flatness vs Gain

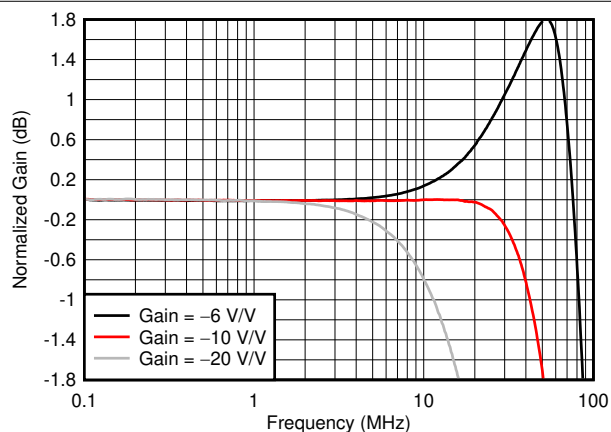
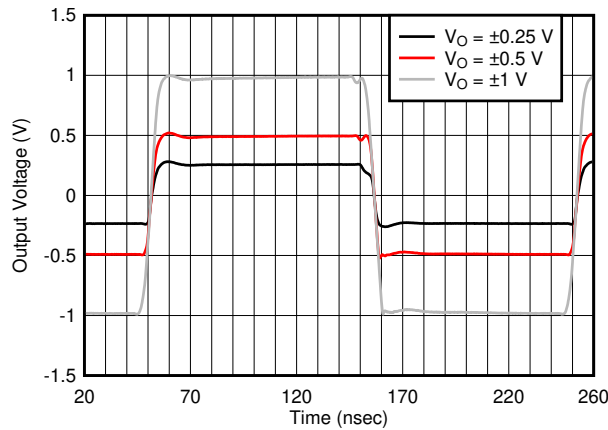


Figure 6-24. Inverting Response Flatness vs Gain

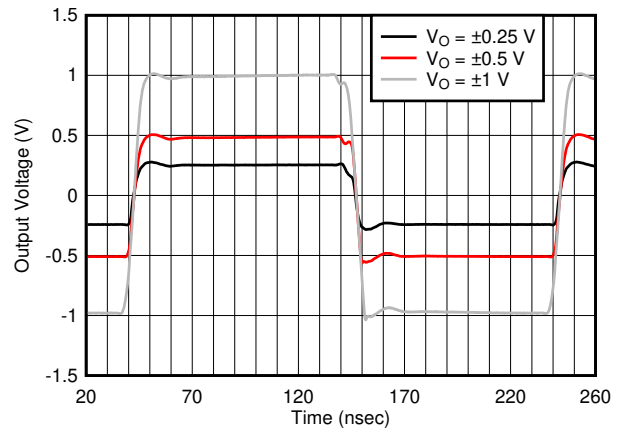
6.8 Typical Characteristics: $V_S = 3\text{ V}$ (continued)

at $V_{S+} = 3\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



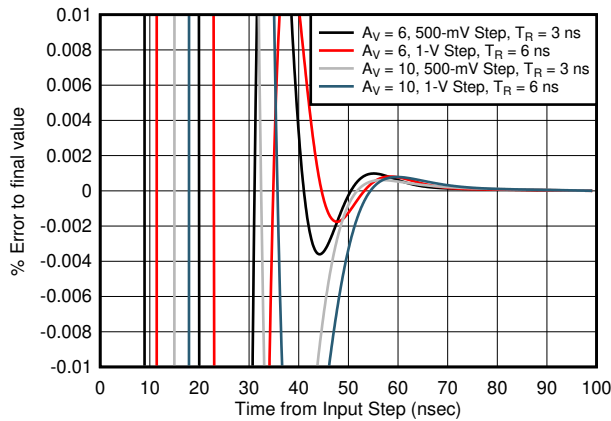
See [Figure 8-1](#) and [Table 8-1](#)

Figure 6-25. Noninverting Step Response vs V_{OPP}



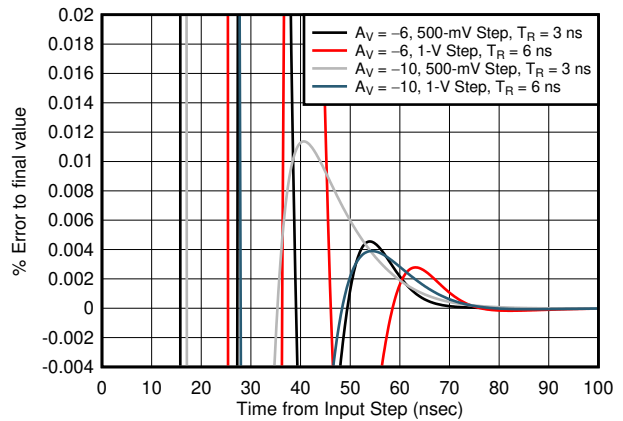
See [Figure 8-2](#) and [Table 8-2](#)

Figure 6-26. Inverting Step Response vs V_{OPP}



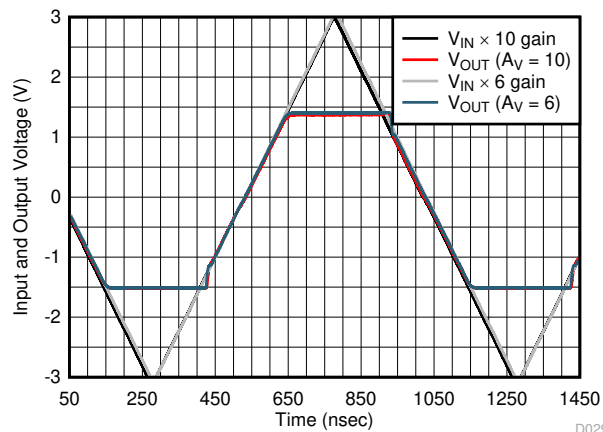
See [Figure 8-1](#) and [Table 8-1](#)

Figure 6-27. Noninverting Settling Time



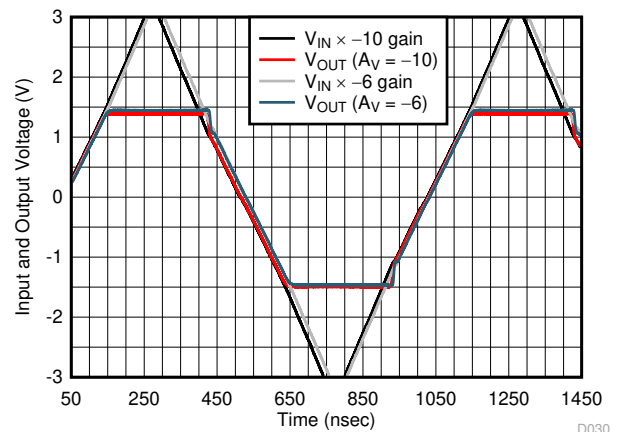
See [Figure 8-2](#) and [Table 8-2](#)

Figure 6-28. Inverting Settling Time



See [Figure 8-1](#) and [Table 8-1](#)

Figure 6-29. Noninverting Overdrive Recovery

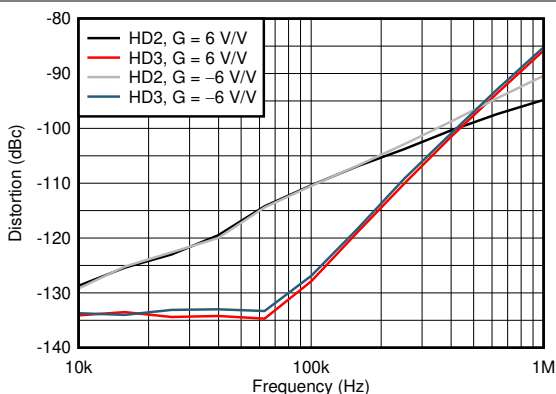


See [Figure 8-2](#) and [Table 8-2](#)

Figure 6-30. Inverting Overdrive Recovery

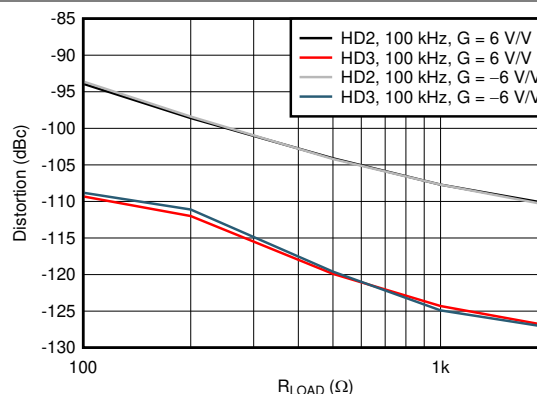
6.8 Typical Characteristics: $V_S = 3\text{ V}$ (continued)

at $V_{S+} = 3\text{ V}$, $V_{S-} = 0\text{ V}$, $R_F = 1\text{ k}\Omega$, $R_G = 200\text{ }\Omega$, $R_L = 2\text{ k}\Omega$, $G = 6\text{ V/V}$, input and output referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



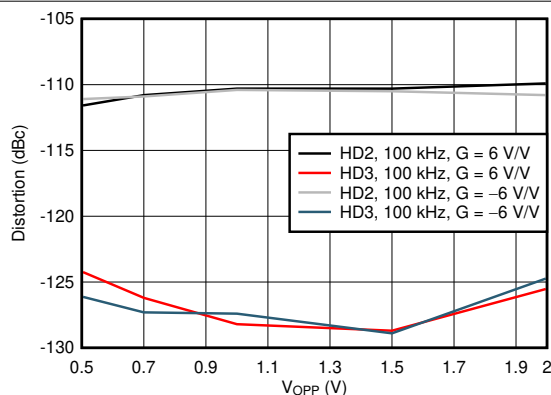
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2

Figure 6-31. Harmonic Distortion vs Frequency



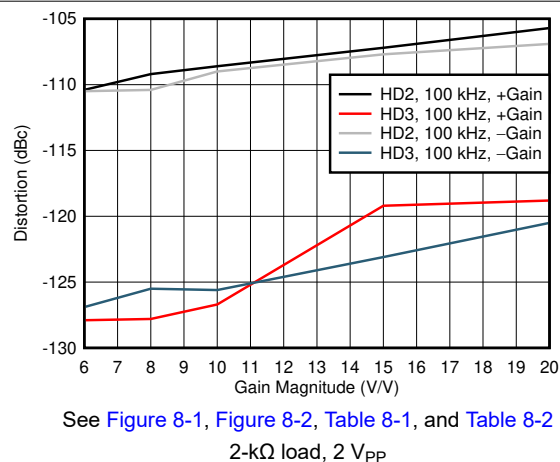
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2

Figure 6-32. Harmonic Distortion vs Load



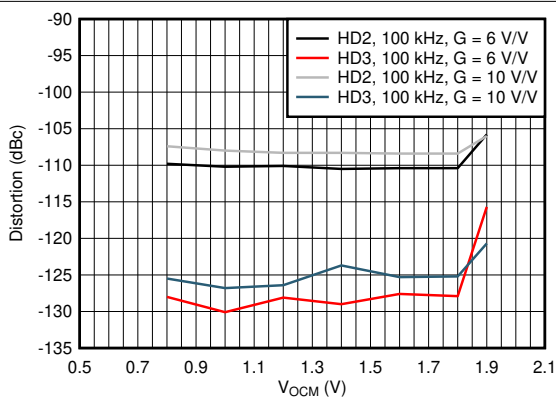
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2

Figure 6-33. Harmonic Distortion vs Output Swing



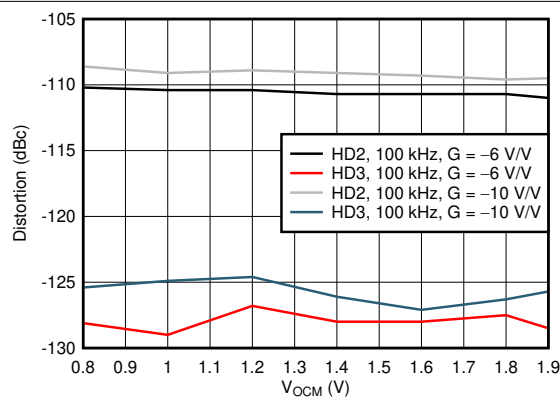
See Figure 8-1, Figure 8-2, Table 8-1, and Table 8-2
2-k Ω load, 2 V_{pp}

Figure 6-34. Harmonic Distortion vs Gain



See Figure 8-1 and Table 8-1, $V_O = 1\text{ V}_{PP}$

Figure 6-35. Noninverting Harmonic Distortion vs Output Common-Mode Voltage



See Figure 8-2 and Table 8-2, $V_O = 1\text{ V}_{PP}$

Figure 6-36. Inverting Harmonic Distortion vs Output Common-Mode Voltage

6.9 Typical Characteristics: Over Supply Range

at $\overline{PD} = V_{S+}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

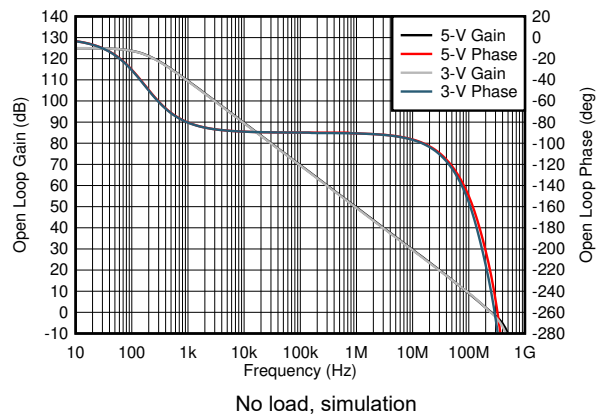


Figure 6-37. Open-Loop Gain and Phase

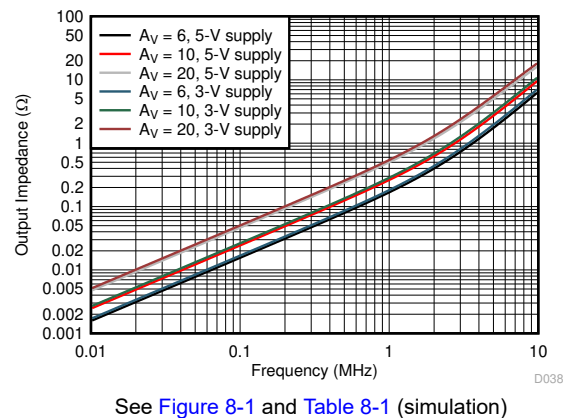


Figure 6-38. Closed-Loop Output Impedance

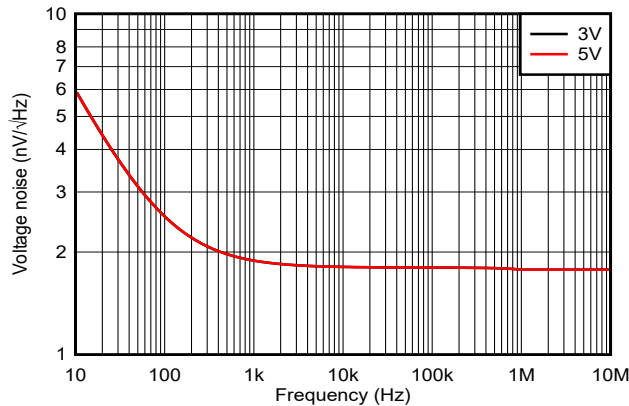


Figure 6-39. Input Voltage Noise Density

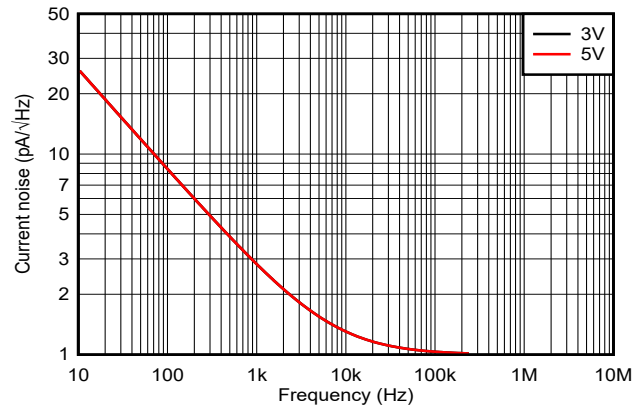


Figure 6-40. Input Current Noise Density

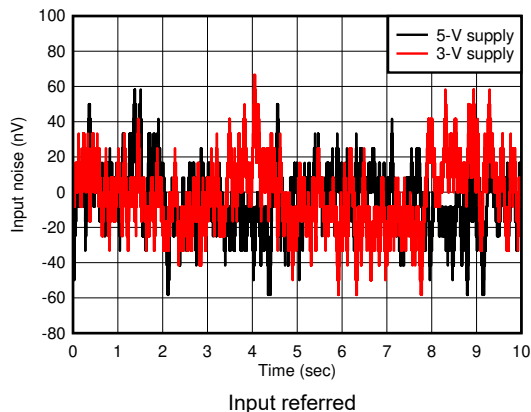


Figure 6-41. Low-Frequency Voltage Noise

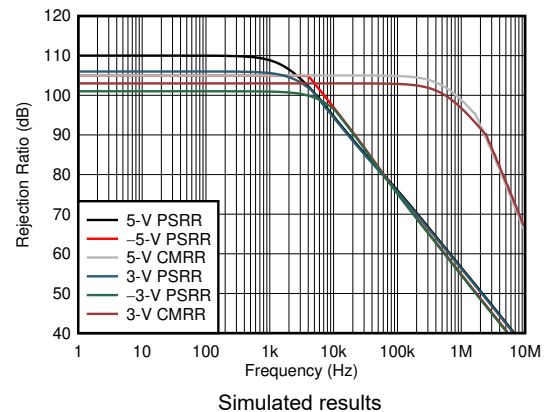


Figure 6-42. PSRR and CMRR

6.9 Typical Characteristics: Over Supply Range (continued)

at $\overline{PD} = V_{S+}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

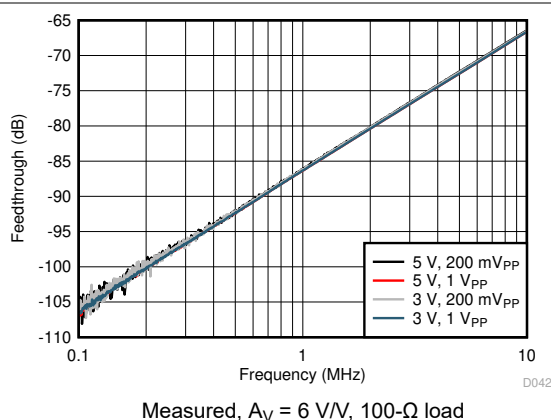


Figure 6-43. Disabled Isolation Noninverting Input to Output

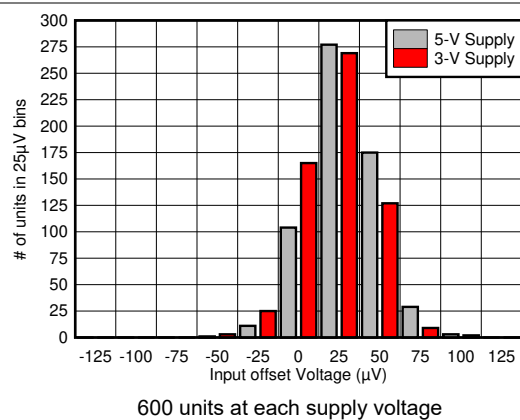


Figure 6-44. Input Offset Voltage Distribution

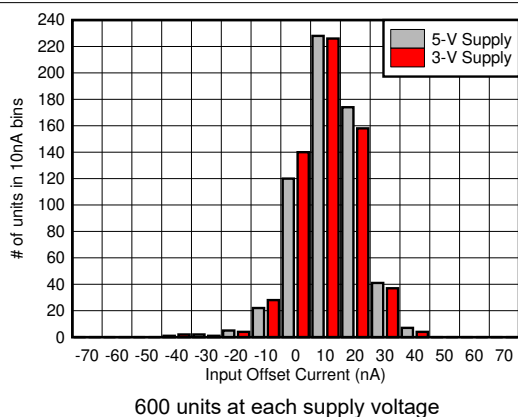


Figure 6-45. Input Offset Current Distribution

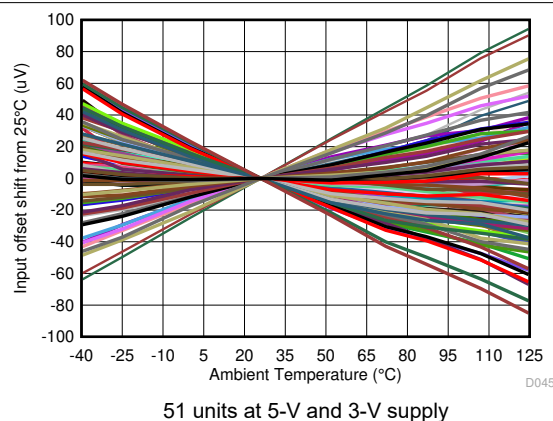


Figure 6-46. Input Offset Voltage vs Temperature

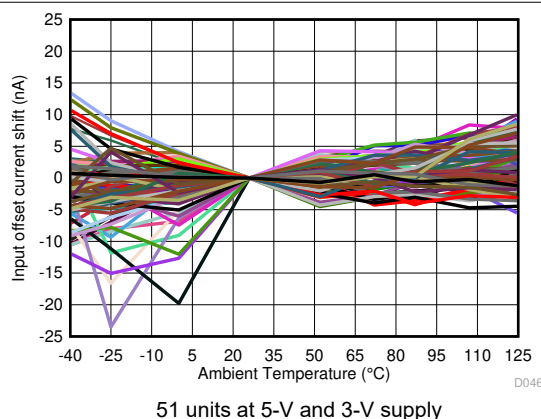


Figure 6-47. Input Offset Current vs Temperature

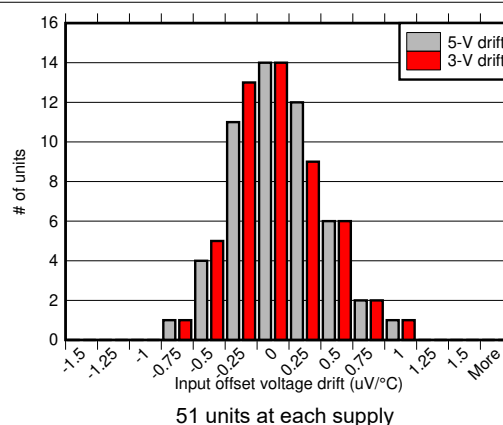
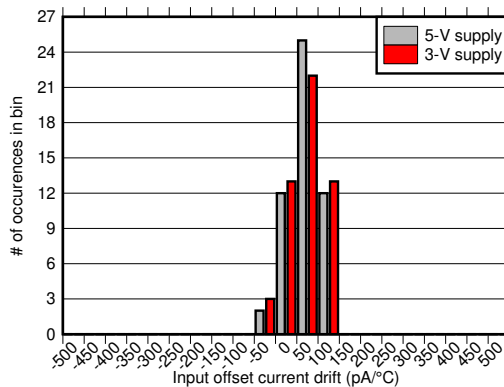


Figure 6-48. Input Offset Voltage Drift Distribution

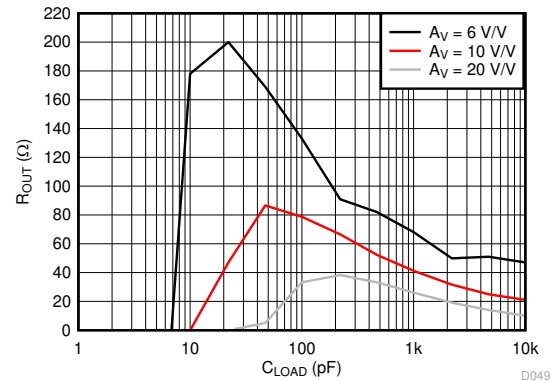
6.9 Typical Characteristics: Over Supply Range (continued)

at $\overline{PD} = V_{S+}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



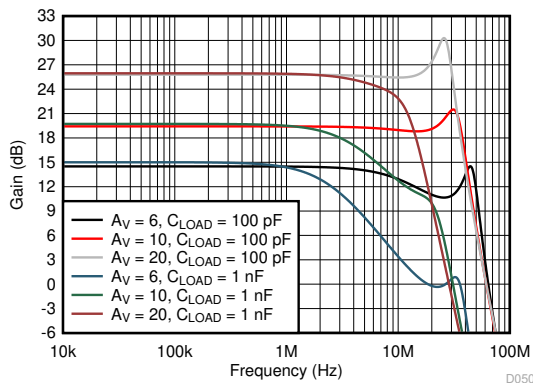
51 units at each supply

Figure 6-49. Input Offset Current Drift Distribution



See [Figure 7-6](#) and [Table 8-1](#)
small signal, targeting 30° phase margin

Figure 6-50. Output Resistor vs C_{LOAD}



See [Figure 7-6](#) and [Table 8-1](#)
2-kΩ parallel load to C_{LOAD}

Figure 6-51. Small-Signal Response Shapes vs C_{LOAD} With Recommended R_{OUT}

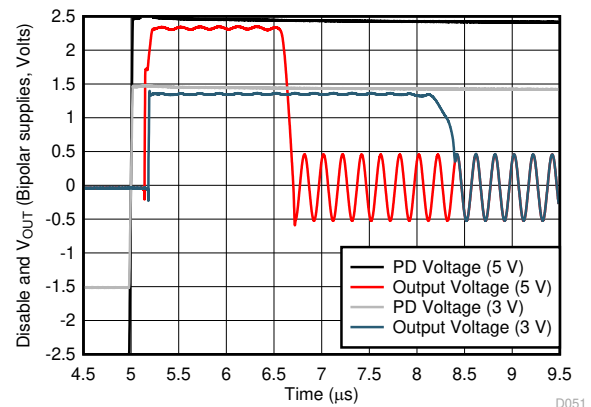


Figure 6-52. Turn-On Time to Sinusoidal Input

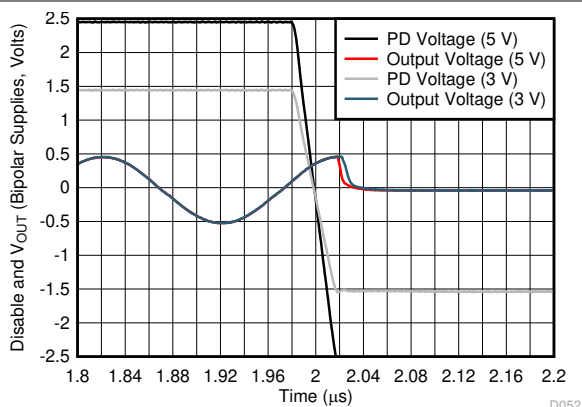
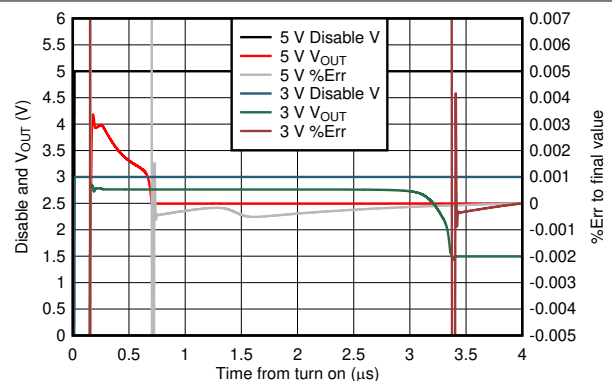


Figure 6-53. Turn-Off Time to Sinusoidal Input

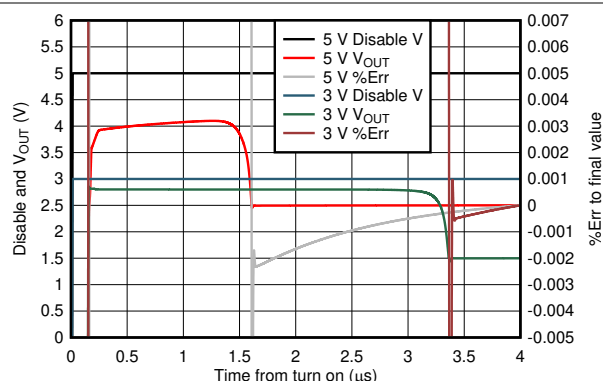


Single-supply, DC input to produce midscale output
(simulation)

Figure 6-54. Gain of 6-V/V Turn-On Time to Final DC Value at Midscale

6.9 Typical Characteristics: Over Supply Range (continued)

at $\overline{\text{PD}} = \text{V}_{\text{S}+}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



Single-supply, DC input to produce midscale output
(simulation)

Figure 6-55. Gain of 10-V/V Turn-On Time to Final DC Value at Midscale

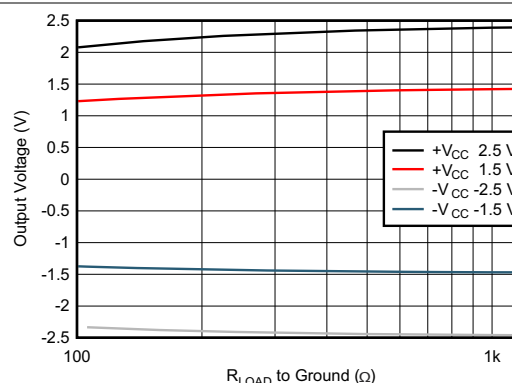


Figure 6-56. Output Voltage Swing vs Load Resistor

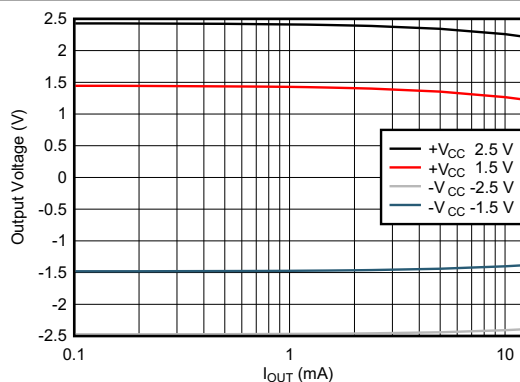


Figure 6-57. Output Saturation Voltage vs Load Current

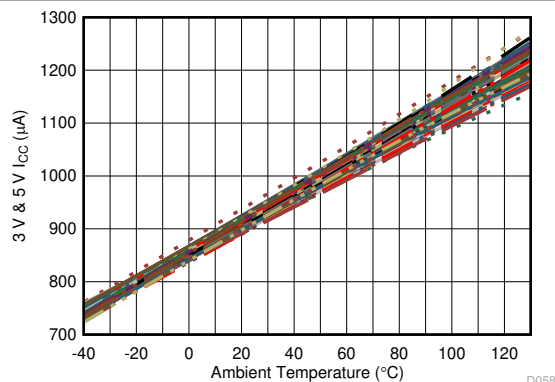
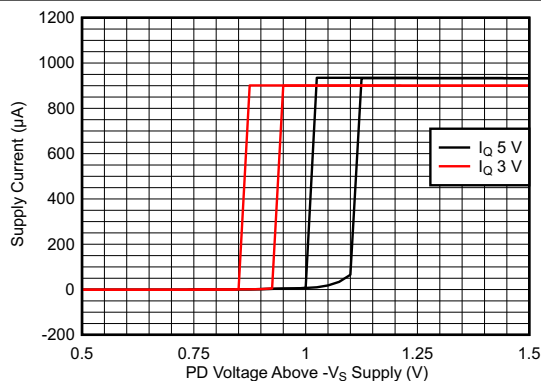
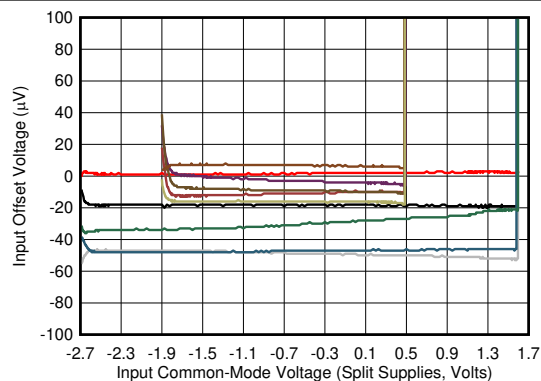


Figure 6-58. Quiescent Current vs Temperature



**Figure 6-59. Supply Current vs Power-Down Voltage:
Turn On Higher Than Turn Off**



**Figure 6-60. Input Offset Voltage vs Input Common-
Mode Voltage**

6.9 Typical Characteristics: Over Supply Range (continued)

at $\overline{PD} = V_{S+}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

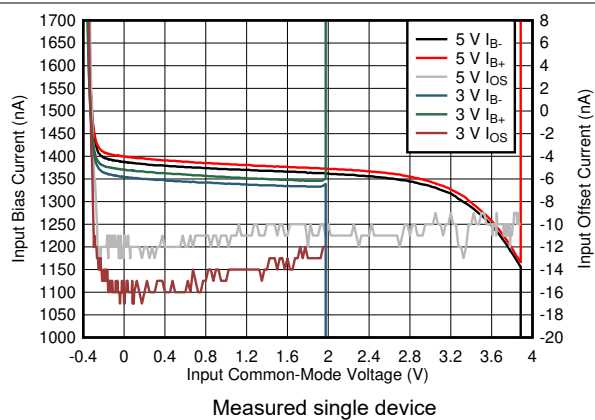


Figure 6-61. Input Bias and Offset Current vs V_{ICM}

7 Detailed Description

7.1 Overview

The OPA838 is a power-efficient, decompensated, voltage-feedback amplifier (VFA). Combining a negative-rail input stage and a rail-to-rail output (RRO) stage, the device provides a flexible option where higher gain or transimpedance designs are required. This 300-MHz gain-bandwidth product (GBP) amplifier requires less than 1 mA of supply current over a 2.7-V to 5.4-V total supply operating range. A shutdown feature on the 6-pin package versions provides power savings where the system requires less than 1 μ A when shut down. A decompensated amplifier operating at low gains (less than 6 V/V) can experience a low phase margin that risks oscillation. The TINA model for the OPA838 predicts those conditions.

7.2 Functional Block Diagram

The OPA838 is a standard voltage-feedback op amp with two high-impedance inputs and a low-impedance output. Standard applications circuits are supported; see [Figure 7-1](#) and [Figure 7-2](#). These application circuits are shown with a dc V_{REF} on the inputs that set the dc operating points for single-supply designs. The V_{REF} is often ground, especially for split-supply applications.

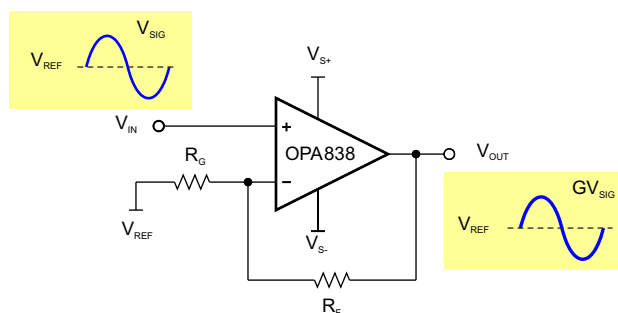


Figure 7-1. Noninverting Amplifier

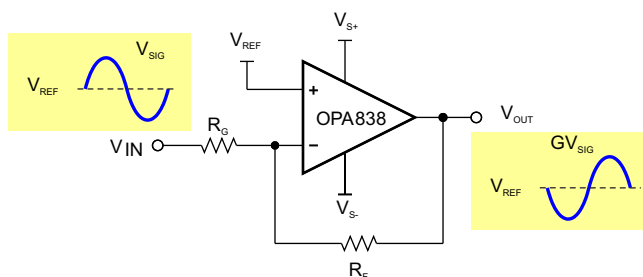


Figure 7-2. Inverting Amplifier

7.3 Feature Description

7.3.1 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier with high CMRR, the input pins must stay within the input operating range (V_{ICR}). These input pins are referenced off of each supply as an input headroom requirement. Specified operation at 25°C is maintained to the negative supply voltage, and to within 1.3 V of the positive supply voltage. The common-mode input range specifications in the table data use CMRR to set the limit. The limits are selected to make sure CMRR does not degrade more than 3 dB less than the minimum CMRR value if the input voltage is within the specified range.

During linear operation, the voltage difference between the input pins is small (0 V) and the input common-mode voltage is analyzed at either input pin, as both pins are at the same potential. The voltage at V_{IN+} is simple to evaluate. In noninverting configuration (see [Figure 7-1](#)), the input signal (V_{IN}) must not violate the V_{ICR} . In inverting configuration (see [Figure 7-2](#)), the reference voltage (V_{REF}), must be within the V_{ICR} .

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For a single 5-V supply, the linear 25°C minimum input voltage ranges from 0 V to 3.7 V, and 0 V to 1.4 V for a single 2.7-V supply. The delta headroom from each power supply rail is the same in each case (0 V and 1.3 V).

7.3.2 Output Voltage Range

The OPA838 device is a rail-to-rail output op amp. Rail-to-rail output typically means that the output voltage swings to within 100 mV of the supply rails. There are different ways to specify this: one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Saturation and linear operation limits are affected by the output current, where higher currents lead to more voltage loss in the output transistors; see [Figure 6-57](#).

The specification tables show saturated output voltage specifications with a 2-k Ω load. [Figure 6-11](#) and [Figure 6-44](#) illustrate saturated voltage-swing limits versus output load resistance, and [Figure 6-12](#) and [Figure 6-45](#) illustrate the output saturation voltage versus load current. With a light load, the output voltage limits have constant headroom to the power rails and track the power supply voltages. For example, with a 1-k Ω load and a single 5-V supply, the linear output voltage ranges from 0.12 V to 4.88 V and ranges from 0.12 V to 2.58 V for a 2.7-V supply. The delta from each power supply rail is the same in each case: 0.12 V.

With devices like the OPA838 where the input range is lower than the output range, the input limits the available signal swing at low gains. Because the OPA838 is intended for higher gains, the smaller input swing range does not limit operation and full rail-to-rail output is available. Inverting voltage gain and transimpedance configurations are typically limited by the output voltage limits of the op amp if the noninverting input pin is biased in range.

7.3.3 Power-Down Operation

The OPA838 includes a power-down feature. Under logic control, the amplifier can switch from normal operation to a standby current of less than 1 μA . When the $\overline{\text{PD}}$ pin is connected high (greater than or equal to 1.5 V over the negative supply), the amplifier is active. Connecting the $\overline{\text{PD}}$ pin low (less than or equal to 0.55 V over the negative supply) disables the amplifier. To protect the input stage of the amplifier, the device uses internal, back-to-back diodes (two in series each way) between the inverting and noninverting input pins. If the differential voltage in shutdown exceeds 1.2 V, those diodes turn on.

Actively drive the $\overline{\text{PD}}$ pin high or low; do not float this pin. If the power-down mode is not used, tie the $\overline{\text{PD}}$ pin to the positive supply rail.

When the op amp is powered from a single-supply and ground, with $\overline{\text{PD}}$ driven from logic devices with similar V_{DD} voltages to the op amp, no special considerations are required. When the op amp is powered from a split-supply with $V_{\text{S-}}$ less than ground, an open-collector type of interface with a pullup resistor is more appropriate. Pullup resistor values must be less than 100 k Ω . Recovery from power down is illustrated in Figure 6-54 and Figure 6-55 for several gains. In single-supply mode, with the gain resistor at ground, the output approaches the positive supply on initial power-up until the internal nodes charge, and then recover to the target output voltage; see Figure 6-52 and Figure 6-53.

7.3.4 Trade-Offs in Selecting The Feedback Resistor Value

The OPA838 is specified using a 1-k Ω feedback resistor with a 200- Ω gain resistor to ground in a noninverting gain of 6 V/V configuration. These values give a good compromise, keeping the noise contribution of the resistors much less than that of the amplifier noise terms and minimal power in the feedback network as the output voltage swing creates load current back into the feedback network. Decreasing these values improves the noise at the cost of more power dissipated in the feedback network. Low values increase the harmonic distortion as the feedback load decreases. Increasing the R_{F} value at a particular gain increases the output noise contribution of those resistors possibly becoming dominant. As the feedback resistor values continue to increase (and R_{G} is at a fixed target gain), there is a loss of phase margin as the impedance that drives the inverting input capacitance brings in an added loop pole at lower frequencies. Figure 7-3 shows this added loop pole at a gain of 6 V/V with increasing R_{F} values. This noninverting test shows more peaking as the R_{F} values increase due to the 1-pF common-mode input capacitance at the inverting input. The TINA simulation model gives excellent prediction of these effects.

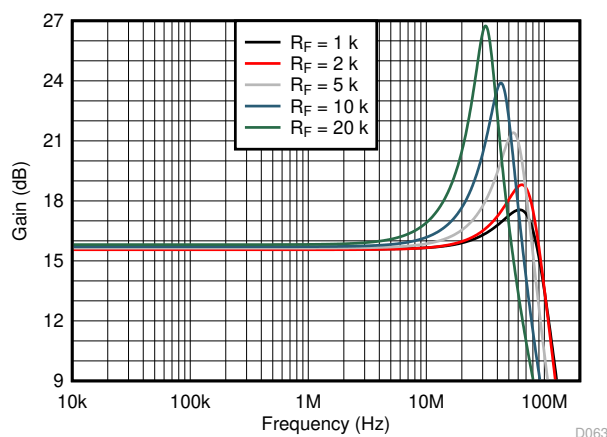


Figure 7-3. Frequency Response With Various Feedback Resistor Values

Operating the OPA838 in inverting mode with higher R_F values increases response peaking due to the loss of phase margin effect. In the inverting case, a pair of capacitors can flatten the response at the cost of lower closed-loop bandwidth. [Figure 7-4](#) shows an example with a 20-k Ω R_F value at an inverting gain of -5 V/V (noise gain = 6 V/V) with optional capacitors (C_F and C_G). [Figure 7-4](#) shows optional bias current cancellation elements on the noninverting input. The total resistance value matches the parallel combination of $R_G \parallel R_F$, which reduces the dc output error term due to bias current to $I_{OS} \times R_F$. The 10-nF capacitor is added across the larger part of this bias current canceling resistance to filter noise and the 20 Ω is split to isolate the capacitor self-resonance from the noninverting input. [Figure 7-5](#) illustrates the small-signal response shape with and without these capacitors. Feedback capacitor C_F is selected to set a desired closed-loop bandwidth with R_F . C_G is added to ground to shape the noise gain up over frequency to be greater than or equal to 6 V/V at higher frequencies. In this example, that higher frequency noise gain is $1 + 6 / 1.2 = 6$ V/V, adding the 1-pF device common-mode capacitance to the external 5 pF. Using the capacitors to set the feedback ratio removes the pole produced in the feedback driving from purely resistive source to the inverting parasitic capacitance.

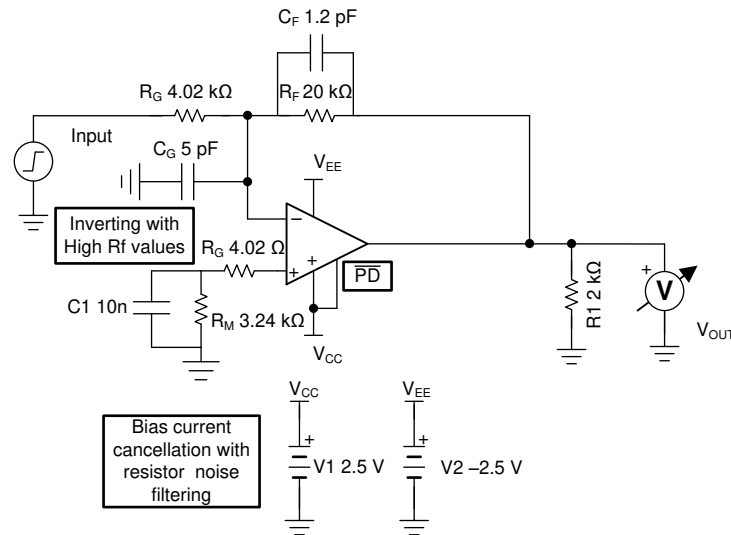


Figure 7-4. G = -5 V/V With Optional Compensation

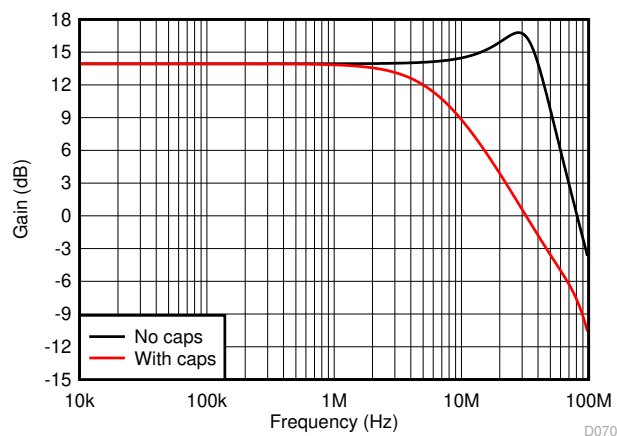


Figure 7-5. Inverting Response With and Without Compensation

7.3.5 Driving Capacitive Loads

The OPA838 drives small capacitive loads directly without oscillation (less than 6pF). When driving capacitive loads greater than 6 pF, [Figure 6-50](#) illustrates the recommended R_{OUT} vs capacitor load parametric on gains. At higher gains, the amplifier starts with greater phase margin into a resistive load and is able to operate with lower R_{OUT} for a given capacitive load. Without R_{OUT} , output capacitance interacts with the output impedance of the amplifier, which causes phase shift in the loop gain of the amplifier that reduces the phase margin. This phase shift causes peaking in the frequency response with overshoot and ringing in the pulse response. [Figure 6-50](#) targets a 30° phase margin for the OPA838. A 30° phase margin produces a 5.7-dB peaking in the frequency response at the amplifier output pin that is rolled off by the output RC pole; see [Figure 7-7](#). This peaking potentially causes clipping for large signals driving a capacitive load. Increasing the R_{OUT} value helps reduce the peaking at the cost of a more band-limited overall response.

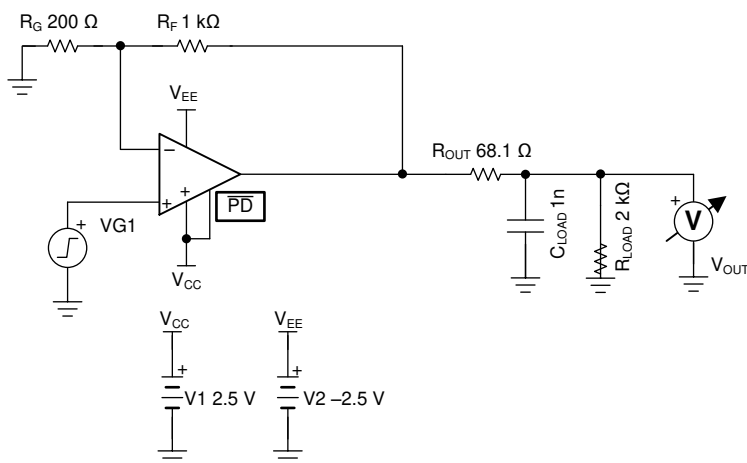


Figure 7-6. R_{OUT} versus C_L Test Circuit

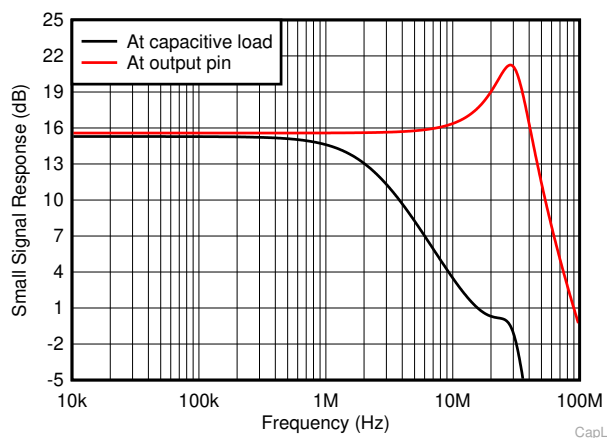


Figure 7-7. Frequency Response to Output Pin and Capacitive Load

7.4 Device Functional Modes

7.4.1 Split-Supply Operation ($\pm 1.35\text{ V}$ to $\pm 2.7\text{ V}$)

To facilitate testing with common lab equipment, the OPA838 EVM (see EVM board link) is built to allow split-supply operation. This configuration eases lab testing because the midpoint between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment have inputs and outputs with a ground reference. This simplifies characterization by removing the requirement for blocking capacitors.

Figure 7-8 shows a simple noninverting configuration analogous to Figure 7-1 with a $\pm 2.5\text{-V}$ supply and V_{REF} equal to ground. The input and output swing symmetrically around ground. For ease of use, split-supplies are preferred in systems where signals swing around ground. Using bipolar (or split) supplies shifts the thresholds for the shutdown control. The disable control is referenced from the negative supply, typically ground, in a single-supply application. However, to disable using a negative supply requires that the pin is set to within 0.55 V greater than the negative supply. If disable is not required, connect that pin to the positive supply to maintain correct operation, even for split-supply applications. Do not float the disable pin; assert the pin to a voltage.

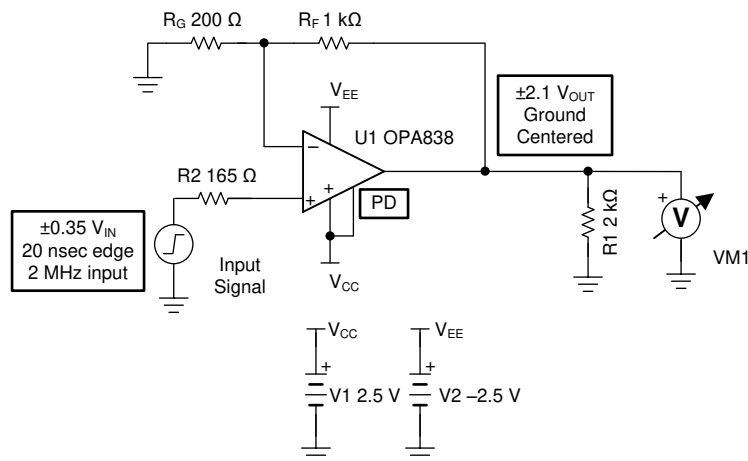


Figure 7-8. Split-Supply Operation

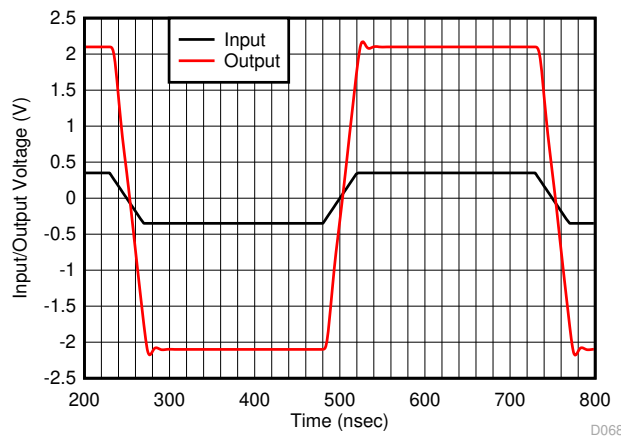


Figure 7-9. Bipolar-Supply Step Response

7.4.2 Single-Supply Operation (2.7 V to 5.4 V)

Most newer systems use a single power supply to improve efficiency and to simplify power supply design. The OPA838 is usable with single-supply power (ground for the negative supply) with no change in performance from split supply, as long as the input and output pins are biased within the linear operating region of the device. The outputs nominally swing rail-to-rail with approximately a 100-mV headroom required for linear operation. The inputs are able to swing to less than the negative rail (typically ground) and to within 1.3 V of the positive supply. For dc-coupled, single-supply operation, the higher-gain operating applications typical of a decompensated op amp, keep the input swings less than the input swing limit to the positive supply. Typically, the 1.3-V input headroom required to the positive supply does not limit operation.

Figure 7-10 shows an example design that takes a 0-V to 0.5-V input range, level shifts the output up to 0.15 V for a 0-V input using the 4.5-V reference voltage common for 5-V SAR ADCs, and sets the gain to produce a 4.1-V output swing for the 0.5-V input swing. This example assumes a 0-Ω source that is required to sink the 39 μA required to bias the positive input pin to produce the 0.15-V output for a 0-V input. The R_F and R_G values are scaled down slightly to provide bias current cancellation by matching the parallel combination of the two bias set-up resistors on the noninverting input. Figure 7-11 illustrates an example step response for this circuit that produces an output from 0.15 V for a 0-V input to 4.35 V for a 0.5-V input.

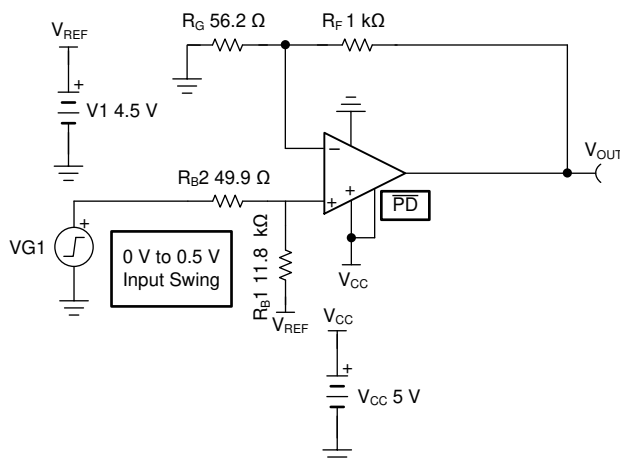


Figure 7-10. DC-Coupled, Single-Supply, Noninverting Interface With Output Level Shift

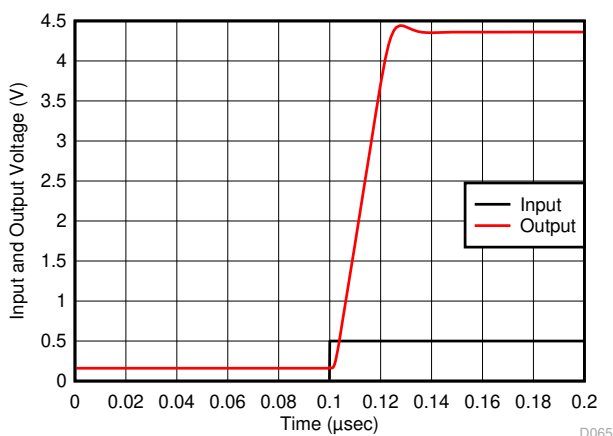


Figure 7-11. Unipolar Input to Level Shifted Output Step Response

If ac-coupling is acceptable, a simple way to operate single-supply is to run inverting. Figure 7-12 shows a low-power, high-gain example. In this example, a gain of -20 V/V is implemented (inverting typically does not matter for ac-coupled channels) where the $V+$ input is biased midscale. This example is showing an optional bias-current cancellation setup, which is not necessary unless the output dc level requires good accuracy. The parallel combination of the divider resistors plus the $80.7\text{-}\Omega$ isolating resistor match the feedback resistor value. With the blocking capacitor at the inverting input, match the feedback resistor impedance to achieve bias current cancellation. In this 3-V supply example, the two inputs and the output are biased at 1.5 V. This places the input pins in range and centers the output for maximum V_{PP} available. Figure 7-13 illustrates the small-signal response for this example showing a f_{-3dB} range from a low-end cutoff of 887 Hz set by the input capacitor value to a 17.5-MHz high-frequency cutoff.

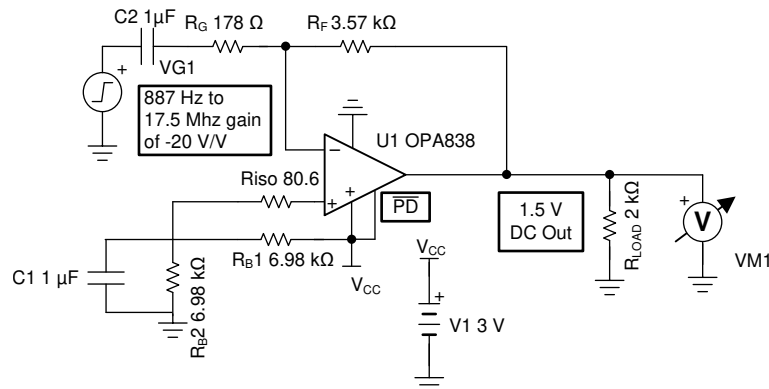


Figure 7-12. Single-Supply Inverting Gain Stage With AC-Coupled Input

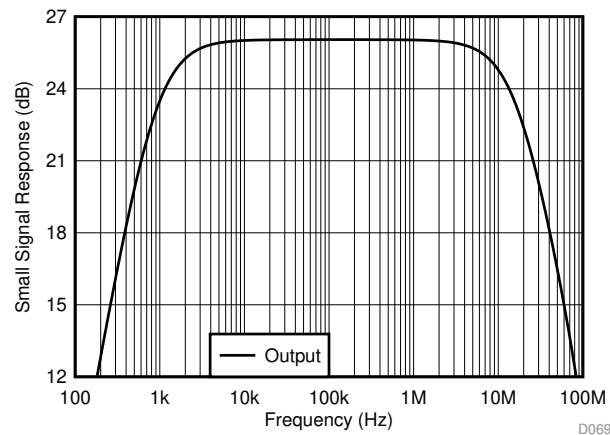


Figure 7-13. Inverting Single-Supply Response With AC-Coupled Input

These methods are just two examples of the many ways a single-supply design is implemented. Many other methods exist, where using a dc reference voltage or ac-coupling are common. A good compilation of options are found in [Single-Supply Op Amp Design Techniques](#).

7.4.3 Power Shutdown Operation

As noted, the 6-pin packages that offer a power-shutdown feature must have that pin asserted. To retain the lowest possible shutdown power, no internal pullup resistors are present in the OPA838. The control threshold is referenced off the negative supply with a nominal internal threshold near 1 V greater than the negative supply. Worst-case tolerances dictate the required low-level voltage to provide a shutdown of 0.55 V (or less) greater than the negative supply, and 1.5 V (or more) greater than the negative supply to maintain enabled operation. The required control pin current is less than ± 50 nA. For SOT-23-6 applications that do not require a shutdown functionality, connect the disable control pin to the positive supply. For SC70 package applications that do not require a shutdown, use the 5-pin package where the control pad is internally connected to the positive supply. When disabled, the output nominally goes to a high-impedance state. However, the feedback network provides a path for discharge for an off-state voltage condition. [Figure 6-52](#) illustrates the turn-on time with a sinusoidal input that is relatively slow, while [Figure 6-53](#) illustrates the turn-off time is fast. [Figure 6-54](#) and [Figure 6-55](#) illustrate the single-supply operation with a dc input to produce a midsupply output at gains of 6 V/V and 10 V/V. In all cases, the output voltage transitions to a point close to the positive supply voltage and then moves to the desired output voltage 0.5 μ s to 1.5 μ s after the disable control line goes high. The supply current in shutdown is a low 0.1 μ A nominally with a maximum 1 μ A.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Noninverting Amplifier

The OPA838 can be used as noninverting amplifier with signal input to the noninverting input (V_{IN+}). Figure 7-1 illustrates a basic block diagram of the circuit. V_{REF} is often ground when split supplies are used.

If $V_{IN} = V_{REF} + V_{SIG}$, and the gain setting resistor (R_G) is dc referenced to V_{REF} , use Equation 1 to calculate the output of the amplifier.

$$V_{OUT} = V_{SIG} \left(1 + \frac{R_F}{R_G} \right) + V_{REF} \quad (1)$$

$$G = 1 + \frac{R_F}{R_G}$$

The noninverting signal gain (also called the noise gain) of the circuit is set by:

V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals within the flat portion of the frequency response. For a high-speed, low-noise device like the OPA838, the values selected for R_F (and the R_G for the desired gain) can strongly influence the operation of the circuit. For the characteristic curves, the noninverting circuit of Figure 8-1 shows the test configuration. Table 8-1 lists the recommended resistor values over gain.

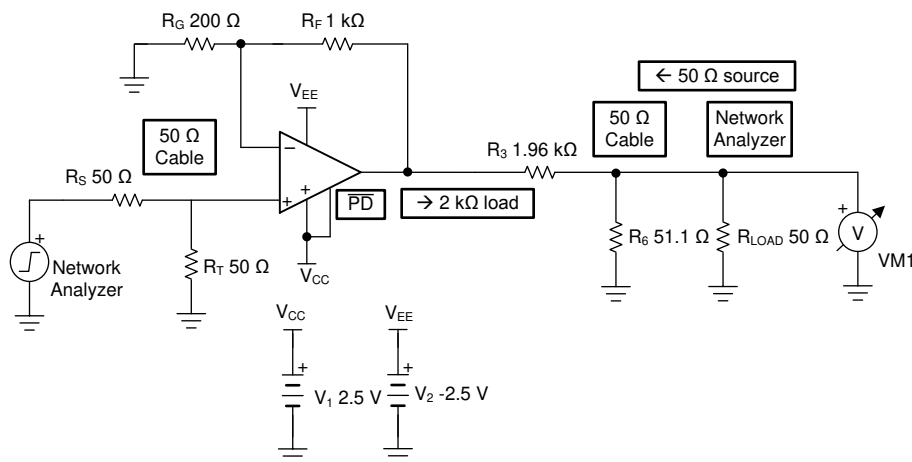


Figure 8-1. Noninverting Characterization Circuit

Table 8-1 lists the recommended resistor values from target gains of 6 V/V to 20 V/V. This table controls the R_F and R_G values to set the resistor noise contribution at approximately 40% of the total output noise power. This increases the spot noise at the output over what the op amp voltage noise produces by 20%. Lower values reduce the output noise of any design at the cost of more power in the feedback circuit. Using the TINA model and simulation tool shows the impact of different resistor value choices on response shape and noise.

Table 8-1. Noninverting Recommended Resistor Values

TARGET AVERAGE	R_F (Ω)	R_G (Ω)	ACTUAL GAIN (V/V)	GAIN (dB)
6	1000	200	6	15.56
7	1180	196	7.02	16.93
8	1370	196	7.99	18.05
9	1540	191	9.06	19.15
10	1690	187	10.04	20.03
11	1870	187	11	20.83
12	2050	187	11.96	21.56
13	2210	182	13.14	22.37
14	2370	182	14.02	22.94
15	2550	182	15.01	23.53
16	2740	182	16.05	24.11
17	2870	178	17.12	24.67
18	3090	182	17.98	25.09
19	3240	178	19.20	25.67
20	3400	178	20.1	26.06
21	3570	178	21.06	26.47

8.1.2 Inverting Amplifier

The OPA838 can be used as an inverting amplifier with signal input to the inverting input (V_{IN-}) through the gain-setting resistor (R_G .) Figure 7-2 illustrates a basic block diagram of the circuit.

If $V_{IN} = V_{REF} + V_{SIG}$, and the noninverting input is dc biased to V_{REF} , the output of the amplifier is calculated according to Equation 2:

$$V_{OUT} = V_{SIG} \left(\frac{-R_F}{R_G} \right) + V_{REF} \quad (2)$$

The signal gain of the circuit $G = \frac{-R_F}{R_G}$ and V_{REF} provides a reference point around which the input and output signals swing. For bipolar-supply operation, V_{REF} is often GND. The output signal is 180° out-of-phase with the input signal in the pass band of the application. Figure 8-2 illustrates the 50- Ω input matched configuration used for the inverting characterization plots. In this case, an added termination resistor is placed in parallel with the input R_G resistor to provide an impedance match to 50- Ω test equipment. Table 8-2 lists the suggested values for R_F , R_G , and R_T for inverting gains from –6 V/V to –20 V/V.

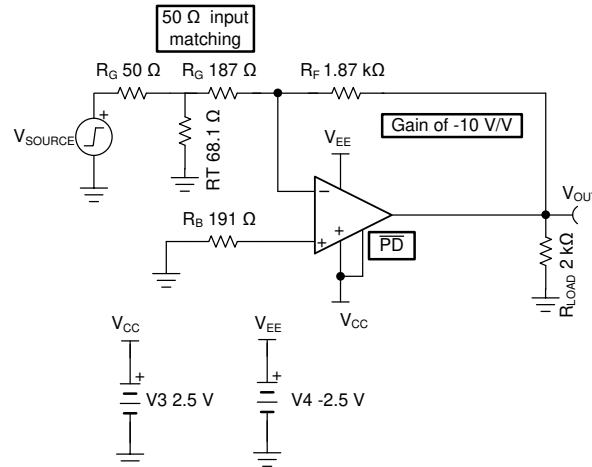


Figure 8-2. Inverting With Input Impedance Matching

Table 8-2. Inverting Recommended Resistor Values

AVERAGE	R _F (Ω)	R _G (Ω)	EXACT R _T	STANDARD R _T	INPUT Z _I	ACTUAL (V/V)	GAIN (dB)
-6	1180	196	67.1	66.5	49.7	-6.02	15.59
-7	1370	196	67.1	66.5	49.7	-6.99	16.89
-8	1540	191	67.7	68.1	50.2	-8.06	18.13
-9	1690	187	68.2	68.1	49.9	-9.04	19.12
-10	1870	187	68.2	68.1	49.9	-10	20
-11	2050	187	68.2	68.1	49.9	-10.96	20.80
-12	2210	182	68.9	68.1	49.6	-12.14	21.69
-13	2370	182	68.9	68.1	49.6	-13.02	22.29
-14	2550	182	68.9	68.1	49.6	-14.01	22.93
-15	2740	182	68.9	68.1	49.6	-15.05	23.55
-16	2870	178	69.5	69.8	50.1	-16.12	24.15
-17	3090	182	68.9	69.8	50.5	-16.98	24.6
-18	3240	178	69.5	69.8	50.1	-18.20	25.2
-19	3400	178	69.5	69.8	50.1	-19.10	25.62
-20	3570	178	69.5	69.8	50.1	-20.06	26.04

8.1.3 Output DC Error Calculations

The OPA838 provides excellent dc signal accuracy as a result of high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, pay careful attention to input bias current cancellation. The low-noise input stage for the OPA838 has a relatively high input bias current (1.6 μ A typical out the pins) but with a close match between the two input currents. This is a negative rail input device using PNP input devices where the base current flows out of the device pins. A large resistor to ground on the V+ input shifts positively because of the input bias current. The mismatch between the two input bias currents is very low, typically only ± 20 nA of input offset current. Match the dc source impedances out of the two inputs to reduce the total output offset voltage. For example, one way to add bias current cancellation to the circuit in [Figure 7-8](#) is to insert a 165- Ω series resistor into the noninverting input to match the parallel combination of R_F and R_G for this basic gain of 6 V/V noninverting gain circuit. These same calculations apply to the output offset drift. Analyzing the simple circuit of [Figure 7-8](#), the noise gain for the input offset voltage drift is $1 + 1k / 200 = 6$ V/V. This results in an output drift term of $\pm 1.6 \mu\text{V}/^\circ\text{C} \times 6 = \pm 9.6 \mu\text{V}/^\circ\text{C}$. The two impedances out of the inputs are matched; therefore, the residual error due to the maximum ± 500 pA/ $^\circ\text{C}$ offset current drift is exactly that number times the 1-k Ω feedback resistor value, or $\pm 0.5 \mu\text{V}/^\circ\text{C}$. The total output dc error drift band is $\pm 10.1 \mu\text{V}/^\circ\text{C}$.

8.1.4 Output Noise Calculations

The decompensated voltage feedback of the OPA838 op amp offers among the lowest input voltage and current noise terms for any device with a supply current less than 1 mA. Figure 8-3 shows the op amp noise analysis model that includes all noise terms. In this model, all the noise terms are shown as noise voltage or current density terms in nV/√Hz or pA/√Hz.

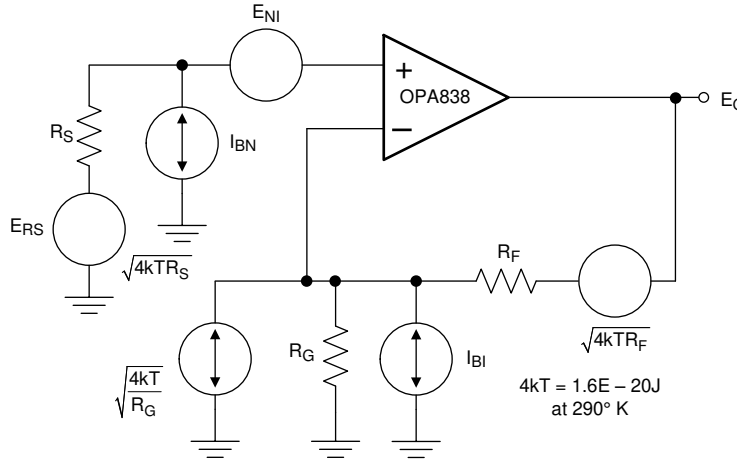


Figure 8-3. Op-Amp Noise-Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to return to a spot noise voltage. Equation 3 shows the general form for this output noise voltage using the terms presented in Figure 8-3.

$$E_O = \sqrt{[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S]NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (3)$$

Dividing this expression by the noise gain ($NG = 1 + R_F / R_G$) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 4.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (4)$$

Using the resistor values shown in Table 8-1 with $R_S = 0 \Omega$ results in a constant input-referred voltage noise of 2.86 nV/√Hz. Reducing the resistor values brings this number closer to the intrinsic 1.9 nV/√Hz of the OPA838. Adding R_S for bias current cancellation in noninverting mode adds the noise from R_S to the total output noise; see Equation 3. In inverting mode, bypass the R_S bias-current cancellation resistor with a capacitor for the best noise performance.

8.2 Typical Applications

8.2.1 High-Gain Differential I/O Designs

A high-gain differential-to-differential I/O circuit can be used to drive a second-stage FDA or a differential-to-single-ended stage. This circuit is frequently used in applications where high input impedance is required (for example, if the source cannot be loaded). [Figure 8-3](#) illustrates an example design where the differential gain is 41 V/V. An added element between the two R_G resistors increases the noise gain for the common-mode feedback. Make sure to provision for the added element; otherwise, a decompensated VFA (such as the OPA838) often oscillates. With only the R_G elements in the differential I/O design, the common-mode feedback is unity-gain and often causes high-frequency, common-mode oscillations. To resolve this issue, split the R_G elements in half and add a low-impedance path, such as a capacitor or a DC reference, between the two R_G values.

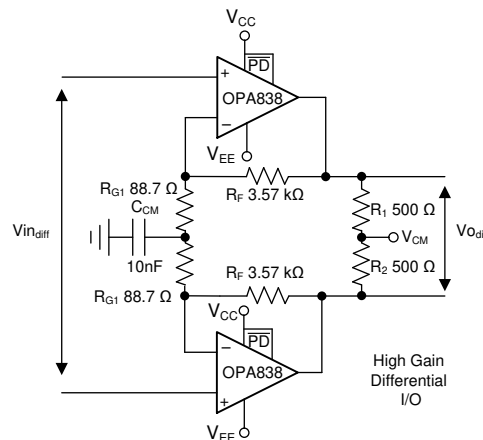


Figure 8-4. High-Gain Differential I/O Stage

Integrated results are available, but the OPA838 provides a low-power, high-frequency result. For best CMRR performance, match the resistors. A good rule is CMRR is approximately equal to the resistor tolerance; therefore, a 0.1% tolerance provides approximately 60-dB CMRR.

8.2.1.1 Design Requirements

As an example design, start with the circuit in [Figure 8-4](#).

- Set the target gain and split the R_G element in half. For this example, target a gain of 41 V/V.
- Assess the DC common-mode biasing on the noninverting inputs. The DC biasing must be in range and have a gain of 1 to the output. This is not illustrated in [Figure 8-3](#).
- If a DC reference is used as the mid- R_G bias, setting the reference equal to the noninverting input bias voltage sets the output common-mode to that voltage. Using a capacitor as illustrated in [Figure 8-3](#) accomplishes the same results.

8.2.1.2 Detailed Design Procedure

- Set the total R_G value near the high gain values using [Table 8-1](#). This 178- Ω total must be split for a center tap to increase the common-mode noise gain, as shown by the 88.7- Ω value in [Figure 8-4](#).
- Set R_F using a standard value near the calculated from solving [Equation 1](#) using half of the total R_G value.
- Simulate the common-mode noise with different elements on the R_G center tap as shown in [Figure 8-5](#). Decide which is most appropriate to the application.

The common-mode loop instability without the R_G center tap is not often apparent in the closed-loop differential simulations. The common-mode loop instability without the R_G center tap can often be detected in a common-mode output-noise simulation as [Figure 8-5](#) shows. Grounding the inputs [Figure 8-4](#) and running an output-noise simulation for the common-mode tap point in [Figure 8-3](#) shows a peaking in the noise at high frequency. This peaking indicates low-phase margin for the common-mode loop. [Figure 8-5](#) shows this peaking in the lowest noise curve, with two options for improving phase margin. The first option used in [Figure 8-4](#) is a capacitor to ground set to increase the common-mode noise gain only at higher frequencies. This increase can be seen by the peaking in the common-mode noise of [Figure 8-5](#). Another alternative is to provide a dc voltage reference on the R_G center tap. This method raises the common-mode noise gain from dc and beyond. Neither of these latter two options show any evidence of low phase-margin peaking. These two options do increase the output common-mode noise significantly at lower frequencies. Typically, an increase in output common-mode noise is more acceptable than low-phase margin because the next stage (FDA, ADC, differential to single stage) rejects common-mode noise.

Using the 10-nF center tap capacitor, [Figure 8-6](#) shows the differential I/O small-signal response showing the expected $300 \text{ MHz} / 41 \approx 7.3 \text{ MHz}$ closed-loop bandwidth. The capacitor to ground between the R_G elements does not impact the differential frequency response.

8.2.1.3 Application Curves

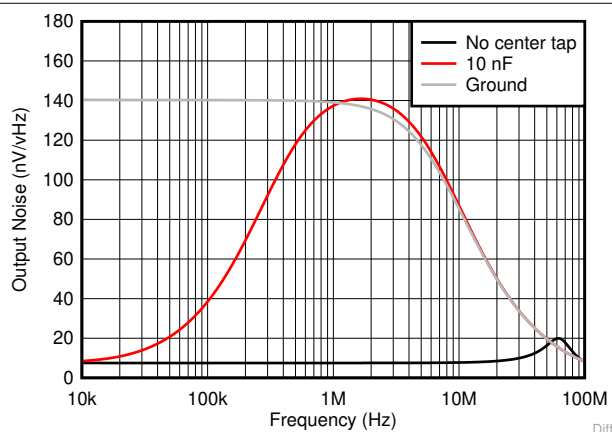


Figure 8-5. Common-Mode Output Noise for Differential I/O Design

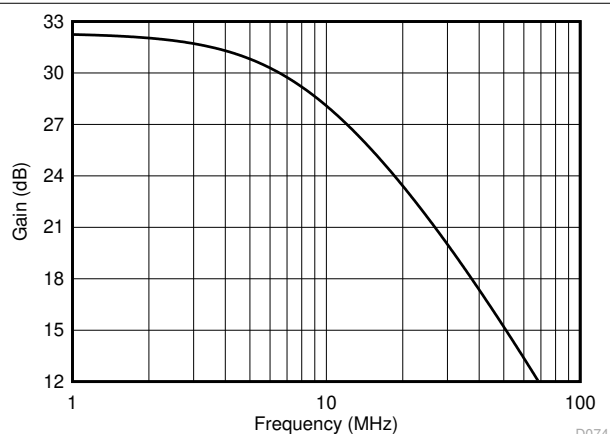


Figure 8-6. Differential Small-Signal Frequency Response

8.2.2 Transimpedance Amplifier

A common application for a high-gain-bandwidth voltage-feedback op amp is to amplify a small photodiode current from a capacitive detector. Figure 8-7 shows the front-page transimpedance circuit with more detail. Here, a fixed -0.23 V negative voltage generator (LM7705) is used on the negative supply to make sure the output has adequate headroom when the output is at 0 V. The transimpedance stage is designed here for a 2.4-MHz flat (Butterworth) response while a simple RC post-filter band-limits the broadband noise and sets the overall bandwidth to 1 MHz. The requirements for a high-dynamic-range transimpedance (or charge) amplifier include the very low input voltage noise intrinsic to a decompensated device like the OPA838. The noise gain over frequency for this type of circuit starts out at unity gain, and then begins to peak with a single zero response. This peaking is due to the pole formed in the feedback by the feedback resistor and the total capacitance on the inverting input. That noise gain response is flattened out at higher frequencies by the feedback capacitor value to be the $1 + C_S / C_F$ capacitor ratio. This noise gain is normally a very high, allowing the decompensated OPA838 to be applied to this application. The noise gain is intentionally peaked to a high value in this application; therefore, the very low input voltage noise ($1.8 \text{ nV}/\sqrt{\text{Hz}}$) of the OPA838 improves dynamic range.

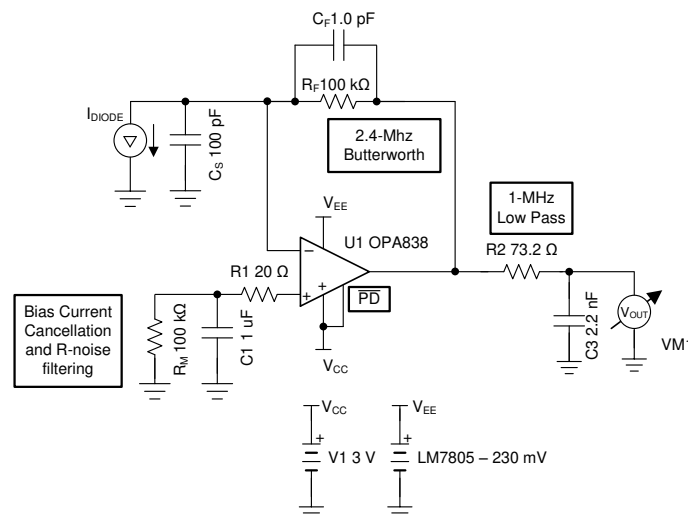


Figure 8-7. 100-kΩ Wide Bandwidth Transimpedance Design

8.2.2.1 Design Requirements

To implement a controlled frequency response transimpedance design, set the transimpedance stage amplifier bandwidth higher than a controlled post RC filter. This allows variation in the source capacitance and amplifier gain bandwidth product with less overall bandwidth variation to the final output. In this example design:

- Assume a nominal source capacitance value of 100 pF. This normally comes from the capacitance versus reverse bias plot for the photodiode. No reverse bias is illustrated in Figure 8-8, but the current source is typically a back biased diode with a negative supply on the anode and the cathode connected to the op amp inverting input. In this polarity, the signal current sinks into the diode and raises the op amp output voltage above ground.
- For the best dc precision, add a matching resistor on the noninverting input to reduce the input bias current error to $I_{OS} \times R_F$. This resistor adds to the input voltage noise; TI recommends bypassing that resistor with as large as a capacitor as required to roll off resistor noise. This capacitor has a relatively low frequency self resonance that interacts with the input stage and can impair stability. Add a small series 20-Ω resistor from the capacitor into the noninverting input to de-Q the resonant source impedance without adding too much noise.
- Set the feedback capacitor to achieve the desired frequency response shape.
- Add a post RC filter to control the overall bandwidth to 1 MHz. In this example, a 2.2-nF capacitor allows a low 73.2-Ω series resistor. When driving a sampling ADC (like a SAR), this combination helps reduce the sampling glitch and speed settling time.

8.2.2.2 Detailed Design Procedure

The primary design requirement is to set the achievable transimpedance gain and compensate the operational amplifier with C_F for the desired response shape. A detailed transimpedance design methodology is available in [Transimpedance Considerations for High-Speed Amplifiers](#). With a source capacitance set and the amplifier selected to provide a particular gain bandwidth product, the achievable transimpedance gain and resulting Butterworth bandwidth are tightly coupled as [Equation 5](#) illustrates. Use [Equation 6](#) to solve for a maximum R_F value. When the R_F is selected, the feedback pole is set by [Equation 7](#) to be at 0.707 of the characteristic frequency. At that compensation point, the closed-loop bandwidth is that characteristic frequency with a Butterworth response.

- With the 100-pF source capacitance, 300-MHz gain bandwidth product, and the 2.2-MHz closed-loop bandwidth target in the transimpedance stage, solve [Equation 6](#) for a maximum gain of 100 k Ω .
- Set the feedback pole at 0.707 times that 2.2-MHz Butterworth bandwidth. This sets the target $1 / (2\pi \times R_F \times C_F) = 1.55$ MHz. Solving for C_F sets the target to 1 pF
- If dc precision is desired, add a 100-k Ω resistor to ground on the noninverting input. If DC precision is not required, ground the noninverting input
- Add a resistor noise filtering capacitor in parallel with the 100-k Ω resistor.
- Add a small series resistor isolating this capacitor from the noninverting input.
- Select a final filter capacitor for the load. (In this example, a value of 2.2 nF is used as a typical SAR input capacitor.)
- Add a series resistor to the final filter capacitor to form a 1-MHz pole. In this example, that is 73.2 Ω .
- Confirm this resistor is greater than the minimum recommended value illustrated in [Figure 6-50](#).

$$F_{-3dB} \approx \sqrt{\frac{GBP}{2\pi R_f C_S}} \quad (5)$$

$$R_{f\max} \approx \frac{GBP}{F_{-3dB}^2 2\pi C_S} \quad (6)$$

$$\frac{1}{2\pi R_f C_f} = 0.707 \times \sqrt{\frac{GBP}{2\pi R_f C_S}} \quad (7)$$

Implementing this design and simulating the performance using the TINA model for the response to the output pin and to the final capacitive load shows the expected results of [Figure 8-8](#). Here, the exact 2.2-MHz flat Butterworth response to the output pin is shown with the final single pole rolloff at 1 MHz at the final 2.2-nF capacitor.

8.2.2.3 Application Curve

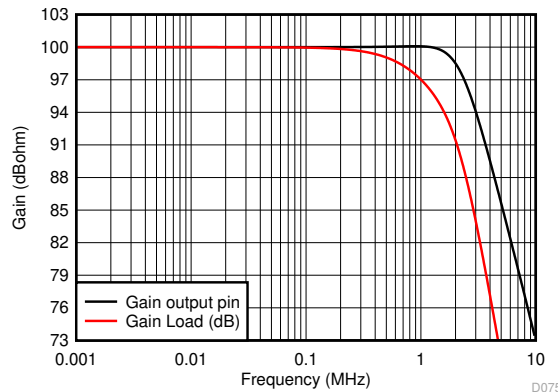


Figure 8-8. Small-Signal Response for 100-k Ω Transimpedance Gain

8.3 Power Supply Recommendations

The OPA838 device is intended to work in a supply range of 2.7 V to 5.4 V. Good power-supply bypassing is required. Minimize the distance (less than 0.1 inch) from the power-supply pins to high-frequency, 0.1- μ F decoupling capacitors. A larger capacitor (2.2 μ F is typical) is used with a high-frequency, 0.1- μ F supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split-supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the PCB. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional 0.1- μ F supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second harmonic distortion.

The OPA838 has a positive supply current temperature coefficient; see [Figure 6-58](#). This temperature coefficient helps improve the input offset voltage drift. Supply current requirements in system design must account for this effect using the maximum intended ambient and [Figure 6-58](#) to size the supply required. The very low power dissipation for the OPA838 typically does not require any special thermal design considerations. For the extreme case of 125°C operating ambient, use the approximate maximum 200°C/W for the three packages, and a maximum internal power of 5.4-V supply \times 1.25-mA 125°C supply current from [Figure 6-58](#) gives a maximum internal power of 6.75 mW. This power dissipation only gives a 1.35°C rise from ambient to junction temperature, which is much less than the maximum 150°C junction temperature. Load power adds to this power dissipation, but also increases the junction temperature only slightly over ambient temperature.

8.4 Layout

8.4.1 Layout Guidelines

Use the [OPA838EVM](#) as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing must be direct and as short as possible into and out of the op amp.
2. Use a short and direct feedback path avoiding vias if possible.
3. Remove ground or power planes from directly under the negative input and output pins of the amplifier.
4. Place a series output resistor as close to the output pin as possible when driving capacitive or matched loads.
5. Place a 2.2- μ F power-supply decoupling capacitor within two inches of the device and share with other op amps if desired. For split-supply operation, a capacitor is required for both supplies.
6. Place a 0.1- μ F power-supply decoupling capacitor as close to the supply pins as possible, preferably within 0.1 inch. For split-supply operation, a capacitor is required for both supplies.
7. The $\overline{\text{PD}}$ pin uses logic levels referenced off the negative supply. If the pin is not used, tie the pin to the positive supply to enable the amplifier. If the pin is used, then actively drive the pin. A bypass capacitor is not necessary, but is used for EMI rejection in noisy environments.

8.4.2 Layout Example

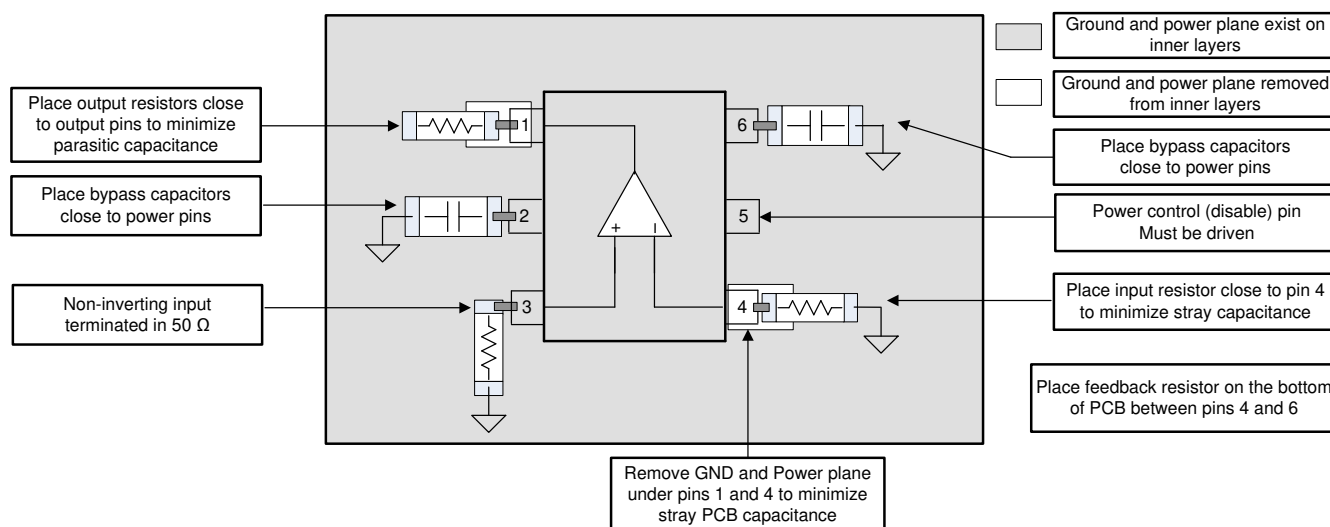


Figure 8-9. EVM Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design and simulation tools](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, [OPA835DBV](#), [OPA836DBV EVM user's guide](#)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.

All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2024) to Revision E (August 2025)	Page
• Changed DXB (X2QFN, 8) package status from preview to production data and added associated content....	1
• Changed <i>Device Comparison Table</i> to <i>Related Products</i>	2
• Moved single voltage-noise and current-noise plot into two separate plots	15
• Updated total drift equation in <i>Output DC Error Calculations</i>	31

Changes from Revision C (October 2023) to Revision D (September 2024)	Page
• Added DXB (X2QFN, 8) package and associated content to data sheet.....	1

Changes from Revision B (October 2018) to Revision C (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Device Information</i> table to <i>Package Information</i> , updated columns, and added note 2.....	1

Changes from Revision A (February 2018) to Revision B (October 2018)	Page
• Changed $< 5\text{-}\mu\text{A}$ <i>Shutdown Current</i> to $< 1\text{-}\mu\text{A}$ <i>Shutdown Current</i> in <i>Features</i> section.....	1
• Changed value of common-mode and differential-mode input impedance in <i>Electrical Characteristics</i> $V_S = 5\text{ V}$ and <i>Electrical Characteristics</i> $V_S = 3\text{ V}$ tables.....	5
• Changed value of power-down quiescent current in <i>Electrical Characteristics: $V_S = 5\text{ V}$</i> and <i>Electrical Characteristics $V_S = 3\text{ V}$</i> tables.....	5
• Changed $5\text{ }\mu\text{A}$ to $1\text{ }\mu\text{A}$ in <i>Overview</i> section	20
• Changed standby current from $5\text{ }\mu\text{A}$ to $1\text{ }\mu\text{A}$ in <i>Power-Down Operation</i> section.....	22
• Changed common-mode input capacitance from 1.3 pF to 1 pF in <i>Trade-Offs in Selecting The Feedback Resistor Value</i> section.....	22
• Changed $1 + 6.3 / 1.2 = 6.25\text{ V/V}$, adding the 1.3-pF device common-mode capacitance to $1 + 6 / 1.2 = 6\text{ V/V}$, adding the 1-pF device common-mode capacitance in <i>Trade-Offs in Selecting The Feedback Resistor Value</i> section.....	22
• Changed $2\text{ }\mu\text{A}$ to $0.1\text{ }\mu\text{A}$ and $5\text{ }\mu\text{A}$ to $1\text{ }\mu\text{A}$ in last sentence of <i>Power Shutdown Operation</i> section.....	28
• Changed <i>Power Supply Recommendations and Thermal Notes</i> title to <i>Power Supply Recommendations</i> ...	37

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA838IDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDBVRG4.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDBVT.B	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1C3F
OPA838IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17Q
OPA838IDCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17Q
OPA838IDCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17Q
OPA838IDCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17Q
OPA838SIDCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19C
OPA838SIDCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19C
OPA838SIDCKT	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19C
OPA838SIDCKT.B	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19C
XOPA838DXBR	Active	Preproduction	X2QFN (DXB) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
XOPA838DXBR.B	Active	Preproduction	X2QFN (DXB) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA838IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA838IDBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA838IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA838IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA838IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA838SIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA838SIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA838IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA838IDBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA838IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA838IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA838IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA838SIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
OPA838SIDCKT	SC70	DCK	6	250	180.0	180.0	18.0

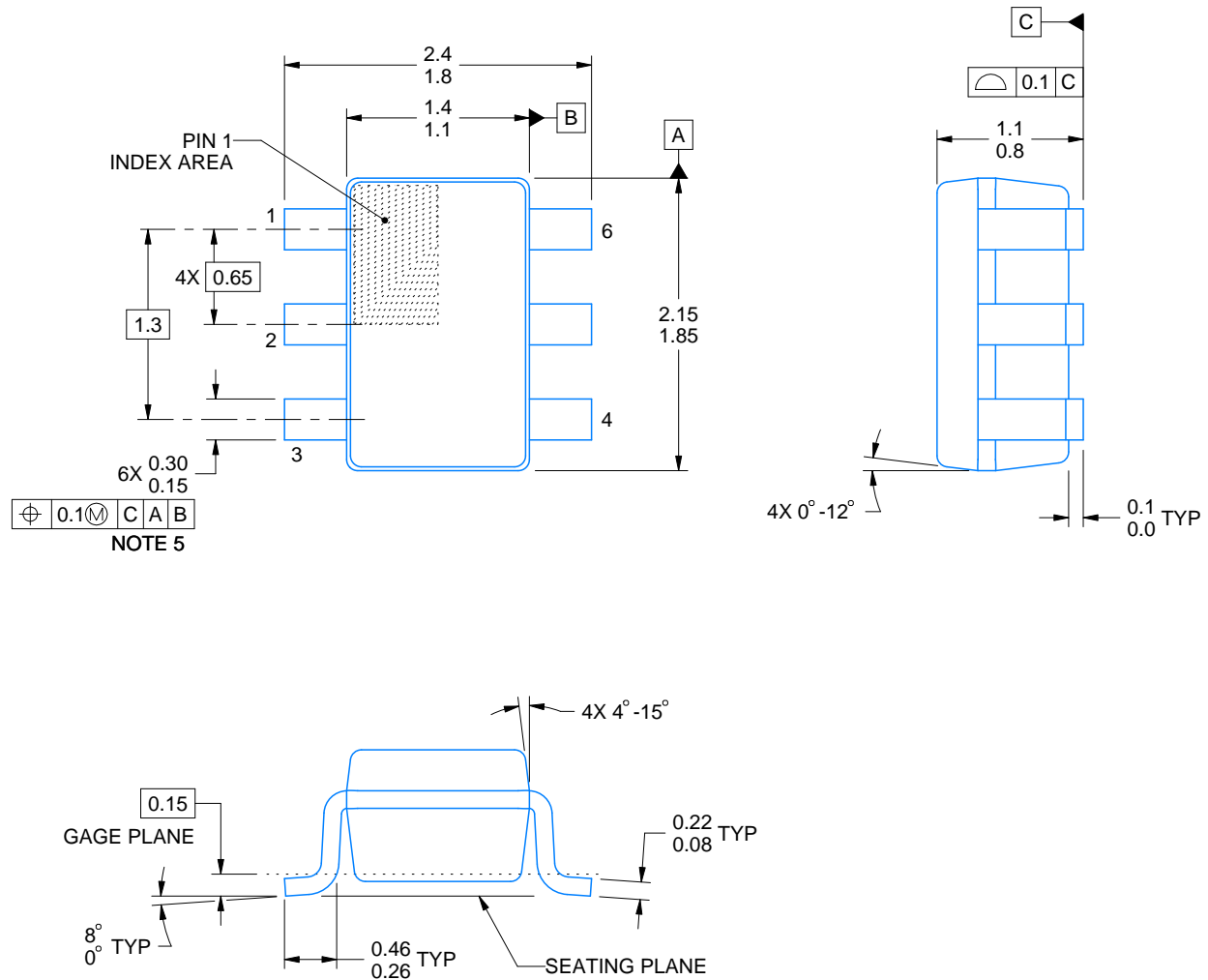
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side.

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

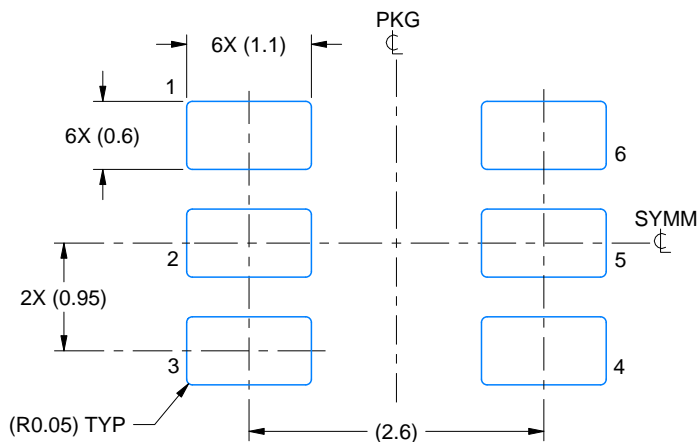
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

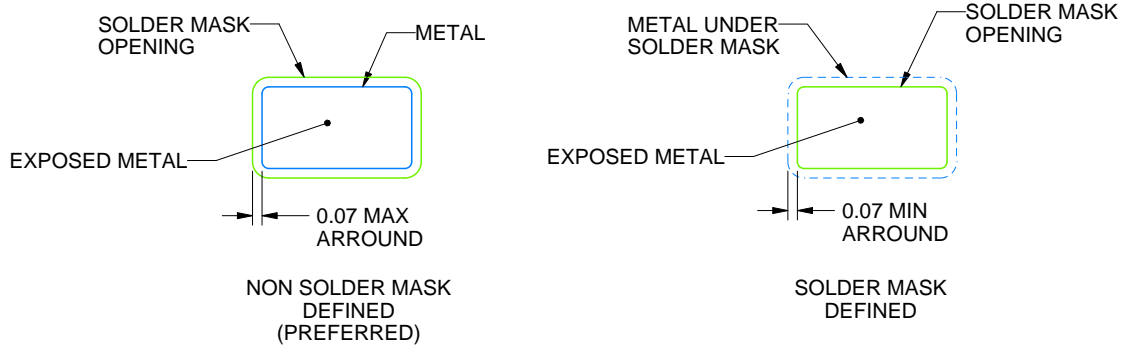
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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