OPA810-Q1 Automotive, 140MHz, Rail-to-Rail Input/Output, FET-Input Operational Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature: –40°C to +125°C, T_A
- Gain-bandwidth product: 70MHz
- Small-signal bandwidth: 140MHz
- Slew rate: 200V/µs
- Wide supply range: 4.75V to 27V
- Low noise:
  - Input voltage noise: 6.3nV/√Hz (f = 500kHz)
  - Input current noise: 5fA/√Hz (f = 10kHz)
- Rail-to-rail input and output:
  - FET input stage: 2pA input bias current (typical)
  - High linear output current: 75mA
- Input offset: ±550µV (maximum)
- Offset drift: ±2.5µV/°C (typical)
- Low power: 3.7mA/channel

2 Applications

- Multichannel sensor interfaces
- Optoelectronic drivers
- Low-side current sensing
- DC/DC converters
- Inverter and motor control
- Onboard and wireless chargers
- HAVC compressors
- Photodiode TIA interface
- Head-up display (HUD)
- Automotive display

3 Description

The OPA810-Q1 is a single-channel, field-effect transistor (FET) input, voltage-feedback operational amplifier (op amp) with bias current in the picoampere (pA) range. The OPA810-Q1 is unity-gain stable with a small-signal, unity-gain bandwidth of 140MHz, and offers excellent dc precision and dynamic ac performance at a low quiescent current (I_Q) of 3.7mA per channel. The OPA810-Q1 is fabricated on Texas Instruments' proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70MHz, slew rate of 200V/µs, and low-noise voltage of 6.3nV/√Hz, the OPA810-Q1 is designed for use in a wide range of high-fidelity data-acquisition and signal-processing applications.

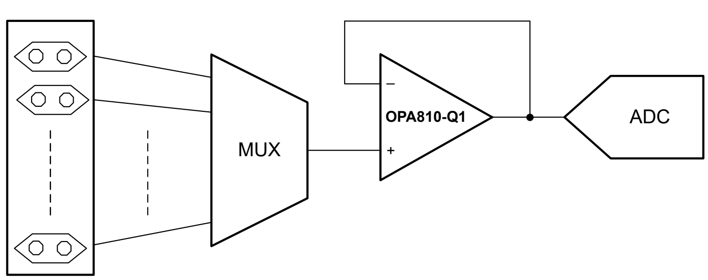
The OPA810-Q1 features rail-to-rail inputs and outputs, and delivers 75mA of linear output current designed to drive optoelectronic components and analog-to-digital converter (ADC) inputs or buffer digital-to-analog converter (DAC) outputs into heavy loads.

The OPA810-Q1 is specified over the extended industrial temperature range of –40°C to +125°C. The OPA810-Q1 is available in SOT-23 package.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA810-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) See Section 4.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Multichannel Sensor Interface Using a Single, Higher-GBWP Amplifier

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4 Device Comparison Table

DEVICE	SUPPLY VOLTAGE, ±V_S (V)	I_Q/CHANNEL TYPICAL (mA)	GAIN BANDWIDTH (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA810-Q1	27	3.8	70	200	6.3	Unity-gain-stable, FET-input amplifier
OPA2863-Q1	12.6	0.69	50	105	5.9	Rail-to-rail input and output, voltage-feedback amplifier
OPAx365-Q1	5.5	4.6	50	25	4.5	Rail-to-rail input/output,low-noise, CMOS amplifier
OPA2836-Q1	5.5	0.95	118	560	4.6	Rail-to-rail-output, negative-rail-input, voltage-feedback amplifier
TLV365-Q1	5.5	4.6	50	27	4.5	Rail-to-rail input and output, CMOS operational amplifiers

5 Pin Configuration and Functions

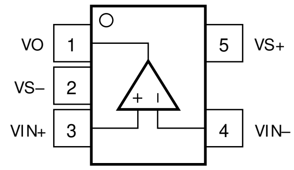


Figure 5-1. DBV Package, 5-Pin SOT23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VIN–	4	Input	Inverting input pin
VIN+	3	Input	Noninverting input pin
VO	1	Output	Output pin
VS–	2	Power	Negative power-supply pin
VS+	5	Power	Positive power-supply pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage (total bipolar supplies)[2]		±14	V
V_{IN}	Input voltage	V_{S-} – 0.5	V_{S+} + 0.5	V
$V_{IN,Diff}$	Differential input voltage[3]		±7	V
I_I	Continuous input current		±10	mA
I_O	Continuous output current[4]		±15	mA
P_D	Continuous power dissipation	See *Section 6.4*		
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) V_S is the total supply voltage given by $V_S = V_{S+} – V_{S–}$.
(3) Equal to the lower of ±7V or total supply voltage.
(4) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	4.75		27	V
T_A	Ambient temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA810-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 24V

at T_A = 25°C, V_{S+} = 12V, V_{S-} = –12V, common-mode voltage (V_{CM}) = midsupply, R_L = 1kΩ connected to midsupply; for ac specifications, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 1, V_O = 20mV_{PP}, R_F = 0Ω		135		MHz
		G = 1, V_O = 20mV_{PP}, R_F = 0Ω, C_L= 10pF		140		
		G = –1, V_O = 20mV_{PP}		68		
LSBW	Large-signal bandwidth	G = 2, V_O = 2V_{PP}		44		MHz
		G = 2, V_O = 10V_{PP}		14		
GBWP	Gain-bandwidth product			70		MHz
	Bandwidth for 0.1dB flatness	G = 2, V_O = 20mV_{PP}		16		MHz
SR	Slew rate (20%–80%)[3]	G = 2, V_O = –2V to +2V step		237		V/µs
		G = –1, V_O = –2V to +2V step		222		
		G = 2, V_O = –4.5V to +3.5V step		254		
	Rise time	V_O = 200mV step		4		ns
	Fall time	V_O = 200mV step		4		ns
	Settling time	G = 2, V_O = 2V step, to 0.1%		47		ns
		G = 2, V_O = 10V step, to 0.1%		70		
		G = 2, V_O = 2V step, to 0.001%		320		
		G = 2, V_O = 10V step, to 0.001%		200		
	Input overdrive recovery	G = 1, R_F = 0Ω, (V_{S-}– 0.5V) to (V_{S+} + 0.5V) input		35		ns
	Output overdrive recovery	G = –1, (V_{S-}– 0.5V) to (V_{S+} + 0.5V) input		45		ns
HD2	2nd harmonic distortion	f = 100kHz, V_O = 2V_{PP}		–118		dBc
		f = 100kHz, V_O = 10V_{PP}		–108		
		f = 1MHz, V_O = 2V_{PP}		–112		
		f = 1MHz, V_O = 10V_{PP}		–91		
HD3	3rd harmonic distortion	f = 100kHz, V_O = 2V_{PP}		–136		dBc
		f = 100kHz, V_O = 10V_{PP}		–130		
		f = 1MHz, V_O = 2V_{PP}		–104		
		f = 1MHz, V_O = 10V_{PP}		–91		
e_n	Input-referred voltage noise	Flat-band, 1/f corner at 1.5kHz		6.3		nV/√Hz
i_n	Input-referred current noise	f = 10kHz		5		fA/√Hz
z_O	Closed-loop output impedance	f = 100kHz		0.007		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	f = dc, V_O = ±8V	108	120		dB
V_{OS}	Input offset voltage			100	550	µV
	Input offset voltage drift	T_A = –40°C to +125°C		2.5	13	µV/°C
	Input bias current			2	30	pA
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = ±5V	88	105		dB
		T_A = –40°C to +125°C	88			

6.5 Electrical Characteristics: 24V (continued)

at T_A = 25°C, V_{S+} = 12V, $V_{S–}$ = –12V, common-mode voltage (V_{CM}) = midsupply, R_L = 1kΩ connected to midsupply; for ac specifications, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Allowable input differential voltage	See Figure 6-39		±7		V
	Common-mode input impedance	In closed-loop configuration		12 || 2.5		GΩ || pF
	Differential input capacitance	In open-loop configuration		0.5		pF
	Most positive input voltage	ΔV_{OS} < 5mV(1)	V_{S+} + 0.2	V_{S+} + 0.3		V
	Most negative input voltage	ΔV_{OS} < 5mV(1)	$V_{S–}$ – 0.2	$V_{S–}$ – 0.3		V
OUTPUT						
V_{OH}	Output voltage high	R_L = 667Ω	V_{S+} – 0.33	V_{S+} – 0.22		V
		T_A = –40°C to +125°C, R_L = 667Ω	V_{S+} – 0.36			
V_{OL}	Output voltage low	R_L = 667Ω		$V_{S–}$ + 0.15	$V_{S–}$ + 0.23	V
		T_A = –40°C to +125°C, R_L = 667Ω			$V_{S–}$ + 0.33	
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_O= 7.25V, R_L = 151Ω, ΔV_{OS} < 1mV	48	64		mA
I_{SC}	Output short-circuit current			108		mA
C_L	Capacitive load drive	< 3dB peaking, R_S = 0Ω		10		pF
POWER SUPPLY						
I_Q	Quiescent current per channel			3.8	4.7	mA
PSRR	Power supply rejection ratio	ΔV_S = ±2V(2)	90	105		dB
		T_A = –40°C to +125°C	90			
AUXILIARY CMOS INPUT STAGE						
	Gain-bandwidth product			27		MHz
	Input-referred voltage noise	f = 1MHz		20		nV/√Hz
	Input offset voltage	V_{CM} = V_{S+} – 1.5V, no load			1.7	mV

(1) Change in input offset when input is biased to midsupply.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and −PSRR.
(3) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, over temperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.

6.6 Electrical Characteristics: 5V

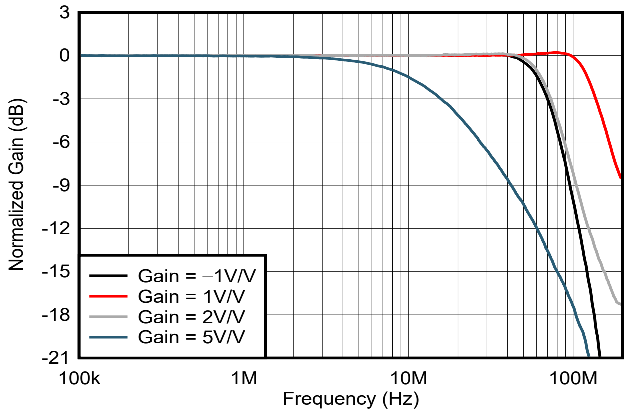
at T_A = 25°C, V_{S+} = 5V, $V_{S–}$ = 0V, common-mode voltage (V_{CM}) = 1.25V, R_L = 1kΩ connected to 1.25V; for ac specifications, V_{S+} = 3.5V, $V_{S–}$ = –1.5V, gain (G) = 2V/V, R_F = 1kΩ, C_L = 4.7pF, and V_{CM} = 0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 1, V_O = 20mV_{PP}, R_F = 0Ω		133		MHz
LSBW	Large-signal bandwidth	G = 2, V_O = 2V_{PP}		36		MHz
GBWP	Gain-bandwidth product			70		MHz
	Bandwidth for 0.1dB flatness	G = 2, V_O = 20mV_{PP}		16		MHz
SR	Slew rate (20%–80%)[3]	G = 2, V_O = –1V to +1V step		134		V/µs
	Rise and fall time	V_O = 200mV step		4		ns
	Settling time	G = 2, V_O = –2V to 0V step, to 0.1%, V_S = ±2.5V		100		ns
	Input overdrive recovery	G = 1, V_S = ±2.5V, ($V_{S–}$ – 0.5V) to (V_{S+} + 0.5V) input		76		ns
	Output overdrive recovery	G = –1, V_S = ±2.5V, ($V_{S–}$ – 0.5V) to (V_{S+} + 0.5V) input		93		ns
HD2	2nd harmonic distortion	f = 100kHz, V_O = 2V_{PP}		–102		dBc
HD3	3rd harmonic distortion	f = 100kHz, V_O = 2V_{PP}		–114		dBc
e_n	Input-referred voltage noise	Flat-band, 1/f corner at 1.5kHz		6.3		nV/√Hz
z_O	Closed-loop output impedance	f = 100kHz		0.007		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	f = dc, V_O = 1.25V to 3.25V		118		dB
V_{OS}	Input offset voltage			100		µV
	Input offset voltage drift	T_A = –40°C to +125°C		2.5		µV/°C
	Input bias current			2		pA
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = 0.75V to 1.75V		92		dB
INPUT						
	Allowable input differential voltage	See Figure 6-39		±5		V
	Common-mode input impedance	In closed-loop configuration		12 || 2.5		GΩ || pF
	Differential input capacitance	In open-loop configuration		0.5		pF
	Most positive input voltage	ΔV_{OS} < 5mV[1]		V_{S+} + 0.3		V
	Most negative input voltage	ΔV_{OS} < 5mV[1]		V_{S-} – 0.3		V
OUTPUT						
V_{OH}	Output voltage high	R_L = 667Ω		V_{S+} – 0.09		V
V_{OL}	Output voltage low	R_L = 667Ω		$V_{S–}$+ 0.06		V
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_O = 1.4V, R_L = 27.5Ω, ΔV_{OS} < 1mV, V_{S+} = 3V, $V_{S–}$ = –2V		64		mA
I_{SC}	Output short-circuit current			96		mA
C_L	Capacitive load drive	< 3dB peaking, R_S = 0Ω		10		pF
POWER SUPPLY						
I_Q	Quiescent current per channel		3.15	3.7	4.5	mA
PSRR	Power-supply rejection ratio	ΔV_S = ±0.5V[2]		100		dB

(1) Change in input offset when input is biased to 0V.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and −PSRR.
(3) Lower of the measured positive and negative slew rate.

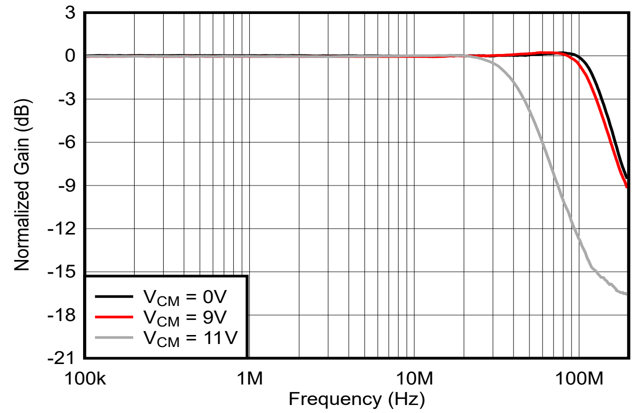
6.7 Typical Characteristics: V_S = 24V

at V_{S+} = 12V, V_{S-} = –12V, R_L = 1kΩ, input and output are biased to midsupply, and T_A ≅ 25°C; for ac specifications, V_O = $2V_{PP}$, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)



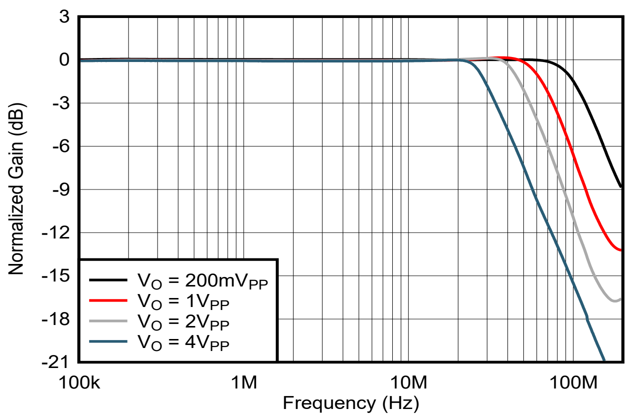
See Figure 8-1 and Figure 8-2, V_O = $20mV_{PP}$

Figure 6-1. Noninverting Small-Signal Frequency Response vs Gain



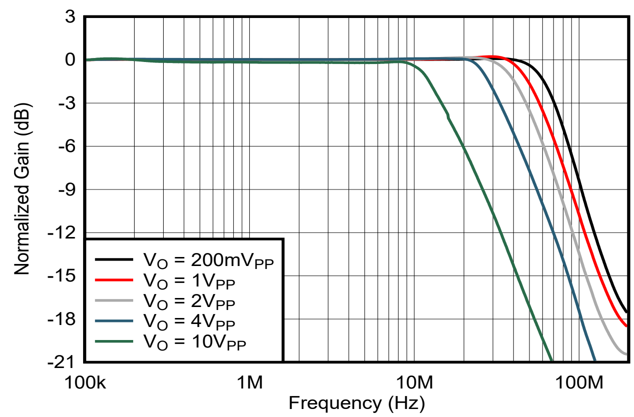
See Figure 8-1, V_O = $20mV_{PP}$, G = 1V/V, C_L = 4.7pF, R_F = 0Ω

Figure 6-2. Small-Signal Frequency Response vs Output Common-Mode Voltage



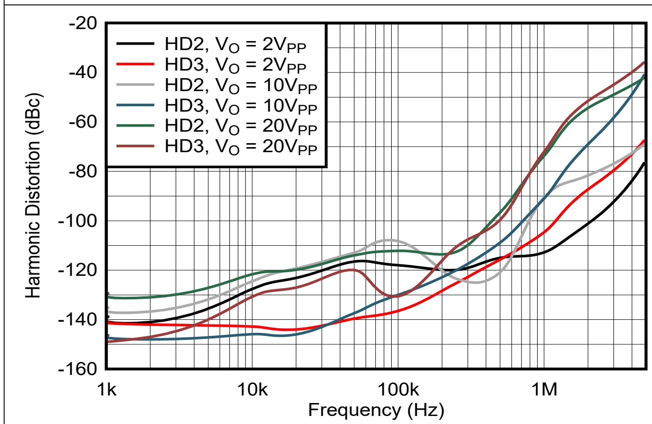
See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-3. Large-Signal Frequency Response vs V_O



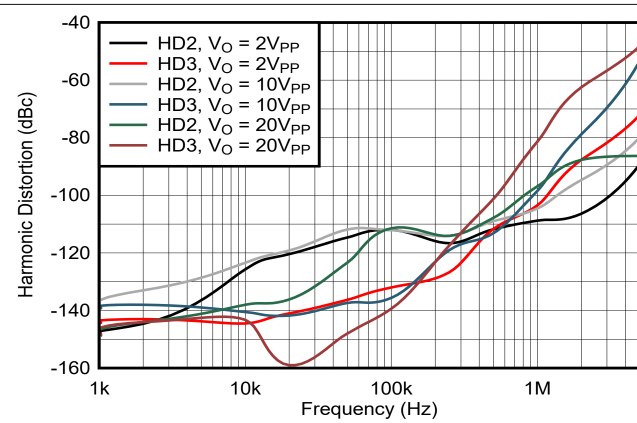
See Figure 8-1, G = 2V/V

Figure 6-4. Large-Signal Frequency Response vs V_O



See Figure 8-1, G = 2V/V

Figure 6-5. Harmonic Distortion vs Frequency vs V_O

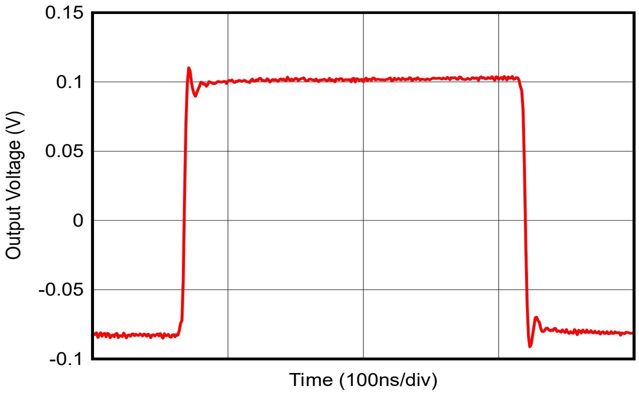


See Figure 8-2, G = –1V/V

Figure 6-6. Harmonic Distortion vs Frequency vs V_O

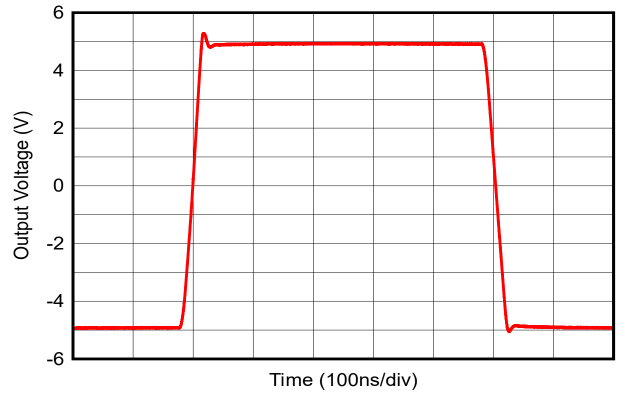
6.7 Typical Characteristics: V_S = 24V (continued)

at V_{S+} = 12V, V_{S-} = –12V, R_L = 1kΩ, input and output are biased to midsupply, and T_A ≅ 25°C; for ac specifications, V_O = $2V_{PP}$, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)



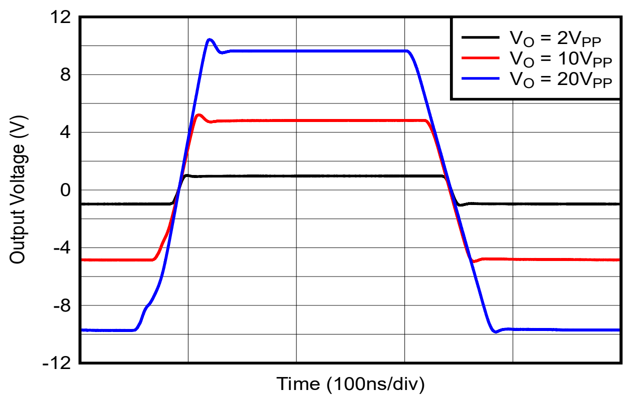
See Figure 8-1, G = 1V/V, R_F = 0Ω, C_L = 10pF

Figure 6-7. Small-Signal Transient Response



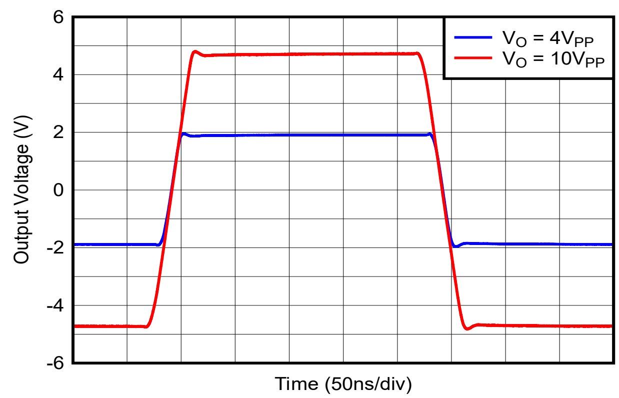
See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-8. Large-Signal Transient Response



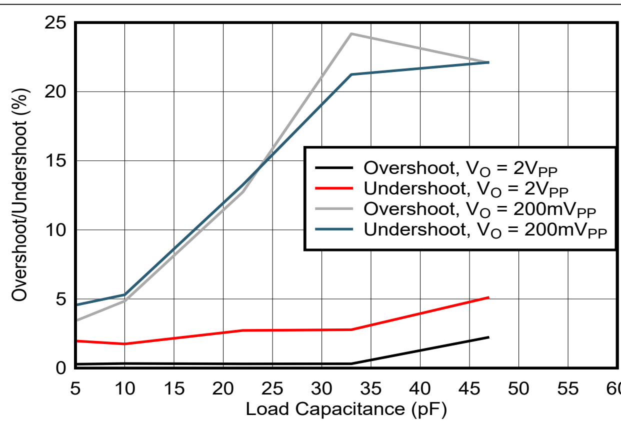
See Figure 8-1, G = 2V/V

Figure 6-9. Large-Signal Transient Response



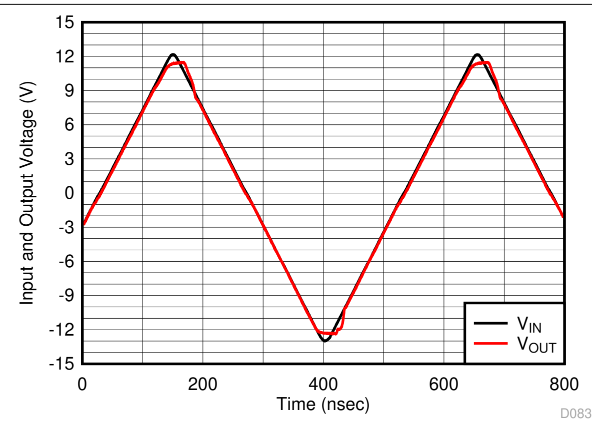
See Figure 8-2, G = –1V/V

Figure 6-10. Large-Signal Transient Response



See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-11. Overshoot and Undershoot vs C_L

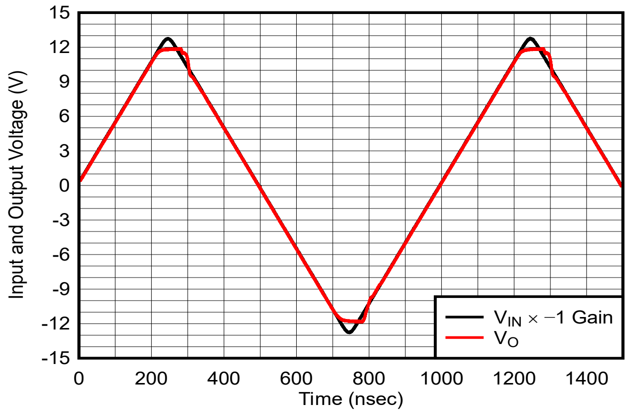


See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-12. Input Overdrive Recovery

6.7 Typical Characteristics: V_S = 24V (continued)

at V_{S+} = 12V, V_{S-} = –12V, R_L = 1kΩ, input and output are biased to midsupply, and T_A ≅ 25°C; for ac specifications, V_O = 2V_{PP}, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)



See Figure 8-2, G = –1V/V

Figure 6-13. Output Overdrive Recovery

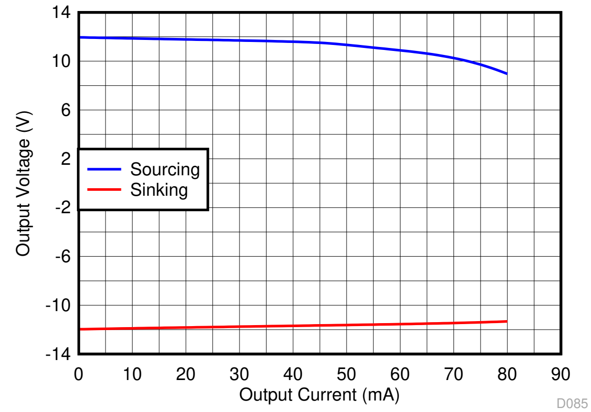
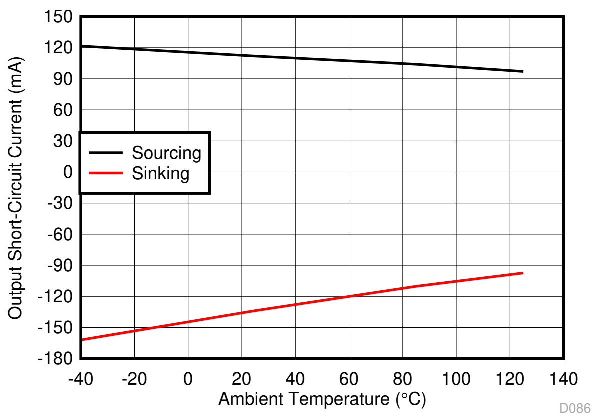
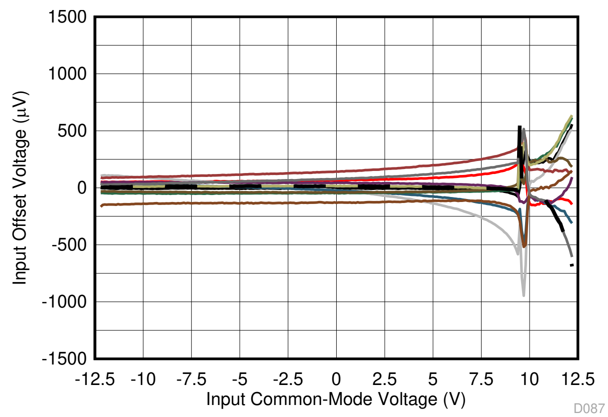


Figure 6-14. Output Voltage Range vs Load Current



Output saturated and then short-circuited

Figure 6-15. Output Short-Circuit Current vs Ambient Temperature

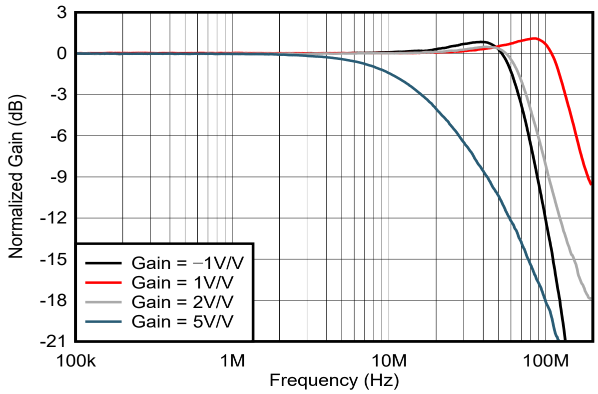


Measured for 12 units

Figure 6-16. Input Offset Voltage vs Input Common-Mode Voltage

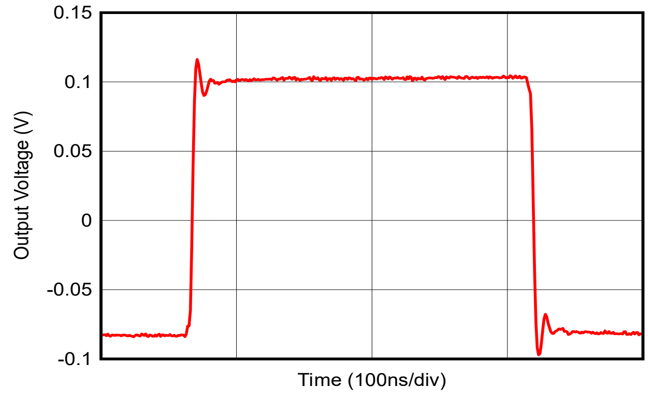
6.8 Typical Characteristics: V_S = 5V

at V_{S+} = 5V, V_{S-} = 0V, V_{CM}= 1.25V, R_L = 1kΩ, output is biased to midsupply, and T_A ≅ 25°C; for ac specifications, V_{S+} = 3.5V, V_{S-} = –1.5V, V_{CM} = 0V, V_O = $2V_{PP}$, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)



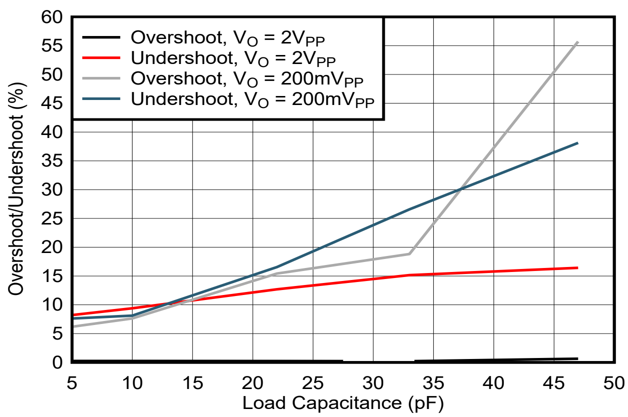
See Figure 8-1 and Figure 8-2, V_O = $20mV_{PP}$

Figure 6-17. Small-Signal Response vs Gain



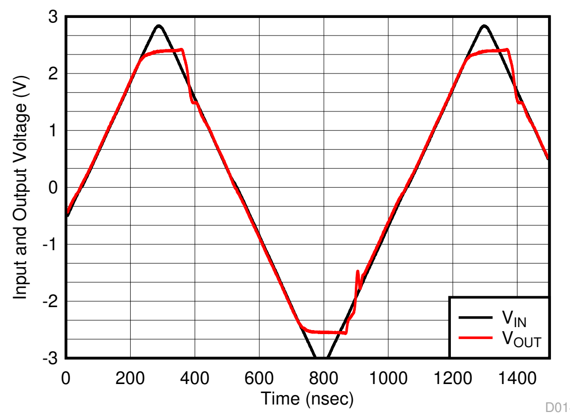
See Figure 8-1, G = 1V/V, R_F = 0Ω, C_L = 10pF

Figure 6-18. Small-Signal Transient Response



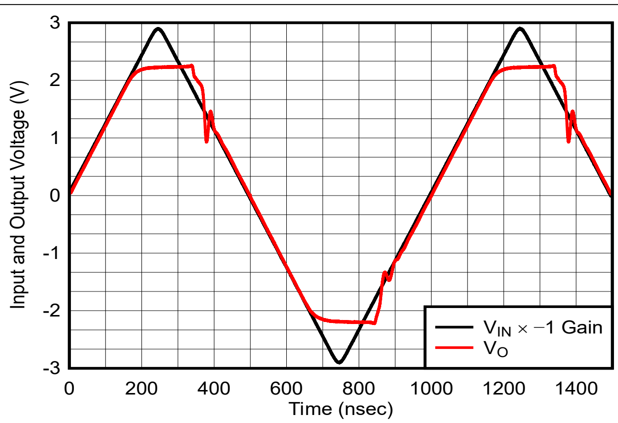
See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-19. Overshoot and Undershoot vs C_L



See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-20. Input Overdrive Recovery



See Figure 8-2, G = –1V/V

Figure 6-21. Output Overdrive Recovery

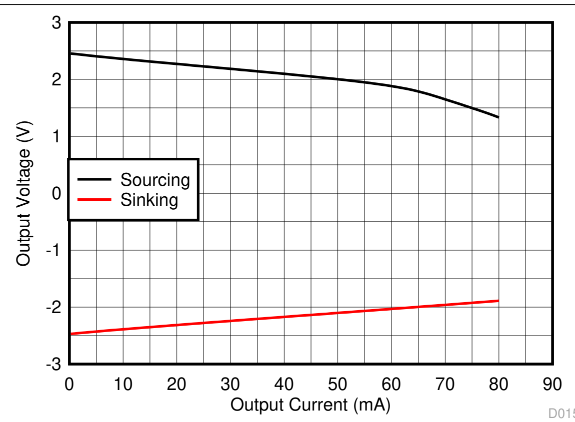
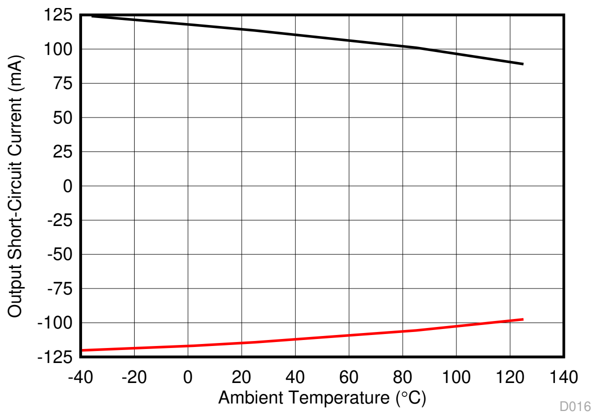


Figure 6-22. Output Voltage Range vs Output Current

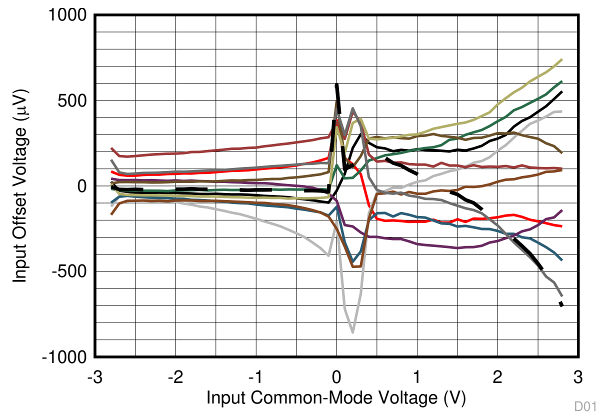
6.8 Typical Characteristics: V_S = 5V (continued)

at V_{S+} = 5V, V_{S-} = 0V, V_{CM}= 1.25V, R_L = 1kΩ, output is biased to midsupply, and T_A ≅ 25°C; for ac specifications, V_{S+} = 3.5V, V_{S-} = –1.5V, V_{CM} = 0V, V_O = $2V_{PP}$, gain (G) = 2V/V, R_F = 1kΩ, and C_L = 4.7pF (unless otherwise noted)



Output saturated and then short-circuited

Figure 6-23. Output Short-Circuit Current vs Ambient Temperature

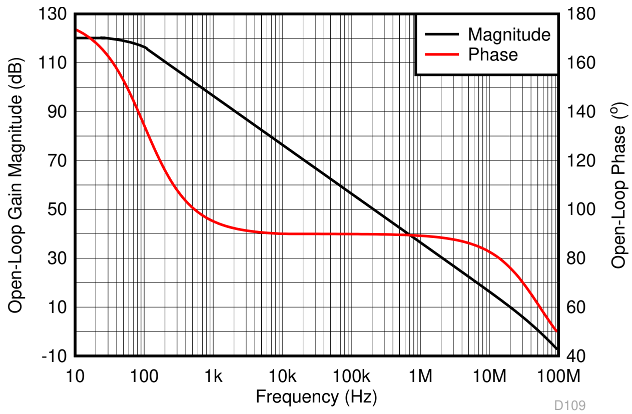


Measured for 12 units

Figure 6-24. Input Offset Voltage vs Input Common-Mode Voltage

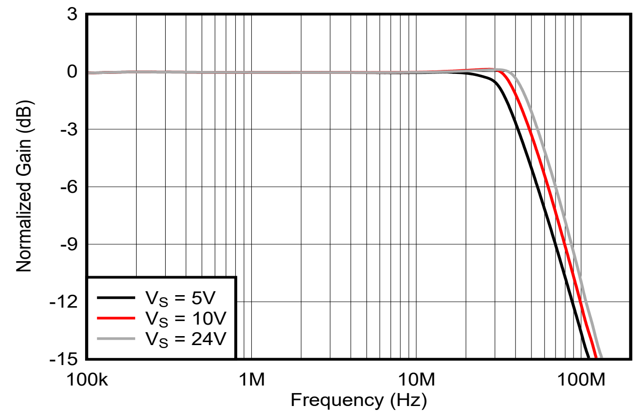
6.9 Typical Characteristics: ±2.375V to ±12V Split Supply

at V_O = 2V_{PP}, R_F = 1kΩ, R_L = 1kΩ, and T_A ≅ 25°C (unless otherwise noted)



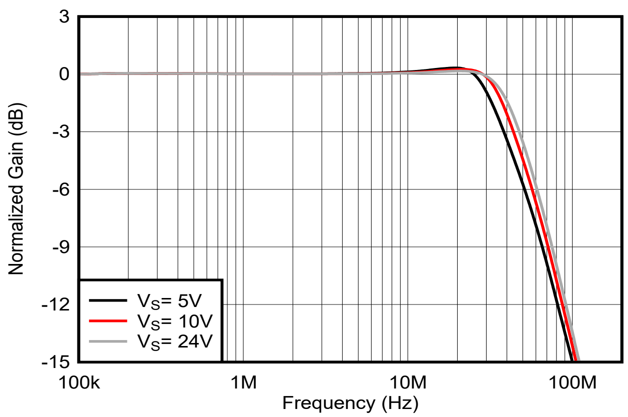
Simulated with no output load

Figure 6-25. Open-Loop Gain and Phase vs Frequency



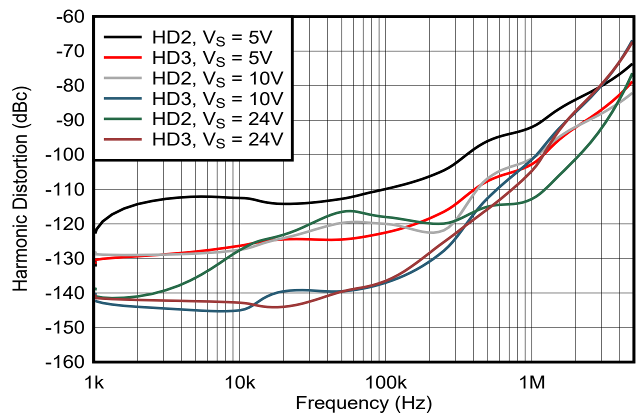
See Figure 8-1, G = 1V/V, R_F = 0Ω

Figure 6-26. Large-Signal Response vs Supply Voltage



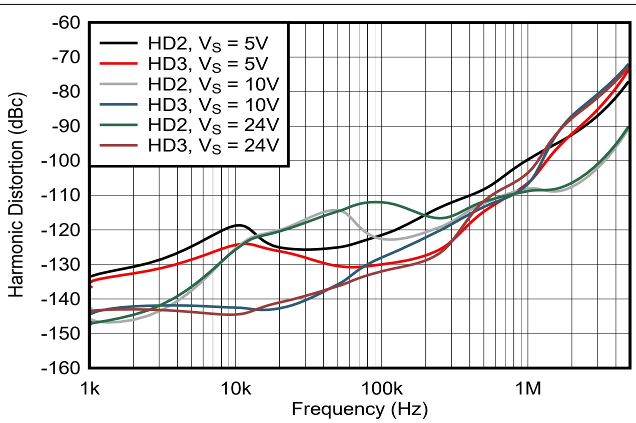
See Figure 8-1, G = 2V/V

Figure 6-27. Large-Signal Response vs Supply Voltage



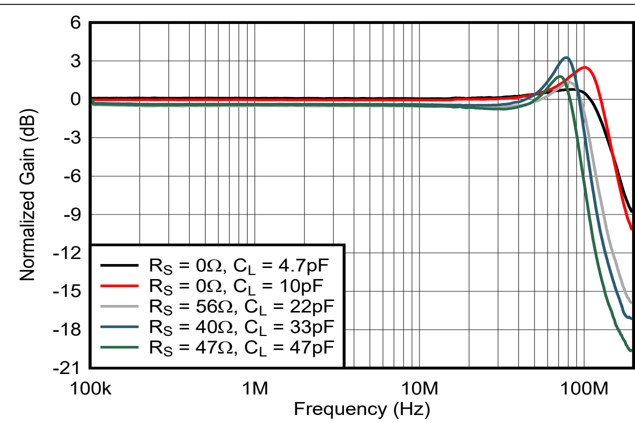
See Figure 8-1, G = 2V/V

Figure 6-28. Harmonic Distortion vs Frequency vs Supply Voltage



See Figure 8-2, G = –1V/V

Figure 6-29. Harmonic Distortion vs Frequency vs Supply Voltage

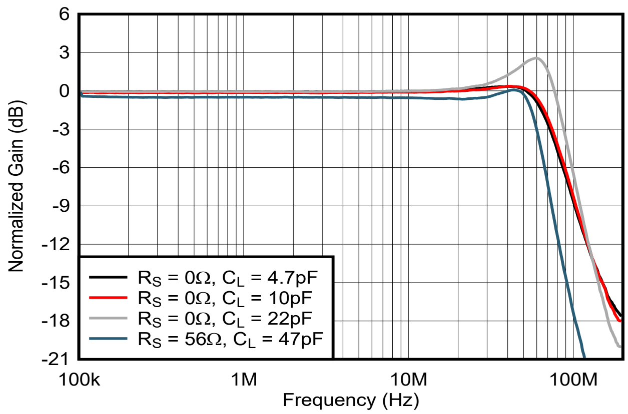


See Figure 8-1 and Figure 7-1,
V_S = 10V, V_O = 20mV_{PP}, gain = 1V/V, R_F = 0Ω

Figure 6-30. Small-Signal Frequency Response vs C_L

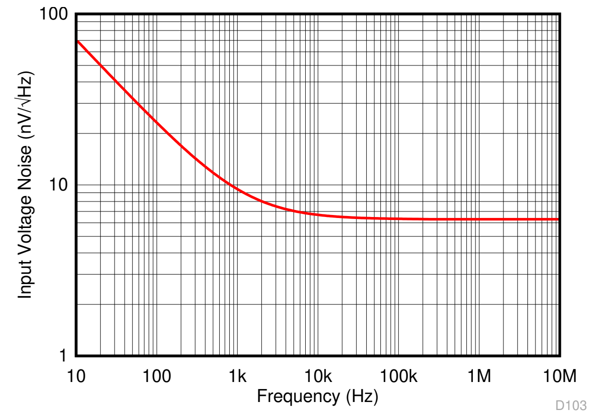
6.9 Typical Characteristics: ±2.375V to ±12V Split Supply (continued)

at V_O = $2V_{PP}$, R_F = 1kΩ, R_L = 1kΩ, and T_A ≅ 25°C (unless otherwise noted)



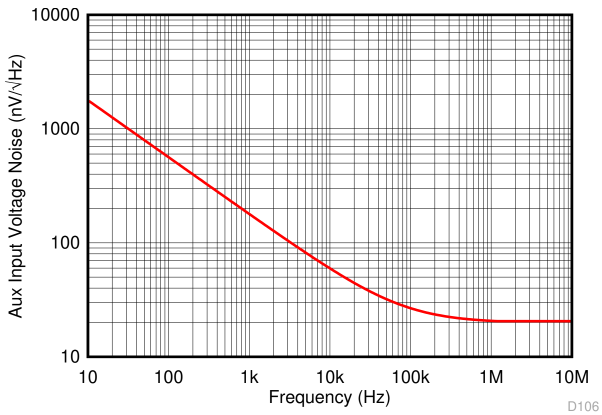
See Figure 8-1and Figure 7-1,
V_S = 10V, V_O = $20mV_{PP}$, gain = 2V/V

Figure 6-31. Small-Signal Frequency Response vs C_L



Measured then fit to 1/f model

Figure 6-32. Input Voltage Noise Density vs Frequency



Measured then fit to 1/f model

Figure 6-33. Auxiliary Input Stage Voltage Noise Density vs Frequency

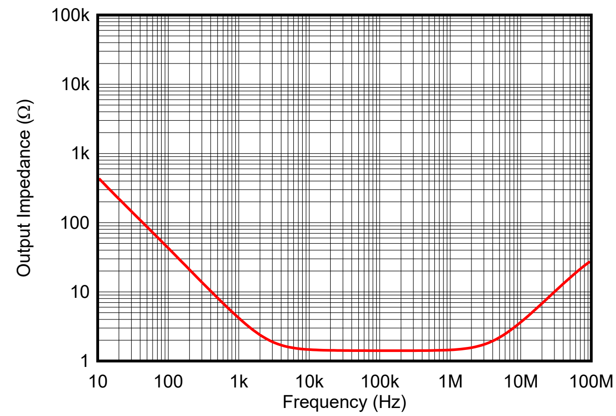
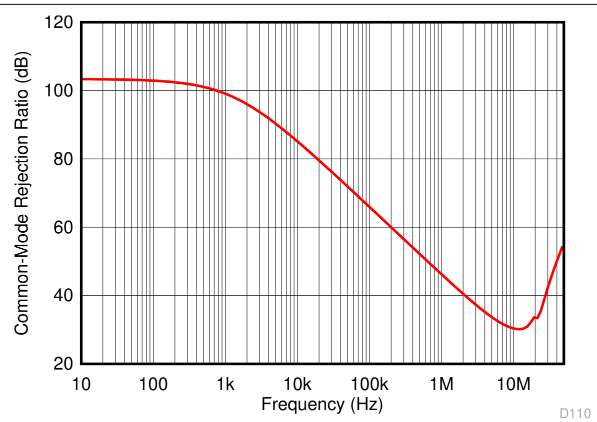
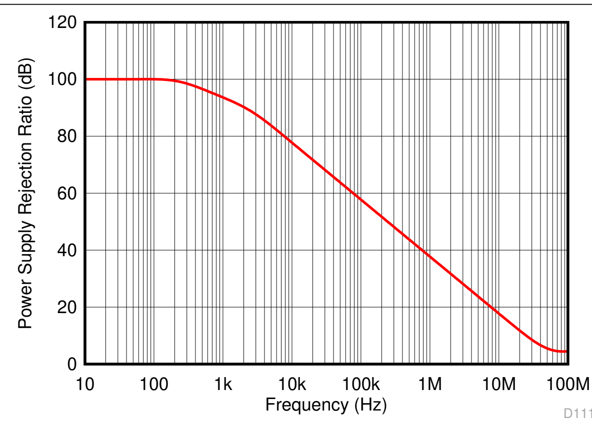


Figure 6-34. Open-Loop Output Impedance vs Frequency



V_S = 10V and 24V

Figure 6-35. Common-Mode Rejection Ratio vs Frequency

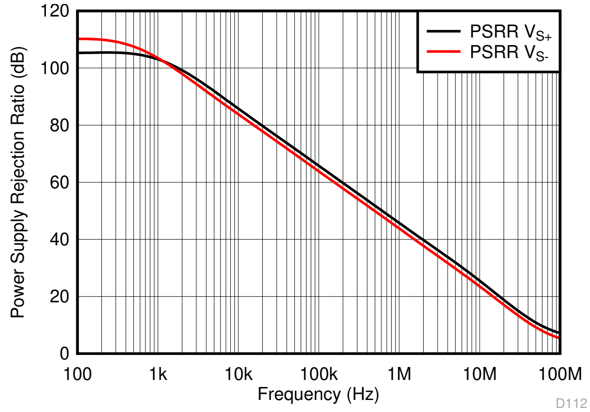


V_S = 5V and 10V

Figure 6-36. Power Supply Rejection Ratio vs Frequency

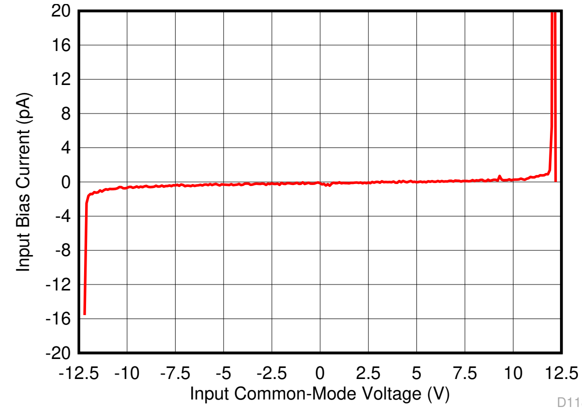
6.9 Typical Characteristics: ±2.375V to ±12V Split Supply (continued)

at V_O = $2V_{PP}$, R_F = 1kΩ, R_L = 1kΩ, and T_A ≅ 25°C (unless otherwise noted)



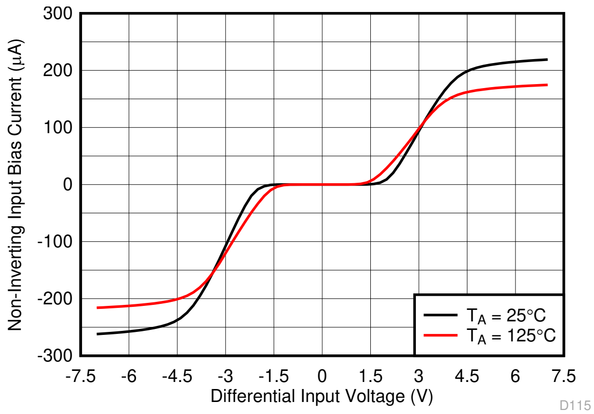
Simulated curves, V_S = 24V

Figure 6-37. Power Supply Rejection Ratio vs Frequency



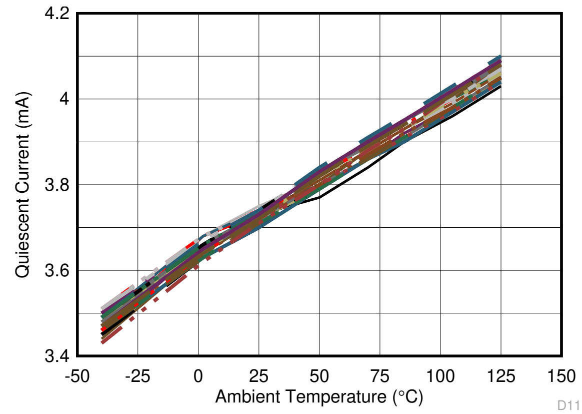
V_S = ±12V

Figure 6-38. Input Bias Current vs Input Common-Mode Voltage



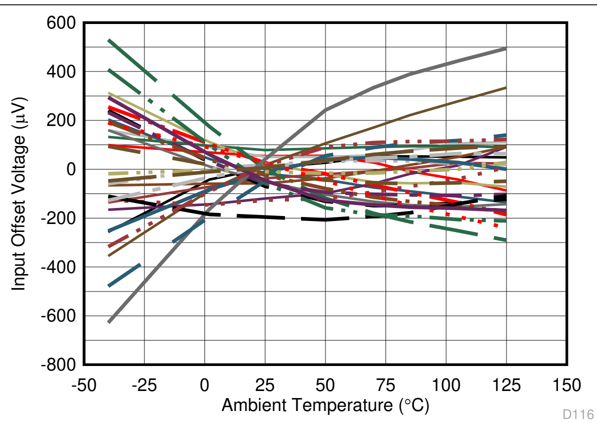
Abs ($V_{IN,Diff\ (max)}$) = V_S when V_S < 7V

Figure 6-39. Input Bias Current vs Differential Input Voltage



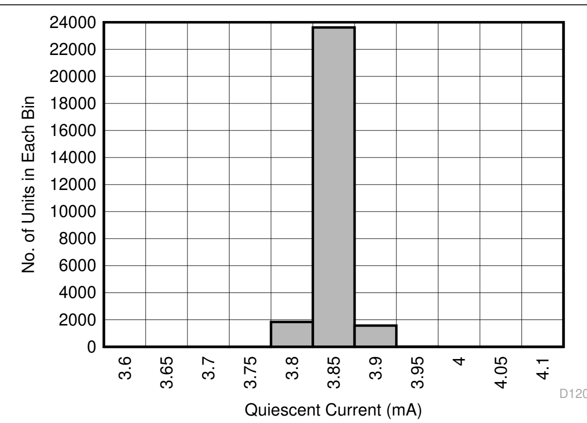
32 units, V_S = ±5V

Figure 6-40. Quiescent Current vs Ambient Temperature



32 units

Figure 6-41. Input Offset Voltage vs Ambient Temperature

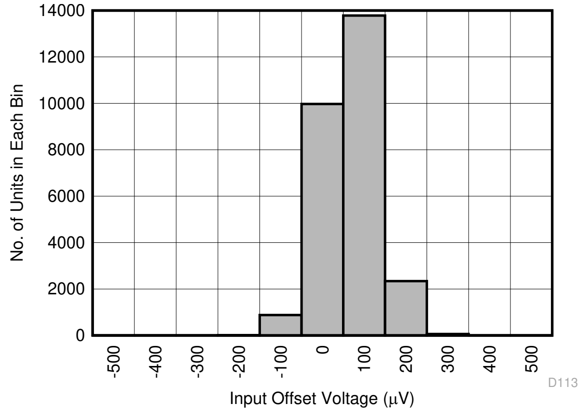


27000 units, μ = 3.82mA, σ = 17μA, V_S = 24V

Figure 6-42. Quiescent Current Distribution

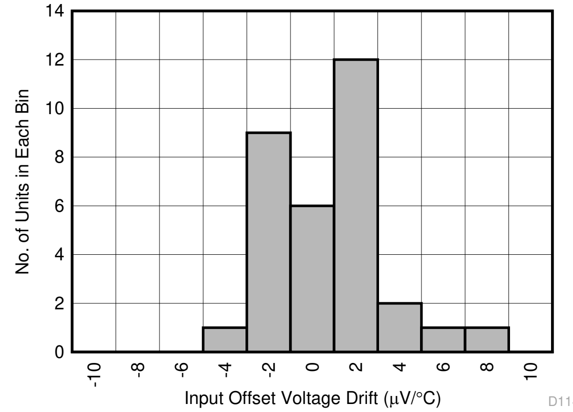
6.9 Typical Characteristics: ±2.375V to ±12V Split Supply (continued)

at $V_O = 2V_{PP}$, $R_F = 1k\Omega$, $R_L = 1k\Omega$, and $T_A \cong 25°C$ (unless otherwise noted)



27000 units, μ = 16μV, σ = 63μV, V_S = 24V

Figure 6-43. Input Offset Voltage Distribution



–40°C to +125°C fit, 32 units, μ = –0.15μV/°C, σ = 2.5μV/°C

Figure 6-44. Input Offset Voltage Drift Distribution

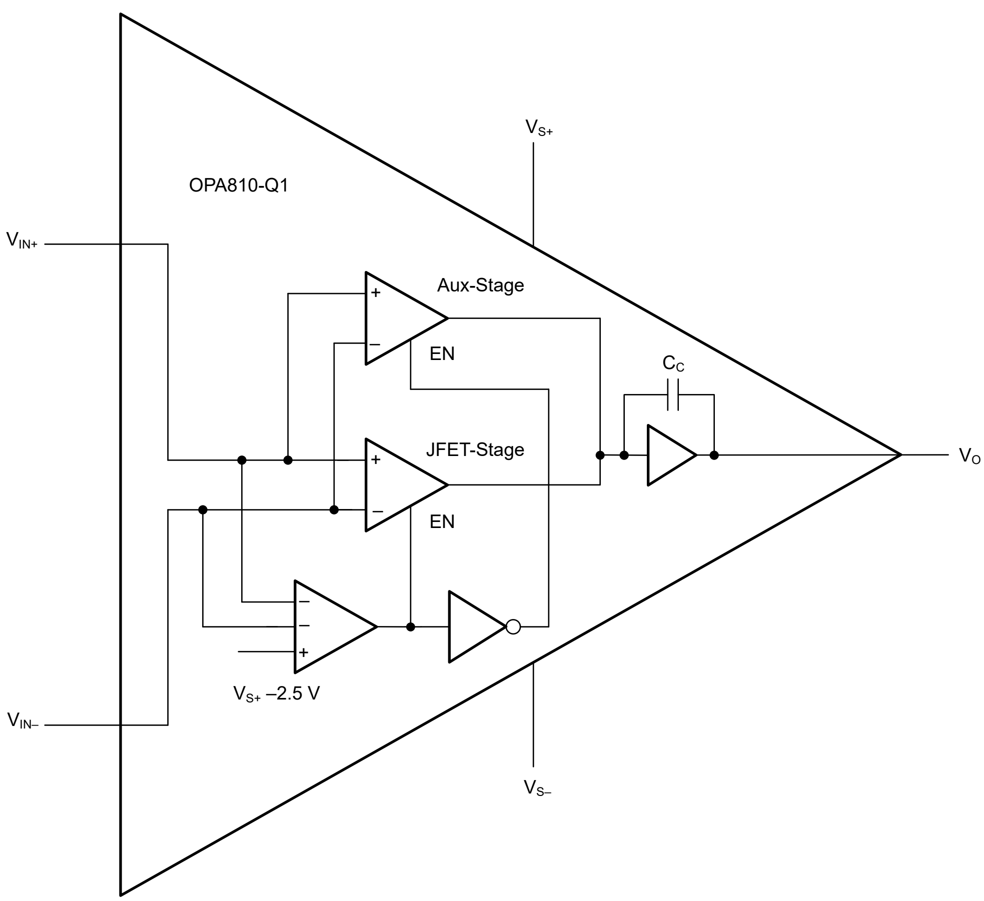
7 Detailed Description

7.1 Overview

The OPA810-Q1 is a single-channel, field-effect transistor (FET)-input, unity-gain stable, voltage-feedback operational amplifier with extremely low input bias current across the common-mode input voltage range. The OPA810-Q1, characterized to operate over a wide supply range of 4.75V to 27V, has a small-signal, unity-gain bandwidth of 140MHz and offers both excellent dc precision and dynamic ac performance at low quiescent power. The OPA810-Q1 is fabricated on Texas Instruments' proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70MHz, extremely high slew rate (200V/µs), and low noise (6.3nV/√Hz), the OPA810-Q1 is designed for a wide range of data-acquisition and signal-processing applications. The OPA810-Q1 includes input clamps to allow maximum input differential voltage of up to 7V, making this device an excellent choice for use with multiplexers and for processing signals with fast transients. The device achieves these benchmark levels of performance while consuming a typical quiescent current (I_Q) of 3.7mA per channel.

The OPA810-Q1 can source and sink large amounts of current without degradation in linearity performance. The wide bandwidth of the OPA810-Q1 implies that the device has low output impedance across a wide frequency range, thereby allowing the amplifier to drive capacitive loads up to 10pF without requiring output isolation. This device is designed for a wide range of data-acquisition, test-and-measurement, front-end buffer, impedance-measurement, power-analyzer, wideband photodiode transimpedance, and signal-processing applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The OPA810-Q1 features a true high-impedance input stage including a JFET differential-input pair main stage and a CMOS differential-input auxiliary (aux) stage operational within 2.5V of the positive supply voltage. The bias current is limited to a maximum of 20pA throughout the common-mode input range of the amplifier. *Section 7.2* provides a block diagram representation for the input stage of the OPA810-Q1. The amplifier exhibits excellent performance for high-speed signals (distortion, noise, and input offset voltage) while the aux stage enables rail-to-rail inputs and prevents phase reversal. The device exhibits a CMRR and PSRR of 75dB (typical) when the input common-mode is in aux stage.

The OPA810-Q1 also includes input clamps that enable the maximum input differential voltage of up to 7V (lower of 7V and total supply voltage). This architecture offers significantly greater differential input voltage capability as compared to one to two times the diode forward voltage drop maximum rating in standard amplifiers, and makes this device an excellent choice for use with multiplexers and processing of signals with fast transients. The input bias currents are also clamped to maximum 300µA, as Figure 6-39 shows, which does not load the previous driver stage or require current-limiting resistors (except limiting current through the input ESD diodes when input common-mode voltages are greater than the supply voltages). This feature also enables this amplifier to be used as a comparator in systems that require an amplifier and a comparator for signal gain and fault detection, respectively. For the lowest offset, distortion, and noise performance, limit the common-mode input voltage to the main JFET-input stage (greater than 2.5V away from the positive supply).

The OPA810-Q1 is a rail-to-rail output amplifier and swings to either of the rails at the output (see also Figure 6-14) for 24V supply operation. The rail-to-rail output configuration is particularly useful for inputs biased near the rails or when the amplifier is configured in a closed-loop gain such that the output approaches the supply voltage. When the output saturates, the output recovers within 55ns when the inputs exceed the supply voltages by 0.5V in an G = –1V/V inverting gain with a 10V supply. The outputs are short-circuit protected with the limits of Figure 6-15.

Figure 7-1 shows how an amplifier phase margin reduces and becomes unstable when driving a capacitive load (C_L) at the output. Using a series resistor (R_S) between the amplifier output and load capacitance introduces a zero that cancels the pole formed by the amplifier output impedance and C_L in the open-loop transfer function. The OPA810-Q1 drives capacitive loads of up to 10pF without causing instability. Use a series resistor for larger load capacitance values (see also Figure 6-30) when the OPA810-Q1 is configured as a unity-gain buffer. Figure 6-31 shows that when used in a gain larger than 1V/V, the OPA810-Q1 is able to drive a load capacitance larger than 10pF without the need for a series resistor at the output.

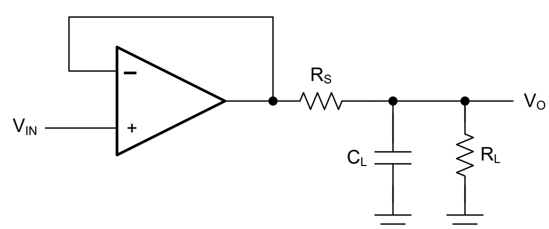


Figure 7-1. OPA810-Q1 Driving Capacitive Load

7.3.2 ESD Protection

As Figure 7-2 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10mA continuous input and output currents. The differential input clamps only limit the bias current when the input common-mode voltages are within the supply voltage range. However, current-limiting series resistors must be added at the inputs if common-mode voltages higher than the supply voltages are possible. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.

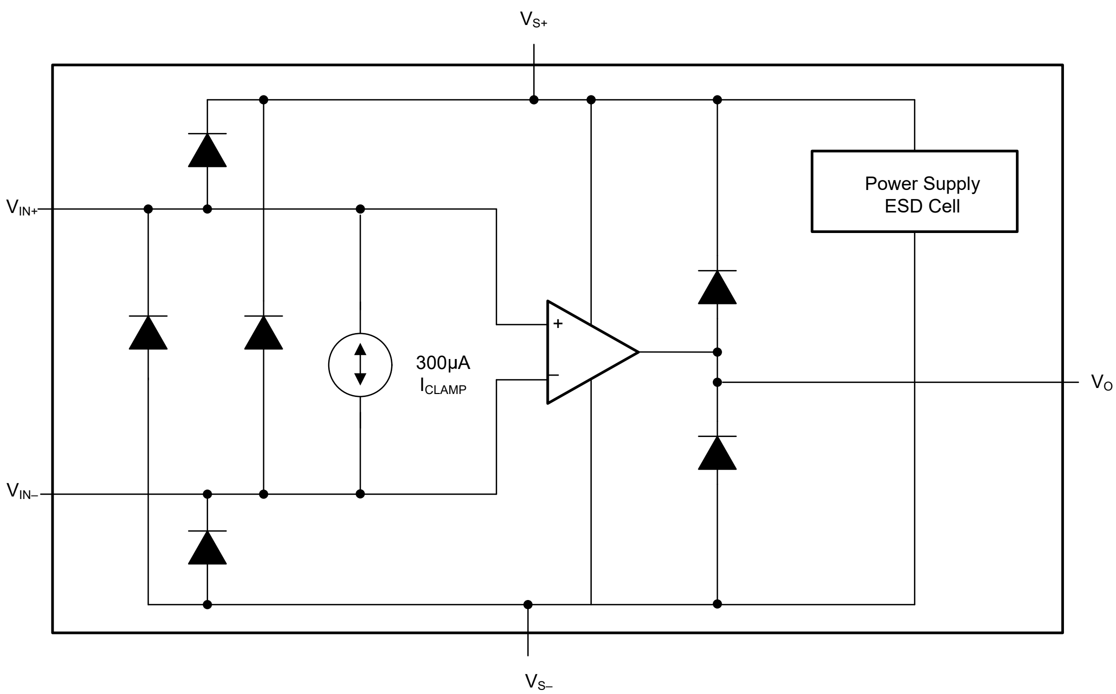


Figure 7-2. Internal ESD Protection

7.4 Device Functional Modes

7.4.1 Split-Supply Operation (±2.375V to ±13.5V)

To facilitate testing with common lab equipment, the OPA810-Q1 can be configured to allow for split-supply operation (see the *SOT-23 5-pin or 6-pin Evaluation Module user guide*). This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference the inputs and outputs to ground. Figure 8-1 depicts the OPA810-Q1 configured as a noninverting amplifier and Figure 8-2 illustrates the OPA810-Q1 configured as an inverting amplifier. For split-supply operation referenced to ground, the power supplies V_{S+} and V_{S-} are symmetrical around ground and V_{REF} is at GND. Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

7.4.2 Single-Supply Operation (4.75V to 27V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA810-Q1 can be used with a single supply (with the negative supply set to ground) with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a balanced, single-supply configuration, level shift all voltages by half the difference between the power-supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the *Single-Supply Op Amp Design Techniques* application report for examples of single-supply designs.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Amplifier Gain Configurations

The OPA810-Q1 is a classic voltage-feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (see also Figure 8-1 and Figure 8-2) include the noninverting and inverting gain configurations. The dc operating point for each configuration is level-shifted by reference voltage V_{REF} that is typically set to midsupply in single-supply operation. V_{REF} is often connected to ground in split-supply applications.

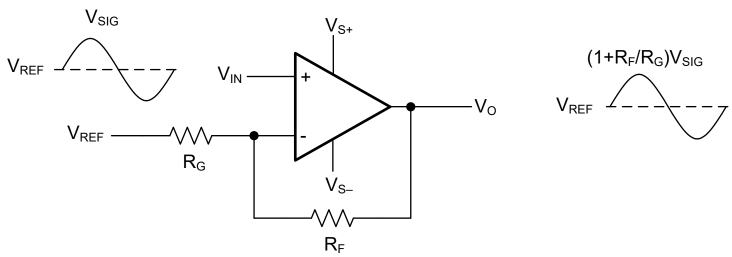


Figure 8-1. Noninverting Amplifier

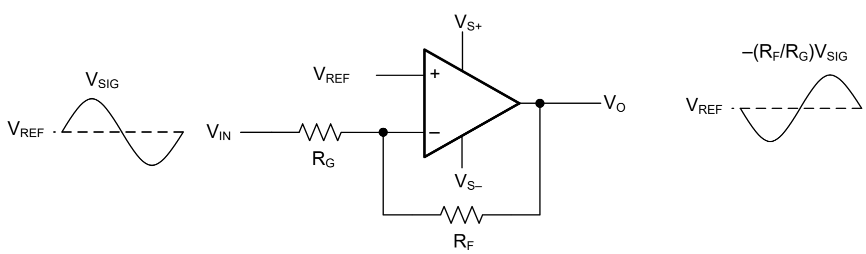


Figure 8-2. Inverting Amplifier

Equation 1 shows the closed-loop gain of an amplifier in a noninverting configuration.

$$V_O = V_{IN}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \tag{1}$$

Equation 2 shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right) + V_{REF} \tag{2}$$

8.1.2 Selection of Feedback Resistors

The OPA810-Q1 is a classic voltage-feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (see also Figure 8-3 and Figure 8-4) include the noninverting- and inverting-gain configurations. The dc operating point for each configuration is level-shifted by the reference voltage V_{REF}, which is typically set to midsupply in single-supply operation. V_{REF} is often connected to ground in split-supply applications.

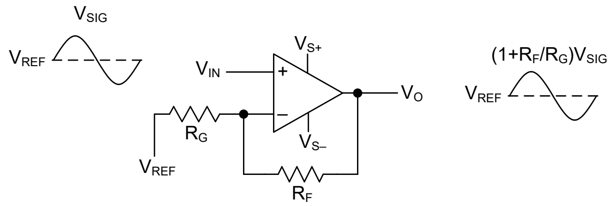


Figure 8-3. Noninverting Amplifier

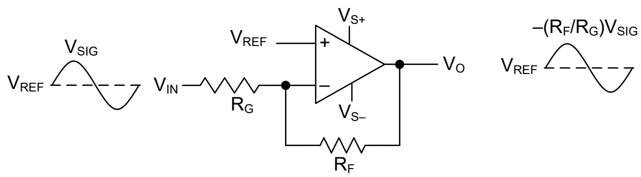


Figure 8-4. Inverting Amplifier

Equation 3 shows the closed-loop gain of an amplifier in noninverting configuration.

$$V_O = V_{IN}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \tag{3}$$

Equation 4 shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right) + V_{REF} \tag{4}$$

The magnitude of the low-frequency gain is determined by the ratio of the magnitudes of the feedback resistor (R_F) and the gain setting resistor R_G. The order of magnitudes of the individual values of R_F and R_G offer a trade-off between amplifier stability, power dissipated in the feedback resistor network, and total output noise. The feedback network increases the loading on the amplifier output. Using large values of the feedback resistors reduces the power dissipated at the amplifier output. Conversely, large feedback-resistor values increase the inherent voltage and amplifier current noise contribution seen at the output while lowering the frequency at which a pole occurs in the feedback factor (β). This pole causes a decrease in the phase margin at zero-gain crossover frequency and potential instability. Using small feedback resistors increases power dissipation and also degrades amplifier linearity due to a heavier amplifier output load. Figure 8-5 illustrates a representative schematic of the OPA810-Q1 in an inverting configuration with the input capacitors shown.

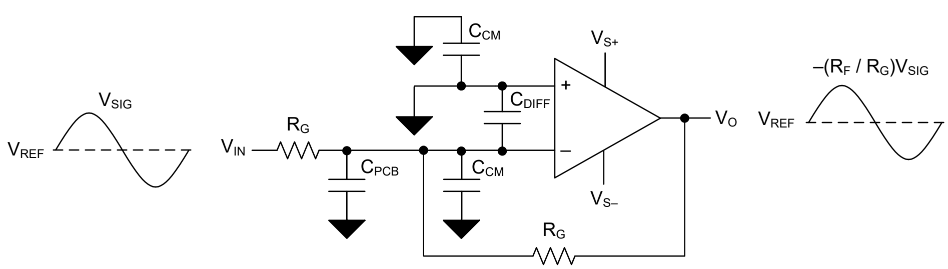


Figure 8-5. Inverting Amplifier With Input Capacitors

The effective capacitance at the amplifier inverting input pin is shown in Equation 5, which forms a pole in β at a cutoff frequency of Equation 6.

$$C_{IN} = C_{CM} + C_{DIFF} + C_{PCB} \quad (5)$$

where

- C_{CM} is the amplifier common-mode input capacitance
- C_{DIFF} is the amplifier differential input capacitance
- C_{PCB} is the printed circuit board (PCB) parasitic capacitance

$$f_C = \frac{1}{2\pi R_F C_{IN}} \quad (6)$$

For low-power systems, greater the values of the feedback resistors, the earlier in frequency does the phase margin begin to reduce and cause instability. Figure 8-6 and Figure 8-7 illustrate the loop gain magnitude and phase plots, respectively, for the OPA810-Q1 simulation in TINA-TI configured as an inverting amplifier with values of feedback resistors varying by orders of magnitudes.

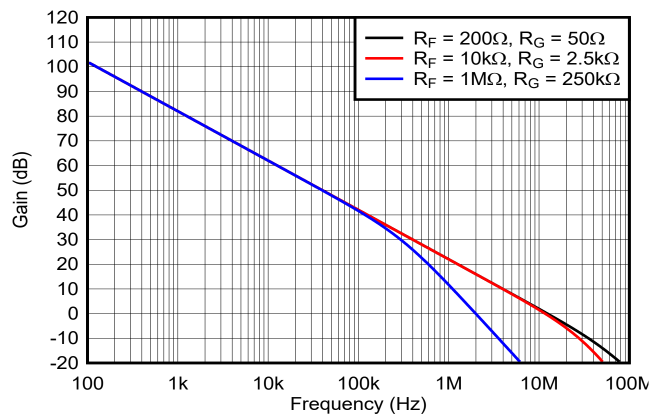


Figure 8-6. Loop-Gain vs Frequency for Circuit of Figure 8-5

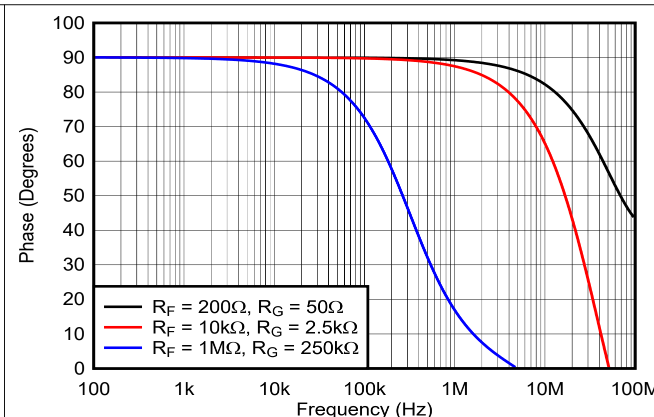


Figure 8-7. Loop-Gain Phase vs Frequency for Circuit of Figure 8-5

A lower phase margin results in peaking in the frequency response and lower bandwidth as Figure 8-8 shows, which is synonymous with overshoot and ringing in the pulse response results. The OPA810-Q1 offers a flat-band voltage noise density of 6.3nV/√Hz. TI recommends selecting an R_F so the voltage noise contribution does not exceed that of the amplifier. Figure 8-9 shows the voltage noise density variation with value of resistance at 25°C. A 2kΩ resistor exhibits a thermal noise density of 5.75nV/√Hz which is comparable to the flat-band noise of the OPA810-Q1. Therefore, use an R_F less than 2kΩ while still large enough to not dissipate excessive power for the output voltage swing and supply current requirements of the application. *Section 8.1.3* shows a detailed analysis of the various contributors to noise.

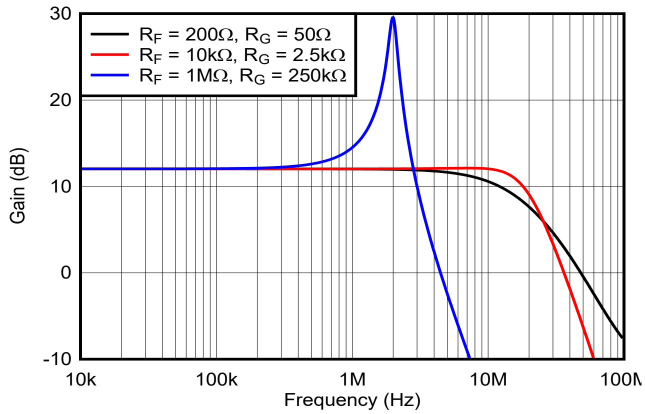


Figure 8-8. Closed-Loop Gain vs Frequency for Circuit of Figure 8-5

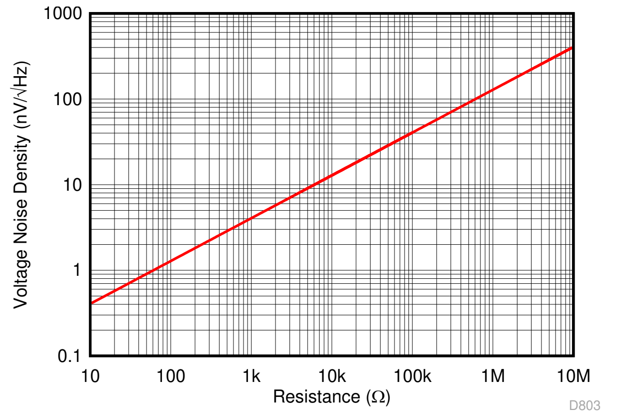


Figure 8-9. Thermal Noise Density vs Resistance

8.1.3 Noise Analysis and the Effect of Resistor Elements on Total Noise

The OPA810-Q1 provides a low input-referred broadband noise voltage density of 6.3nV/√Hz while requiring a low 3.7mA quiescent supply current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 8-10 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in nV/√Hz or pA/√Hz.

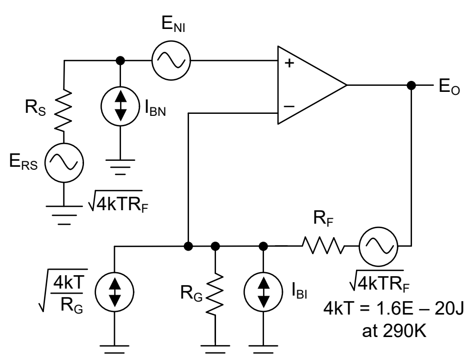


Figure 8-10. Operational-Amplifier Noise-Analysis Model

The total output-spot-noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then calculates the square root to get back to a spot noise voltage. Figure 8-10 shows the general form for this output noise voltage using the terms shown in Equation 7.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \tag{7}$$

Dividing this expression by the noise gain (NG = 1 + R_F / R_G) shows the equivalent input referred spot noise voltage at the noninverting input; see Equation 8.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \tag{8}$$

Substituting large resistor values into Equation 8 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 2kΩ adds a Johnson voltage noise term similar to that of the amplifier (6.3nV/√Hz).

Table 8-1 compares the noise contributions from the various terms when the OPA810-Q1 is configured in a noninverting gain of 5V/V as Figure 8-11 shows. Two cases are considered where the resistor values in case 2 are 10 × the resistor values in case 1. The total output noise in case 1 is 34nV/√Hz, whereas the noise in case 2 is 51.5nV/√Hz. The large value resistors in case 2 dilute the benefits of selecting a low-noise amplifier like the OPA810-Q1. To minimize total system noise, reduce the size of the resistor values. This reduction increases the amplifiers output load and results in a degradation of distortion performance. The increased loading increases the dynamic power consumption of the amplifier. The circuit designer must make the appropriate tradeoffs to maximize the overall performance of the amplifier to match the system requirements.

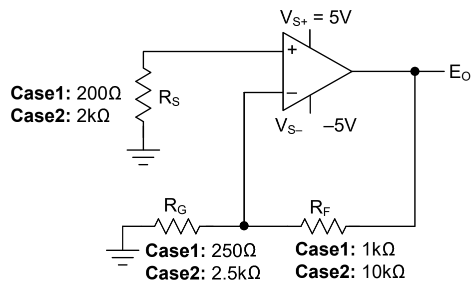


Figure 8-11. Comparing Noise Contributors: Two Cases With the Amplifier in a Noninverting Gain of 5V/V

Table 8-1. Comparing Noise Contributions for the Circuit in Figure 8-11

NOISE SOURCE	OUTPUT NOISE EQUATION	CASE 1				CASE 2			
		NOISE SOURCE VALUE	VOLTAGE NOISE CONTRIBUTION (nV/√Hz)	NOISE POWER CONTRIBUTION (nV^2/Hz)	CONTRIBUTION (%)	NOISE SOURCE VALUE	VOLTAGE NOISE CONTRIBUTION (nV/√Hz)	NOISE POWER CONTRIBUTION (nV^2/Hz)	CONTRIBUTION (%)
Source resistor, R_S	E_{RS} (1 + R_F /R_G)	1.82nV/√Hz	9.1	82.81	7.15	5.76nV/√Hz	28.8	829.44	31.29
Gain resistor, R_G	E_{RG} (R_F / R_G)	2.04nV/√Hz	8.16	66.59	5.75	6.44nV/√Hz	25.76	663.58	25.03
Feedback resistor, R_F	E_{RF}	4.07nV/√Hz	4.07	16.57	1.43	12.87nV/√Hz	12.87	165.64	6.25
Amplifier voltage noise, E_{NI}	E_{NI} (1 + R_F / R_G)	6.3nV/√Hz	31.5	992.25	85.67	6.3nV/√Hz	31.5	992.25	37.43
Inverting current noise, I_{BI}	I_{BI} (R_F || R_G)	5fA/√Hz	5.0E-3	—	—	5fA/√Hz	50E-3	—	—
Noninverting current noise, I_{BN}	$I_{BN}R_S$ (1 + R_F/ R_G)	5fA/√Hz	1.0E-3	—	—	5fA/√Hz	10E-3	—	—

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

The high GBWP and low input voltage and current noise for the OPA810-Q1 make this device an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

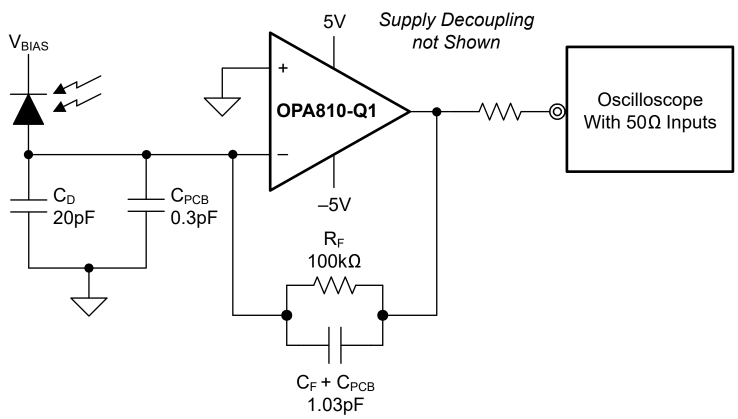


Figure 8-12. Wideband, High-Sensitivity, Transimpedance Amplifier

8.2.1.1 Design Requirements

Table 8-2 lists the design requirements for a high-bandwidth, high-gain transimpedance amplifier circuit.

Table 8-2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Target bandwidth	> 2MHz
Transimpedance gain	100kΩ
Photodiode capacitance	20pF

8.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA810-Q1. This input voltage noise is peaked up over frequency by the diode source capacitance, and can (in many cases) become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_{BIAS}) applied, the desired transimpedance gain, R_F, and the GBWP for the OPA810-Q1 (70MHz). Figure 8-12 shows a transimpedance circuit with the parameters as described in Table 8-2. With these three variables set (and including the parasitic input capacitance for the OPA810-Q1 and the printed circuit board (PCB) added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response. The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses using high-speed amplifiers for transimpedance applications. Set the feedback pole according to Equation 9 to achieve a maximally-flat second-order Butterworth frequency response:

$$\frac{1}{2\pi R_F C_{IN}} = \sqrt{\frac{GBWP}{4\pi R_F C_D}} \tag{9}$$

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (2.0 + 0.5)pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3pF. Using Equation 5 gives a total input capacitance of C_D = 22.8pF. From Equation 9, set the feedback pole at 1.55MHz. Setting the pole at 1.55MHz requires a total feedback capacitance of 1.03pF.

Equation 10 shows the approximate –3dB bandwidth of the transimpedance amplifier circuit:

$$f_{-3dB} = \sqrt{\frac{GBWP}{2\pi R_F C_D}}Hz \quad (10)$$

Equation 10 estimates a closed-loop bandwidth of 2.19MHz. Figure 8-13 and Figure 8-14 show the loop-gain magnitude and phase plots from the TINA-TI simulations of the transimpedance amplifier circuit of Figure 8-12. The 1/β gain curve has a zero from R_F and C_{IN} at 70kHz and a pole from R_F and C_F canceling the 1/β zero at 1.5MHz, resulting in a 20dB per decade rate-of-closure at the loop-gain crossover frequency (the frequency where A_{OL} equals 1/β), providing a stable circuit. A phase margin of 62° is obtained with a closed-loop bandwidth of 3MHz and a 100kΩ transimpedance gain.

8.2.1.3 Application Curves

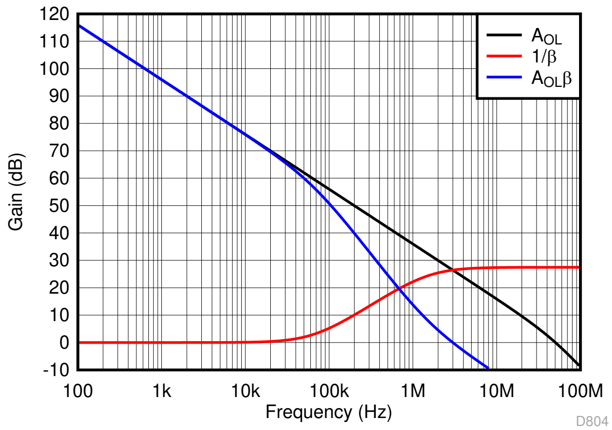


Figure 8-13. Loop-Gain Magnitude vs Frequency for the Transimpedance Amplifier Circuit of Figure 8-12

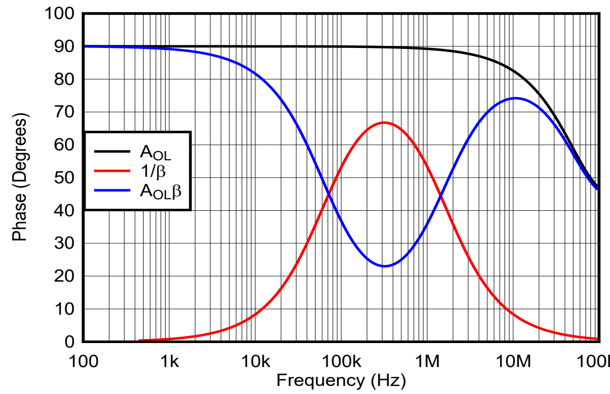


Figure 8-14. Loop-Gain Phase vs Frequency for the Transimpedance Amplifier Circuit of Figure 8-12

8.2.2 Multichannel Sensor Interface

High-Z input amplifiers are particularly useful when interfaced with sensors that have relatively high output impedance. Such multichannel systems typically interface these sensors with the signal chain through a multiplexer. Figure 8-15 shows one such implementation using an amplifier for the interface with each sensor, and driving into an ADC through a multiplexer. An alternate circuit, shown in Figure 8-16, can use a single higher GBWP and fast-settling amplifier at the output of the multiplexer. This architecture gives rise to large signal transients when switching between channels, where the settling performance of the amplifier and maximum allowed differential input voltage limits signal chain performance and amplifier reliability, respectively.

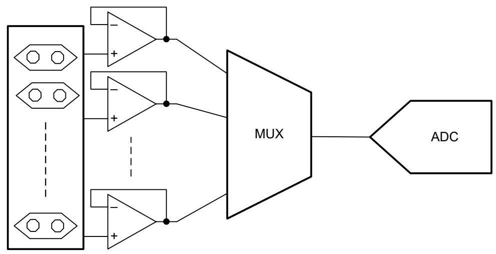


Figure 8-15. Multichannel Sensor Interface Using Multiple Amplifiers

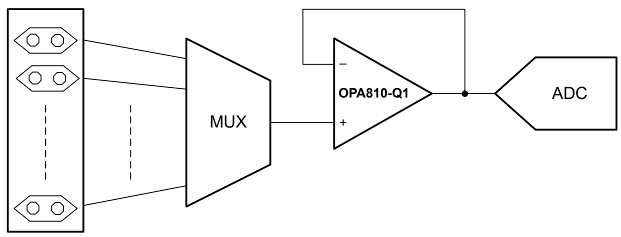


Figure 8-16. Multichannel Sensor Interface Using a Single Higher GBWP Amplifier

Figure 8-17 shows the output voltage and input differential voltage when a 8V step is applied at the noninverting terminal of the OPA810-Q1 configured as a unity-gain buffer of Figure 8-16.

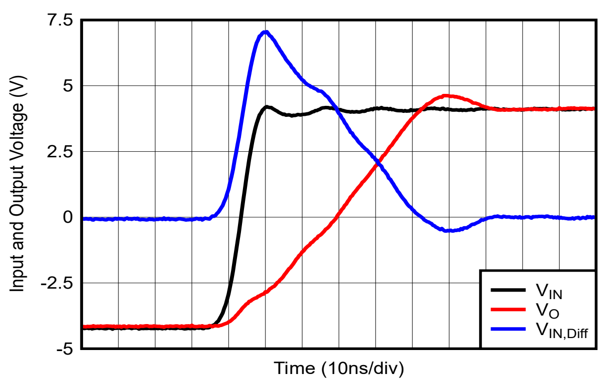


Figure 8-17. Large-Signal Transient Response Using the OPA810-Q1

Because of the fast input transient, the amplifier is slew-limited and the inputs cease to track each other (a maximum $V_{IN,Diff}$ of 7V is shown in Figure 8-17) until the output reaches the final value and the negative feedback loop is closed. For standard amplifiers with a 0.7V to 1.5V maximum $V_{IN,Diff}$ rating, current-limiting resistors must be used in series with the input pins to protect the device from irreversible damage, which also limits the device frequency response. The OPA810-Q1 has built-in input clamps that allow the application of as much as 7V of $V_{IN,Diff}$, with no external resistors required and no damage to the device or a shift in performance specifications. Such an input-stage architecture, coupled with the fast settling performance, makes the OPA810-Q1 an excellent choice for multichannel sensor multiplexed systems.

8.3 Power Supply Recommendations

The OPA810-Q1 is intended for operation on supplies ranging from 4.75V to 27V. The OPA810-Q1 can be operated on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the dc errors resulting from the –PSRR term can be minimized. Typically, ac performance improves slightly at 10V operation with minimal increase in supply current. Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.01µF decoupling capacitors. A larger capacitor (2.2µF typical) is used along with a high-frequency, 0.01µF, supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

8.4 Layout

8.4.1 Layout Guidelines

To achieve optimized performance with a high-frequency amplifier such as the OPA810-Q1requires, pay careful attention to board layout parasitics and external component types. The *DEM-OPA-SOT-1A* can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any ac ground for all signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, this capacitance can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 inch) from the power-supply pins to high-frequency, 0.01µF decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. Use larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, on the supply pins. Place these capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserve the high-frequency performance of the OPA810-Q1.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values greater than 10kΩ, this parasitic capacitance can add a pole or zero close to the GBWP of 70MHz and subsequently affects circuit operation. Keep resistor values as low as possible and consistent with load driving considerations. Lowering the resistor values keeps the resistor noise terms low, and minimizes the effect of parasitic capacitance, however lower resistor values increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network. Transimpedance applications (see also *Section 8.2.1*) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.

4. **Connections to other wideband devices** on the board can be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S for sufficient phase margin and stability. Low parasitic capacitive loads (< 10pF) do not always require an R_S because the OPA810-Q1 is nominally compensated to operate with a 10pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed with increase in signal gain (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using micro-strip or strip-line techniques (consult an ECL design handbook for micro-strip and strip-line layout techniques). A 50Ω environment is normally not necessary onboard, and a higher impedance environment improves distortion. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA810-Q1 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; set this total effective impedance to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value to obtain sufficient phase margin and stability. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, the signal attenuates because of the voltage divider formed by the series output into the terminating impedance.
5. **Take care to design the PCB layout for optimized thermal dissipation.** For the extreme case of 125°C operating ambient, using the approximate 134.8°C/W for the SOIC package, and an internal power of 24V supply × 4.7mA 125°C supply current gives a maximum internal power dissipation of 113mW. This power gives a 15°C increase from ambient to junction temperature. Load power adds to this value, and this dissipation must also be calculated to determine the worst-case safe operating point.
6. **Do not socket a high-speed device such as the OPA810-Q1.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can almost make achieving a smooth, stable frequency response impossible. Best results are obtained by soldering the OPA810-Q1 onto the board.

8.4.1.1 Thermal Considerations

The OPA810-Q1 does not require a heat sink or airflow in most applications. Maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load, is at a maximum when the output is fixed at a voltage equal to half of either supply voltage (for equal split-supplies). Under this condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$, where R_L includes feedback network loading.

The power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using a DCK (SC70 package) configured as a unity gain buffer, operating on ±12V supplies at an ambient temperature of 25°C and driving a grounded 500Ω load.

P_D = 24V × 4.7mA + 12^2 / (4 × 500Ω) = 184.8mW

Maximum T_J = 25°C + (0.185W × 190.8°C/W) = 60°C, which is much less than the maximum allowed junction temperature of 150°C.

8.4.2 Layout Example

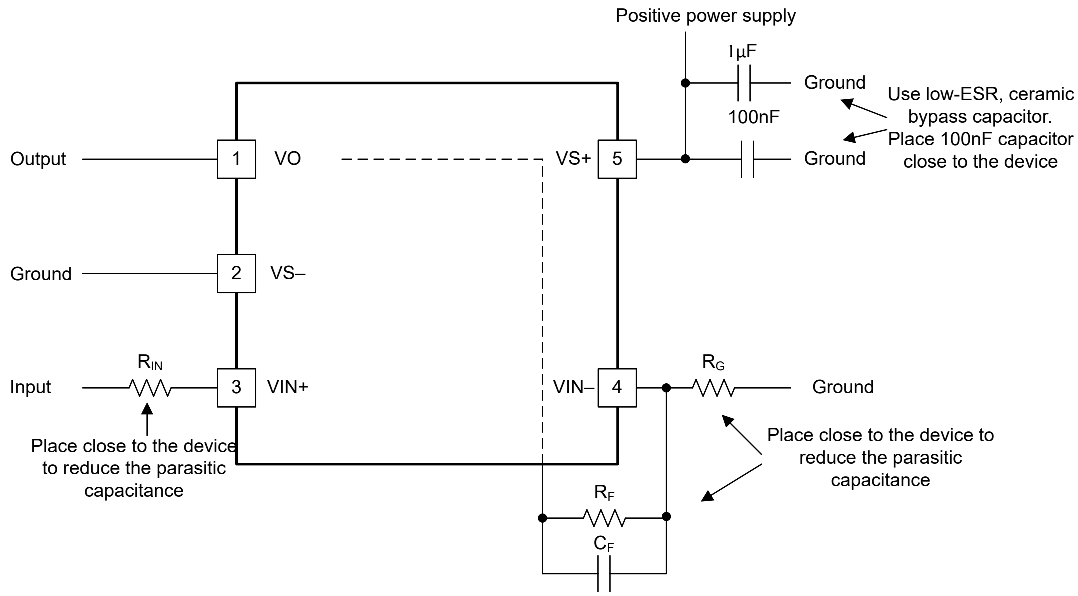


Figure 8-18. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ADS9110 18-Bit, 2MSPS, 15mW, SAR ADC With Enhanced Performance Features data sheet*
- Texas Instruments, *THS4561 Low-Power, High Supply Range, 70MHz, Fully Differential Amplifier data sheet*
- Texas Instruments, *OPAx837 Low-Power, Precision, 105MHz, Voltage-Feedback Op Amp data sheet*
- Texas Instruments, *OPAx378 Low-Noise, 900kHz, RRIO, Precision Operational Amplifier Zerø-Drift Series data sheet*
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference data sheet*
- Texas Instruments, *Single-Supply Op Amp Design Techniques application report*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 1*
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 2*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps application report*
- Texas Instruments, *TINA model and simulation tool*
- Texas Instruments, *TIDA-01057 Reference Design Maximizing Signal Dynamic Range for True 10 Vpp Differential Input to 20 bit ADC*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA810QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O810Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA810-Q1 :

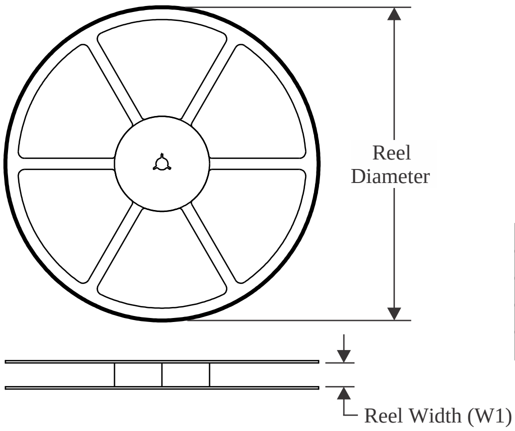
- Catalog : OPA810

NOTE: Qualified Version Definitions:

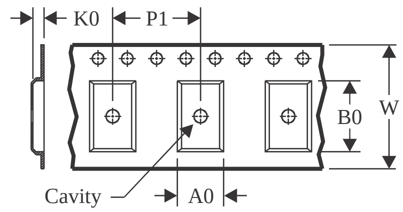
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

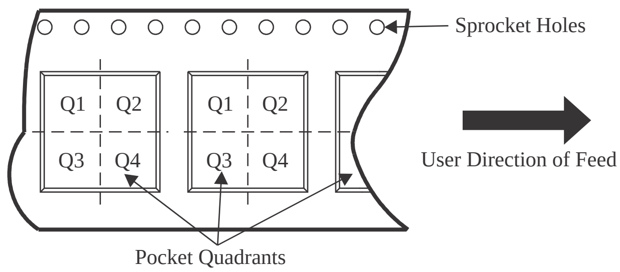


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

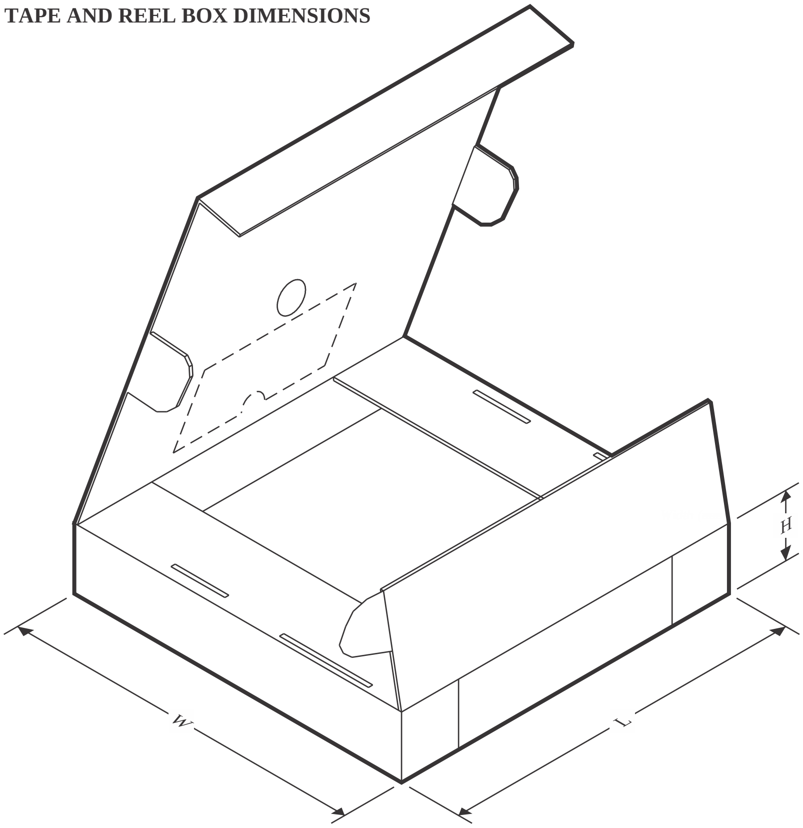
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

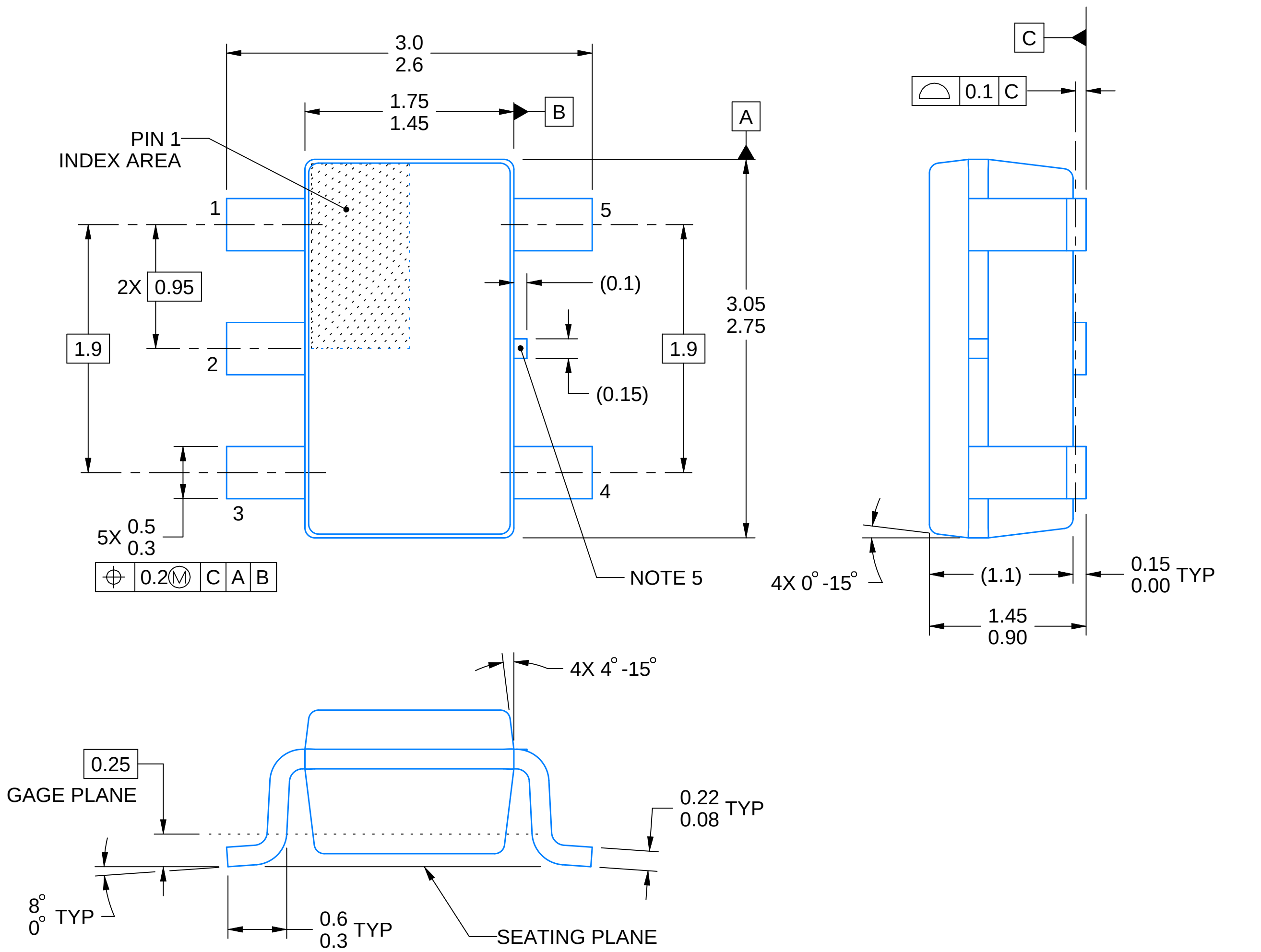
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA810QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA810QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0



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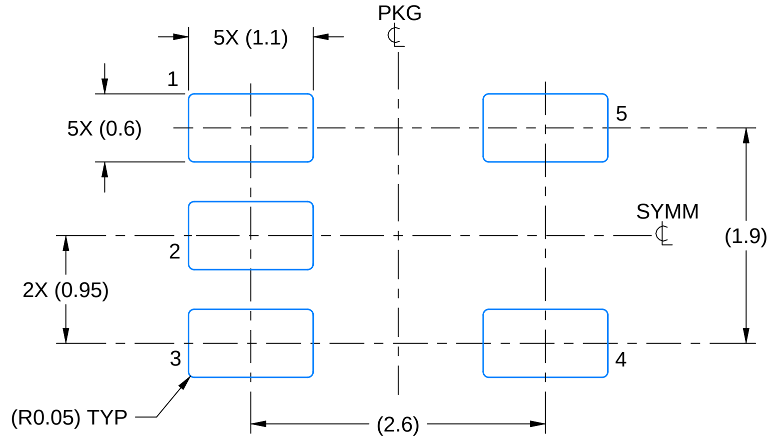
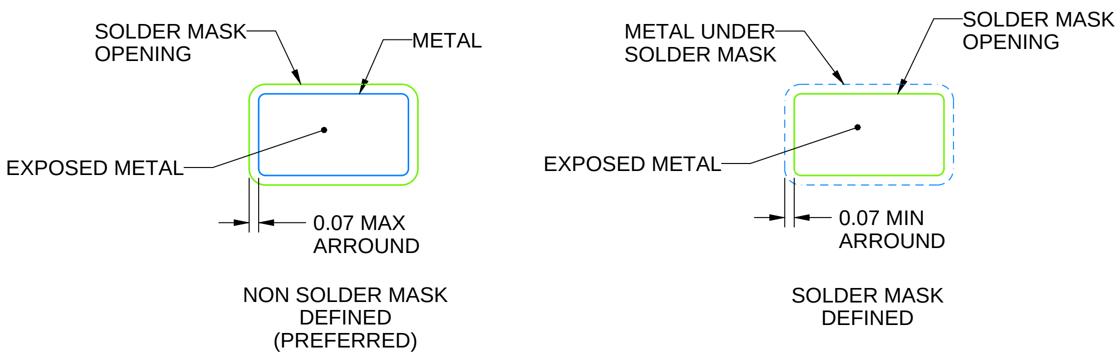
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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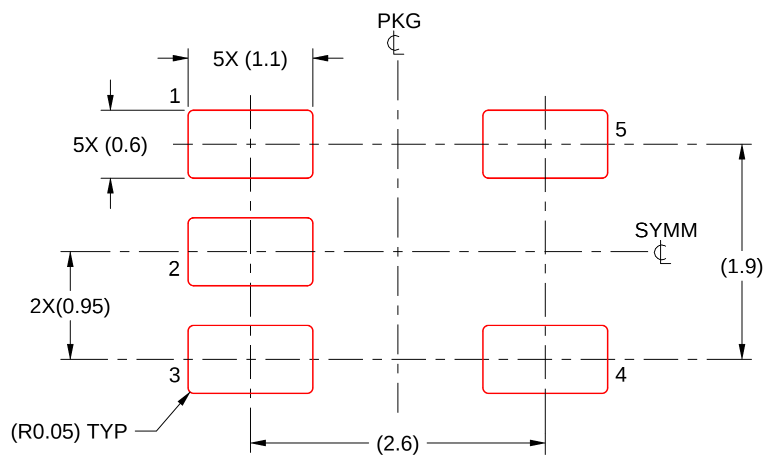
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.