GAIN +4 STABLE WIDEBAND VOLTAGE LIMITING AMPLIFIER

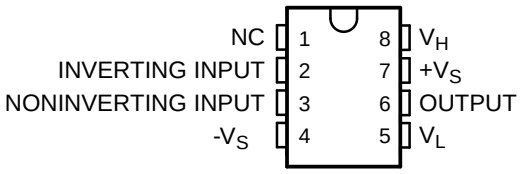
FEATURES

- **High Linearity Near Limiting**
- **Fast Recovery from Overdrive: 1 ns**
- **Limiting Voltage Accuracy: ±15 mV**
- **–3-dB Bandwidth (G = +6): 260 MHz**
- **Stable for G ≥ +4**
- **Slew Rate: 1400 V/µs**
- **±5-V and 5-V Supply Operation**
- **High Gain Version of the OPA698**
- **Low Prop Delay Comparator**
- **Non-Linear Analog Signal Processing**
- **Difference Amplifier**
- **IF Limiting Amplifier**
- **OPA689M Replacement**

APPLICATIONS

- **Transimpedance With Fast Overdrive Recovery**
- **Fast Limiting ADC Input Buffers**

JD PACKAGE
(TOP VIEW)



NC - No internal connection

P0013-01

DESCRIPTION

The OPA699 is a wideband, voltage feedback op amp that offers bipolar output voltage limiting, and is stable for gains ≥ +4. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15 mV. The op amp operates linearly to within 30 mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100 mV of the desired linear output range 1-ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain and allows the OPA699 to be used in all standard op amp applications.

Non-linear analog signal processing circuits will benefit from the ability of the OPA699 to sharply transition from linear operation to output limiting. The quick recovery time supports high speed applications.

The OPA699M is available in an industry-standard pinout in a CDIP-8 package. For lower gain applications requiring output limiting with fast recovery, consider the OPA698M.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – JD	Tube	OPA699MJD	OPA699MJD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
	Power supply	±6.5 V
V_{ICM}	Common-mode input voltage	$\pm V_S$
V_{ID}	Differential input voltage	$\pm V_S$
	Limiter voltage range	$\pm(V_S$ - 0.7 V)
T_A	Operating free-air temperature range	–55°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C
	Case temperature for 10 seconds	260°C
T_J	Junction temperature	150°C
θ_{JC}	Package thermal impedance(2) (JD Package)	14.5°C/W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is measured per MIL-STD-883, Method 1012.1.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Operating voltage	Split-rail operation		±5	±6	V
	Single-supply operation		5	12	
Operating free-air temperature		–55		125	°C

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (see Figure 47)						
Small signal bandwidth	V_O < 0.5 Vp-p, G = +6			260		MHz
	V_O < 0.5 Vp-p, G = +12			86		
	V_O < 0.5 Vp-p, G = –6			269		
Gain bandwidth product (G ≥ +20)	V_O < 0.5 Vp-p			1000		MHz
Gain peaking	V_O = 0.5 V, G = +4			7.5		dB
Bandwidth for 0.1-dB gain flatness	V_O = 0.5 V			30		MHz
Large signal bandwidth	V_O = 2 Vp-p			290		MHz
Slew rate	V_O = 2 V step			1400		V/µs
Rise and falll time	V_O = 0.5 V step			1.6		ns
Settling time to 0.05%	V_O = 2 V step			8		ns
Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz	Even		67		dB
		Odd		87		
Differential gain	R_L = 500 Ω, NTSC, PAL			0.012%		
Differential phase	R_L = 500 Ω, NTSC, PAL			0.008		°
Input noise, voltage noise density	f ≥ 1 MHz			4.1		nV/√Hz
Input noise, current noise density	f ≥ 1 MHz			2		pA/√Hz
DC PERFORMANCE						
Open-loop voltage gain (AVOL)	V_O = ±0.5 V	T_A = 25°C	54	62		dB
		T_A = Full range	47			
Input offset voltage (V_{IO})		T_A = 25°C		±1.5	±8	mV
		T_A = Full range			±12	
Input bias current (I_{IB})(2)		T_A = 25°C		3	±10	µA
		T_A = Full range			±18	
Input offset current (I_{IO})		T_A = 25°C		±0.3	±3	µA
		T_A = Full range			±4	
INPUT						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	54	62		dB
		T_A = Full range	50			
Common-mode input voltage range (V_{ICR})(3)		T_A = 25°C	±3.2	±3.3		V
		T_A = Full range	±3.1			
Input impedance, differential mode				0.32 1		MΩ pF
Input impedance, common mode				3.5 1		MΩ pF
OUTPUT						
Output voltage range (V_{OH}, V_{OL})	V_H = 4.3 V, V_L = -4.3 V, R_L≥ 500 Ω	T_A = 25°C	±3.9	±4.1		V
		T_A = Full range	±3.7			
Current output, sourcing (I_{OH})	V_H = 4.3 V, V_L = -4.3 V, R_L = 20 Ω	T_A = 25°C	110	165		mA
		T_A = Full range	100			
Current output, sinking (I_{OL})	V_H = 4.3 V, V_L = -4.3 V, R_L = 20 Ω	T_A = 25°C	–90	–130		mA
		T_A = Full range	–80			
Closed-loop output impedance	G = +4, f < 100 kHz			0.8		Ω

(1) All typical limits are at T_A = 25°C unless otherwise specified.
(2) Current is considered positive out of node.
(3) CMIR tested as <3-dB degradation from minimum CMRR at specified limits.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY						
Operating voltage (V_S)				±5	±6	V
Quiescent current (I_S)		T_A = 25°C	15	15.5	16	mA
		T_A = Full range	13.5		18	
ower supply rejection ratio (PSRR)	Input referred, V_S = ±4.5 V to ±5.5 V	T_A = 25°C	65	76		dB
		T_A = Full range	60			
OUTPUT VOLTAGE LIMITERS (PINS 5 AND 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	±3.3	±3.6		V
		T_A = Full range	±3			
Limiter output offset voltage	(V_O– V_H) or (V_O– V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude(4)	V_O = 0 V	T_A = 25°C	40	55	65	µA
		T_A = Full range	35		70	
Limiter input impedance				3.4 1		MΩ pF
Limiter feedthrough(5)	f = 5 MHz			–60		dB
Maximum limiter voltage					±4.3	V
Minimum limiter voltage separation			400			mV
Op amp bias current shift(2)				3		µA
Limiter small signal bandwidth	V_I = ±2 V, V_O < 0.02 Vp-p			600		MHz
Limter slew rate(6)				125		V/µs
Limiter step response, overshoot	V_I = ±2 V			250		mV
Limiter step response, recovery time	V_I = ±2 V			1		ns
Linearity guardband(7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(4) I_{VH} (V_H bias current) is positive and I_{VL} (V_L bias current) is negative, under these conditions. See Note 2, Figure 47, and Figure 58.
(5) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when VIN = 0.
(6) V_H slew rate conditions are: V_{IN} = +0.7 V, G = +6, V_L = -2 V, V_H = step between 2 V and 0 V. VL slew rate conditions are similar.
(7) Linearity Guardband is defined for an output sinusoid (f = 1 MHz, V_O = 2 Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 59).

ELECTRICAL CHARACTERISTICS

V_S = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (see Figure 48)						
Small signal bandwidth	V_O < 0.5 Vp-p, G = +6			234		MHz
	V_O < 0.5 Vp-p, G = +12			83		
	V_O < 0.5 Vp-p, G = –6			242		
Gain bandwidth product	V_O < 0.5 Vp-p, G ≥ +20			880		MHz
Gain peaking	V_O < 0.5 V, G = +4			8		dB
Bandwidth for 0.1-dB gain flatness	V_O = 0.5 Vp-p			30		MHz
Large signal bandwidth	V_O = 2 Vp-p			250		MHz
Slew rate	V_O = 2 V step			1050		V/µs
Rise and falll time	V_O = 0.5 V step			1.75		ns
Settling time to 0.05%	2 V step			8		ns
Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz	Even		64		dB
		Odd		70		
Input noise, voltage noise density	f ≥ 1 MHz			4.2		nV/√Hz
Input noise, current noise density	f ≥ 1 MHz			2.1		pA/√Hz
DC PERFORMANCE						
Open-loop voltage gain (AVOL)	V_O = ±0.4 V	T_A = 25°C	54	61		dB
		T_A = Full range	47			
Input offset voltage (V_{IO})		T_A = 25°C		±2	±8	mV
		T_A = Full range			±12	
Input bias current (I_{IB})(2)		T_A = 25°C		±3	±10	µA
		T_A = Full range			±15	
Input offset current (I_{IO})		T_A = 25°C		±0.4	±3	µA
		T_A = Full range			±4	
INPUT						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	52	60		dB
		T_A = Full range	48			
Common-mode input voltage range (V_{ICR})(3)		T_A = 25°C	V_{ICM} ±0.7V	V_{ICM} ±0.8V		V
		T_A = Full range	V_{ICM} ±0.6V			
Input impedance, differential mode				0.32 1		MΩ pF
Input impedance, common mode				1 1		MΩ pF
OUTPUT						
Output voltage range (V_{OH}, V_{OL})	V_H = V_{ICM} + 1.8 V, V_L = V_{ICM} – 1.8 V, R_L ≥ 500 Ω	T_A = 25°C	V_{ICM} ±1.4V	V_{ICM} ±1.6V		V
		T_A = Full range	V_{ICM} ±1.3V			
Current output, sourcing (I_{OH})	V_S = ±2.5 V, R_L = 20 Ω	T_A = 25°C	70	100		mA
		T_A = Full range	60			
Current output, sinking (I_{OL})	V_S = ±2.5 V, R_L = 20 Ω	T_A = 25°C	–60	–90		mA
		T_A = Full range	–50			
Closed-loop output impedance	G = +4, f < 100 kHz			0.2		Ω

(1) All typical limits are at T_A = 25°C unless otherwise specified.
(2) Current is considered positive out of node.
(3) CMIR tested as <3-dB degradation from minimum CMRR at specified limits.

ELECTRICAL CHARACTERISTICS (continued)

V_S = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY						
Operating voltage (V_S)				5	12	V
Quiescent current (I_S)		T_A = 25°C	13.5	14.3	15	mA
		T_A = Full range	12		16.5	
Power supply rejection ratio (PSRR)	Input referred, V_S = 4 V to 6 V	T_A = Full range	58	74		dB
OUTPUT VOLTAGE LIMITERS (PINS 5 AND 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	V_{ICM} ±0.8V	V_{ICM} ±1.1V		V
		T_A = Full range	V_{ICM} ±0.6V			
Limiter output offset voltage	(V_O – V_H) or (V_O – V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude(4)	V_O = 2.5 V	T_A = 25°C	40	50	65	µA
		T_A = Full range	35		70	
Limiter input bias current drift				30		nA/°C
Limiter input impedance				3.4 1		MΩ pF
Limiter feedthrough(5)	f = 5 MHz			–60		dB
Maximum limiter voltage					V_{ICM} ±1.8V	V
Minimum limiter voltage separation			400			mV
Output bias current shift(2)				5		µA
Limiter small signal bandwidth	V_I = V_{ICM} ±0.4 V, V_O < 0.02 Vp-p			450		MHz
Limter slew rate(6)				100		V/µs
Limiter step response, overshoot	V_I = V_{ICM} ±0.4 V			55		mV
Limiter step response, recovery time	V_I = V_{ICM} ±0.4 V			3		ns
Linearity guardband(7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

(4) I_{VH} (V_H bias current) is positive and I_{VL} (V_L bias current) is negative, under these conditions. See Note 2, Figure 47, and Figure 58.
(5) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
(6) V_H slew rate conditions are: V_{IN} = 0.7 V, G = +6, V_L = -2 V, V_H = stepped between 2 V and 0 V. V_L slew rate conditions are similar.
(7) Linearity Guardband is defined for an output sinusoid (f = 1 MHz, V_O = 2 Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3 dB (see Figure 59).

TYPICAL CHARACTERISTICS: V_S = ±5 V

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

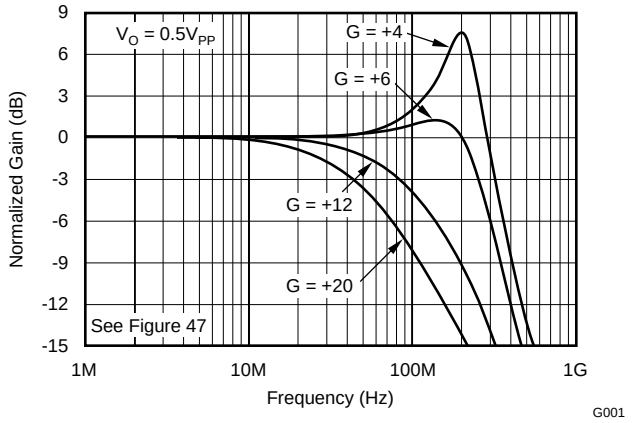


Figure 1.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

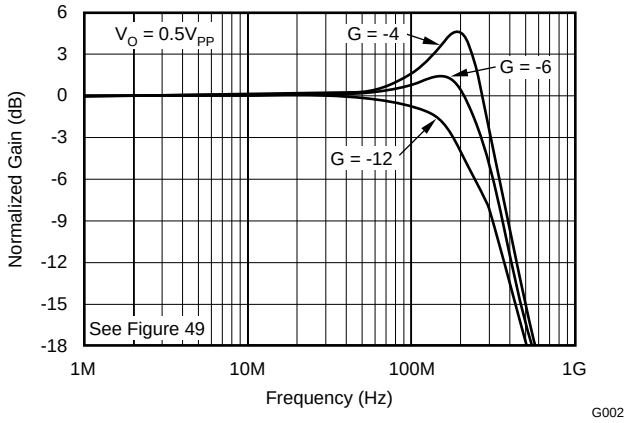


Figure 2.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

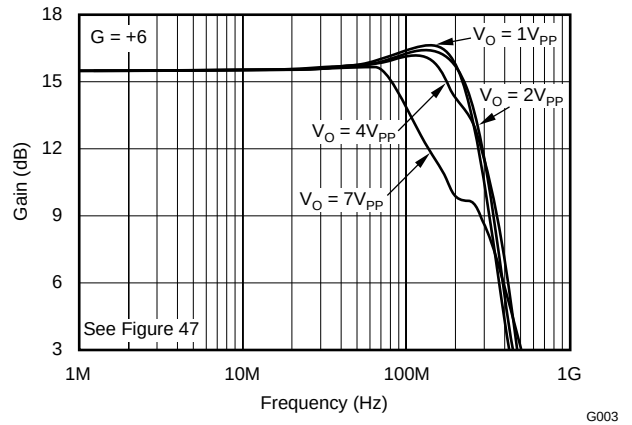


Figure 3.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

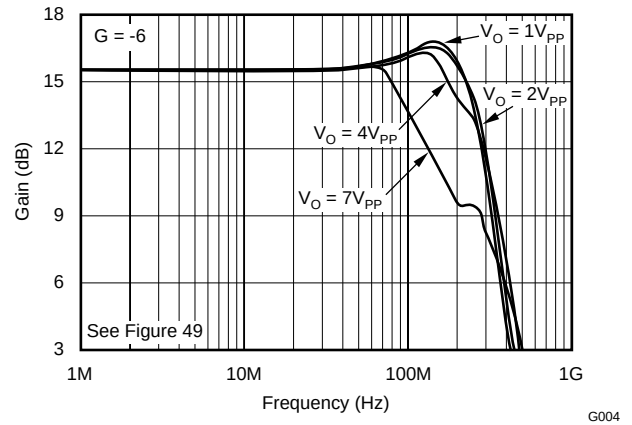


Figure 4.

V_H–LIMITER SMALL-SIGNAL FREQUENCY RESPONSE

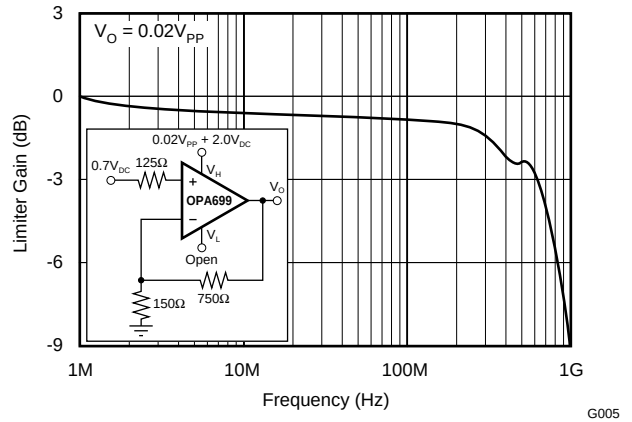


Figure 5.

V_L–LIMITER SMALL-SIGNAL FREQUENCY RESPONSE

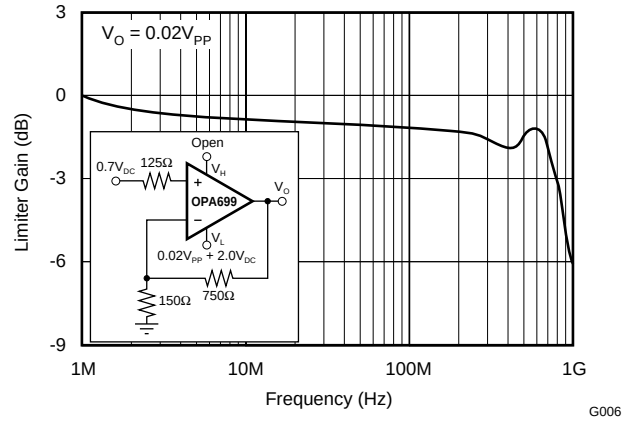
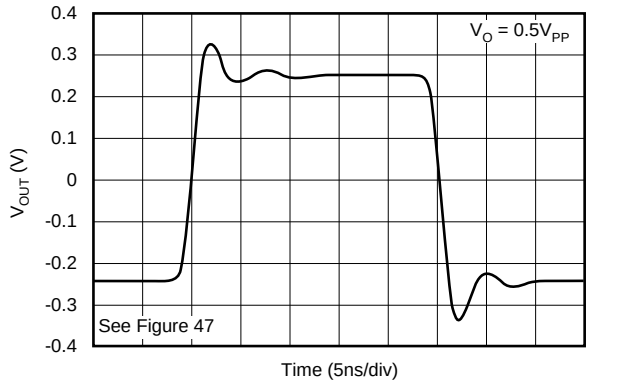


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

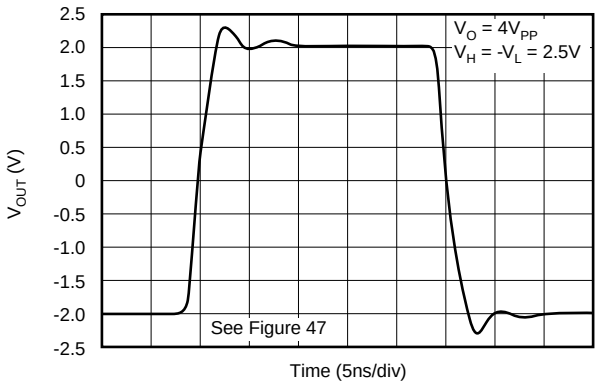
SMALL-SIGNAL PULSE RESPONSE



G007

Figure 7.

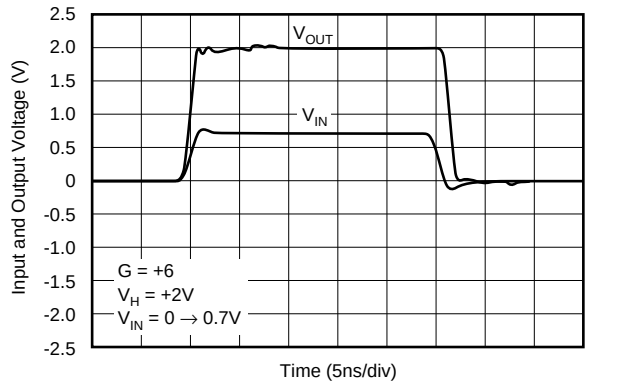
LARGE-SIGNAL PULSE RESPONSE



G008

Figure 8.

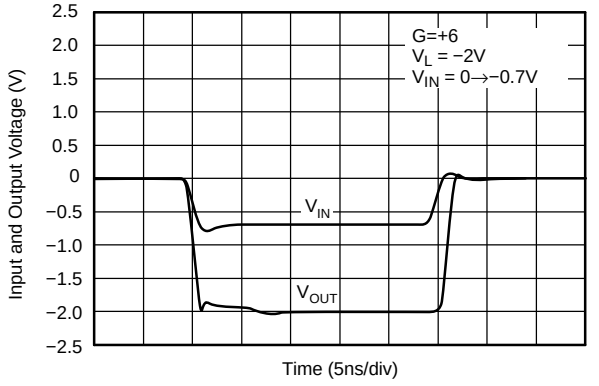
V_H–LIMITED PULSE RESPONSE



G009

Figure 9.

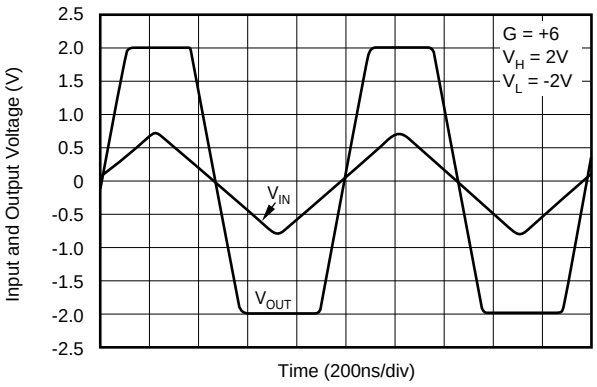
V_L–LIMITED PULSE RESPONSE



G010

Figure 10.

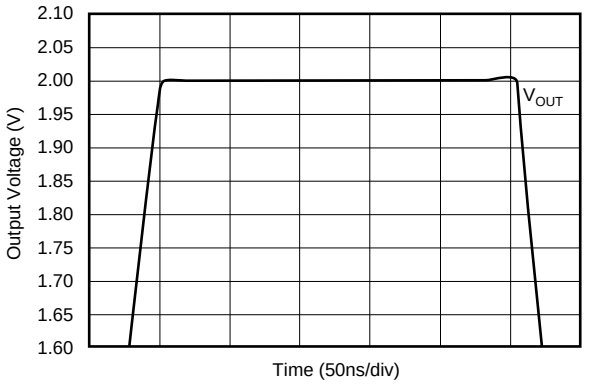
LIMITED OUTPUT RESPONSES



G011

Figure 11.

DETAIL OF LIMITED OUTPUT RESPONSE



G012

Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

HARMONIC DISTORTION vs LOAD RESISTANCE

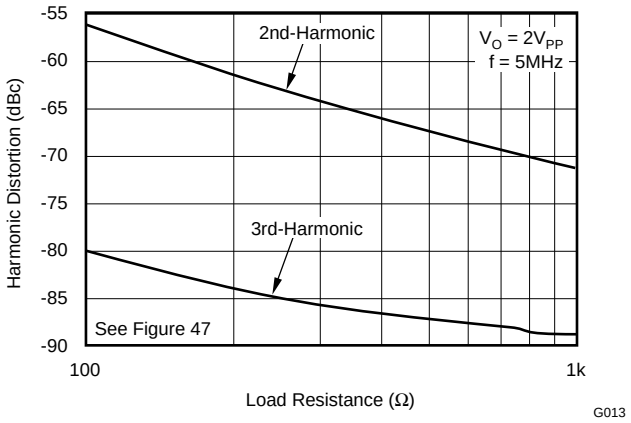


Figure 13.

5 MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

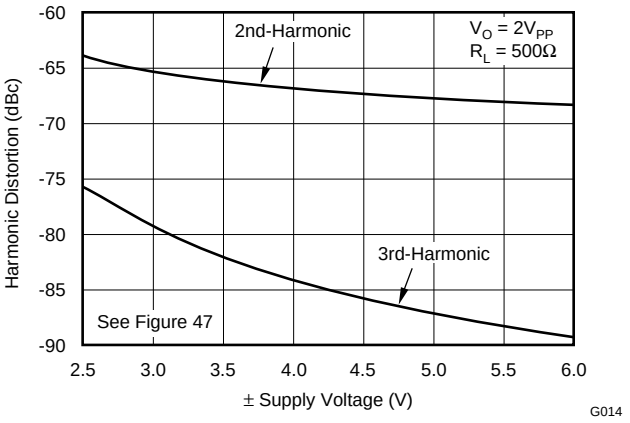


Figure 14.

HARMONIC DISTORTION vs FREQUENCY

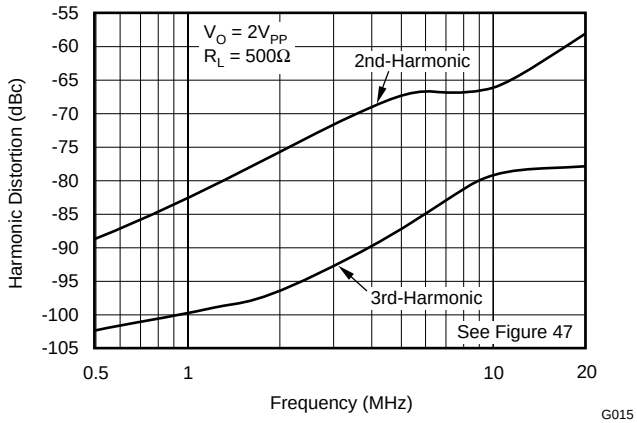


Figure 15.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

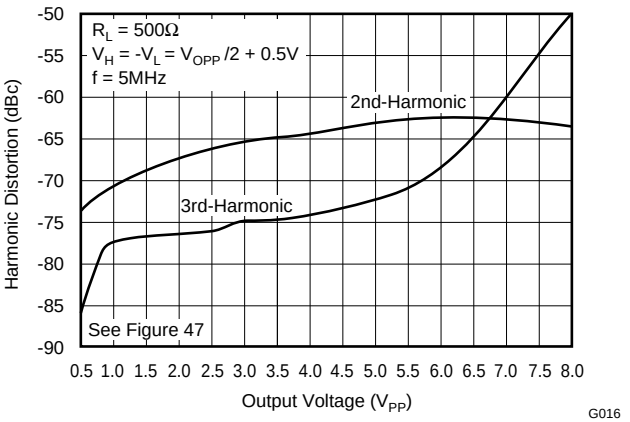


Figure 16.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

HARMONIC DISTORTION VS NONINVERTING GAIN

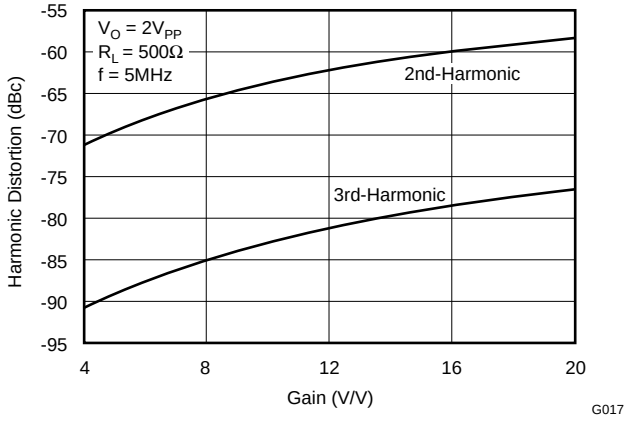


Figure 17.

HARMONIC DISTORTION VS INVERTING GAIN

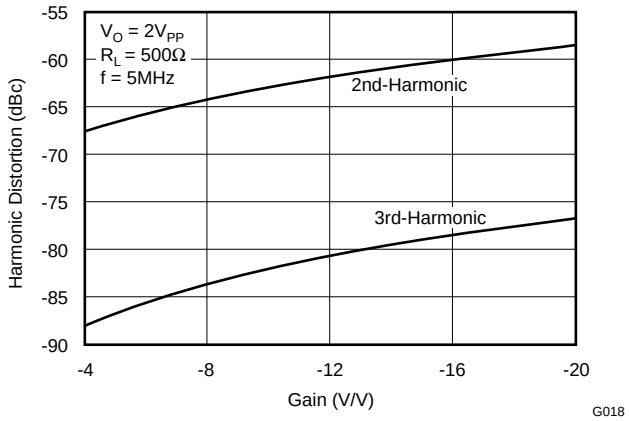


Figure 18.

HARMONIC DISTORTION NEAR LIMITING VOLTAGES

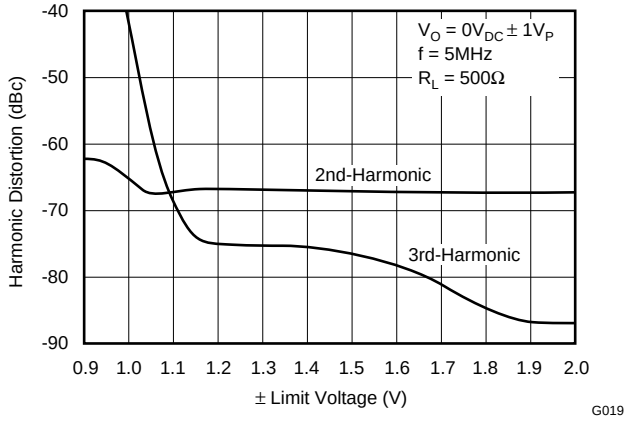


Figure 19.

2-TONE, 3rd-ORDER INTERMODULATION INTERCEPT

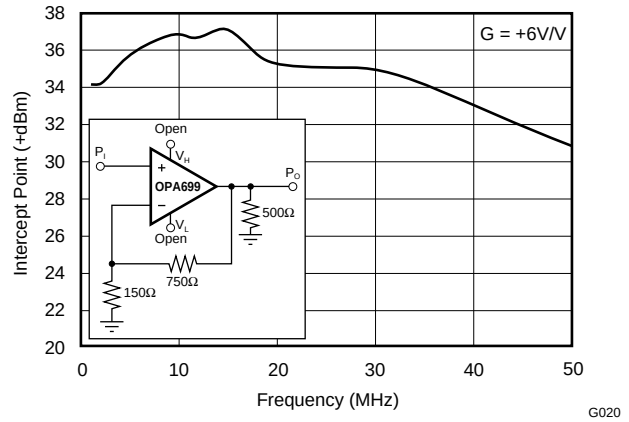


Figure 20.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

RECOMMENDED R8 VS CAPACITIVE LOAD

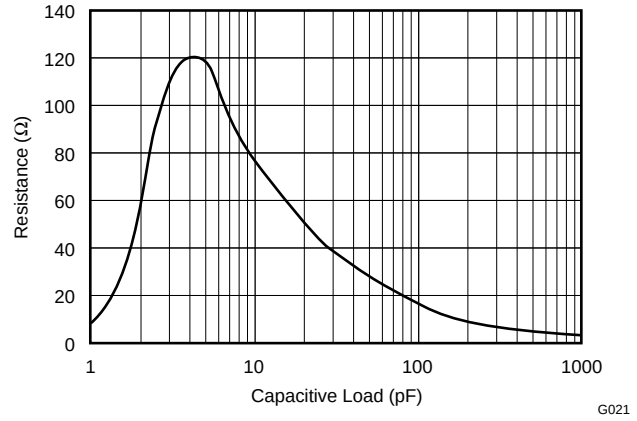


Figure 21.

FREQUENCY RESPONSE VS CAPACITIVE LOAD

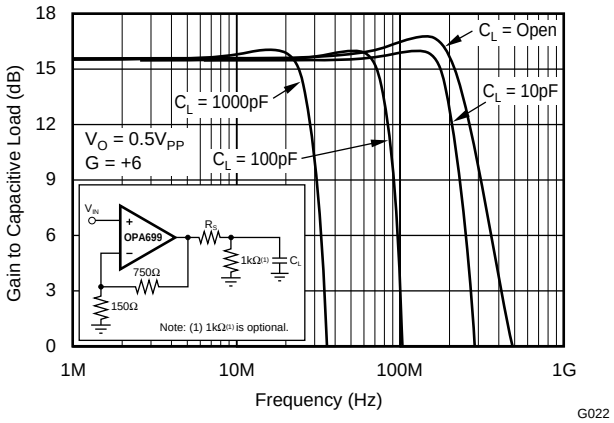


Figure 22.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

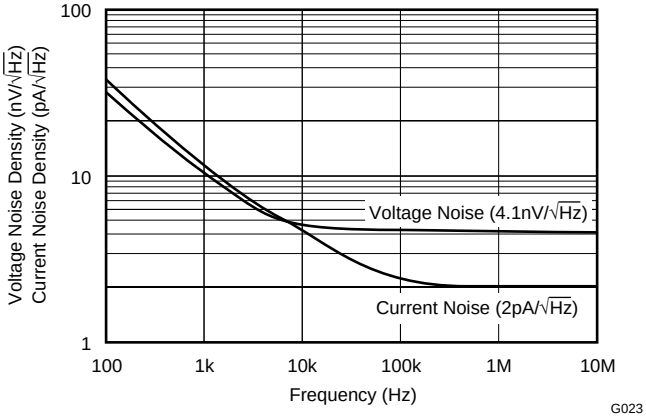


Figure 23.

OPEN-LOOP GAIN AND PHASE

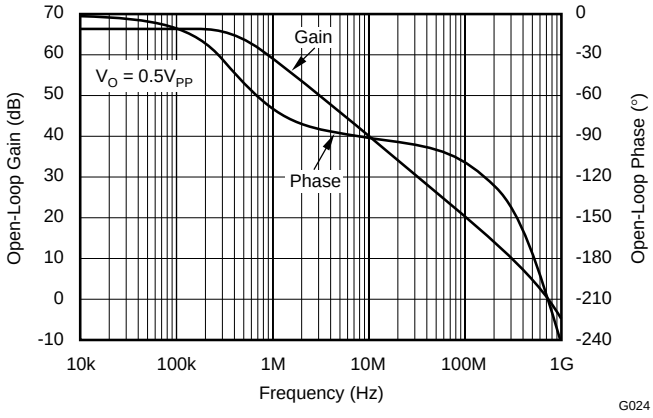


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

VOLTAGE RANGES vs TEMPERATURE

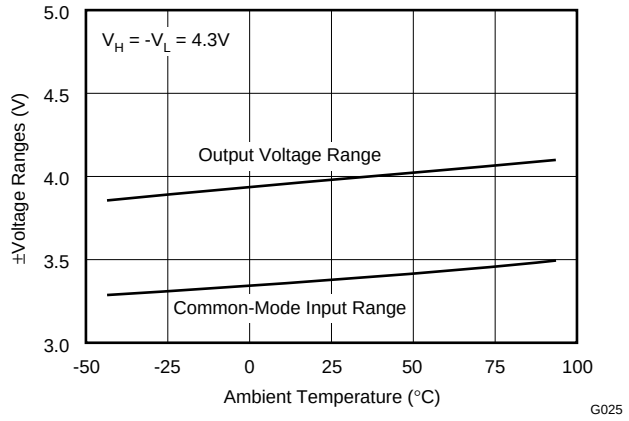


Figure 25.

LIMITED VOLTAGE RANGE vs TEMPERATURE

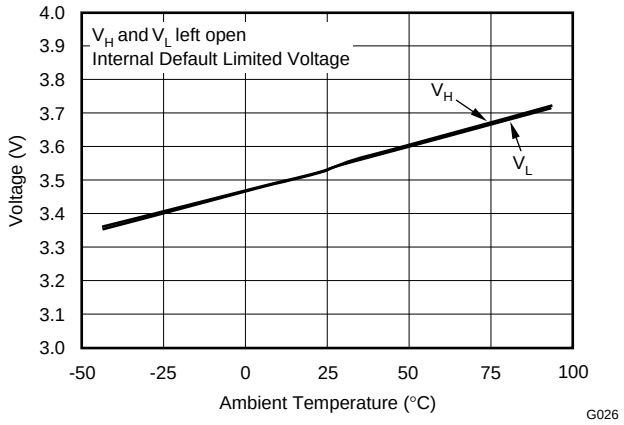


Figure 26.

LIMITED INPUT BIAS CURRENT vs BIAS VOLTAGE

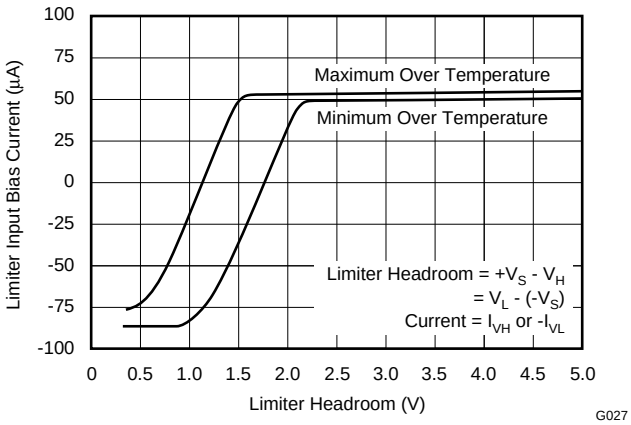


Figure 27.

SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE

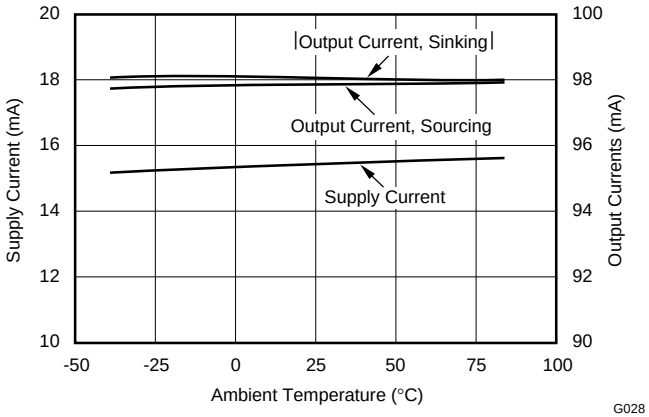


Figure 28.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

CMRR AND POWER-SUPPLY REJECTION VS FREQUENCY

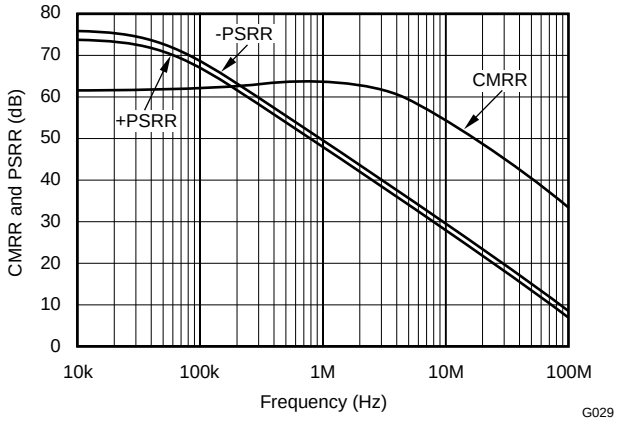


Figure 29.

TYPICAL DRIFT OVER TEMPERATURE

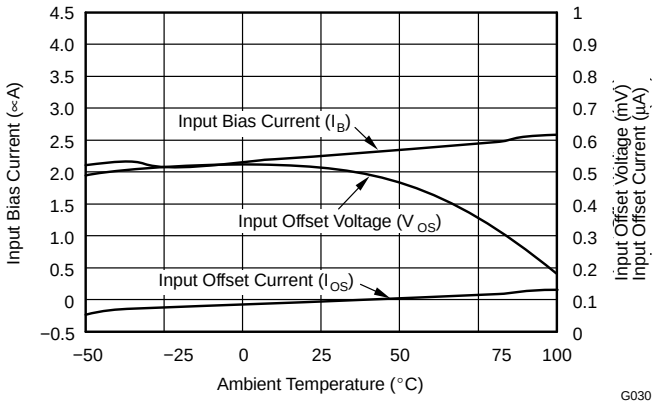


Figure 30.

LIMITER FEEDTHROUGH

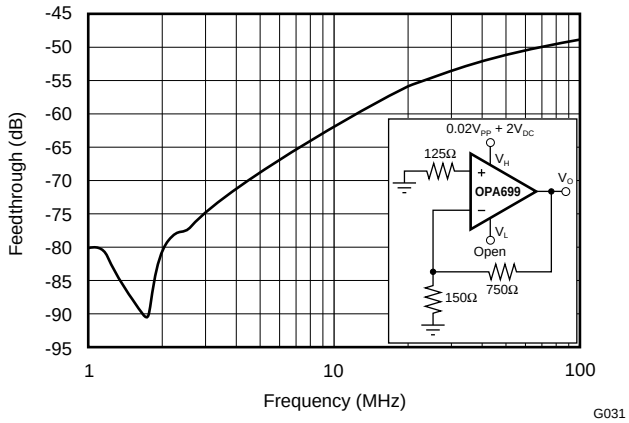


Figure 31.

CLOSSED-LOOP OUTPUT IMPEDANCE

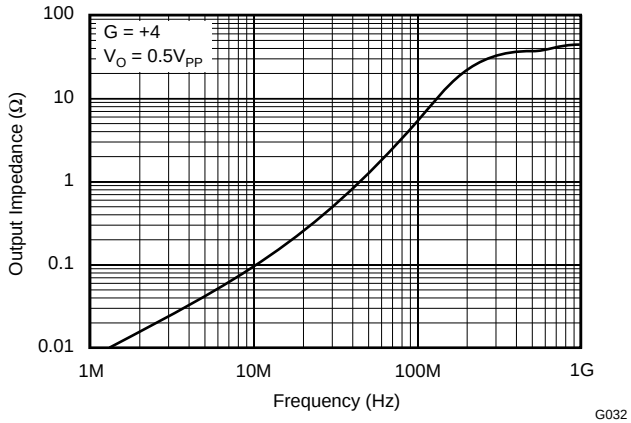


Figure 32.

TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω, V_H = –V_L = 2 V, unless otherwise noted

CMRR AND PSRR(±) vs TEMPERATURE

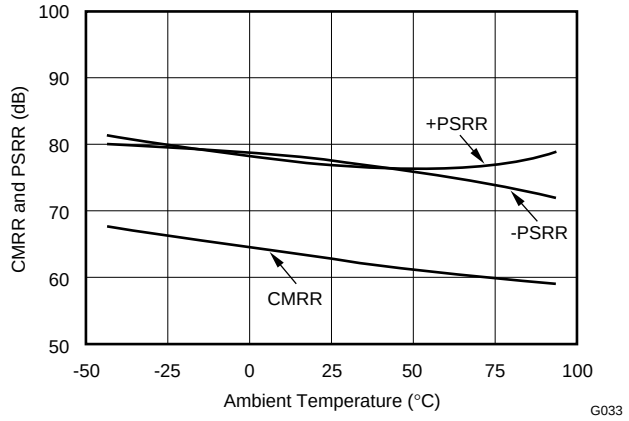


Figure 33.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

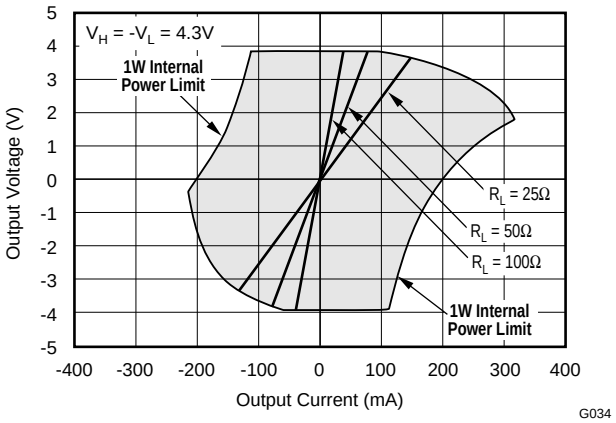


Figure 34.

TYPICAL CHARACTERISTICS V_S = +5 V

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω to V_{CM} = +2.5 V, V_L = V_{CM}– 1.2 V, V_H = V_{CM} + 1.2 V, unless otherwise noted

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

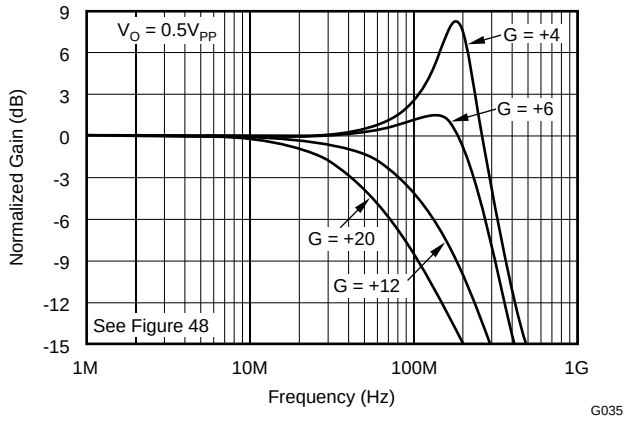


Figure 35.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

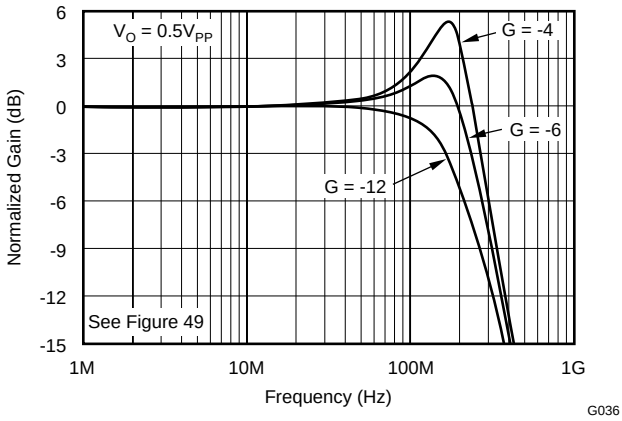


Figure 36.

TYPICAL CHARACTERISTICS V_S = +5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω to V_{CM} = +2.5 V, V_L = V_{CM} – 1.2 V, V_H = V_{CM} + 1.2 V, unless otherwise noted

LARGE-SIGNAL FREQUENCY RESPONSE

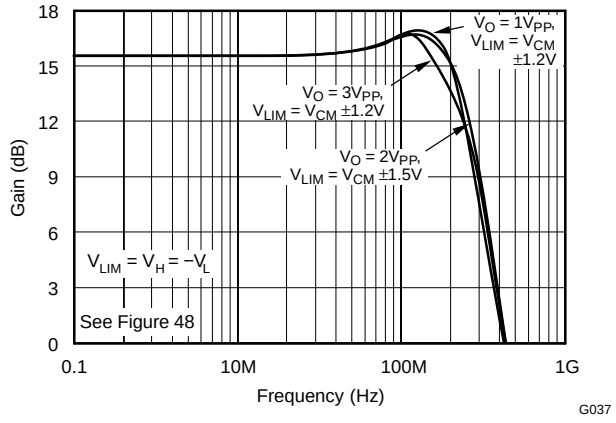


Figure 37.

SMALL-SIGNAL PULSE RESPONSE

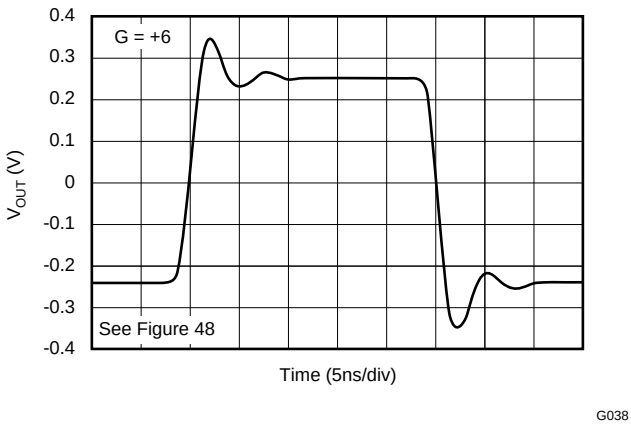


Figure 38.

LARGE-SIGNAL PULSE RESPONSE

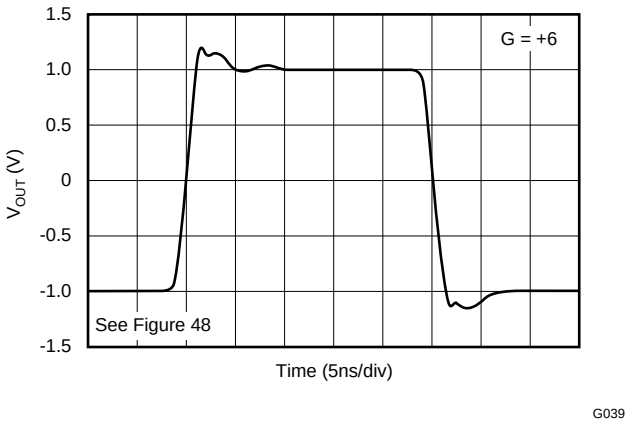


Figure 39.

V_H AND V_L – LIMITED PULSE RESPONSE

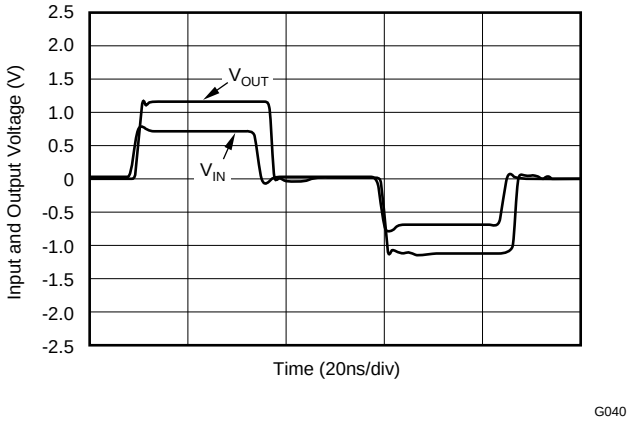


Figure 40.

HARMONIC DISTORTION vs LOAD RESISTANCE

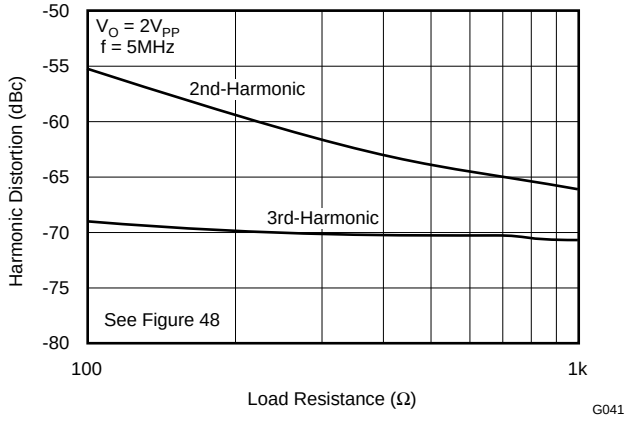


Figure 41.

HARMONIC DISTORTION vs FREQUENCY

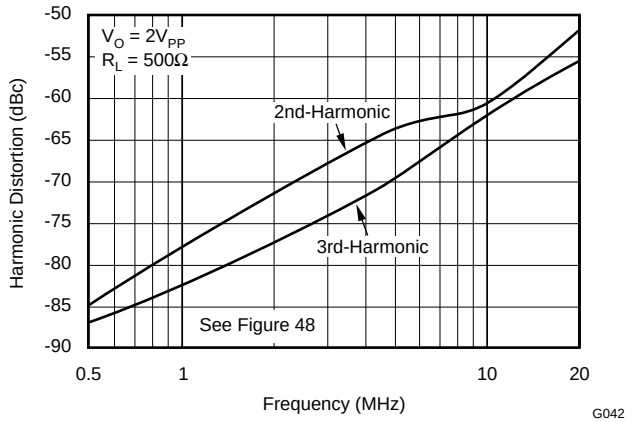


Figure 42.

TYPICAL CHARACTERISTICS V_S = +5 V (continued)

T_A = 25°C, G = +6, R_F = 750 Ω, and R_L = 500 Ω to V_{CM} = +2.5 V, V_L = V_{CM} – 1.2 V, V_H = V_{CM} + 1.2 V, unless otherwise noted

HARMONIC DISTORTION vs OUTPUT VOLTAGE

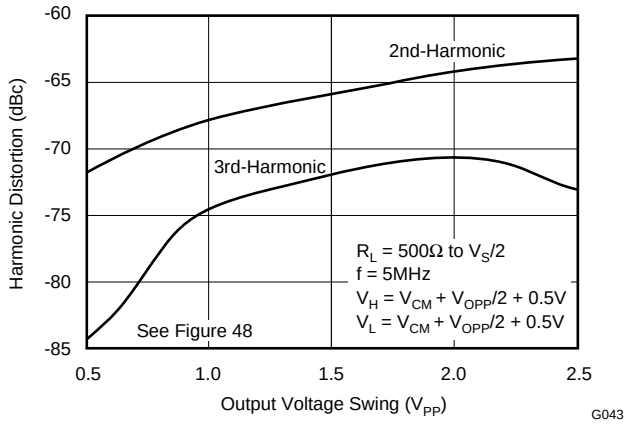


Figure 43.

2-TONE, 3rd-ORDER INTERMODULATION INTERCEPT

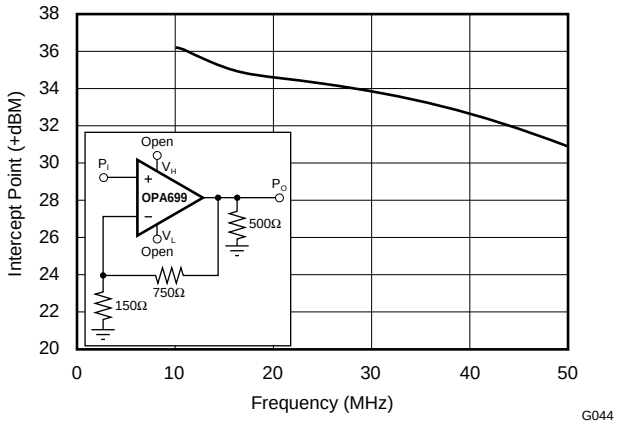


Figure 44.

HARMONIC DISTORTION NEAR LIMITING VOLTAGES

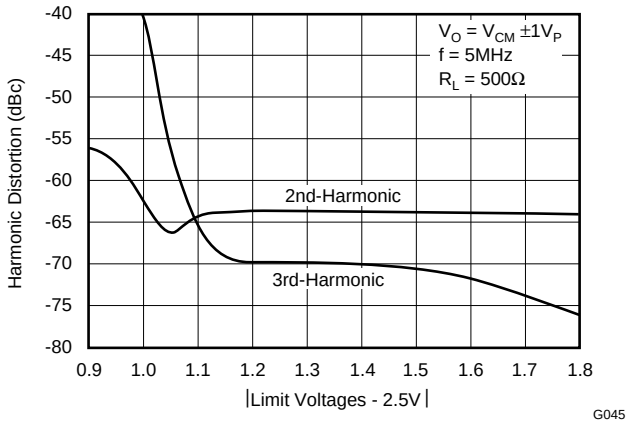


Figure 45.

LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE

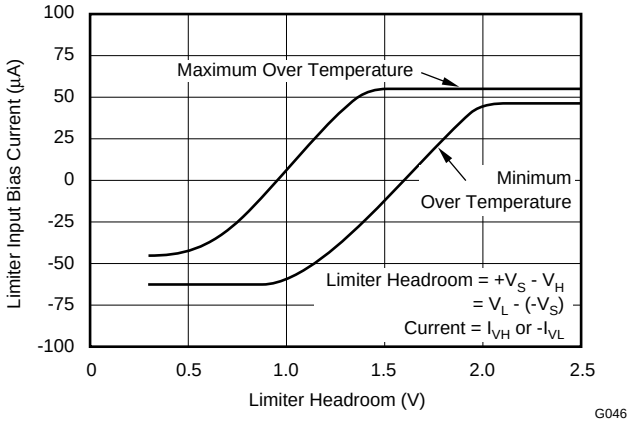


Figure 46.

APPLICATION INFORMATION

DUAL-SUPPLY, NON-INVERTING AMPLIFIER

The OPA699 is a +4 V/V minimum gain voltage-feedback amplifier that combines features of a wideband, high slew rate amplifier with output voltage limiters. Its output can swing up to 1 V from each rail and can deliver up to 120 mA. These capabilities make it an ideal interface to drive an ADC while adding overdrive protection for the ADC inputs.

Figure 47 shows the ac-coupled, gain of +6 V/V, dual power-supply circuit configuration used as the basis of the ±5-V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50 Ω with a resistor to ground and the output is set to 500 Ω. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 47, the total output load will be 500 Ω || 900 Ω = 321 Ω. The voltage limiting pins are set to ±2 V through a voltage divider network between $+V_S$ and ground for V_H and between $–V_S$ and ground for V_L. These limiter voltages are adequately bypassed with a 0.1-µF ceramic capacitor to ground. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. One additional component is included in Figure 47. An additional resistor (100 Ω) is included in series with the noninverting input. Combined with the 25-Ω dc source resistance looking back towards the signal generator, this gives an input bias current-canceling resistance that matches the 125-Ω source resistance seen at the inverting input (see the dc accuracy and offset control section). The power-supply bypass for each supply consists of two capacitors: one electrolytic 2.2 µF and one ceramic 0.1 µF. The power-supply bypass capacitors are shown explicitly in Figure 47 and Figure 48, but will be assumed in the other figures. An additional 0.01-µF power-supply decoupling capacitor (not shown here) can be included between the two power-supply pins. In practical PC board layouts, this optional, added capacitor typically improves the 2nd harmonic distortion performance by 3 dB to 6 dB.

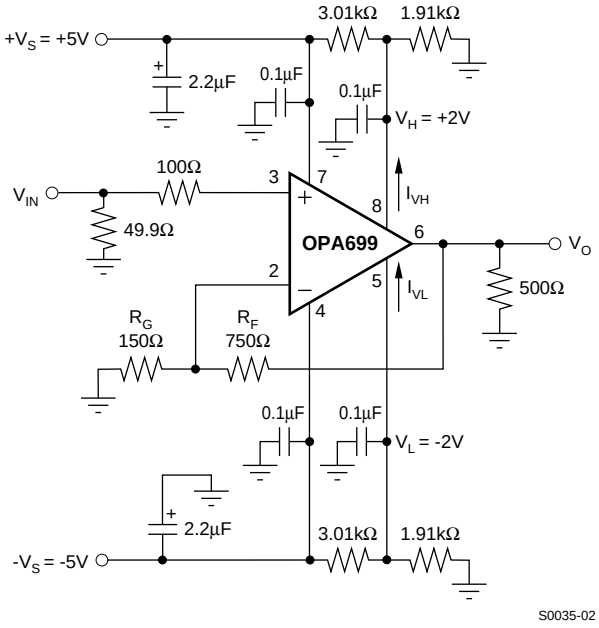


Figure 47. DC-Coupled, Dual Supply Amplifier

SINGLE-SUPPLY, NON-INVERTING AMPLIFIER

Figure 48 shows an ac-coupled, noninverting gain amplifier for single +5-V supply operation. This circuit was used for ac characterization of the OPA699, with a 50-Ω source (which it matches) and a 500-Ω load. The mid-point reference on the noninverting input is set by two 1.5-kΩ resistors. This gives an input bias current-canceling resistance that matches the 750-Ω dc source resistance seen at the inverting input (see the dc accuracy and offset control section). The power-supply bypass for the supply consists of two capacitors: one electrolytic 2.2 µF and one ceramic 0.1 µF. The power-supply bypass capacitors are shown explicitly in Figure 47

APPLICATION INFORMATION (continued)

and Figure 48, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. These limiter voltages are adequately bypassed with a 0.1-µF ceramic capacitor to ground. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground. While this circuit shows +5-V operation, the same circuit may be used for single supplies up to +12 V.

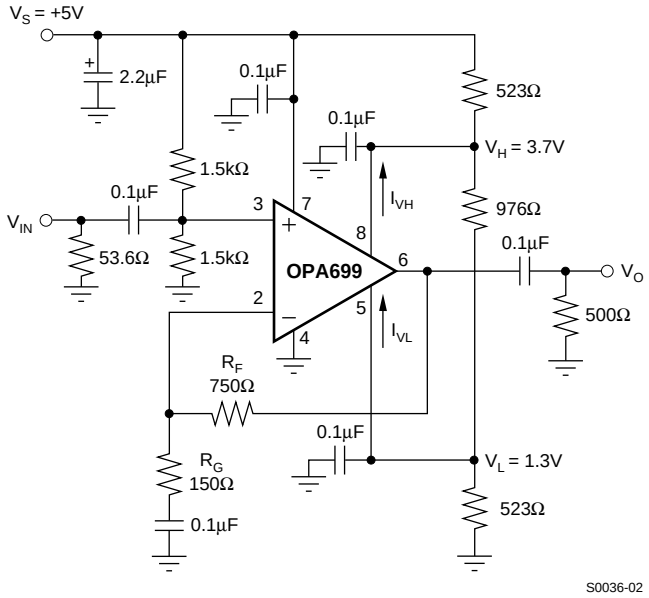


Figure 48. AC-Coupled, Single Supply Amplifier

WIDEBAND INVERTING OPERATION

Operating the OPA699 as an inverting amplifier has several benefits and is particularly useful when a matched 50-Ω source and input impedance are required. Figure 49 shows the inverting gain of –4 V/V circuit used as the basis of the inverting mode typical characteristics.

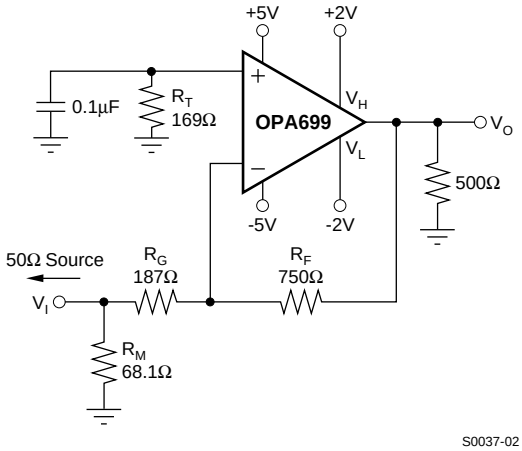


Figure 49. Inverting G = –4 Specifications and Test Circuit

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. For a 500-Ω load used in the typical characteristics, this gives a total load of 329 Ω in this inverting

APPLICATION INFORMATION (continued)

configuration. The gain resistor is set to get the desired gain (in this case, 187 Ω for a gain of –4) while an additional input resistor (R_M) can be used to set the total input impedance equal to the source, if desired. In this case, R_M = 68.1 Ω in parallel with the 187-Ω gain setting resistor gives a matched input impedance of 50 Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 49.

For bias current-cancellation matching, the noninverting input requires a 169-Ω resistor to ground. The calculation for this resistor includes a dc-coupled 50-Ω source impedance along with R_G and R_M. Although this resistor provides cancellation for the bias current, it must be well-decoupled (0.1 µF in Figure 49) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50 Ω at higher gains, the bandwidth for the circuit in Figure 49 far exceeds the bandwidth at that same gain magnitude for the noninverting circuit of Figure 47. This occurs due to the lower noise gain for the circuit of Figure 49 when the 50-Ω source impedance is included in the analysis. For instance, at a signal gain of –15 (R_G = 50 Ω, R_M = open, R_F = 750 Ω) the noise gain for the circuit of Figure 49 will be 1 + 750 Ω/(50 Ω + 50 Ω) = 8.5 due to the addition of the 50-Ω source in the noise gain equation. This approach gives considerably higher bandwidth than the noninverting gain of +15. Using the 1-GHz gain bandwidth product for the OPA699, an inverting gain of –15 from a 50-Ω source to a 50-Ω RG gives 140-MHz bandwidth, whereas the noninverting gain of +6 gives 55 MHz, as shown in the measured results of Figure 50.

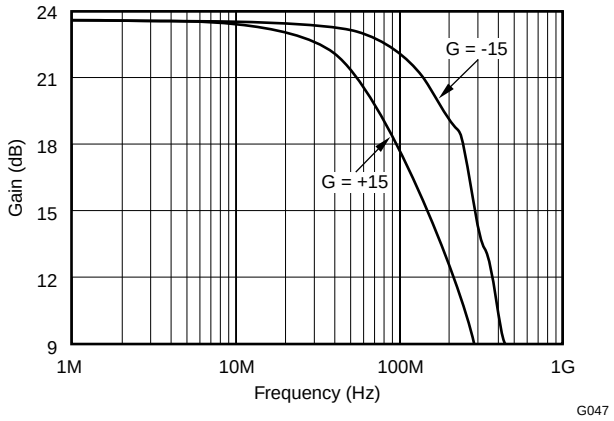


Figure 50. G = +15 and -15 Frequency Response

LOW-GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired and inverting operation is acceptable, a new external compensation technique can be used to retain the full slew rate and noise benefits of the OPA699, while giving increased loop gain and the associated distortion improvements offered by a non-unity-gain stable op amp. This technique shapes the loop gain for good stability, while giving an easily controlled 2nd-order low-pass frequency response. To set the compensation capacitors (C_S and C_F), consider the half-circuit of Figure 51, where the 50-Ω source is used.

Considering only the noise gain for the circuit of Figure 51, the low-frequency noise gain (N_{G1}) is set by the resistor ratio, while the high-frequency noise gain (N_{G2}) is set by the capacitor ratio. The capacitor values set both the transition frequencies and the high-frequency noise gain. If the high-frequency noise gain, determined by $N_{G2} = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a well controlled 2nd-order low-pass frequency response results.

APPLICATION INFORMATION (continued)

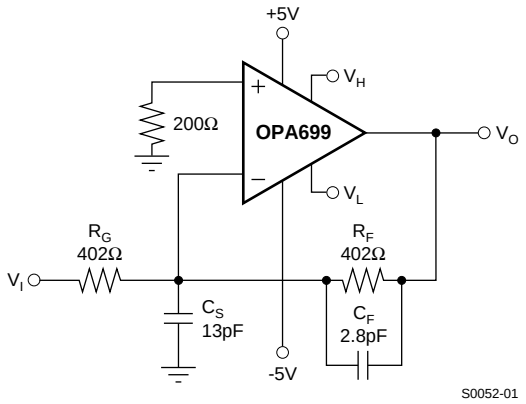


Figure 51. Broadband, Low-Inverting Gain External Compensation

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain (N_{G2}), which should be greater than the minimum stable gain for the OPA699. Here, a target of N_{G2} = 26 is used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain (N_{G1}). To simplify this discussion, we target a maximally flat 2nd-order low-pass Butterworth frequency response (Q = 0.707). The signal gain shown in Figure 51 sets the low-frequency noise gain to $N_{G1} = 1 + R_F/R_G$ (= 2 in this example). Then, using only these two gains and the gain bandwidth product for the OPA699 (1000 MHz), the key frequency in the compensation is set by Equation 1.

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1 - \frac{N_{G1}}{N_{G2}}\right) - \sqrt{1 - 2\frac{N_{G1}}{N_{G2}}}\right] \quad (1)$$

Physically, this Z_O (22.3 MHz for the values shown above) is set by $1/[2\pi R_F(C_F + C_S)]$ and is the frequency at which the rising portion of the noise gain would intersect the unity gain if projected back to a 0 dB gain. The actual zero in the noise gain occurs at $N_{G1} \times Z_O$ and the pole in the noise gain occurs at $N_{G2} \times Z_O$. That pole is physically set by $1/(R_FC_F)$. Since GBP is expressed in Hz, multiply Z_O by 2π and use to get C_F by solving Equation 2.

$$C_F = \frac{1}{2\pi R_F Z_O N_{G2}} \; (= 3 \text{ pF}) \quad (2)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S using Equation 3 (solving for C_S by using N_{G2} = 6):

$$C_S = \left(N_{G2} - 1\right)C_F \quad (3)$$

which gives C_S = 15 pF.

Both of these calculated values have been reduced slightly in Figure 51 to account for parasitics. The resulting closed-loop bandwidth is approximately equal to Equation 4.

$$f_{-3dB} \equiv \sqrt{Z_O - GBP} \quad (4)$$

For the values shown in Figure 51, $f_{-3\ dB}$ is approximately 149 MHz. This is less than that predicted by simply dividing the GBP product by N_{G1}. The compensation network controls the bandwidth to a lower value, while providing the full slew rate at the output and an improved distortion performance due to increased loop gain at frequencies below $N_{G1} \times Z_O$.

APPLICATION INFORMATION (continued)

LOW DISTORTION, LIMITED OUTPUT, ADC INPUT DRIVER

Figure 52 shows a simple ADC driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive. Note that the limiting voltages have been set 100 mV above/below the corresponding reference voltage from the converter. This circuit also implements an improved distortion for an inverting gain of –2 using external compensation.

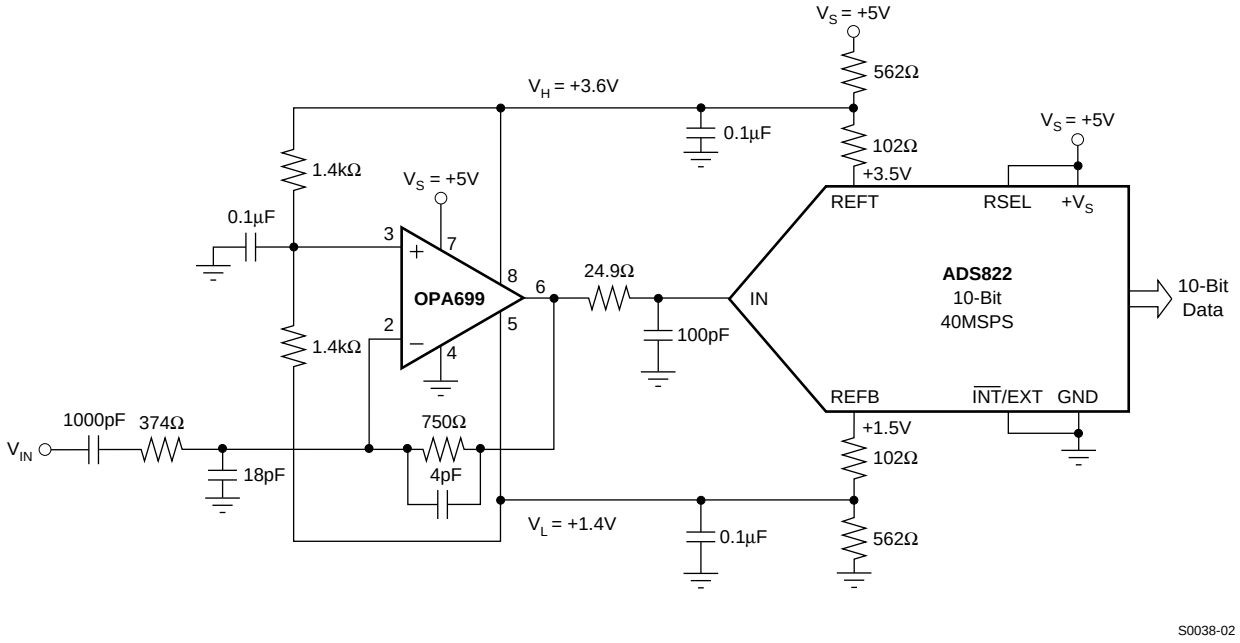


Figure 52. Single Supply, Limiting ADC Input Driver

LIMITED OUTPUT, DIFFERENTIAL ADC INPUT DRIVER

Figure 53 shows a differential ADC driver that takes advantage of the OPA699 limiters to protect the input of the ADC. Two OPA699s are used. The first one is an inverting configuration at a gain of –2. The second one is in a noninverting configuration at a gain of +2. See the *Low Gain Compensation for Improved SFDR* section for a discussion of stability issues of the OPA699 operating at a gain less than four. Each amplifier is swinging 2 V_{PP} providing a 4-V_{PP} differential signal to drive the input of the ADC. Limiters have been set 100 mV away from the magnitude of each amplifier maximum signal to provide input protection for the ADC, while maintaining an acceptable distortion level.

APPLICATION INFORMATION (continued)

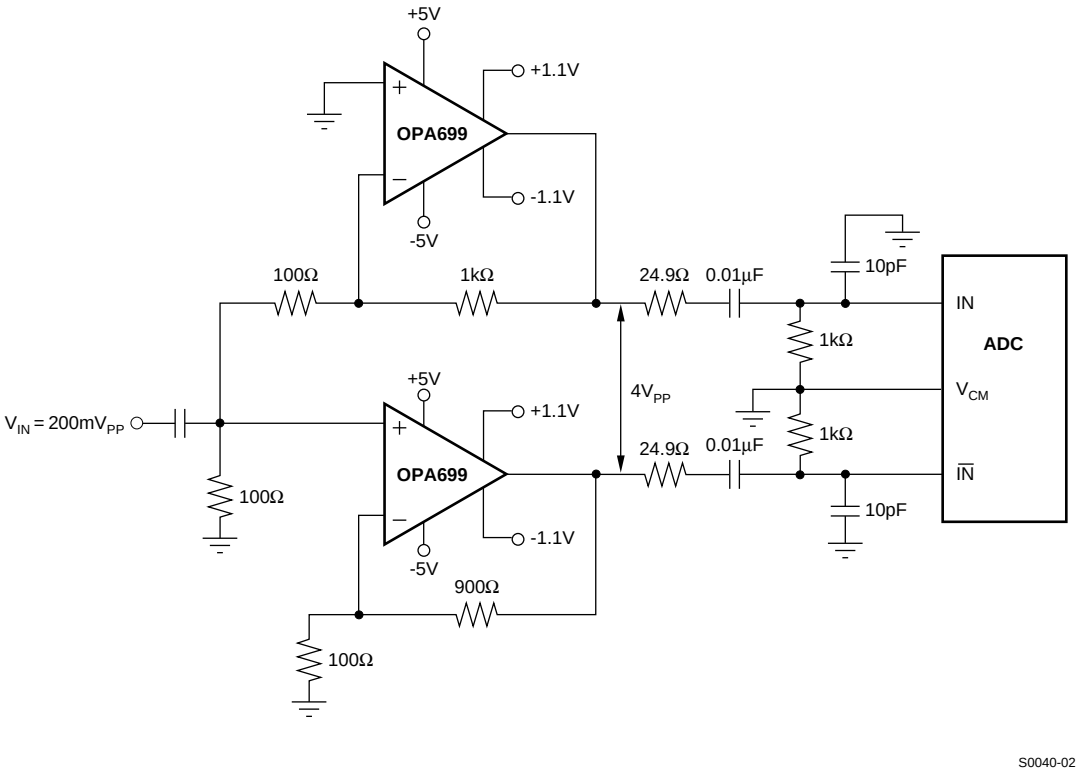


Figure 53. Single to Differential AC-Coupled, High Gain Output Limited ADC Driver

PRECISION HALF-WAVE RECTIFIER

Figure 54 shows a half-wave rectifier with outstanding precision and speed. V_H (pin 8) defaults to 3.5 V typically if left open, while the negative limit is set to ground.

The gain for the circuit in Figure 54 is set at +6. Figure 55 shows input and output for ±0.5 V 100-MHz input.

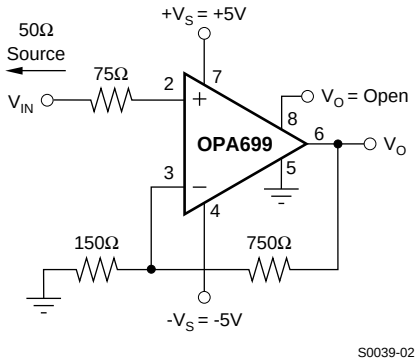


Figure 54. Precision Half-Wave Rectifier

APPLICATION INFORMATION (continued)

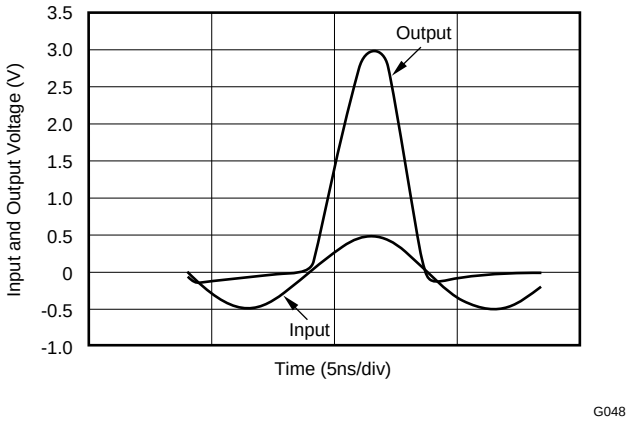


Figure 55. 100-MHz Sinewave Rectified

HIGH-SPEED Schmitt TRIGGER

Figure 56 shows a high-speed Schmitt Trigger. The output levels are precisely defined and the switching time is exceptional. The output voltage swings between V_H and V_L.

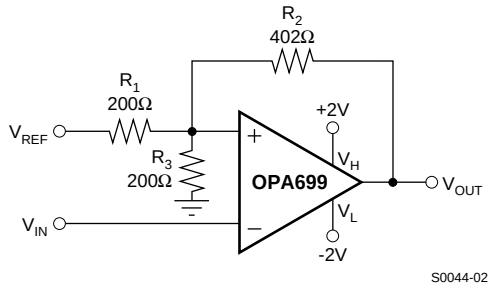


Figure 56. High-Speed Schmitt Trigger

The circuit operates as follows. When the input voltage is less than V_{HL} then the output is limiting at V_H. When the input is greater than V_{HH}, then the output is limiting at V_L, with V_{HL} and V_{HH} defined as in Equation 5.

$$V_{HL,HH} = \left(\frac{R1 \parallel R2 \parallel R3}{R1} \times V_{ref}\right) + \left(\frac{R1 \parallel R2 \parallel R3}{R2} \times V_{OUT}\right) \quad (5)$$

Due to the inverting function realized by the Schmitt Trigger, V_{HL} corresponds to $V_{OUT} = V_H$, and V_{HH} corresponds to $V_{OUT} = V_L$.

Figure 57 shows the Schmitt Trigger operating with V_{REF} = +5 V. This gives us V_{HH} = 2.4 V and V_{HL} = 1.6 V. The propagation delay for the OPA699 in a Schmitt Trigger configuration is 4 ns from high-to-low and 4 ns from low-to-high.

APPLICATION INFORMATION (continued)

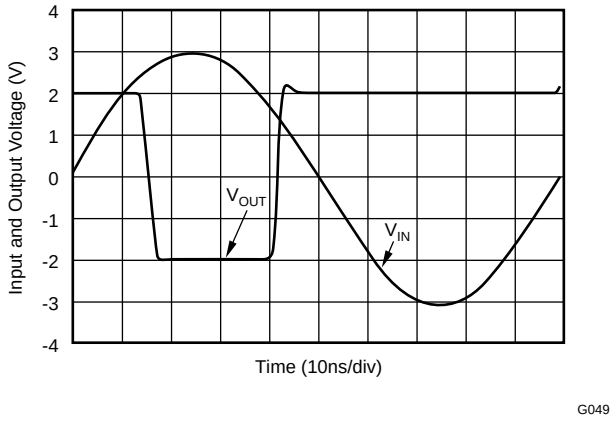


Figure 57. Schmitt Trigger Time Domain Response for a 10-MHz Sinewave

DESIGN-IN TOOLS

Applications Support

The Texas Instruments Applications Department is available for design assistance at 1-972-644-5580. The Texas Instruments web site (www.ti.com) has the latest product data sheets and other design tools.

Demonstration Boards

A PC board is available to assist in the initial evaluation of circuit performance of the OPA699ID. It is available as an unpopulated PCB with descriptive documentation, and can be requested through the Texas Instruments web site. See the demonstration board literature for more information. The summary information for this board is shown in Table 1.

Table 1. Evaluation Module Ordering Information

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE NUMBER
OPA699ID	SO-8	DEM-OPA-SO-1A	SBOU009

OPERATING SUGGESTIONS

Theory of Operation

The OPA699 is a voltage-feedback, gain of +4 V/V stable op amp. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This action from the limiters avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain. The limiters have a sharp transition from the linear region of operation to output limiting. This transition allows the limiter voltages to be set near (< 100 mV) the desired signal range. The distortion performance is also good near the limiter voltages.

Output Limiters

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L. Because the limiters act on the output, their accuracy does not change with the gain. The transition from the linear region of operation to output limiting is sharp—the desired output signal can safely come to within 30 mV of V_H or V_L with no onset of non-linearity. The limiter voltages can be set to within 0.7 V of the supplies ($V_L = -V_S + 0.7$ V, $V_H = +V_S - 0.7$ V). They must also be at least 400 mV apart ($V_H - V_L = 0.4$ V). When pins 5 and 8 are left open, V_H and V_L go to the default voltage limit; the minimum values are given in the electrical specifications. Looking at Figure 58 for the zero bias current case shows the expected range of (V_S – default limit voltages) = headroom.

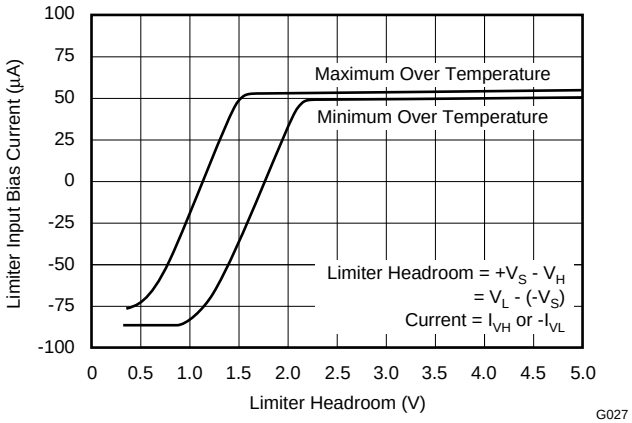


Figure 58. Limit Bias Current vs Bias Voltage

When the limiter voltages are more than 2.1 V from the supplies ($V_L = –V_S + 2.1$ V or $V_H = +V_S– 2.1$ V), you can use simple resistor dividers to set V_H and V_L (see Figure 47). Make sure to include the limiter input bias currents (see Figure 54) in the calculations (that is, I_{VL} = 50 µA into pin 5, and I_{VH} = +50 µA out of pin 8). For good limiter voltage accuracy, run a minimum 1-mA quiescent bias current through these resistors. When the limiter voltages need to be within 2.1 V of the supplies ($V_L = –V_S + 2.1$ V or $V_H = +V_S– 2.1$ V), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This condition typically is the case for single-supply operation (V_S = +5 V). Figure 48 runs 2.5 mA through the resistive divider that sets V_H and V_L. This limits errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages. The limiters' dc accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (for example, ±5%). Using a more accurate source and bypassing pins 5 and 8 with good capacitors, improves limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors. Other error sources also contribute, but should have little impact on the limiters' dc accuracy.
- Reduce offsets caused by the limiter input bias currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path dc errors as contributing to uncertainty in the useable output swing.
- The limiter offset voltage only slightly degrades limiter accuracy. Figure 59 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages. In this plot a fixed ±1-V output swing is driven while the limiter voltages are reduced symmetrically. Until the limiters are reduced to ±1.1 V, little distortion degradation is observed.

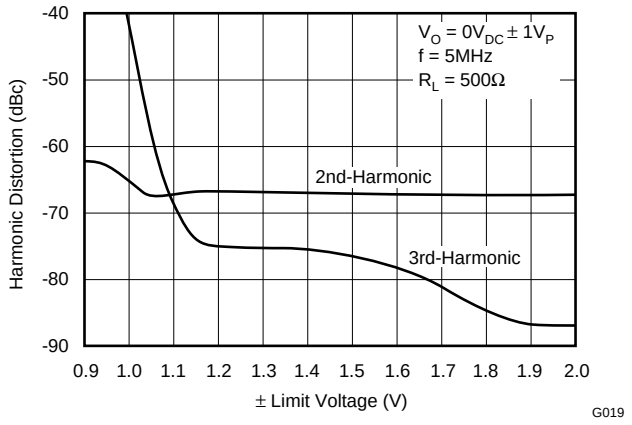


Figure 59. Harmonic Distortion Near Limit Voltages

Output Drive

The OPA699 has been optimized to drive 500-Ω loads, such as ADCs. It still performs well driving 100-Ω loads; the specifications are shown for the 500-Ω load. This makes the OPA699 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve *Output Impedance vs Frequency*, the OPA699 maintains low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

Thermal Considerations

The OPA699 does not require heat sinking under most operating conditions. Maximum desired junction temperature sets a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}), while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \times \theta_{JA}$, where T_A is the ambient temperature. For example, the maximum T_J for a OPA699ID with G = +6, R_F = 750 Ω, R_L = 500 Ω, and $\pm V_S$ = ±5 V at the maximum T_A = 85°C is calculated as:

$$P_{DQ} = (10\ V \times 15.5\ mA) = 155\ mW$$

$$P_{DL} = \frac{(5V)^2}{4 \times (500\ \Omega \parallel 900\ \Omega)} = 19.4\ mW$$

$$P_D = 155\ mW + 19.4\ mW = 174.4\ mW$$

$$T_J = 85^oC + 174.4\ mW \times 125^oC/W = 107^oC \quad (6)$$

This would be the maximum T_J from $V_O = \pm 2.5\ V_{DC}$. Most applications will be at a lower output stage power and have a lower T_J. Care must be taken when operating at higher ambient temperatures.

Capacitive Loads

Capacitive loads, such as the input to ADCs, decreases the amplifier phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads ≥2 pF should be isolated by connecting a small resistor in series with the output, as shown in Figure 60. Increasing the gain from +2 improves the capacitive drive capabilities due to increased phase margin.

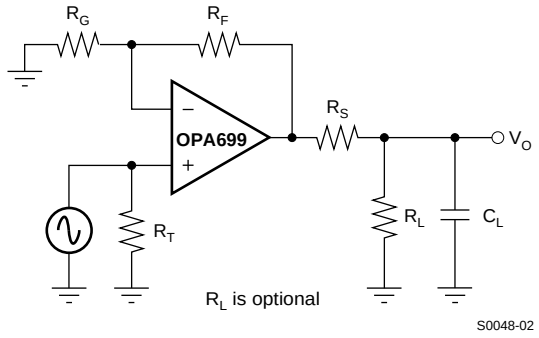


Figure 60. Driving Capacitive Loads

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29 pF/ft for RG-58) does not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

Frequency Response Compensation

The OPA699 is internally compensated to be +4 gain stable and has a nominal phase margin of 60° at a gain of +6. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –5 is equivalent to a gain of +6 for bandwidth purposes (that is, noise gain = 6). Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

For unity-gain stable amplifier applications, the OPA698 is recommended.

In applications where a large feedback resistor is required, such as a photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth is limited by the pole that the feedback resistor and this capacitor create. In other high-gain applications, use a three-resistor *Tee* network to reduce the RC time constants set by the parasitic capacitances.

Pulse Settling Time

The OPA699 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve *Recommended R_S vs Capacitive Load*. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics, when recovering from overdrive, are extremely good as shown in the typical characteristics.

Distortion

The OPA699's distortion performance is specified for a 500-Ω load, such as an ADC. Driving loads with smaller resistance increases the distortion as illustrated in Figure 61. Remember to include the feedback network in the load resistance calculations.

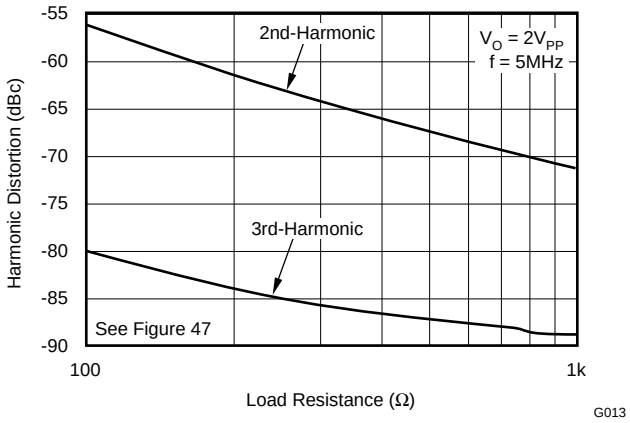


Figure 61. 5-MHz Harmonic Distortion vs Load Resistance

Noise Performance

High slew rate, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 4.1-nV/√Hz input voltage noise for the OPA699, however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 62 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

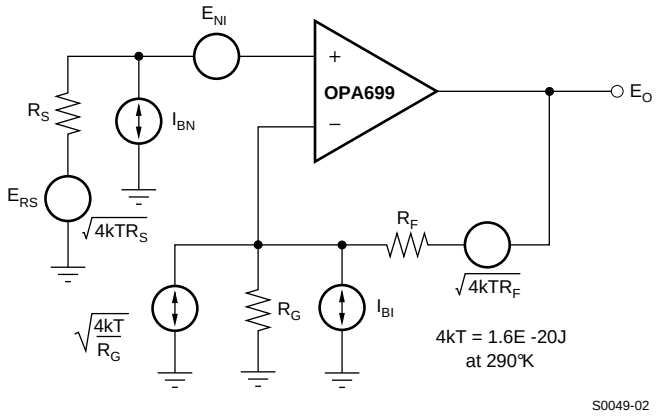


Figure 62. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 7 shows the general form for the output noise voltage using the terms shown in Figure 62.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (7)$$

Dividing this expression by the noise gain [NG = $(1+R_F/R_G)$] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 8.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (8)$$

Evaluating these two equations for the OPA699 circuit and component values (see Figure 47) gives a total output spot noise voltage of 27.4 nV/√Hz and a total equivalent input spot noise voltage of 4.6 nV/√Hz. This total input-referred spot noise voltage is only slightly higher than the 4.1-nV/√Hz specification for the op amp voltage noise alone. This is the case as long as the impedances appearing at each op amp input are limited to a maximum value of 300 Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300 Ω satisfies both noise and frequency response flatness considerations. Since the resistor-induced noise is negligible, additional capacitive decoupling across the bias current cancellation resistor (R_T) for the inverting op amp configuration of Figure 49 is not required, but is still desirable.

DC-Accuracy and Offset Control

The balanced input stage of a wideband voltage feedback op amp allows good output dc accuracy in a large variety of applications. The power-supply current trim for the OPA699 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 3 µA at each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. The total output offset voltage may be considerably reduced by matching the dc source resistances appearing at the two inputs. This reduces the output dc error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 47, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage, with NG = noninverting signal gain, equal to:

$\pm[NG \times V_{IO(MAX)}] \pm [R_F \times I_{IO(MAX)}]$
$= \pm(2 \times 8\ mV) \pm (750\ \Omega \times 3\ \mu A)$
$= \pm 18.3\ mV$

A fine-scale output offset null or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc-offset control into an op amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the dc offset voltage on the summing junction sets up a dc current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, Figure 63 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This insures that the adjustment circuit has minimal effect on the loop gain as well as the frequency response.

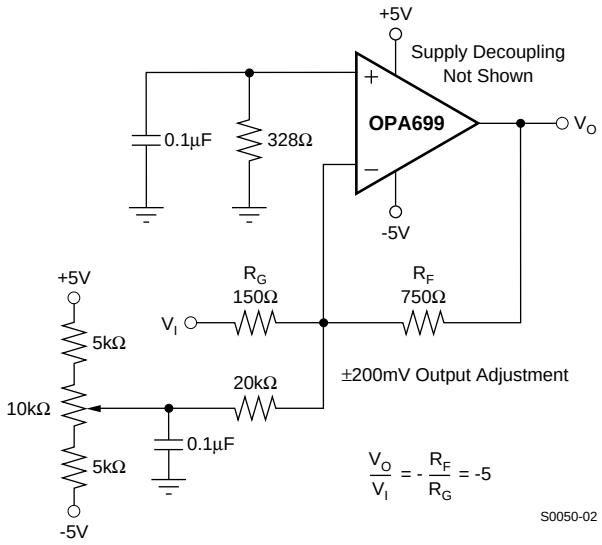


Figure 63. DC-Coupled, Inverting Gain of –5, With Offset Adjustment

Board Layout Guidelines

Achieving optimum performance with the high-frequency OPA699 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

1. **Minimize parasitic capacitance to any ac ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.
2. **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high frequency 0.1-µF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2 µF to 6.8 µF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device and be shared among several adjacent devices.
3. **Place external components close** to the OPA699. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.
4. **Use high-frequency components** to minimize parasitic elements. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work well. Use R_F type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2 µF to 6.8 µF) should be tantalum for better high frequency and pulse performance.

5. **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2-pF parasitic parallel capacitance. For resistors > 1.5 kΩ, this adds a pole and/or zero below 500 MHz. Make sure that the output loading is not too heavy. The recommended 750-Ω feedback resistor is a good starting point in most designs.
6. **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output and use the series isolation resistor recommended in the typical performance curve, *Recommended R_S vs Capacitive Load*. Parasitic loads < 2 pF may not need the isolation resistor.
7. **When long traces are necessary**, use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω transmission line is not required on board—a higher characteristic impedance helps reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line and a matched load resistor at the other end to make the line appear as a resistor. If the 6 dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This isolates the source from the reactive load presented by the line, but the frequency response will be degraded. Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors alters the transmission line match and can cause unwanted signal reflections and reactive loading.
8. **Do not use sockets** for high-speed parts like the OPA699. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

Power Supplies

The OPA699 is nominally specified for operation using either ±5-V supplies or a single +5-V supply. The maximum specified total supply voltage of 12 V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as required headroom to the supply voltage. Observing this input and output headroom requirement allows a design of non-standard or single-supply operation circuits. Figure 48 shows one approach to single-supply operation.

input and ESD protection

The OPA699 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 64.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (e.g., in systems with ±15-V supply parts driving into the OPA699), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

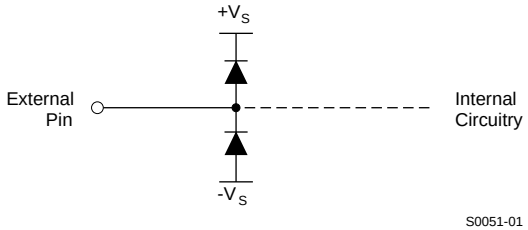


Figure 64. I/O Pin ESD Protection

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA699MJD	Active	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA699MJD
OPA699MJD.A	Active	Production	CDIP SB (JD) | 8	45 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA699MJD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA699M :

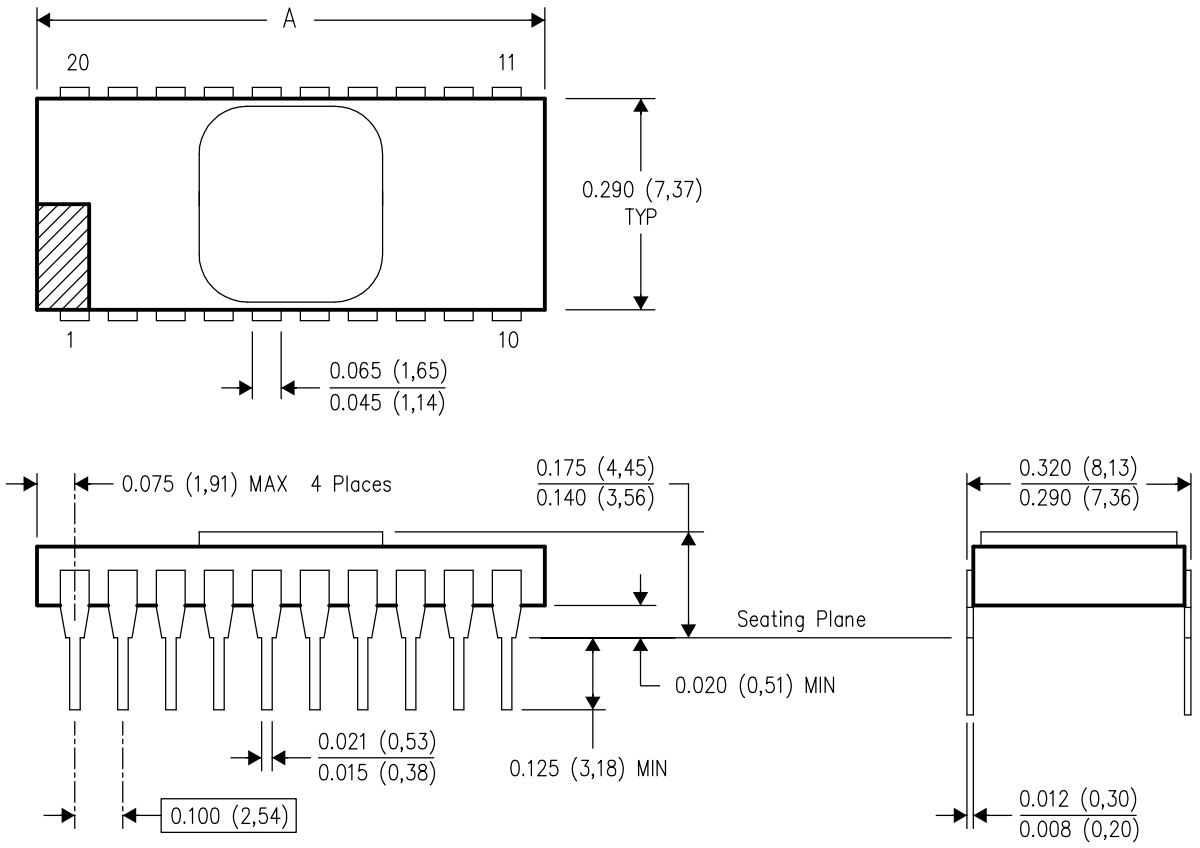
- Catalog : OPA699

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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