OPA698 Unity-Gain Stable, Wideband Voltage Limiting Amplifier

1 Features

- High linearity near limiting
- Fast recovery from overdrive: 1ns
- Limiting voltage accuracy: ±5mV
- –3db bandwidth (g = +1): 650MHz
- Gain bandwidth product: 300MHz
- Slew rate: 1800V/µs
- ±5V and +5V supply operation
- High-gain version available: OPA699

2 Applications

- Fast limiting analog-to-digital converter (ADC) input buffers
- CCD pixel clock stripping
- Video sync stripping
- HF mixers
- IF limiting amplifiers
- AM signal generation
- Nonlinear analog signal processing
- OPA688 upgrade

3 Description

The OPA698 is a wide-band, unity-gain stable voltage-feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when attempting to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±5mV.

The op amp operates linearly to within 20mV of the output limit voltages. The combination of a narrow nonlinear range and the low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 1ns recovery from limiting provides overdrive signals that are transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA698 to be used in all standard op-amp applications.

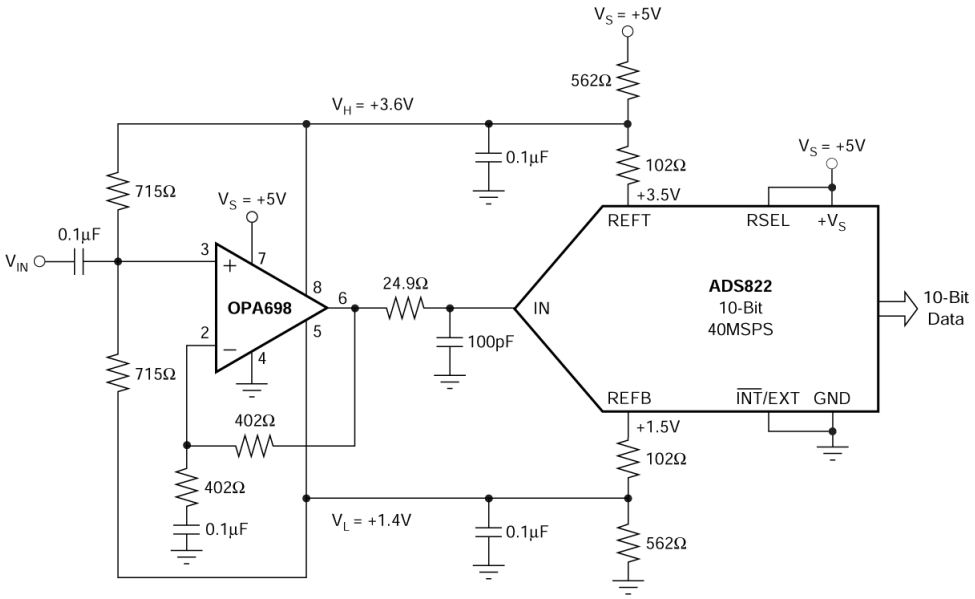
Nonlinear analog signal processing benefits from the ability of the OPA698 to sharply transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

The OPA698 is available in an industry-standard pin-out SOIC-8 package. For higher gain, or transimpedance applications that require output limiting with fast recovery, consider the OPA699.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA698	D (SOIC, 8)	4.9mm × 6mm

(1) See Section 4.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Single-Supply Limiting ADC Input Driver

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4 Related Products

DEVICE	V_S (V)	GBW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	ARCHITECTURE
OPA817	±6.3	400	1000	4.5	FET-input, voltage-feedback
OPA818	±6.5	2700	1400	2.2	FET-input, voltage-feedback
OPA690	±6	300	1900	4.6	Bipolar-input, voltage-feedback
OPA695	±6	N/A	5000	2	Bipolar-input, current-feedback
OPA698	±6.5	300	1800	4	Bipolar-input, voltage-feedback
OPA699	±6.5	1000	1400	4.1	Bipolar-input, voltage-feedback

5 Pin Configuration and Functions

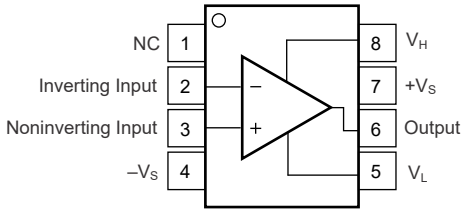

Figure 5-1. D Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Inverting Input	2	Input	Inverting input
Noninverting Input	3	Input	Noninverting input
NC	1	—	No internal connection (float this pin)
Output	6	Output	Output
$–V_S$	4	Supply	Negative (lowest) supply
$+V_S$	7	Supply	Positive (highest) supply
V_L	5	Supply	Limiter input low
V_H	8	Supply	Limiter input high

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage		13	V_{DC}
	Internal power dissipation	See *Thermal Analysis*		
V_{ID}	Differential input voltage		$\pm V_S$	V
	dVS/dT for supply turn-on and turn-off(2)		±0.4	V/µs
	Limiter voltage range		$\pm(V_S - 0.7)$	V
I_{IN}	Continuous input current(3)		10	mA
	Input voltage		$\pm V_S$	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying less than this specification keeps the edge-triggered ESD absorption devices across the supply pins off.
(3) Continuous input current limit for the ESD diodes to supply pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	±2.5	±5	±6	V
T_A	Operating temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA698 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics V_S = ±5V

at T_A ≅ 25°C, R_F = 402Ω, R_L = 500Ω, G = 2V/V, V_H = –V_L = 2V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	G = 1V/V, V_O = 0.2V_{PP}, R_F = 25Ω			650		MHz
		G = 2V/V, V_O = 0.2V_{PP}			215		
		G = –1V/V, V_O = 0.2V_{PP}			215		
GBP	Gain bandwidth product	G ≥ 5V/V			300		MHz
	Bandwidth for 0.1dB gain flatness	V_O = 0.2V_{PP}			30		MHz
	Peaking at a gain of 1V/V	R_F = 25Ω, V_O = 0.2V_{PP}			1.5		dB
	Large-signal bandwidth	V_O = 4V_{PP} V_H = – V_L = 2.5V			160		MHz
	Slew rate	4V step, V_H = – V_L = 2.5V			1800		V/µs
	Rise-and-fall time	V_O = 0.2V step			1.4		ns
	Settling time	0.05%, V_O = 2V step			25		ns
	2nd-order harmonic distortion	f = 5MHz, V_O = 2V_{PP}, R_L = 500Ω			–94		dBc
	3rd-order harmonic distortion	f = 5MHz, V_O = 2V_{PP}, R_L = 500Ω			–85		dBc
	Input voltage noise	f ≥ 1MHz			4		nV/√Hz
	Input current noise	f ≥ 1MHz			1.5		pA/√Hz
DC PERFORMANCE(1)							
A_{OL}	Open-loop voltage gain	V_O = ±0.5V		56	80		dB
			T_A = –40°C to +85°C	52			
V_{OS}	Input offset voltage				±2	±5	mV
		T_A = –40°C to +85°C				±8	
	Average offset voltage drift	T_A = –40°C to +85°C				±20	µV/°C
	Input bias current(1)				+0.2	±10	µA
		T_A = –40°C to +85°C				±12	
	Average bias current drift	T_A = –40°C to +85°C				±20	nA/°C
	Input offset current				±0.1	±2	µA
		T_A = –40°C to +85°C				±3	
	Average offset current drift	T_A = –40°C to +85°C				±10	nA/°C
INPUT							
CMIR	Common-mode input voltage(2)			±3.2	±3.3		V
		T_A = –40°C to +85°C		±3.1			
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5V		55	82		dB
			T_A = –40°C to +85°C	52			
	Input impedance	Differential mode			1 || 0.3		MΩ || pF
		Common-mode			33 || 1.4		

6.5 Electrical Characteristics V_S = ±5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 500Ω, G = 2V/V, V_H = –V_L = 2V, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	R_L = 500Ω, V_H = –V_L = 4.3V		±3.9	±4.0		V
			T_A = –40°C to +85°C	±3.8			
	Current output	Sourcing, V_O = 0V		90	190		mA
			T_A = –40°C to +85°C	80			
		Sinking, V_O = 0V		–90	–190		
			T_A = –40°C to +85°C	–80			
	Closed-loop output impedance	G = 1V/V, R_F = 25Ω, f < 100kHz			0.01		Ω
OUTPUT VOLTAGE LIMITER							
	Output voltage limited range	Pins 5 and 8			±3.8		V
			T_A = –40°C to +85°C				
	Default limit voltage, upper	Limiter pins open		+3.3	+3.5		V
			T_A = –40°C to +85°C	+3.1			
	Default limit voltage, lower	Limiter pins open		–3.3	–3.5		V
			T_A = –40°C to +85°C	–3.1			
	Minimum limiter separation (V_H –V_L)			400	400		mV
		T_A = –40°C to +85°C		400			
	Maximum limit voltage			±4.3			V
		T_A = –40°C to +85°C		±4.3			
	Limiter input bias current magnitude(3)	V_O = 0V		40	50	60	µA
		T_A = –40°C to +85°C		36		65	
	Limiter input bias average drift	T_A = –40°C to +85°C				35	nA/°C
	Limiter input impedance				10 || 0.85		MΩ || pF
	Limiter feedthrough(4)	f = 5MHz			–68		dB
	Limiter offset	V_{IN} = ±2V, V_O – V_H) or (V_O – V_L)			±5	±30	mV
			T_A = –40°C to +85°C			±40	
	Op amp input bias current shift	V_{IN} = ±2V, linear to limited output			0.15		µA
	Limiter small-signal bandwidth	$2V_{DC}$ + $20mV_{PP}$			700		MHz
	Limiter slew rate(5)	2 × overdrive, V_H or V_L			175		V/µs
	Limiter overshoot	2 × overdrive, V_{IN} = V_{CM} to V_{CM} ±2V step			250		mV
	Recovery time	2 × overdrive	V_{IN} = ±2V to 0V step		1		ns
	Linearity guardband(6)	f = 5MHz, V_O = $2V_{PP}$	f = 5MHz, V_O = $2V_{PP}$		30		mV
POWER SUPPLY							
	Quiescent current	V_S = ±5V		13.8	15.5	17.3	mA
			T_A = –40°C to +85°C	13.4		17.7	
PSRR	Power-supply rejection ratio	Input-referred		68	90		dB
			T_A = –40°C to +85°C	66			

(1) Current is considered positive out of node.
(2) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
(3) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Figure 7-8 and Figure 7-15.
(4) Limiter feedthrough is the ratio of the output magnitude to the sine wave added to V_H (or V_L) when V_{IN} = 0V.
(5) V_H slew rate conditions are: V_{IN} = 2V, G = 2V/V, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar.
(6) Linearity guardband is defined for an output sinusoid (f = 5MHz, V_O = $0V_{DC}$ ±$1V_{PP}$) centered between the limiter levels (V_H and V_L). Linearity guardband is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB.

6.6 Electrical Characteristics V_S = 5V

at T_A ≅ 25°C, R_F = 402Ω, R_L = 500Ω, G = 2V/V, $V_L = V_{CM} – 1.2V$, and $V_H = V_{CM} + 1.2V$, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Small-signal bandwidth	G = 1V/V, V_O = 0.2V_{PP}, R_F = 25Ω			550		MHz
		G = 2V/V, V_O = 0.2V_{PP}			200		
		G = –1V/V, V_O = 0.2V_{PP}			210		
	Gain bandwidth product	G ≥ 5V/V, V_O < 0.2V_{PP}			300		MHz
	Bandwidth for 0.1dB gain flatness	V_O < 0.2V_{PP}			26		MHz
	Peaking at a gain of 1V/V	G = 1V/V, R_F = 25Ω, V_O = 0.2V_{PP}			2.5		dB
	Large-signal bandwidth	V_O = 2V_{PP}			200		MHz
	Slew rate	2V step			820		V/µs
	Rise-and-fall time	V_O = 0.2V step			1.4		ns
	Settling time	0.05%, G = 2V/V, V_O = 1V step			28		ns
	2nd-order harmonic distortion	f = 5MHz, V_O = 2V_{PP}, R_L = 500Ω			–95		dBc
	3rd-order harmonic distortion	f = 5MHz, V_O = 2V_{PP}, R_L = 500Ω			–81		dBc
	Input voltage noise	f > 1MHz			4		nV/√Hz
	Input current noise	f > 1MHz			1.43		pA/√Hz
DC PERFORMANCE[1]							
A_{OL}	Open-loop voltage gain	V_O = ±0.5V, V_{CM} = 2.5V		54	77		dB
			T_A = –40°C to +85°C	51			
	Input offset voltage	V_{CM} = 2.5V			±1	±6	mV
			T_A = –40°C to +85°C			±8	
	Average offset voltage drift	V_{CM} = 2.5V	T_A = –40°C to +85°C			±15	µV/°C
	Input bias current	V_{CM} = 2.5V			±0.5	±10	µA
			T_A = –40°C to +85°C			±12	
	Average bias current drift	V_{CM} = 2.5V	T_A = –40°C to +85°C			±25	nA/°C
	Input offset current	V_{CM} = 2.5V			±0.1	±2	µA
			T_A = –40°C to +85°C			±3	
	Average offset current drift	V_{CM} = 2.5V	T_A = –40°C to +85°C			±15	nA/°C
CMIR	Common-mode input voltage		T_A = 25°C	V_{CM} ±0.7	V_{CM} ±0.8		V
CMIR	Common-mode input voltage[2]		T_A = –40°C to +85°C	V_{CM} ±0.6			V
INPUT							
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5V		54	82		dB
			T_A = –40°C to +85°C	52			
	Input impedance	Differential mode, V_{CM} = 2.5V			0.77 || 0.3		MΩ || pF
		Common-mode, V_{CM} = 2.5V			24 || 1.5		

6.6 Electrical Characteristics V_S = 5V (continued)

at T_A ≅ 25°C, R_F = 402Ω, R_L = 500Ω, G = 2V/V, $V_L = V_{CM} – 1.2V$, and $V_H = V_{CM} + 1.2V$, and input and output referenced to midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Most-positive output voltage	R_L ≥ 500Ω, $V_H = V_{CM} + 1.8V$		3.9	4.1		V
			T_A = –40°C to +85°C	3.8			
	Least-positive output voltage	R_L ≥ 500Ω, $V_L = V_{CM} – 1.8V$		1.1	0.9		V
			T_A = –40°C to +85°C	1.2			
	Current output	Sourcing, V_O = 2.5V		60	170		mA
			T_A = –40°C to +85°C	50			
		Sinking,, V_O = 2.5V		–60	–170		
			T_A = –40°C to +85°C	–50			
	Closed-loop output impedance	G = 1V/V, f < 100kHz, R_F = 25Ω			0.1		Ω
OUTPUT VOLTAGE LIMITER							
	Limiter voltage high	Pin 8			3.9		V
	Limiter voltage low	Pin 5			1.1		V
	Default limiter voltage	Limiter pins open		V_{CM} ±0.8	V_{CM} ±1.1		V
			T_A = –40°C to +85°C	V_{CM} ±0.6			
	Minimum limiter separation ($V_H – V_L$)			400	400		mV
		T_A = –40°C to +85°C		400			
	Maximum limit voltage					V_{CM} ±1.8	V
	Limiter input bias current magnitude(3)	V_O = 2.5V			8		µA
	Limiter input impedance				1 || 7		MΩ || pF
	Limiter feedthrough(4)	f = 5MHz			–92		dB
	Limiter voltage accuracy	$V_{IN} = V_{CM}$ ± 1.2V, ($V_O – V_H$) or ($V_O – V_L$)			±15	±30	mV
			T_A = –40°C to +85°C			±40	
	Limiter small-signal bandwidth	$V_{IN} = V_{CM}$ ± 1.2V, $V_O < 0.02V_{PP}$			515		MHz
	Limiter slew rate(5)	2 × overdrive, V_H or V_L			150		V/µs
	Overshoot	2 × overdrive, $V_{IN} = V_{CM}$ to V_{CM} ± 1.2V step			40		mV
	Recovery time	2 × overdrive, $V_{IN} = V_{CM}$ ± 1.2V to V_{CM} step			2.5		ns
	Linearity guardband(6)	f = 5MHz, $V_O = 2V_{PP}$			30		mV
POWER SUPPLY							
	Quiescent current	V_S = 5V		13.6	15.6	17.2	mA
			T_A = –40°C to +85°C	13.2		17.6	
+PSRR	Power-supply rejection ratio	V_S = 4.5V to 5.5V			85		dB

(1) Current is considered positive out of node.
(2) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
(3) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Figure 7 -9 and Figure 7-15.
(4) Limiter feedthrough is the ratio of the output magnitude to the sine wave added to V_H (or V_L) when V_{IN} = 0V.
(5) V_H slew rate conditions are: V_{IN} = 2V, G = 2V/V, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar.
(6) Linearity guardband is defined for an output sinusoid (f = 5MHz, $V_O = 0V_{DC} ±1V_{PP}$) centered between the limiter levels (V_H and V_L). Linearity guardband is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB.

6.7 Typical Characteristics: V_S = ±5V

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

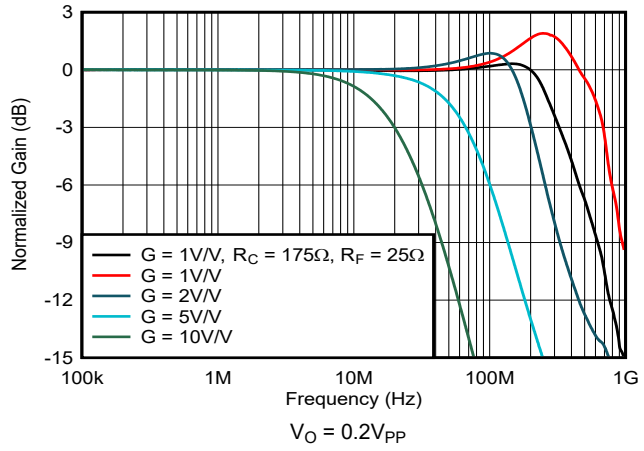

Figure 6-1. Noninverting Small-Signal Frequency Response

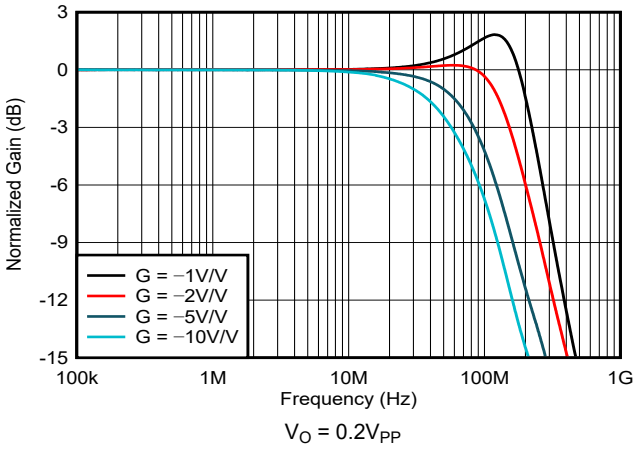

Figure 6-2. Inverting Small-Signal Frequency Response

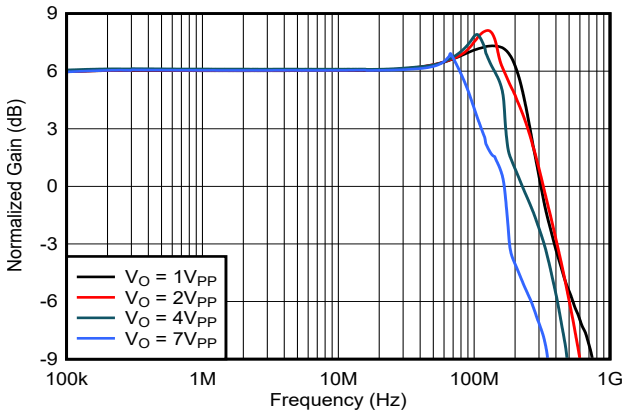

Figure 6-3. Noninverting Large-Signal Frequency Response

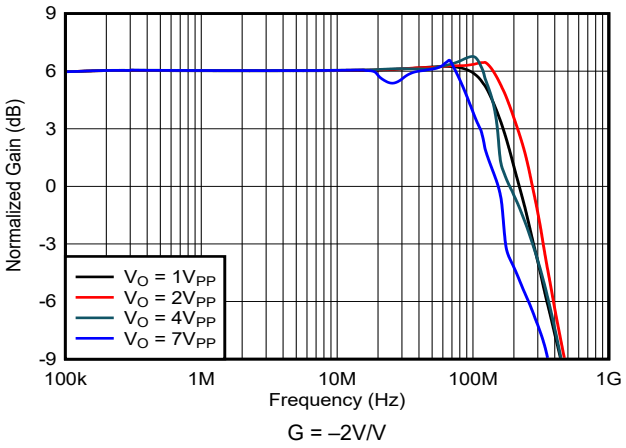

Figure 6-4. Inverting Large-Signal Frequency Response

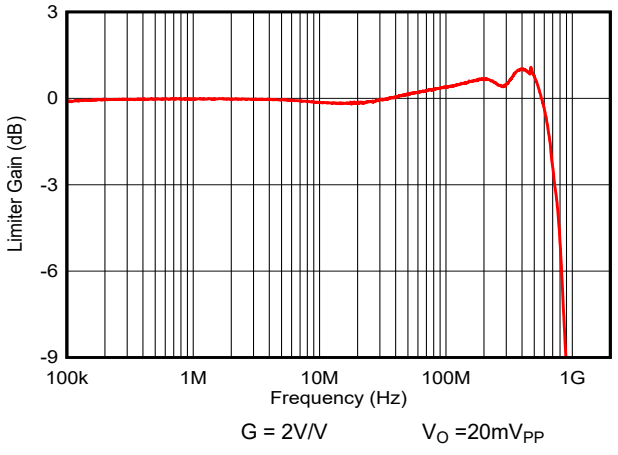

Figure 6-5. V_H—Limiter Small-Signal Frequency Response

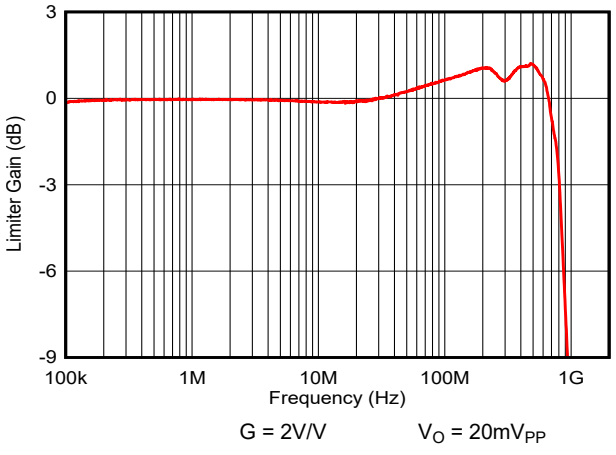

Figure 6-6. V_L—Limiter Small-Signal Frequency Response

6.7 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

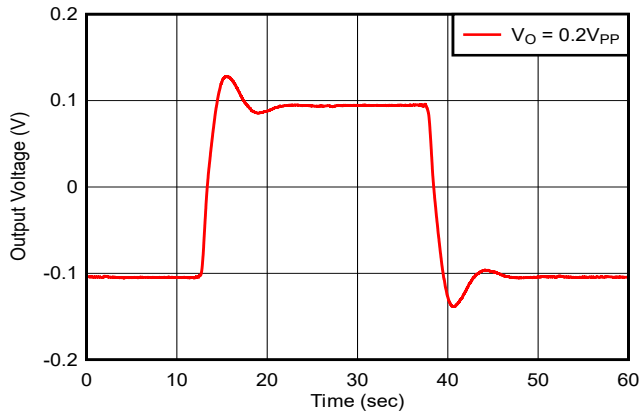

Figure 6-7. Small-Signal Pulse Response

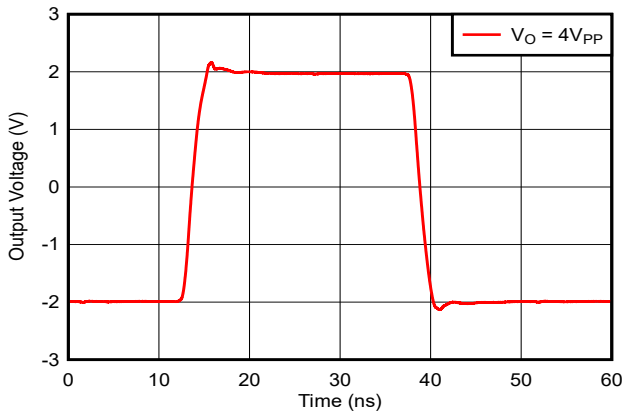

Figure 6-8. Large-Signal Pulse Response

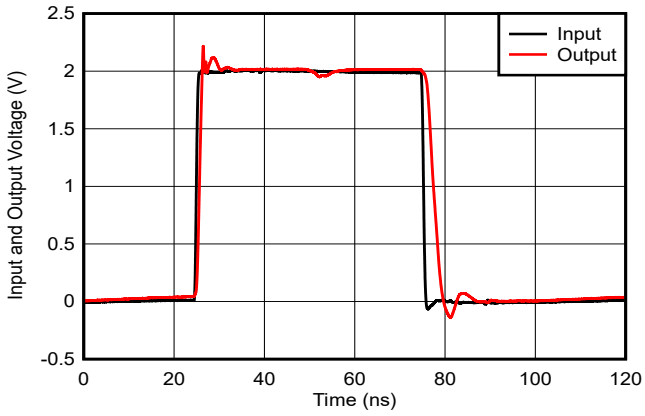

Figure 6-9. V_H—Limited Pulse Response

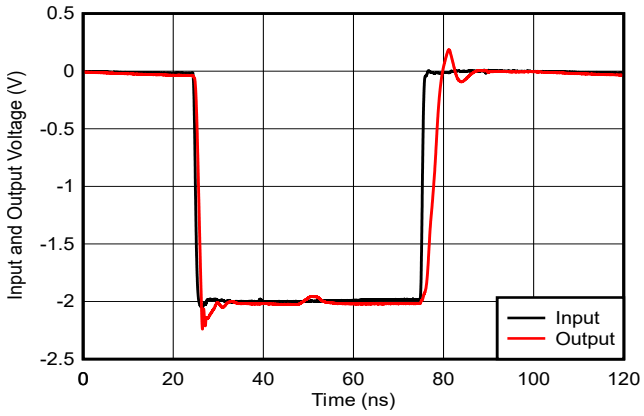

Figure 6-10. V_L—Limited Pulse Response (20MHz)

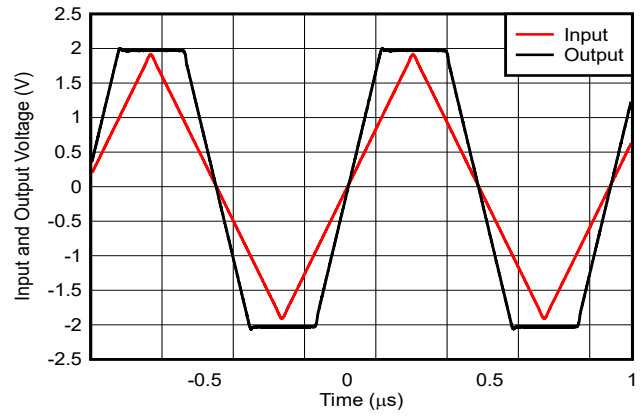

Figure 6-11. Limited Output Response

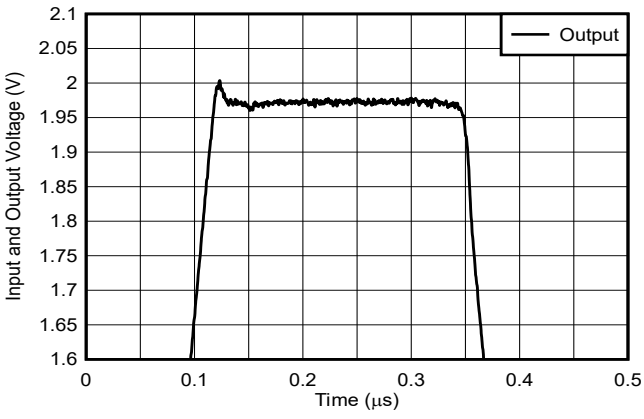

Figure 6-12. Detail of Limited Output Voltage

6.7 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

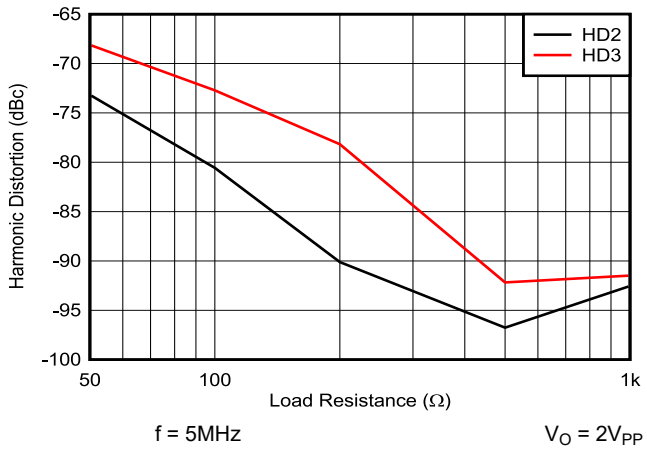

Figure 6-13. Harmonic Distortion vs Load Resistance

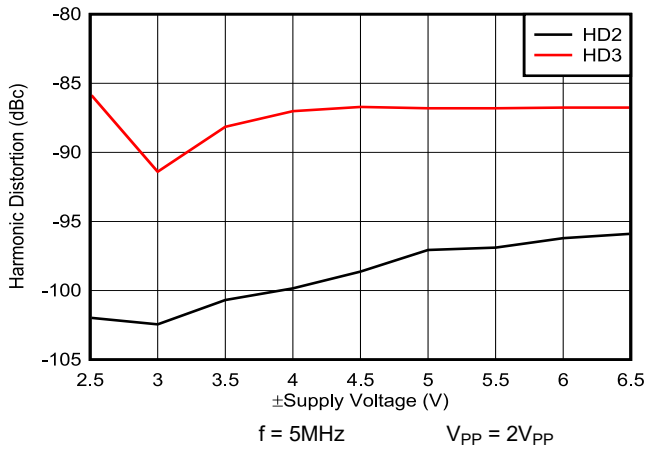

Figure 6-14. 5MHz Harmonic Distortion vs Supply Voltage

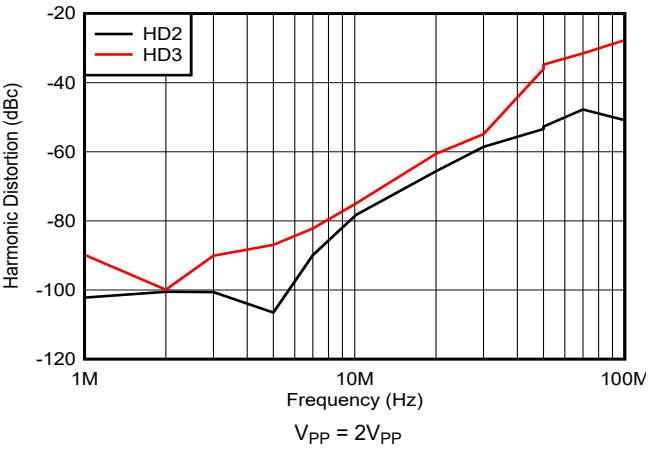

Figure 6-15. Harmonic Distortion vs Frequency

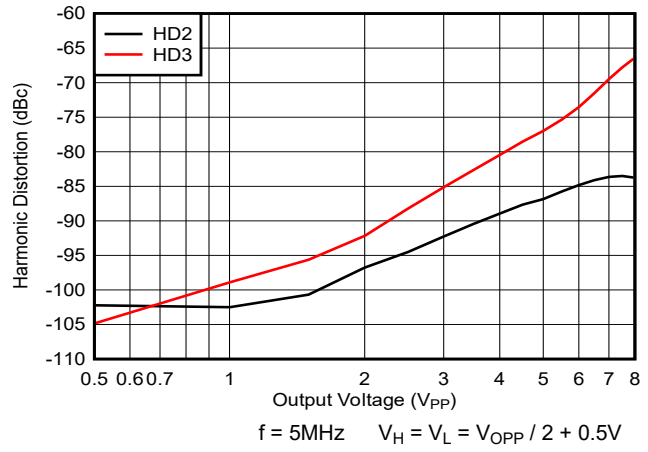

Figure 6-16. 5MHz Harmonic Distortion vs Output Voltage

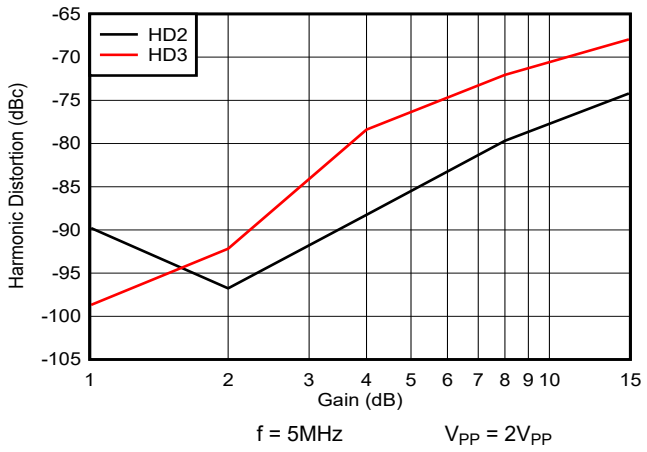

Figure 6-17. Harmonic Distortion vs Noninverting Gain

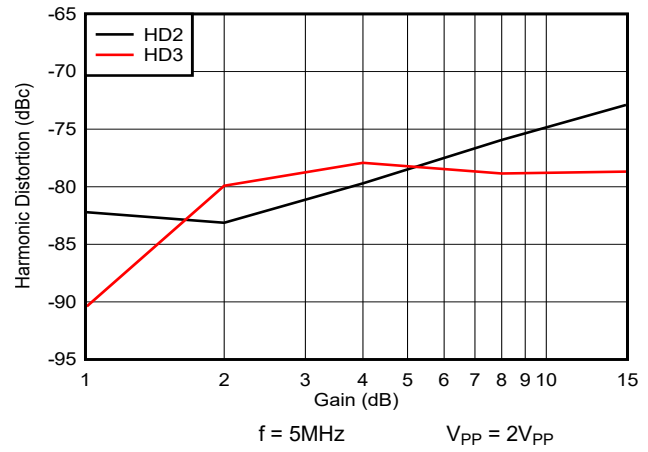

Figure 6-18. Harmonic Distortion vs Inverting Gain

6.7 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

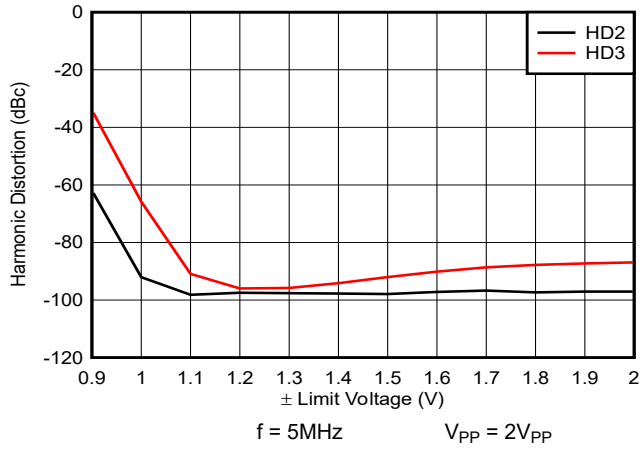

Figure 6-19. Harmonic Distortion Near Limiting Voltages

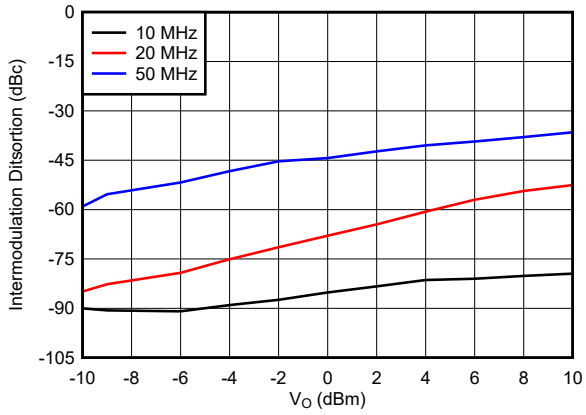

Figure 6-20. 2-Tone, 3rd-Order Intermodulation Intercept

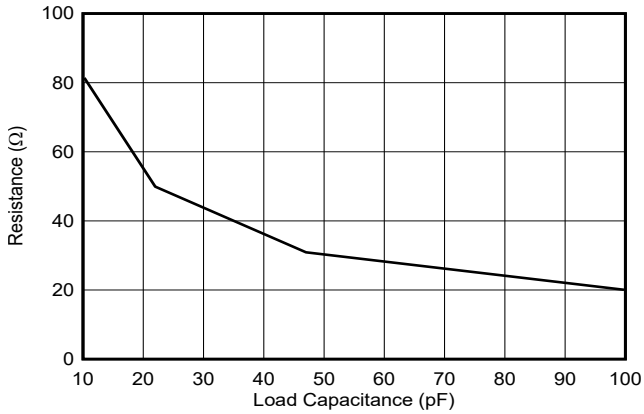

Figure 6-21. Recommended R_S vs Capacitive Load

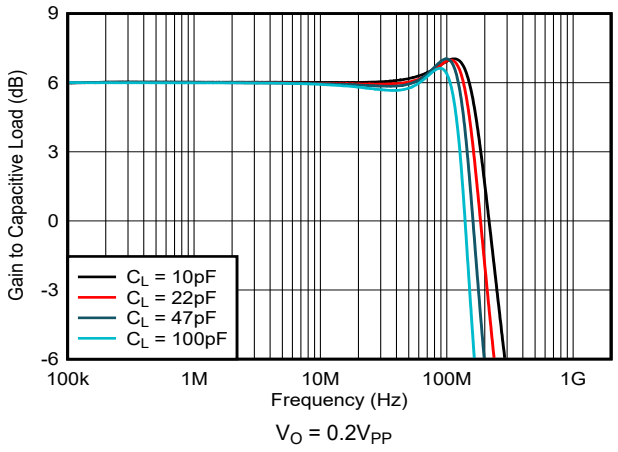

Figure 6-22. Frequency Response vs Capacitive Load

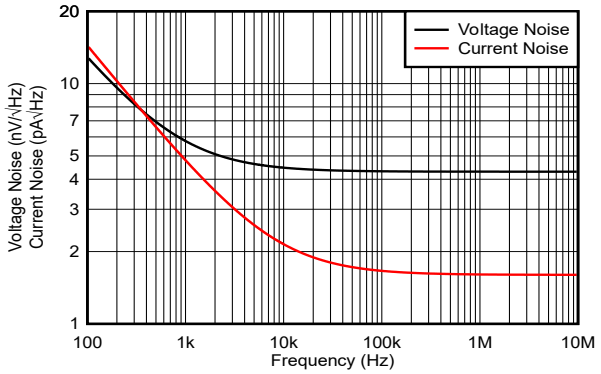

Figure 6-23. Input Voltage and Current Noise Density

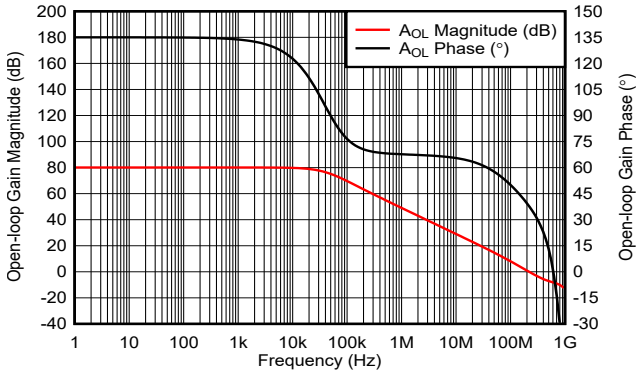

Figure 6-24. Open-Loop Frequency Response

6.7 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

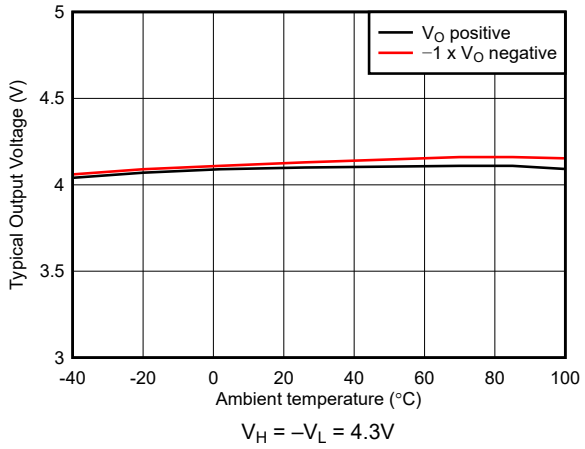

Figure 6-25. Voltage Range vs Temperature

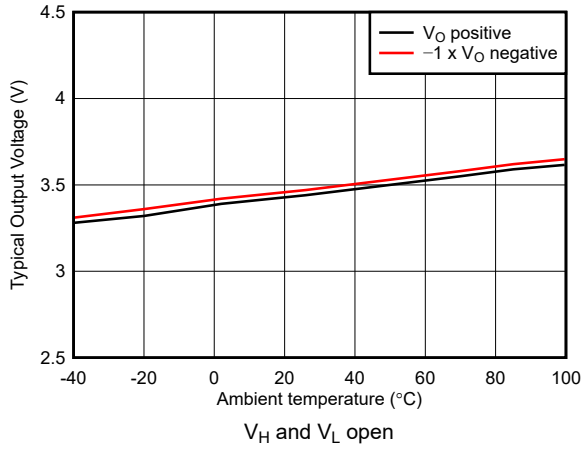

Figure 6-26. Limited Voltage Range vs Temperature

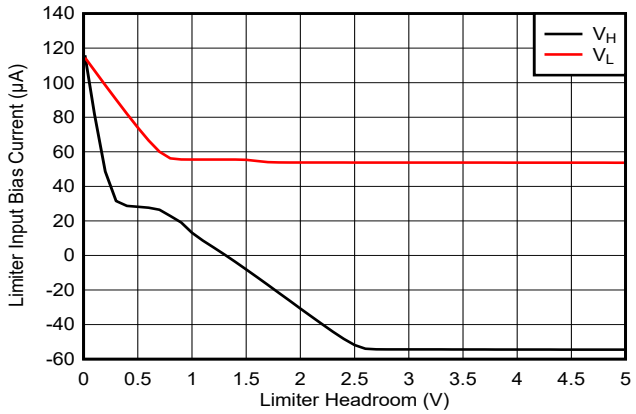

Figure 6-27. Limiter Input Bias Current vs Bias Voltage

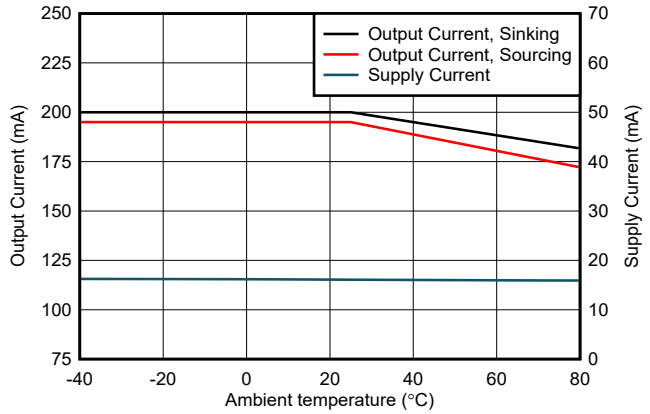

Figure 6-28. Supply and Output Currents vs Temperature

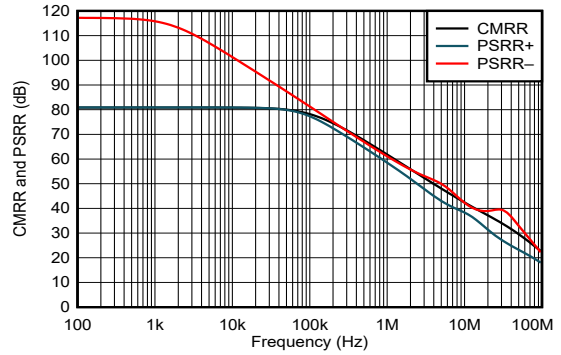

Figure 6-29. Common-Mode Rejection Ratio and Power-Supply Rejection vs Frequency

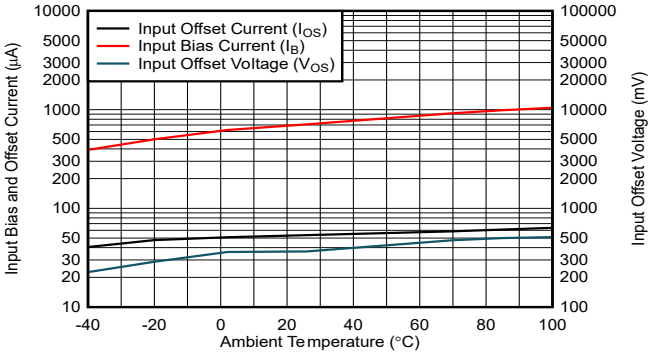

Figure 6-30. Typical DC Drift Over Temperature

6.7 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (unless otherwise noted)

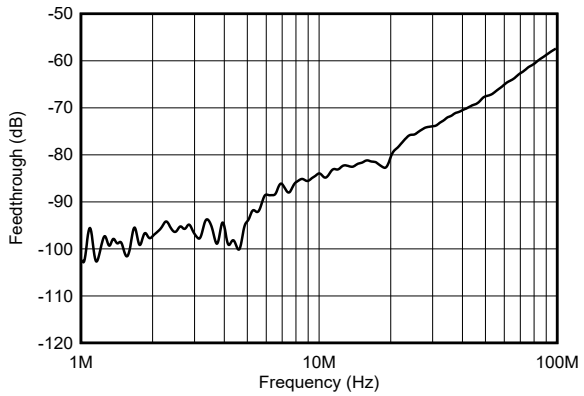

Figure 6-31. Limiter Feedthrough

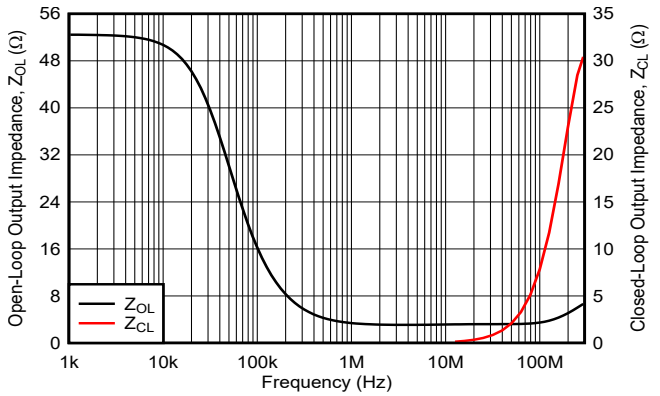

Figure 6-32. Closed-Loop Output Impedance

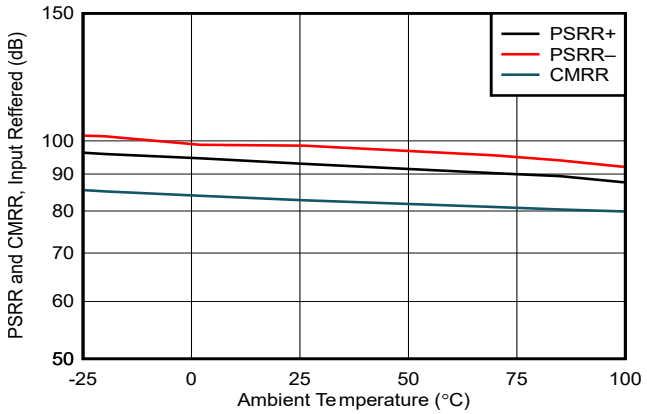

Figure 6-33. ±PSRR and CMRR vs Temperature

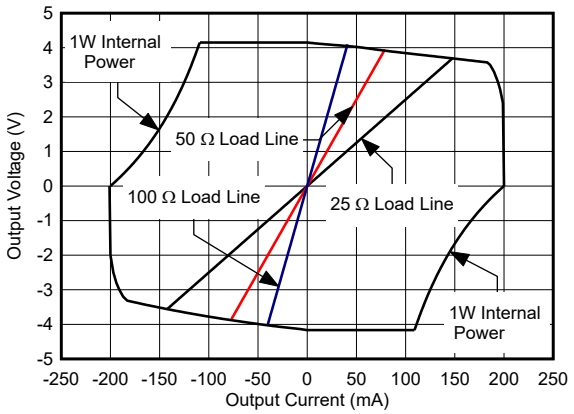

Figure 6-34. Output Voltage and Current Limitations

6.8 Typical Characteristics: V_S = 5V

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω to V_{CM} = 2.5V, V_L = V_{CM} – 1.2V, and V_H = V_{CM} + 1.2V (unless otherwise noted)

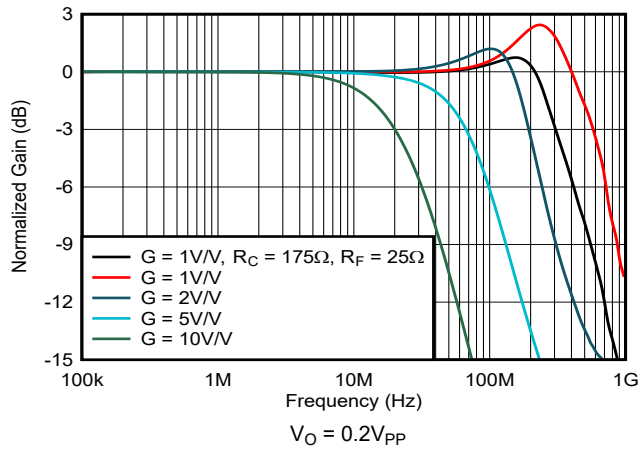

Figure 6-35. Noninverting Small-Signal Frequency Response

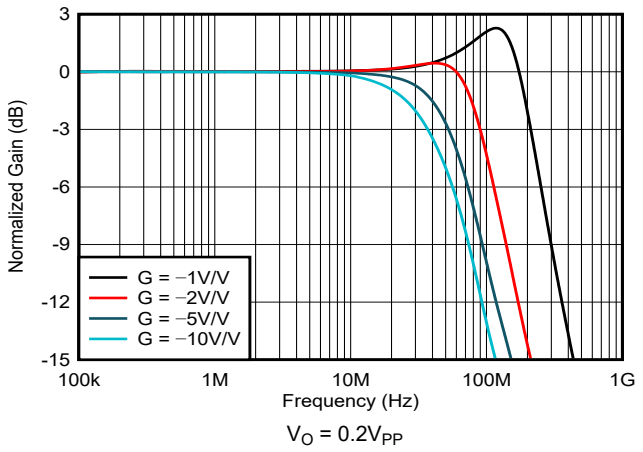

Figure 6-36. Inverting Small-Signal Frequency Response

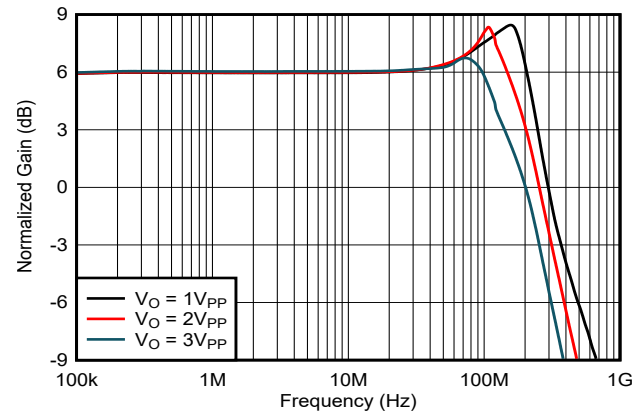

Figure 6-37. Noninverting Large-Signal Frequency Response

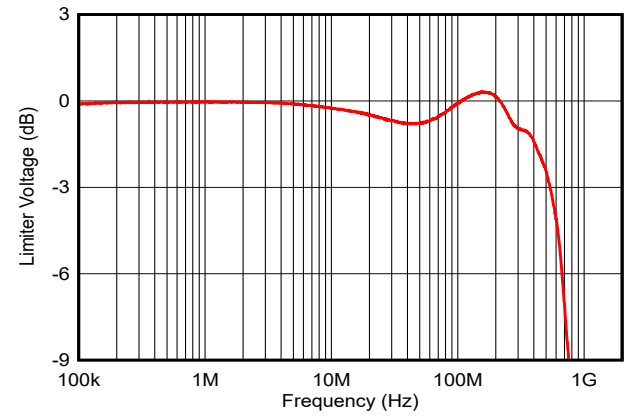

Figure 6-38. V_H—Limiter Small-Signal Frequency Response

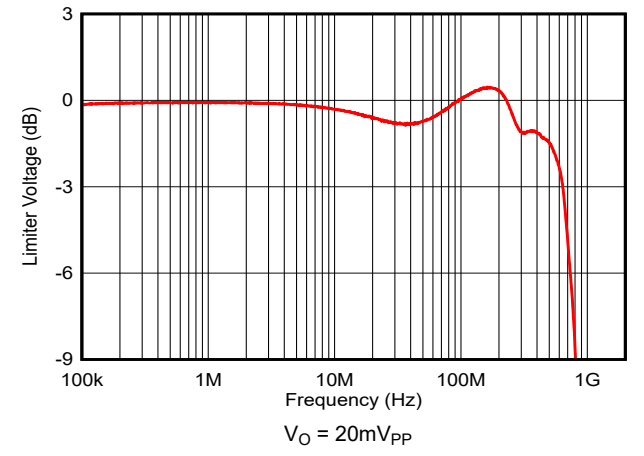

Figure 6-39. V_L—Limiter Small-Signal Frequency Response

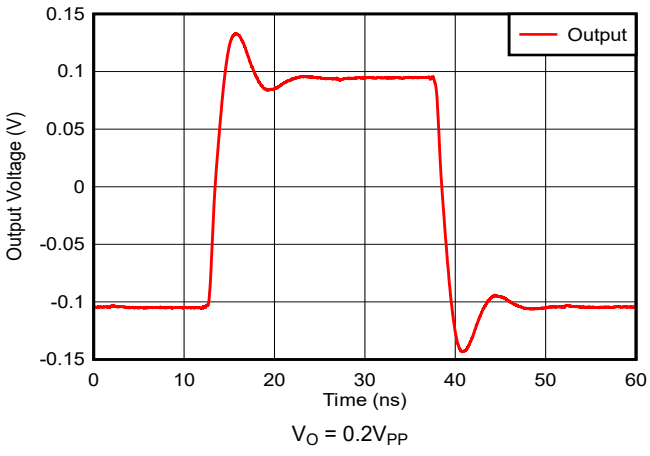

Figure 6-40. Small-Signal Pulse Response

6.8 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω to V_{CM} = 2.5V, V_L = V_{CM} – 1.2V, and V_H = V_{CM} + 1.2V (unless otherwise noted)

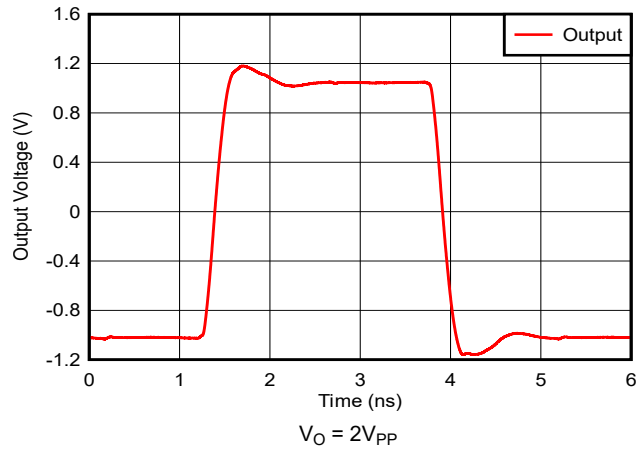

Figure 6-41. Noninverting Large-Signal Step Response

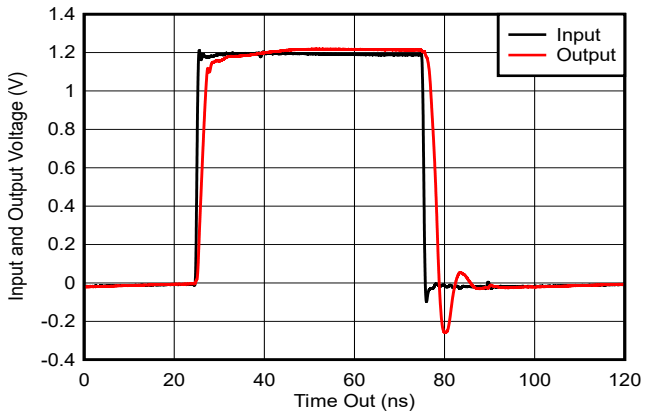

Figure 6-42. V_H- Limiter Pulse Response

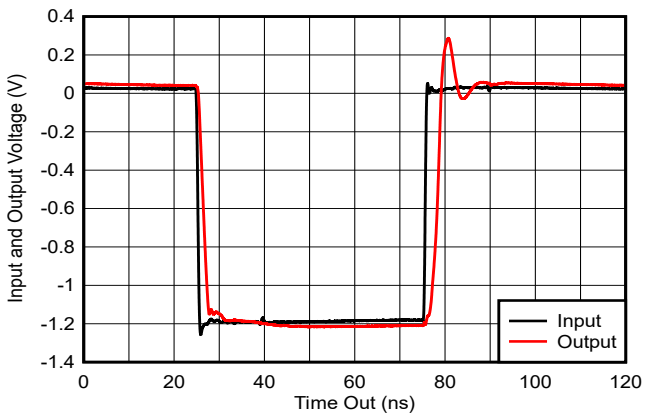

Figure 6-43. V_L- Limiter Pulse Response

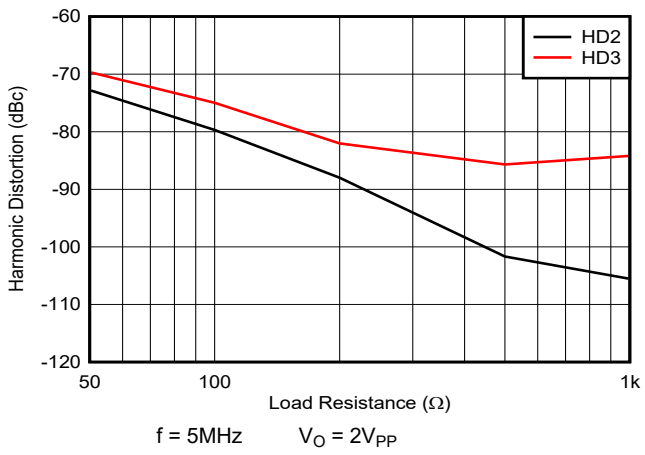

Figure 6-44. Harmonic Distortion vs Load Resistance

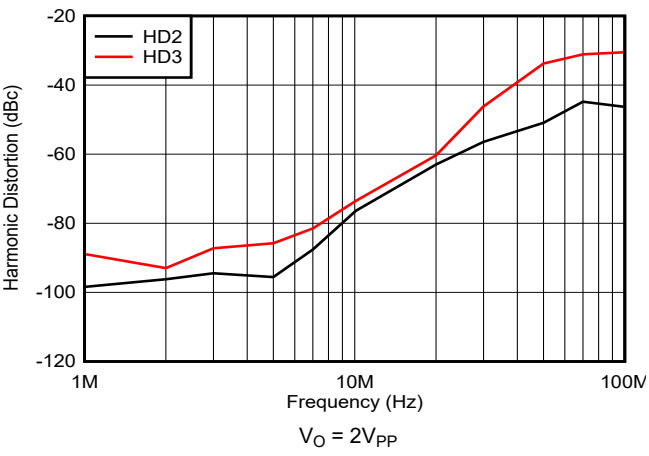

Figure 6-45. Harmonic Distortion vs Frequency

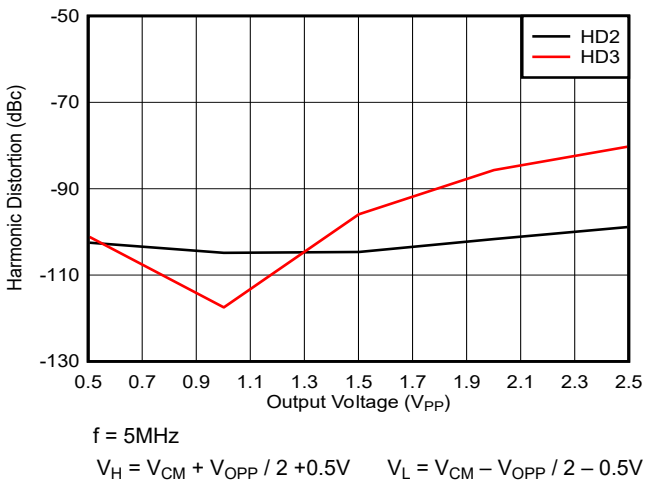

Figure 6-46. Harmonic Distortion vs Output Voltage

6.8 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = 2V/V, R_F = 402Ω, R_L = 500Ω to V_{CM} = 2.5V, V_L = V_{CM} – 1.2V, and V_H = V_{CM} + 1.2V (unless otherwise noted)

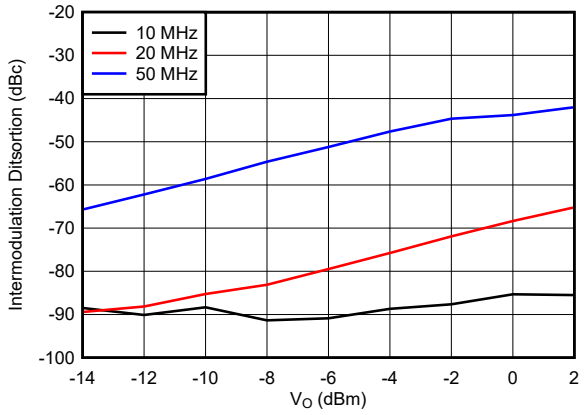

Figure 6-47. 2-Tone, 3rd-Order Intermodulation Intercept

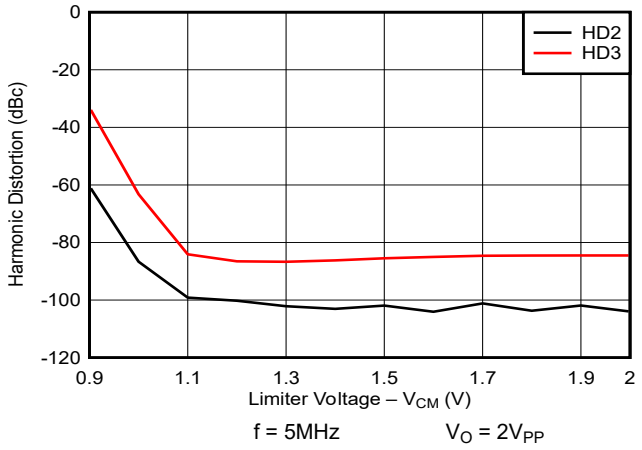

Figure 6-48. Harmonic Distortion Near Limiting Voltages

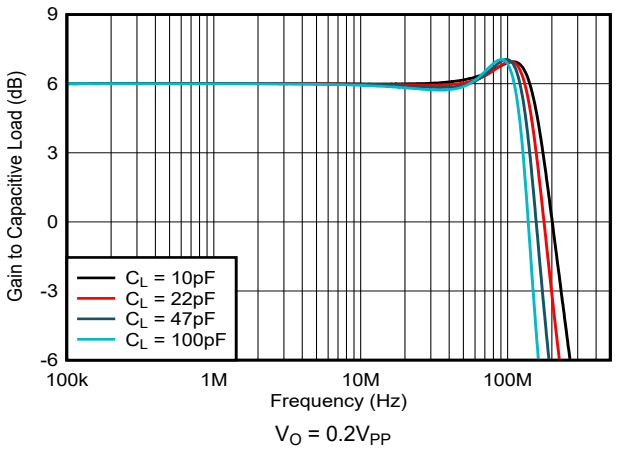

Figure 6-49. Frequency Response vs Capacitive Load

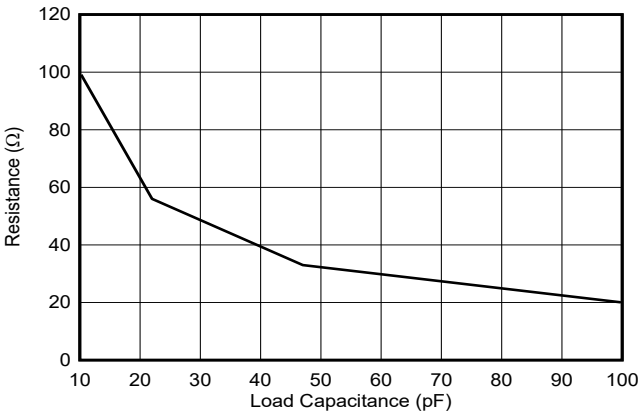

Figure 6-50. Recommended R_S vs Capacitive Load

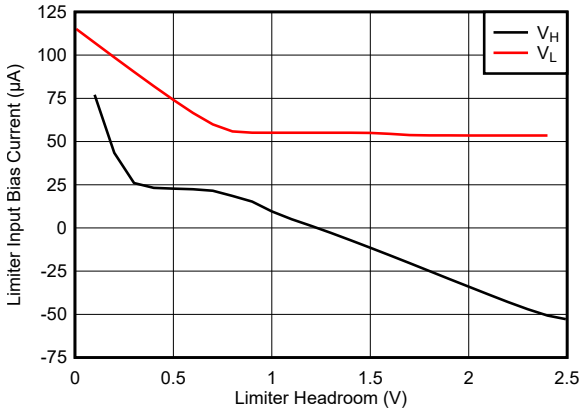

Figure 6-51. Limiter Input Bias Current vs Bias Voltage

7 Detailed Description

7.1 Overview

The OPA698 is a voltage-feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This action from the limiters avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain. The limiters have a very sharp transition from the linear region of operation to output limiting. This transition allows the limiter voltages to be set very near (< 100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Limiters

The output voltage linearly depends on the input voltage when in between limiter voltages V_H (pin 8) and V_L (pin 5). When the output exceeds V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds at V_H or V_L. Accuracy does not change with gain because the limiters act on the output. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30mV of V_H or V_L with no onset of non-linearity. The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S + 0.7V$, $V_H \leq +V_S - 0.7V$), but must also be at least 400mV apart ($V_H - V_L \geq 0.4V$). When pins 5 and 8 are left open, V_H and V_L go to the default voltage limit; the minimum values are given in the *Electrical Characteristics*. Figure 8-1 shows the typical values of limiter input bias current across limiter headroom.

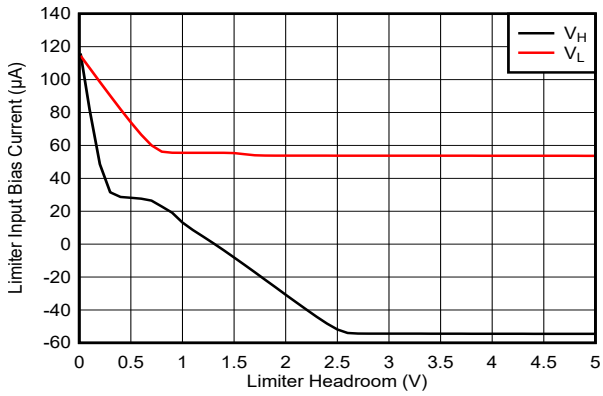

Figure 8-1. Limiter Bias Current vs Bias Voltage

When the limiter voltages are greater than 2.5V from the supplies ($V_L \geq -V_S + 2.5V$ or $V_H \leq +V_S - 2.5V$), use simple resistor dividers to set V_H and V_L (see Figure 8-8). Include the limiter input bias currents (Figure 8-15) in the calculations (that is, I_{VL} = –50µA out of pin 5, and I_{VH} = +50µA out of pin 8). For good limiter voltage accuracy, run at least 1mA quiescent bias current through these resistors. When the limiter voltages must be within 2.5V of the supplies ($V_L \leq -V_S + 2.5V$ or $V_H \geq +V_S - 2.5V$), consider using low-impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This condition is typically the case for single-supply operation (V_S = 5V). Figure 8-9 runs 2.5mA through the resistive divider that sets V_H and V_L. This configuration limits errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages. The limiters dc accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (for example, ±5%). Use a more accurate source, and bypass pins 5 and 8 with good capacitors, to improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors. Other error sources also contribute, but the little impact on the limiters dc accuracy.
- Reduce offsets caused by the limiter input bias currents. Select the resistors in the resistive dividers so that the quiescent bias current is greater than the limiter input bias current.
- Consider the signal path dc errors as contributing to uncertainty in the useable output swing.
- The limiter offset voltage only slightly degrades limiter accuracy. Figure 8-2 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging directly up to the limiter voltages.

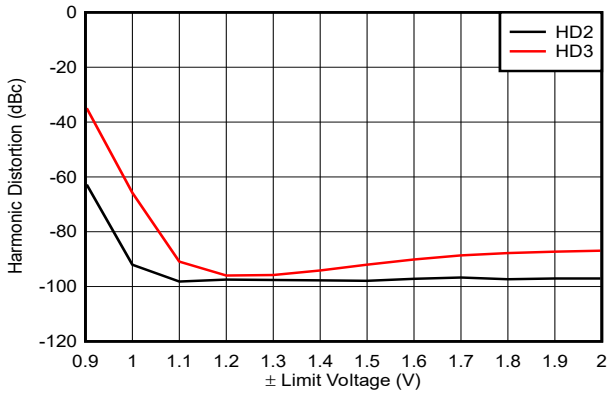

Figure 8-2. Harmonic Distortion Near Limit Voltages

8.1.2 Output Drive

The OPA698 has been optimized to drive 500Ω loads, such as ADCs. This device still performs very well driving 100Ω loads; however, the specifications are shown for the 500Ω load. The OPA698 is an excellent choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. Typical performance curve *Output Impedance vs Frequency* shows that the OPA698 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency because loop gain decreases with frequency.

8.1.3 Thermal Considerations

The OPA698 does not require an additional heat sink under most operating conditions. Maximum desired junction temperature sets a maximum allowed internal power dissipation. Do not exceed the maximum junction temperature of 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the device. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, is at maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S{}^2 / (4R_L)$, where R_L includes the feedback network loading. The power in the output stage, and not in the load, determines internal power dissipation.

The operating junction temperature is $T_J = T_A + P_D \times \theta_{JA}$, where T_A is the ambient temperature. For example, the maximum T_J for a OPA698ID with G = +2, R_F = 402Ω, R_L = 100Ω, and $\pm V_S$ = ±5V at the maximum T_A = +85°C is calculated as:

$$P_{DQ} = \left(10V \times 15.5mA\right) = 155mW \quad (1)$$

$$P_{DL} = \frac{(5V)^2}{4 \times (100\Omega \,||\, 804\Omega)} = 70mW \quad (2)$$

$$P_D = 155mW + 70mW = 225mW \quad (3)$$

$$T_J = 85°C + 225mW \times 118°C/W = 111.6°C \quad (4)$$

This result is the maximum T_J from $V_O = \pm 2.5V_{DC}$. Most applications can be at a lower output stage power and have a lower T_J.

8.1.4 Capacitive Loads

Capacitive loads, such as the input to ADCs, decreases the amplifier phase margin, which can cause high-frequency peaking or oscillations. Figure 8-3 shows how capacitive loads ≥ 2pF can be isolated by connecting a small resistor in series with the output. Increasing the gain from 2V/V improves the capacitive drive capabilities as a result of increased phase margin.

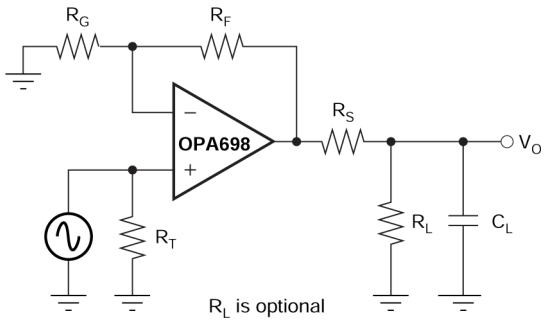

Figure 8-3. Driving Capacitive Loads

In general, minimize capacitive loads for optimized high-frequency performance. The capacitance of coax cable (29pF/ft for RG-58) cannot load the amplifier when the coaxial cable, or transmission line, is terminated in the characteristic impedance.

8.1.5 Frequency Response Compensation

The OPA698 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of 2V/V. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –1V/V is equivalent to a gain of 2V/V for bandwidth purposes (that is, noise gain = 2V/V). Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth is limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This configuration has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high-gain optimized OPA699.

In applications where a large feedback resistor is required, such as a photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth is limited by the pole that the feedback resistor and this capacitor create. In other high-gain applications, use a three-resistor *Tee* network to reduce the RC time constants set by the parasitic capacitances. Be careful not to increase the noise generated by this feedback network too much.

8.1.6 Pulse Settling Time

The OPA698 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve Figure 6-21. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The OPA698 offers excellent pulse settling characteristics when recovering from overdrive.

8.1.7 Distortion

The OPA698 distortion performance is specified for a 500Ω load, such as an ADC. Figure 8-4 illustrates how driving loads with smaller resistance can increase the distortion. Remember to include the feedback network in the load resistance calculations.

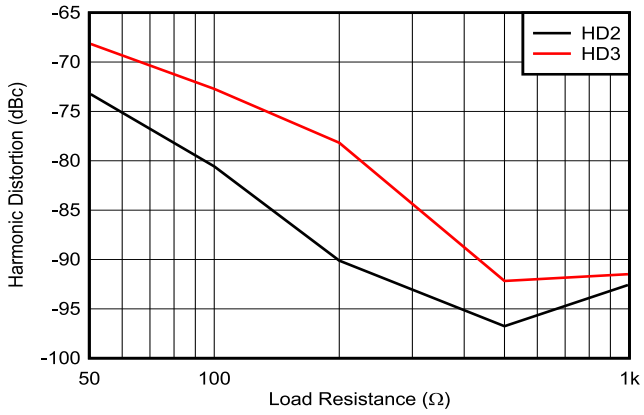

Figure 8-4. 5MHz Harmonic Distortion vs Load Resistance

8.1.8 Noise Performance

High slew rate, unity-gain stable, voltage feedback op amps usually achieve slew rate at the expense of a higher input noise voltage. However, the 4nV/√Hz input voltage noise for the OPA698 is much less than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 8-5 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

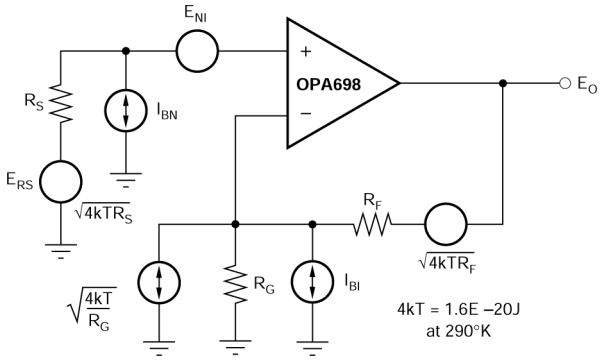

Figure 8-5. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 5 shows the general form for the output noise voltage using the terms shown in Figure 8-6.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (5)$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (6)$$

Evaluating these two equations for the OPA698 circuit and component values (see Figure 8-8) gives a total output spot noise voltage of 9.5nV/√Hz and a total equivalent input spot noise voltage of 4.8nV/√Hz. This total input-referred spot noise voltage is only slightly greater than the 4nV/√Hz specification for the op amp voltage noise alone. The total noise is dominated by the input-referred spot noise of the OPA698 as long as the impedance appearing at each op amp input is limited to a maximum value of 300Ω. Keep both (R_F || R_G) and the noninverting input source impedance less than 300Ω to satisfy both noise and frequency response flatness considerations. The resistor-induced noise is relatively negligible; therefore, additional capacitive decoupling across the bias current cancellation resistor (R_T) for the inverting op amp configuration of Figure 8-10 is not required, but is still desirable.

8.1.9 DC Accuracy and Offset Control

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a large variety of applications. The power-supply current trim for the OPA698 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically ±8µA) at each input pin, use close impedance matching between the input pins to reduce the output dc error caused by this current. The total output offset voltage can be considerably reduced by matching the dc source resistances appearing at the two inputs. This matching reduces the output dc error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 8-8 for a noninverting signal gain (NG) of 2V/V, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$$\pm\left(NG \times V_{OS(max)}\right) \pm \left(R_F \times I_{OS(max)}\right) \quad (7)$$

$$= \pm\left(2 \times 5mV\right) \pm \left(402\Omega \times 1.4\mu A\right) \quad (8)$$

$$= \pm 10.6mV \quad (9)$$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op-amp circuit. Most of these techniques eventually reduce to adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. However, the dc offset voltage on the summing junction sets up a dc current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a dc-coupled inverting amplifier, Figure 8-6 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the dc offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. Using this configuration, the adjustment circuit has minimal effect on the loop gain, as well as the frequency response.

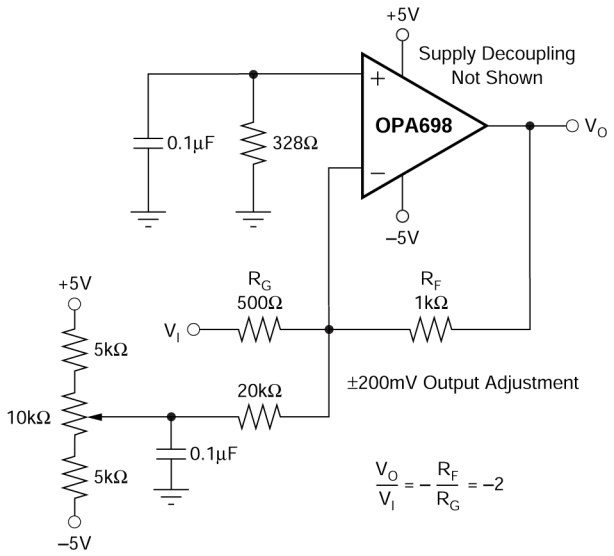

Figure 8-6. DC-Coupled, Inverting Gain of –2, With Offset Adjustment

8.1.10 Input and ESD Protection

CAUTION

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This caution is particularly true for very high-speed, fine-geometry processes. ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this damage can cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA698.

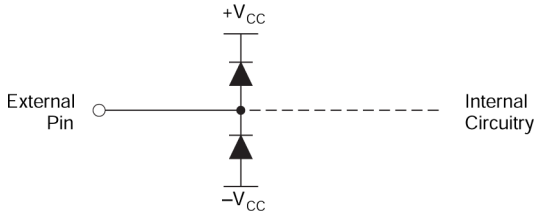

Figure 8-7. Internal ESD Protection

8.2 Typical Applications

8.2.1 Wideband Voltage-Limiting Operation

The OPA698 is a voltage-feedback amplifier that combines features of a wideband, high-slew-rate amplifier with output-voltage limiters. The output swings up to 1V from each rail and delivers up to 190mA. These capabilities makes this device an excellent choice to drive ADCs while adding overdrive protection for the ADC inputs.

Figure 8-8 shows the dc-coupled, gain of 2V/V, dual power-supply circuit configuration used as the basis of the ±5V electrical characteristics and typical characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 500Ω. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 8-8, the total output load is 500Ω || 804Ω = 308Ω. The voltage limiting pins are set to ±2V through a voltage divider network between the $+V_S$ and ground for V_H, and between $-V_S$ and ground for V_L. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. One additional component is included in Figure 8-8. An additional resistor (174Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance directed back towards the signal generator, an input bias current-canceling resistance is obtained that matches the 200Ω source resistance seen at the inverting input; see also Section 8.1.9. The power-supply bypass for each supply in Figure 8-8 consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. Figure 8-8 and Figure 8-9 explicitly show the power-supply bypass capacitors, but is assumed in the other figures. An additional 0.01µF power-supply decoupling capacitor (not shown here) can be included between the two power-supply pins.

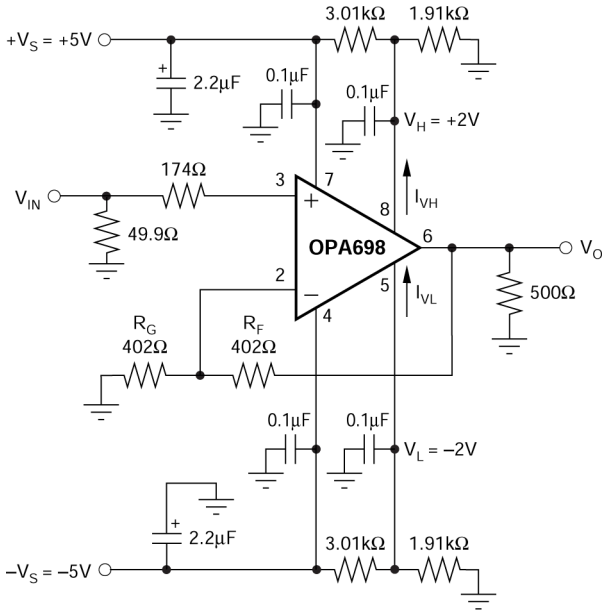

Figure 8-8. DC-Coupled, Dual-Supply Amplifier

8.2.2 Single-Supply, Noninverting Amplifier

Figure 8-9 shows an ac-coupled, noninverting gain amplifier for single 5V supply operation. This circuit was used for ac characterization of the OPA698, with a 50Ω source (that matches) and a 500Ω load. The midpoint reference on the noninverting input is set by two 806Ω resistors. This configuration gives an input bias current-canceling resistance that matches the 402Ω DC source resistance seen at the inverting input (see Section 8.1.9). The power-supply bypass for the supply consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. The power-supply bypass capacitors are shown explicitly in Figure 8-8 and Figure 8-9, but is assumed in the other figures. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. The single-supply circuit can use three resistors to set V_H and V_L, whereas the dual-supply circuit usually uses four resistors to reference the limit voltages to ground. While this circuit shows 5V operation, the same circuit can be used for single supplies up to 12V.

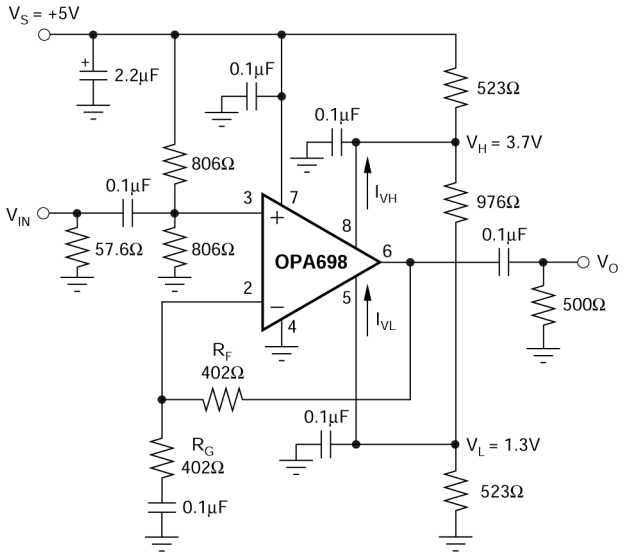

Figure 8-9. AC-Coupled, Single-Supply Amplifier

8.2.3 Wideband Inverting Operation

Operating the OPA698 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance are required. Figure 8-10 shows the inverting gain of –2 circuit used as the basis of the inverting mode typical characteristics.

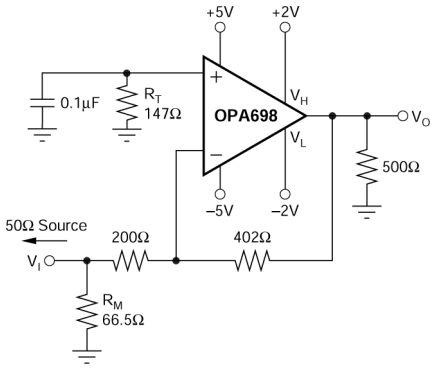

Figure 8-10. Inverting G = –2V/V Specifications and Test Circuit

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. Using the 500Ω load used in the typical characteristics gives a total load of 222Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case, 200Ω for a gain of –2V/V) while an additional input resistor (R_M) can be used to set the total input impedance equal to the source, if desired. In this case, R_M = 66.5Ω in parallel with the 200Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 8-10.

For bias current-cancellation matching, the noninverting input requires a 147Ω resistor to ground. The calculation for this resistor includes a dc-coupled 50Ω source impedance along with R_G and R_M. Although this resistor provides cancellation for the bias current, the circuit must be well-decoupled (0.1µF in Figure 8-10) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 8-10 exceeds the bandwidth at that same gain magnitude for the noninverting circuit of Figure 8-8. This result occurs because of the lower noise gain for the circuit of Figure 8-10 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of –10V/V (R_G = 50Ω, R_M = open, R_F = 500Ω) the noise gain for the circuit of Figure 8-10 is 1 + 500Ω/(50Ω + 50Ω) = 6 due to the addition of the 50Ω source in the noise gain equation. This approach gives considerably higher bandwidth than the noninverting gain of 10V/V. Using the 250MHz gain bandwidth product for the OPA698, an inverting gain of –10V/V from a 50Ω source to a 50Ω R_G gives 52MHz bandwidth; whereas, the noninverting gain of 10V/V gives 28MHz, as shown in Figure 8-11.

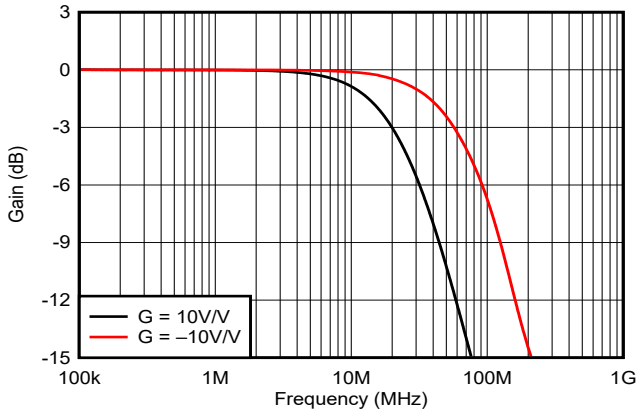

Figure 8-11. G = 10V/V and –10V/V Frequency Response

8.2.4 Limited Output, ADC Input Driver

Figure 8-12 shows a simple ADC driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive. The limiting voltages are set 100mV greater than or less than the corresponding reference voltage from the converter.

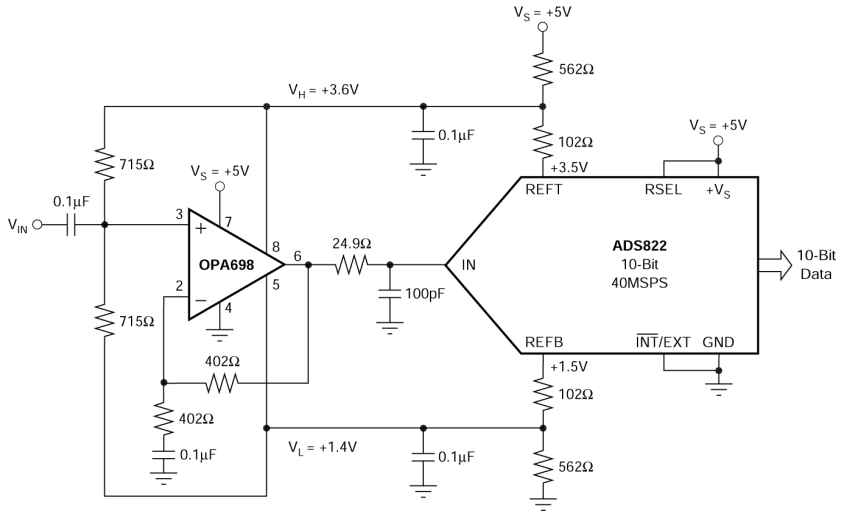

Figure 8-12. Single-Supply, Limiting ADC Input Driver

8.2.4.1 Limited-Output, Differential ADC Input Driver

Figure 8-13 shows a differential ADC driver that takes advantage of the OPA698 limiters to protect the input of the ADC. Two OPA698s are used. The first OPA698 has an inverting configuration at a gain of –2V/V. The second OPA698 has a noninverting configuration at a gain of 2V/V. Each amplifier swings $2V_{PP}$ providing a $4V_{PP}$ differential signal to drive the input of the ADC. Limiters have been set 100mV away from the magnitude of each amplifier maximum signal to provide input protection for the ADC while maintaining an acceptable distortion level.

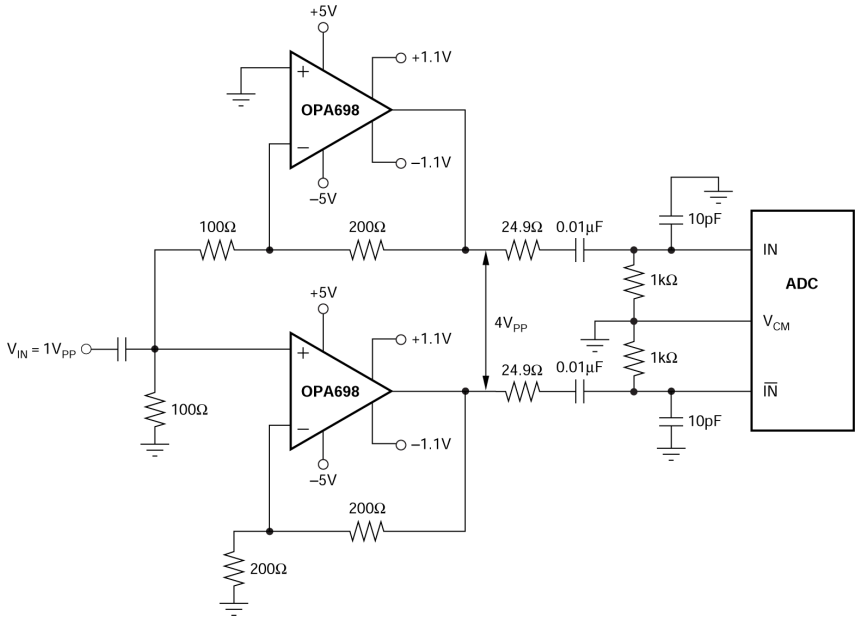

Figure 8-13. Single-to-Differential, AC-Coupled, Output-Limited ADC Driver

8.2.4.2 Precision Half-Wave Rectifier

Figure 8-14 shows a half-wave rectifier with outstanding precision and speed. V_H (pin 8) set to a default voltage between 3.1V and 3.8V if left open, while the negative limit is set to ground.

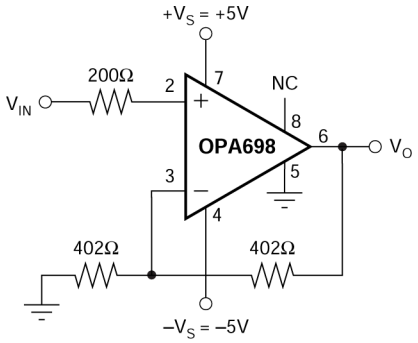

Figure 8-14. Precision Half Wave Rectifier.

The gain for the circuit in Figure 8-14 is set at 2V/V. Figure 8-15 shows a 100MHz sine-wave amplifier, with a gain of 2V/V and rectified.

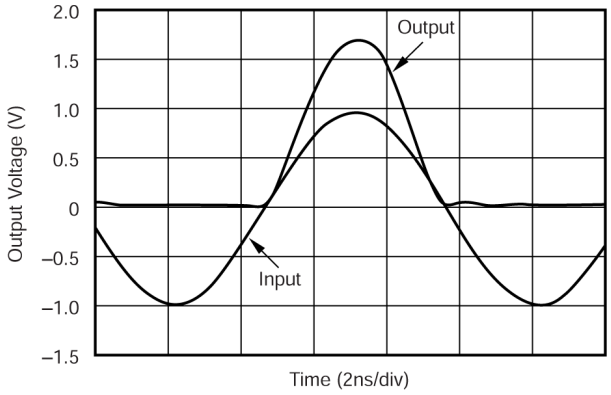

Figure 8-15. 100MHz Sine Wave Rectified

8.2.5 High-Speed Full-Wave Rectifier

There are two methods shown here to build a high-speed full wave rectifier with a limiting amplifier. Use the half-wave rectifier described previously with another amplifier to obtain the full-wave rectified output, or use the input to set the limiting voltage.

8.2.5.1 High-Speed Full-Wave Rectifier #1

The circuit shown in Figure 8-16 uses only one amplifier, in an inverting gain of –1V/V configuration. The upper limiting voltage is left open, resulting in an upper limiting voltage of 3.5V. The lower limiting voltage is connected to the input signal, resulting in the following behavior. When the input voltage is negative, the amplifier is not limiting, resulting in the inversion of the input sine wave to the output. During the positive excursion of the input signal, the output signal is being driven by the limiting input pin. The output is driven from the limiter input pin from positive inputs, the lower slew rate in the input path restricts the application of this approach to lower amplitude, frequencies, or both. Figure 8-17 shows a 2MHz fully rectified sine wave.

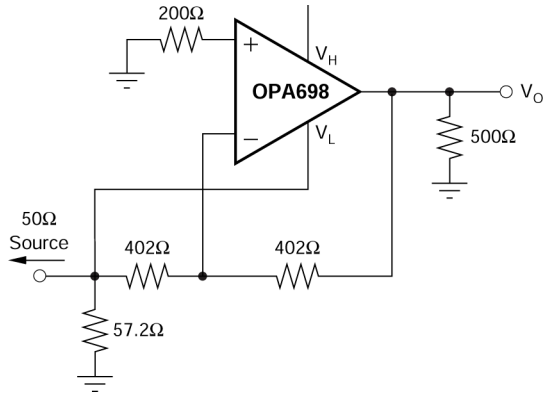

Figure 8-16. High-Speed Full-Wave Rectifier #1

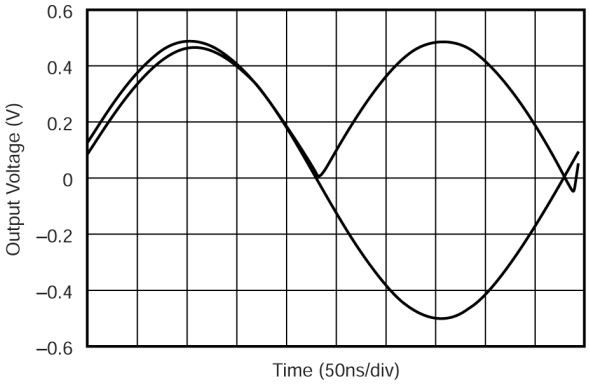

Figure 8-17. Rectified 2MHz Sine Wave

To reach higher frequencies, a second method is recommended.

8.2.5.2 High-Speed Full-Wave Rectifier #2

The circuit shown in Figure 8-18 combines a half-wave rectifier driving the OPA693 in an inverting configuration, while the input signal drives the noninverting input of the fixed gain amplifier OPA693, resulting in a full wave rectifier function. Figure 8-19 shows the results.

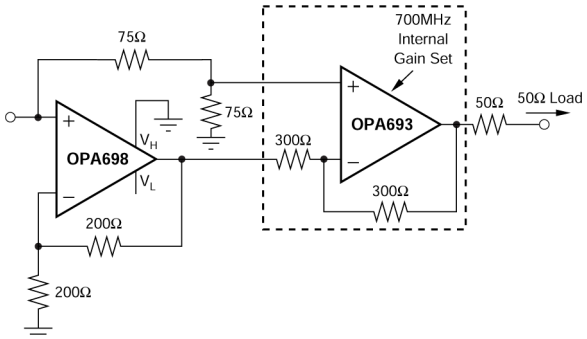

Figure 8-18. High-Speed Full-Wave Rectifier #2

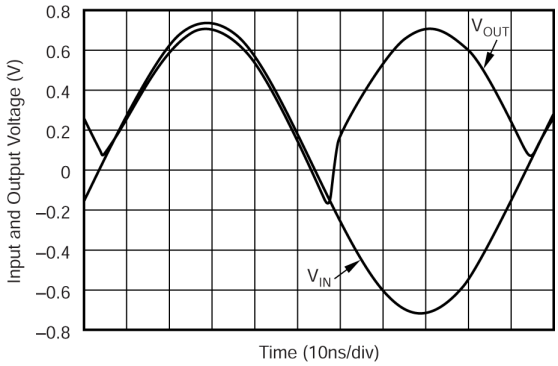

Figure 8-19. Rectified 10MHz Sine Wave

If the negative excursion of the rectified signal is not desired, can easily be removed by replacing the OPA693 with the OPA698 configured as a difference amplifier with V_L connected to ground and V_H left floating.

8.2.6 Soft-Clipping (Compression) Circuit

Figure 8-20 shows a soft-clipping circuit. As soon as the input voltage exceeds either V_{CH} or V_{CL}, the limiting voltages are driven by the following equations:

$$V_H = V_H = \frac{R_2 \times V_{CH} + R_1 \times V_{IN}}{R_1 + R_2} \quad (10)$$

$$V_L = \frac{R_4 \times V_{CL} + R_3 \times V_{IN}}{R_3 + R_4} \quad (11)$$

As the amplifier is operating in the limiting mode, the output voltage is compressed with a gain of R_1+R_2/R_1 for the positive excursion above V_{CH}, and by a gain of R_3+R_4/R_3 for the negative excursion below V_{CL}. Figure 8-21 shows a $5V_{PP}$ on the input being compressed above ±1V with a compression gain of one-third.

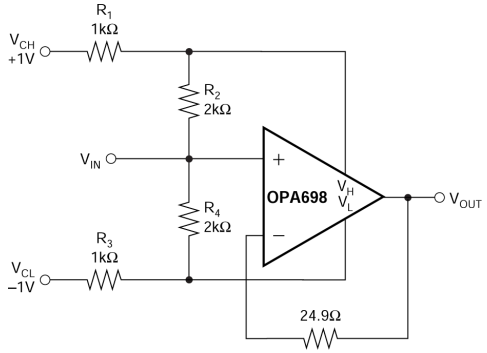

Figure 8-20. Soft-Clipping Circuit

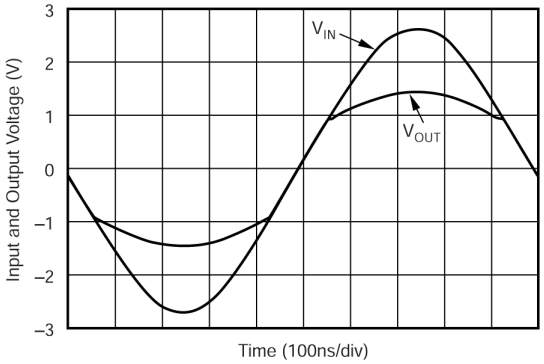

Figure 8-21. Soft Clipping With a Gain of 1/3 Above the Clamp Level (±1V)

8.2.7 Very High-Speed Schmitt Trigger

Figure 8-22 shows a very high-speed Schmitt trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between V_H and V_L. The circuit operates as follows. When the input voltage is less than V_{HL}, then the output is limiting at V_H. When the input is greater than V_{HH} then the output is limiting at V_L, with V_{HL} and V_{HH} defined as:

$$V_{HL,\,HH} = \frac{R_1 \,||\, R_2 \,||\, R_3}{R_1} \times V_{REF} + \frac{R_1 \,||\, R_2 \,||\, R_3}{R_2} \times V_{OUT} \quad (12)$$

Due to the inverting function realized by the Schmitt trigger, V_{HL} corresponds to $V_{OUT} = V_H$, and V_{HH} corresponds to $V_{OUT} = V_L$. Figure 8-23 shows the Schmitt trigger operating with $V_{REF} = 5V$, and gives $V_{HH} = 2.4V$ and $V_{HL} = 1.6V$. The OPA698 propagation delay in a Schmitt-trigger configuration is 6ns from high-to-low and 5ns from low-to-high.

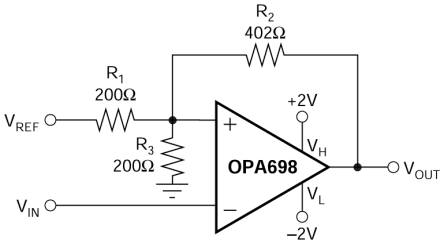

Figure 8-22. Very High-Speed Schmitt Trigger

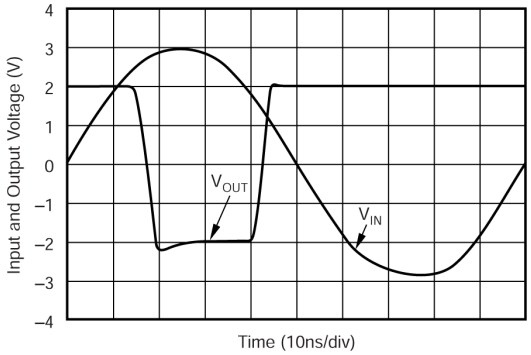

Figure 8-23. Schmitt-Trigger Time-Domain Response for a 10MHz Sine Wave

8.2.8 Unity-Gain Buffer

Figure 8-24 shows a unity-gain voltage buffer using the OPA698. The feedback resistor (R_F) isolates the output from the input capacitance at the inverting input. R_F = 24.9Ω is recommended for unity-gain buffer applications. R_C is an optional compensation resistor that reduces the peaking typically seen at G = 1V/V. Choosing R_C = R_S + R_F gives a unity-gain buffer with approximately the G = 2V/V frequency response. Figure 6-1 shows the frequency response for the circuit of Figure 8-24.

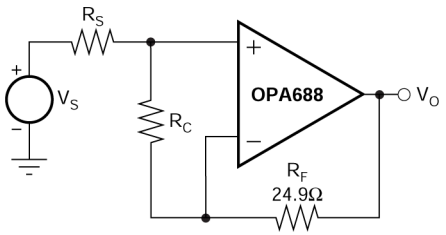

Figure 8-24. Unity-Gain Buffer

8.2.9 DC Restorer

Figure 8-25 shows a dc restore circuit using the OPA698 and OPA660. The buffer element of the OPA660 is used to buffer the input signal while the transconductance element is used to restore the dc level after the decoupling capacitor C_1. The dc level is set using R_1 and R_2. The OPA698 is configured at a gain of 2V/V to compensate for the 75Ω series into a 75Ω load. The OPA698 also limits the output to ground.

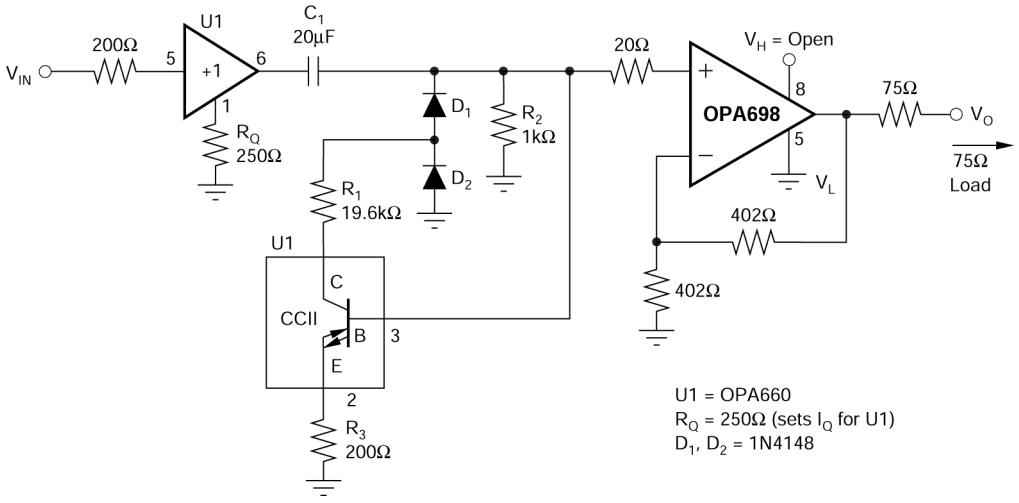

Figure 8-25. DC Restore to Ground

8.2.10 Video Sync Stripper

Figure 8-26 shows a sync stripper using two OPA698 output-limiting op amps. One OPA698 is configured as a limiting inverting comparator. Referred to the input, the negative excursions lower than –0.2V are clipped to ground, and all excursions greater than –0.2V generate an output voltage set by the default limiting value (–3.5V). The second OPA698 is using this waveform to effectively remove the sync pulse from the video signal.

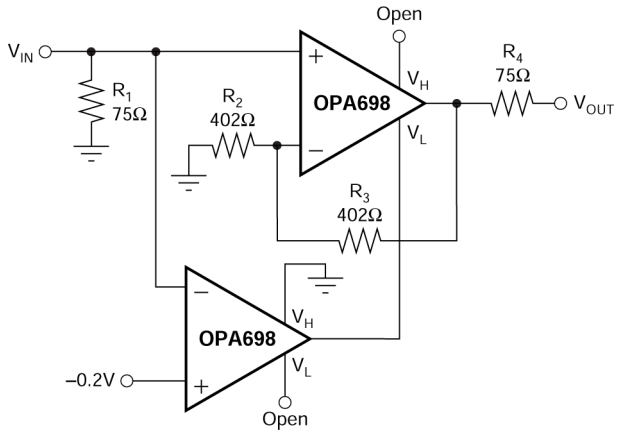

Figure 8-26. Sync Stripper Circuit

8.3 Power Supply Recommendations

The OPA698 is nominally specified for operation using either ±5V supplies or a single 5V supply. The maximum specified total supply voltage of 12V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement can allow design of nonstandard or single-supply operation circuits. Figure 8-9 shows one approach to single-supply operation.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimum performance with the high-frequency OPA698 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

1. **Minimize parasitic capacitance to any ac ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.
2. **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high frequency 0.1µF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2µF to 6.8µF) high-frequency decoupling capacitors to bypass lower frequencies, which can be some-what further from the device, and be shared among several adjacent devices.
3. **Place external components close** to the OPA698. This placement minimizes inductance, ground loops, transmission line effects, and propagation delay problems. Be extra careful with the feedback (R_F), input, and output resistors.
4. **Use high-frequency components** to minimize parasitic elements. Resistors can be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when leads are as short as possible. Never use wire-wound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitance and inductance. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use R_F type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2µF to 6.8µF) can be tantalum for better high-frequency and pulse performance.

5. **Choose low resistor values** to minimize the time constant set by the resistor and the parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this capacitance adds a pole, zero less than 500MHz, or both. Ensure that the output loading is not too heavy. The recommended 402Ω feedback resistor is a good starting point in most designs.
6. **Use short direct traces to other wide-band devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) can be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve, *RS vs Capacitive Load*. Parasitic loads < 2pF can not need the isolation resistor.
7. **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for micro-strip and strip line layout techniques). A 50Ω transmission line is not required on board—a higher characteristic impedance helps reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This configuration isolates the source from the reactive load presented by the line, but the frequency response is degraded. Multiple destination devices are best handled as separate transmission lines, each with a series source and shunt load termination. Any parasitic impedance acting on the terminating resistors alters the transmission line match, and can cause unwanted signal reflections and reactive loading.
8. **Do not use sockets** for high-speed parts such as the OPA698. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Demonstration Fixture

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA698. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. Table 9-1 shows the summary information for this fixture.

Table 9-1. Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA698ID	SO-8	DEM-OPA-SO-1A	SBOU009

This demonstration fixture can be requested at the Texas Instruments web site through the OPA698 product folder.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2008) to Revision E (April 2025) — **Page**

- Updated *Features*, *Applications*, and *Description* sections and with die redesign specifications; for updated specifications, see the *Specifications* section....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added *Pin Configuration and Functions* 2
- Changed the supply voltage specification from ±6.5V to 13V in *Absolute Maximum Ratings* 3
- Updated the table note in *Absolute Maximum Ratings* to add clarification....3

- Added Supply turn-on and turn-off rate and Continuous input current to *Absolute Maximum Ratings* 3
- Deleted soldering flow specification from *Absolute maximum specifications* 3
- Deleted machine model (MM) specification from *ESD Ratings* 3
- Added *Recommended Operating Conditions* 3
- Deleted minimum and overtemperature specifications in both *Electrical Characteristics AC Performance* 4
- Updated test conditions to both *Electrical Characteristics* for added clarity..... 4
- Updated table format for both *Electrical Characteristics* 4
- Deleted T_A = 0°C to +70°C specifications from all *Electrical Characteristics* 4
- Deleted Test Level column from all *Electrical Characteristics* 4
- Changed SSBW at G = 1V/V from 450MHz to 650MHz..... 4
- Added T_A = 25°C to the default test conditions to both *Electrical Characteristics*..... 4
- Updated *AC Performance* section with improved typical small signal bandwidth, slew rate, voltage noise, current noise, and distortion values in both *Electrical Characteristics* 4
- Changed Gain bandwidth product from 250MHz to 300MHz..... 4
- Changed typical Peaking at a gain of 1V/V from 5dB to 1.5dB..... 4
- Changed typical Slew rate from 1100V/µs to 1800V/µs..... 4
- Changed Rise and fall time at V_O = 0.2V Step from 1.6ns to 1.4ns..... 4
- Changed Settling time from 8ns to 25ns..... 4
- Changed typical 2nd-order harmonic distortion at R_L = 500Ω from –74dBc to –94dBc..... 4
- Deleted Differential gain and Differential phase specifications..... 4
- Changed typical 3rd-order harmonic distortion at R_L = 500Ω from –87dBc to –85dBc..... 4
- Changed typical Open-loop voltage gain from 63dB to 80dB..... 4
- Changed typical Input bias current from 3µA to ±0.2µA and Input offset current from ±0.3µA to ±0.1µA..... 4
- Changed typical Common-mode rejection ratio from 61dB to 82dB..... 4
- Changed Input impedance Differential-mode from 0.32 || 1MΩ || pF to 1 || 0.3MΩ || pF..... 4
- Changed the typical Input impedance common-mode from 3.5 || 1MΩ || pF to 33 || 1.4MΩ || pF..... 4
- Changed Current output sourcing and sinking from 120mA and –120mA to +190mA and –190mA..... 4
- Changed maximum Limiter input bias current magnitude, T_A = –40°C to +85°C from 64µA to 65µA..... 4
- Changed the typical Limiter input impedance from 3.4 || 1 MΩ || pF to 10 || 0.85 MΩ || pF..... 4
- Changed typical Limiter feedthrough from –68dB to –95dB..... 4
- Changed typical Limiter offset ±5mV from ±10mV..... 4
- Changed Op amp input bias current shift from 3µA to 0.15µA..... 4
- Changed Limiter small signal bandwidth from 600MHz to 700MHz..... 4
- Changed Limiter slew rate from 125V/µs to 175V/µs 4
- Changed maximum and minimum Quiescent current from 15.9mA to 17.3mA and 15.2mA to 13.8mA..... 4
- Changed minimum and maximum Quiescent current, T_A = –40°C to +85°C from 16.6mA to 17.7mA and 14.6mA to 13.4mA..... 4
- Changed typical Power-supply rejection ratio from 75dB to 90dB..... 4
- Moved *Thermal Characteristics* to *Thermal Information* table and *Recommended Operating Conditions* table 4
- Changed SSBW at G = 1V/V from 375MHz to 550MHz..... 6
- Changed Gain bandwidth product from 230MHz to 300MHz..... 6
- Changed typical Bandwidth for 0.1dB gain flatness typical value from 30MHz to 26MHz..... 6
- Changed typical Peaking at a gain of 1V/V from 7dB to 2.5dB..... 6
- Changed Rise and fall time at V_O = 0.2V step from 1.9ns to 1.4ns..... 6
- Changed Settling time from 12ns to 28ns..... 6
- Changed typical 2nd-order harmonic distortion at R_L = 500Ω from 69dBc to –95dBc..... 6
- Changed typical 3rd-order harmonic distortion at R_L = 500Ω from 73dBc to –81dBc..... 6
- Changed the typical Input voltage noise from 5.7nV/√Hz to 4nV/√Hz..... 6
- Changed the typical Input current noise from 2.3pA/√Hz to 1.4pA/√Hz..... 6
- Changed typical Open-loop voltage gain from 60dB to 77dB..... 6
- Changed typical Input bias current from ±3µA to ±0.5µA and Input offset current from ±0.4µA to ±0.1µA..... 6
- Changed typical Common-mode rejection ratio from 58dB to 82dB..... 6
- Changed Input impedance Differential-mode from 0.32 || 1 MΩ || pF to 0.77 || 0.3 MΩ || pF..... 6

- Changed the typical Input impedance common-mode from 3.5 || 1 MΩ || pF to 24 || 1.5MΩ || pF....6
- Changed Current output Sourcing and sinking from 70mA and –70mA to 170mA and –170mA....6
- Changed the typical closed-loop output impedance from 0.2Ω to 0.1Ω....6
- Changed Limiter Input Bias Current Magnitude from 16µA to 8µA....6
- Changed Limiter input impedance from 3.4 || 1 MΩ || pF to 1 || 7 MΩ || pF....6
- Changed typical Limiter feedthrough from –60dB to –92dB....6
- Deleted Bias current shift specification....6
- Changed Limiter small signal bandwidth from 450MHz to 515MHz....6
- Changed Limiter slew rate from 100V/µs to 150V/µs....6
- Changed Limited step response overshoot from 55mV to 40mV....6
- Changed Limited step response recovery time from 3ns to 2.5ns....6
- Changed maximum Quiescent current from 14.9mA to 17.2mA....6
- Changed typical quiescent current from 14.3mA to 15.6mA....6
- Changed maximum quiescent current, T_A = –40°C to +85°C from 15.3mA to 17.6mA....6
- Changed typical Power-supply rejection ratio from 70dB to 85dB....6
- Updated *Typical Characteristics: V_S = ±5V* with new die characteristics....8
- Updated *Typical Characteristics: V_S = 5V* with new die characteristics....14
- Updated *Typical Application* with data from *Electrical* and *Typical Characteristics* 23

Changes from Revision C (March 2006) to Revision D (December 2008)	Page
• Changed minimum Storage temperature range from −40°C to −65°C	3

Changes from Revision B (September 2003) to Revision C (March 2006)	Page
• Changed board part number in the *Demonstration Fixture* section	33

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA698ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 698
OPA698IDG4	NRND	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA698IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 698
OPA698IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 698
OPA698IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 698

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA698 :

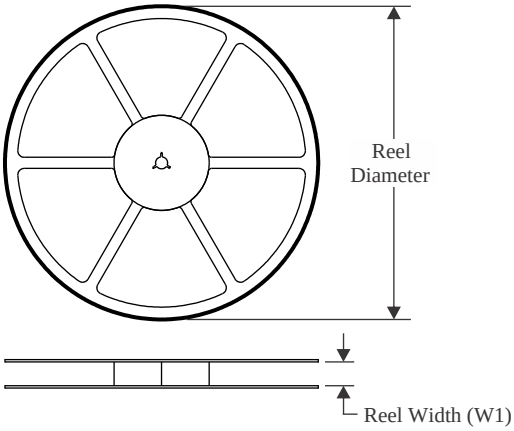
- Military : OPA698M

NOTE: Qualified Version Definitions:

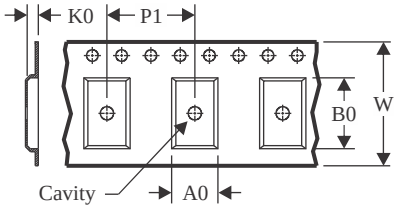
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

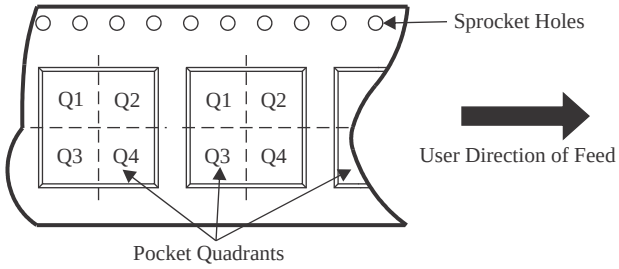


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

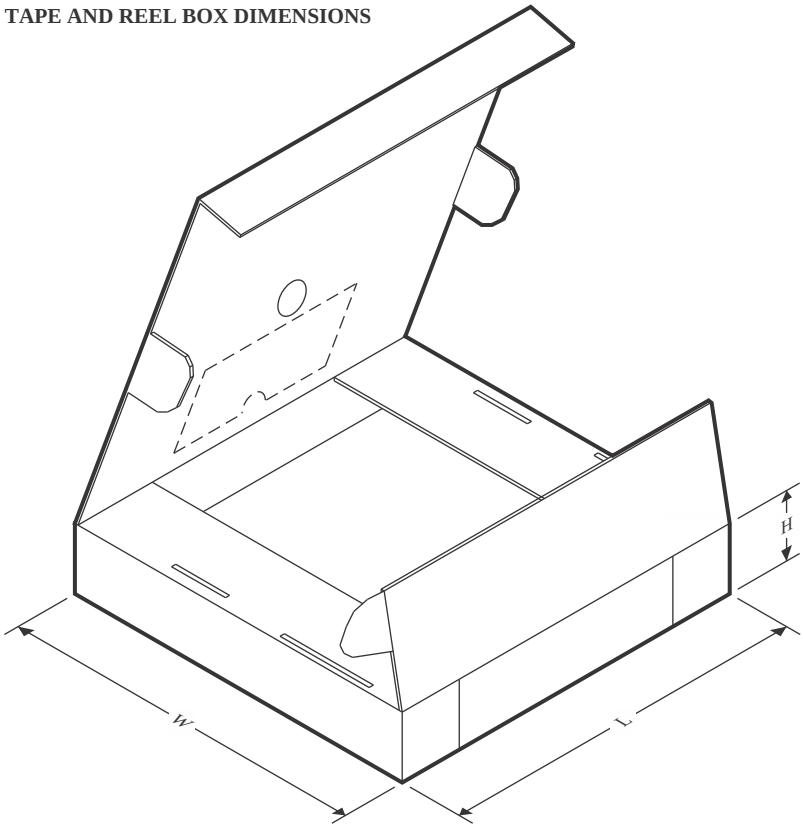
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

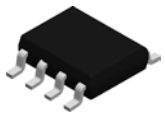
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA698IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA698IDR	SOIC	D	8	2500	353.0	353.0	32.0

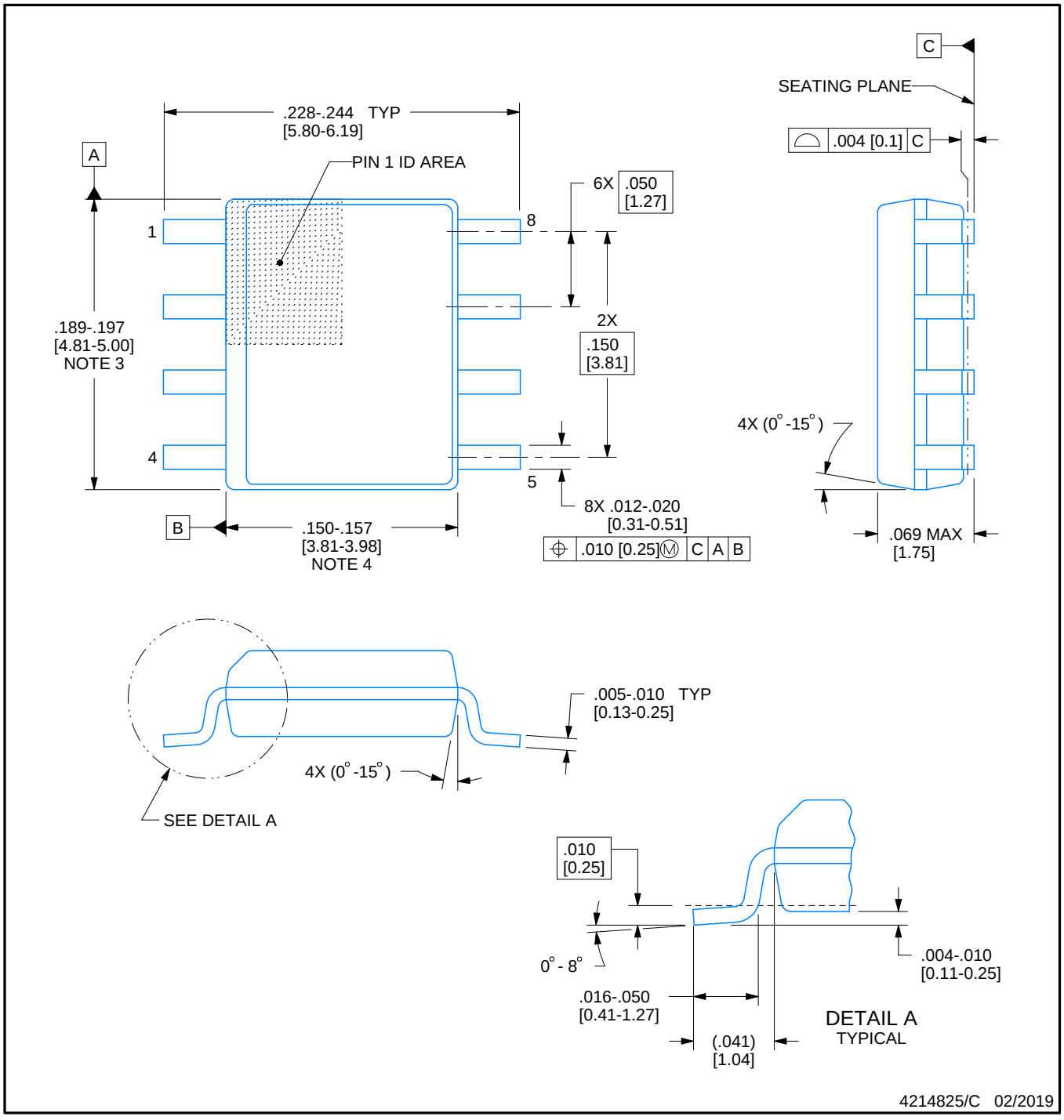


PACKAGE OUTLINE

D0008A

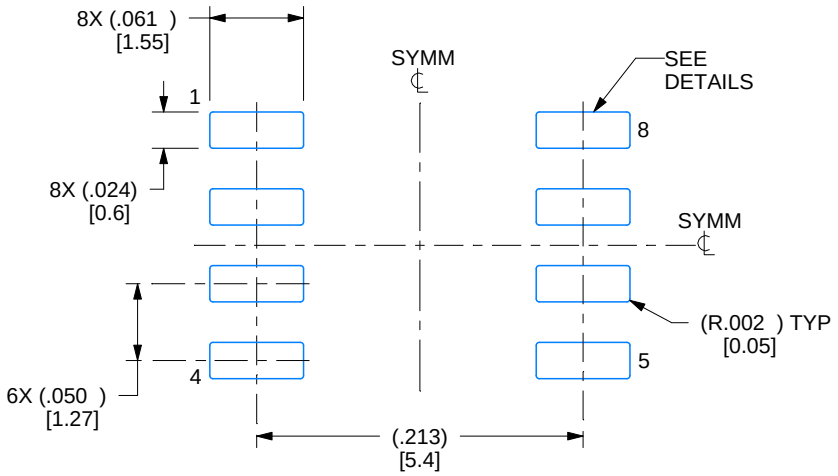
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

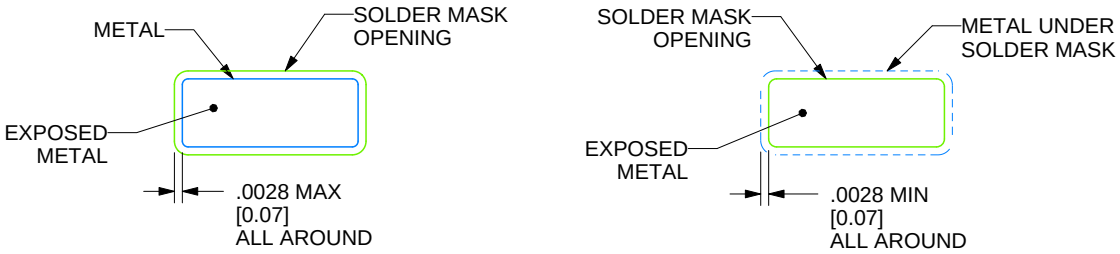


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

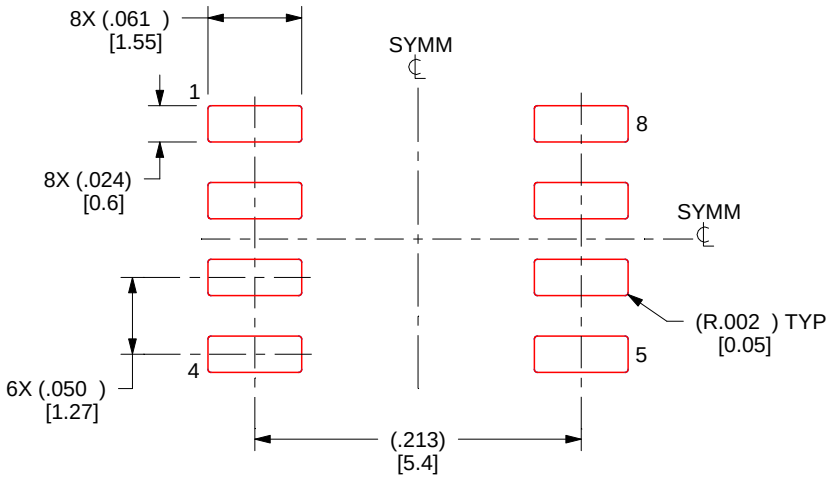
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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