SBOS287A – JUNE 2005 – REVISED SEPTEMBER 2005

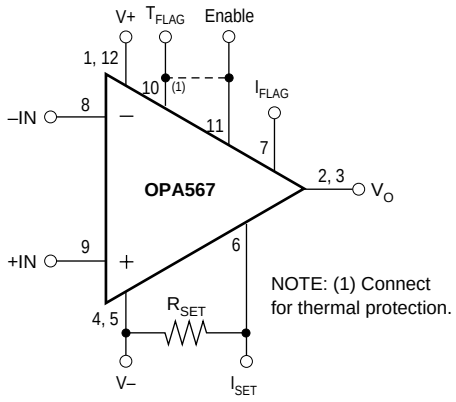
Rail-to-Rail I/O, 2A POWER AMPLIFIER

FEATURES

- **HIGH OUTPUT CURRENT: 2A**
- **OUTPUT SWINGS TO: 150mV of Rails with I_O = 2A**
- **THERMAL PROTECTION**
- **ADJUSTABLE CURRENT LIMIT**
- **TWO FLAGS: Current Limit and Temperature Warning**
- **LOW SUPPLY VOLTAGE OPERATION: 2.7V to 5.5V**
- **SHUTDOWN FUNCTION WITH OUTPUT DISABLE**
- **SMALL POWER PACKAGE**

APPLICATIONS

- **THERMOELECTRIC COOLER DRIVER**
- **LASER DIODE PUMP DRIVER**
- **VALVE, ACTUATOR DRIVER**
- **SYNCHRO, SERVO DRIVER**
- **TRANSDUCER EXCITATION**
- **GENERAL LINEAR POWER BOOSTER FOR OP AMPS**



DESCRIPTION

The OPA567 is a low-cost, high-current, operational amplifier designed for driving a wide variety of loads while operating on low-voltage supplies. It operates from either single or dual supplies for design flexibility and has rail-to-rail swing on the input and output. Output swing is within 300mV of the supply rails, with output current of 2A. Smaller loads allow an output swing closer to the rails.

The OPA567 is unity gain stable, easy to use, and free from the phase inversion problems found in some power amplifiers. High performance is maintained at voltage swings near the output rails.

The OPA567 provides an accurate user-selected current limit set with an external resistor, or digitally adjusted via a Digital-to-Analog Converter (DAC).

The output of the OPA567 can be independently disabled using the Enable pin. This feature saves power and protects the load.

Two flags are provided. The current limit flag, I_{FLAG}, warns of current limit conditions. T_{FLAG} is a thermal flag that warns of thermal overstress. The T_{FLAG} pin can be connected to the Enable pin to provide a thermal shutdown solution.

The OPA567 is available in a tiny 5mm x 5mm Quad Flatpack No-lead (QFN) package and features an exposed thermal pad that enhances thermal and electrical characteristics. It is small and easy to heat sink. The OPA567 is specified for operation over the industrial temperature range, –40°C to +85°C.

OPA567 RELATED PRODUCTS

FEATURES	PRODUCT
Same features as the OPA567, plus current monitor output and paralleling ability in SO-20 PowerPAD™ package.	**OPA569**

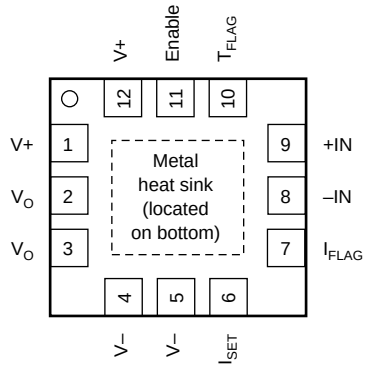
ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7.5V
Output Current	See SOA Curves
Signal Input Terminals (pins 8 and 9):	
Voltage(2)	(V–) – 0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit(3)	Continuous when thermal protection enabled
Enable Pin (pin 11)	(V–) – 0.5V to (V–) + 7.5V
Current Limit Set, I_{LIMIT} Pin (pin 6)	(V–) – 0.5V to (V+) + 0.5V
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
ESD Rating:	
Human Body Model	3kV
Charged Device Model	1500V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground.

PIN CONFIGURATION

Top View **QFN**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1, 12	V+	Positive Power-Supply Voltage
2, 3	V_O	Output
4, 5	V–	Negative Power-Supply Voltage
6	I_{SET}	Current Limit Set Pin(1)
7	I_{FLAG}	Current Limit Flag—Indicates when part is in current limit (active LOW).
8	–IN	Inverting Input
9	+IN	Noninverting Input
10	T_{FLAG}	Thermal Flag—Indicates thermal stress (active LOW).
11	ENABLE	Enabled HIGH, shut down LOW.

NOTE: (1) This pin limits the output current. The limited value, I_{LIMIT}, is 9800(I_{SET}), where I_{SET} is the current flowing through the I_{SET} pin. This current is programmed by the resistor R_{SET} connected to V–.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_{CASE} = +25°C, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA567 MIN	OPA567 TYP	OPA567 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	I_O = 0V, V_S = +5V		±0.5	±2	mV
vs Temperature	**dV_{OS}/dT**	**T_A = –40°C to +85°C**		**±1.3**		**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = (V–) +0.55V		12	60	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±1	±10	pA
vs Temperature				**(doubles every 10°C)**		
Input Offset Current	I_{OS}			±2	±10	pA
NOISE						
Input Voltage Noise Density, f = 1kHz	e_n			12		nV/√Hz
f = 0.1Hz to 10Hz				8		μV_{PP}
Current Noise Density, f = 1kHz	i_n			0.6		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	Linear Operation	(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = +5V, –0.1V < V_{CM} < 3.2V	80	100		dB
		V_S = +5V, –0.1V < V_{CM} < 5.1V	60	80		dB
INPUT IMPEDANCE						
Differential				10^{13} || 4.5		Ω || pF
Common-Mode				10^{13} || 9		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	0.2V < V_O < 4.8V, R_L = 1kΩ, V_S = +5V	100	126		dB
		0.3V < V_O < 4.7V, R_L = 1.15Ω, V_S = +5V		90		dB
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBW			1.2		MHz
Slew Rate	SR	G = +1, V_O = 4.0V Step		1.2		V/µs
Full-Power Bandwidth(1)				See Typical Characteristics		
Settling Time: ±0.1%		G = –1, V_O = 4.0V Step		5		µs
Total Harmonic Distortion + Noise(2)	THD+N			See Typical Characteristics		
OUTPUT						
Voltage Output Swing from Rail	V_O	R_L = 1kΩ, A_{OL} > 100dB	(V–) + 0.2	(V_S) ± 0.02	(V+) – 0.2	V
		I_O = ±2A, V_S = +5V, A_{OL} > 80dB(3)	(V–) + 0.3	(V_S) ± 0.2	(V+) – 0.3	V
Maximum Continuous Current Output: dc(4)					2.4	A
Capacitive Load Drive(5)	C_{LOAD}			See Typical Characteristics		
Closed-Loop Output Impedance(6)	R_O	G = 1, dc		0.1		Ω
		G = 1, f = 10kHz		0.44		Ω
		G = 1, f = 1.2MHz		45		Ω
Output Disabled Output Impedance				12M || 570		Ω || pF
CURRENT LIMIT (I_{SET} Pin)						
Output Current Limit(7)		Externally Adjustable		±0.2 to ±2.2		A
Current Limit Equation(8)				$I_{LIMIT} = I_{SET} \bullet 9800$		A
R_{SET} Equation				$R_{SET} = 9800\ (1.18V/I_{LIMIT})$		Ω
Current Limit Tolerance(8), Positive		I_{LIMIT} = 1A		±3	±10	%
Negative		I_{LIMIT} = 1A		±3	±15	%
V_{SET} Tolerance(9)			(V–) + 1.05	(V–) + 1.18	(V–) + 1.3	V
ENABLE/SHUTDOWN INPUT						
Enable Pin Bias Current		V_{SD} = 0V		0.2		µA
HIGH (Output enabled)	V_{SD}	Pin Open or Forced HIGH	(V–) + 2.5			V
LOW (Output disabled)	V_{SD}	Pin Forced LOW			(V–) + 0.8	V
Output Disable Time		R_L = 1Ω		0.5		µs
Output Enable Time		R_L = 1Ω		15		µs

NOTES:
(1) See typical characteristic, *Maximum Output Voltage vs Frequency*.
(2) See typical characteristic, *Total Harmonic Distortion + Noise vs Frequency*.
(3) Swing to the rail is measured in final test. Under those conditions, the A_{OL} is derived from characterization.
(4) See Safe Operating Area (SOA) plots.
(5) See typical characteristic, *Overshoot vs Load Capacitance*.
(6) See the *Typical Characteristics* section. Higher frequency output impedance can affect frequency stability.
(7) External current limit setting resistor is required; see Figure 1.
(8) I_{LIMIT} is the value of the desired current limit and is equal to 9800(I_{SET}), where I_{SET} is the current through the I_{SET} pin. I_{LIMIT} tolerance is proportional to the ratio of I_{LIMIT}/I_{SET}. Errors from this parameter can be calibrated out—see the *Applications Information* section.
(9) V_{SET} is a voltage reference that equals the difference between the voltage of the I_{SET} pin and V–, and is referenced to the negative rail. Errors from this parameter can be calibrated out—see the *Applications Information* section.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (Cont.)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_{CASE} = +25°C, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

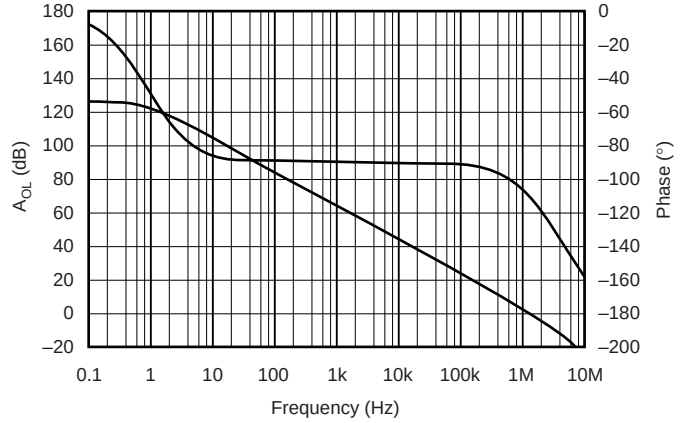
PARAMETER	CONDITION	OPA567 MIN	OPA567 TYP	OPA567 MAX	UNITS
THERMAL FLAG PIN (T_{FLAG})					
Junction Temperature: T_J					
Alarm (thermal status pin Low)	Thermal overstress		+147		°C
Return to normal operation (Thermal Flag pin High)	Normal operation		+130		°C
Thermal Flag Pin Voltage					
During normal operation	T_{FLAG} pin sourcing 25µA	(V+) – 0.8V	V+		V
During thermal overstress	T_{FLAG} pin sinking 25µA		V–	(V–) + 0.8	V
CURRENT LIMIT FLAG PIN (I_{FLAG})					
Current Limit Flag Pin Voltage					
During normal operation	I_{FLAG} pin sourcing 25µA	(V+) – 0.8V	V+		V
During current limit	I_{FLAG} pin sinking 25µA		V–	(V–) + 0.8	V
POWER SUPPLY					
Specified Voltage Range V_S		+2.7		+5.5	V
Operating Voltage Range		+2.5		+5.5	V
Quiescent Current(10) I_Q	I_O = 0, I_{LIMIT} = 200mA, V_S = 5V		+3.4	+6	mA
	I_O = 0, I_{LIMIT} = 2A, V_S = 5V		+9	+11	mA
Quiescent Current in Shutdown Mode	I_O = 0, V_{SD} = 0.8V, V_S = 5V		+0.01		mA
TEMPERATURE RANGE					
Specified Range	Junction Temperature	–40		+85	°C
Operating Range	Junction Temperature	–55		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance: Junction-to-Case θ_{JC}			6		°C/W
Junction-to-Ambient θ_{JA}			38		°C/W

NOTES: (10) Quiescent current is a function of the current limit setting. See *Adjustable Current Limit and Current Limit Flag Pin* in the *Applications Information* section.

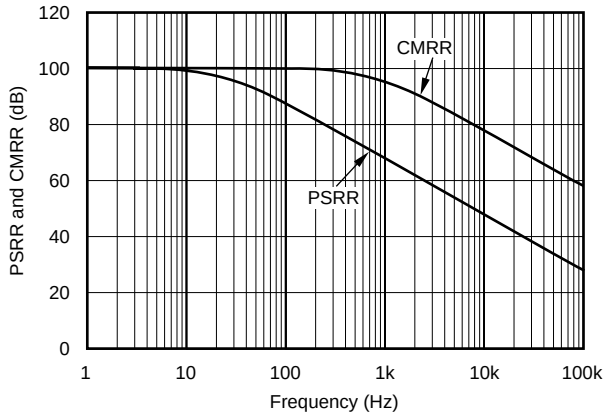
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, unless otherwise noted.

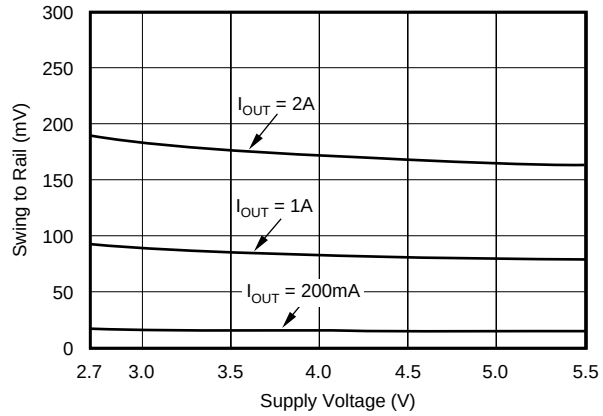
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



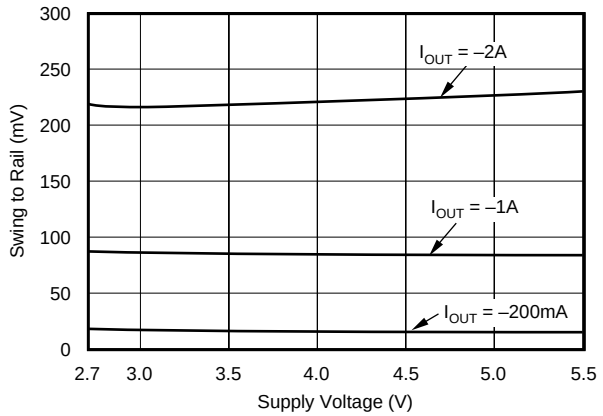
POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



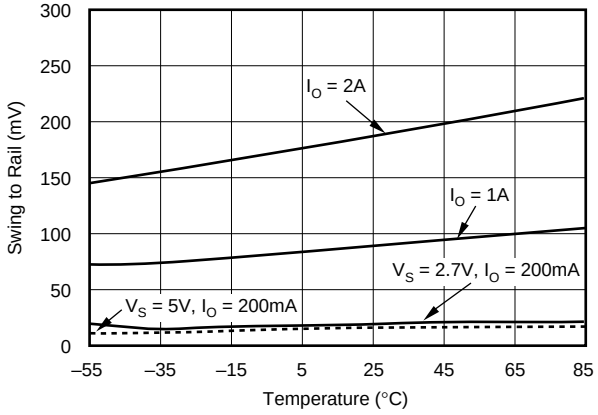
OUTPUT SWING TO POSITIVE RAIL vs SUPPLY VOLTAGE



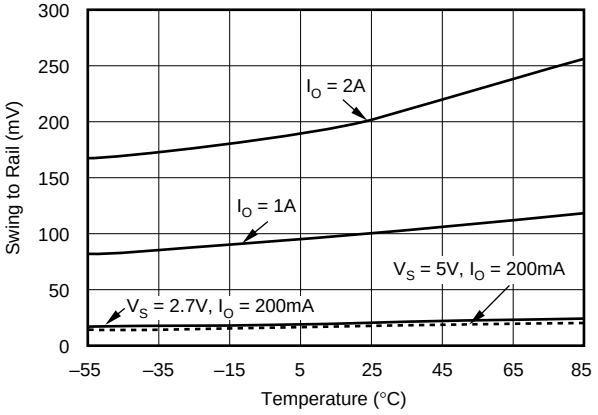
OUTPUT SWING TO NEGATIVE RAIL vs SUPPLY VOLTAGE



OUTPUT SWING TO POSITIVE RAIL vs TEMPERATURE



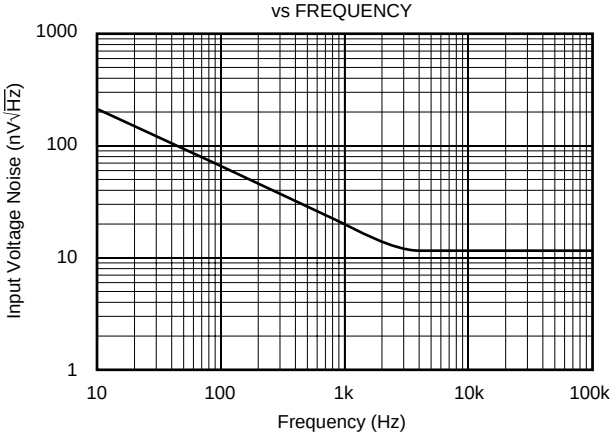
OUTPUT SWING TO NEGATIVE RAIL vs TEMPERATURE



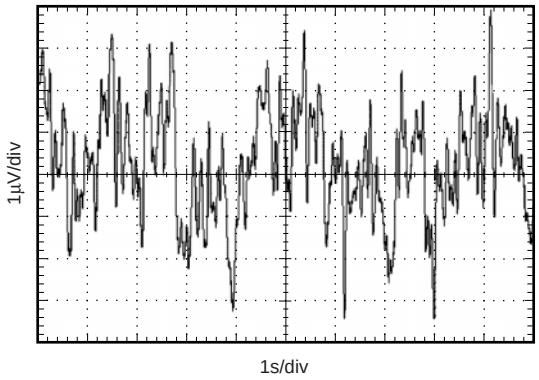
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

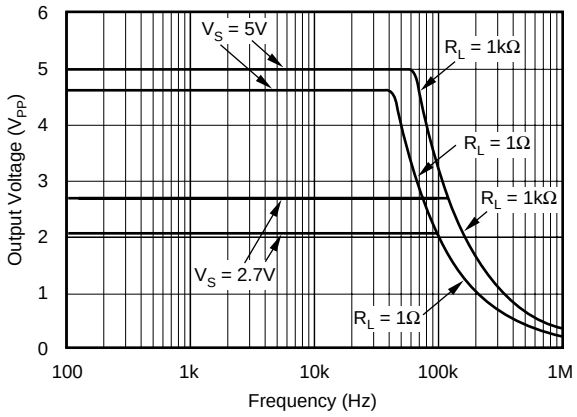
INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



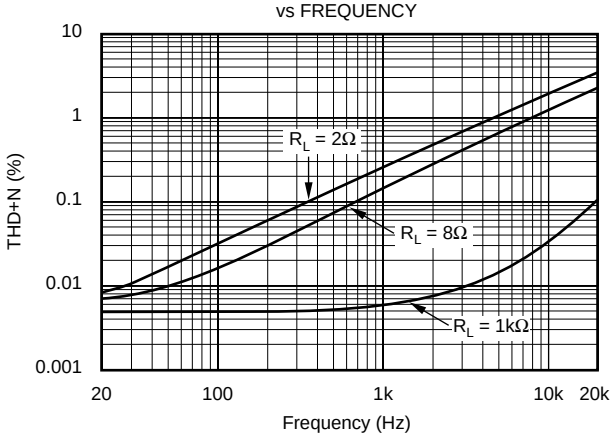
0.1Hz TO 10Hz INPUT VOLTAGE NOISE



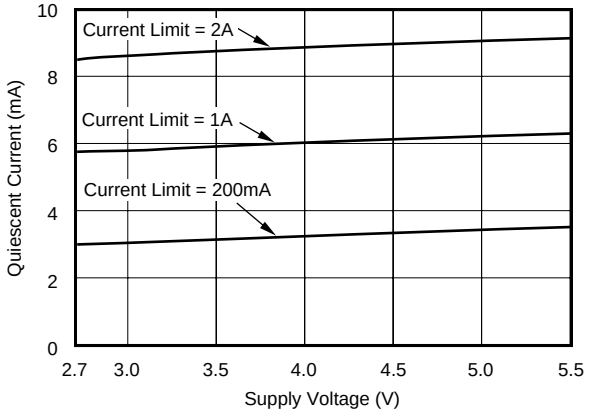
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



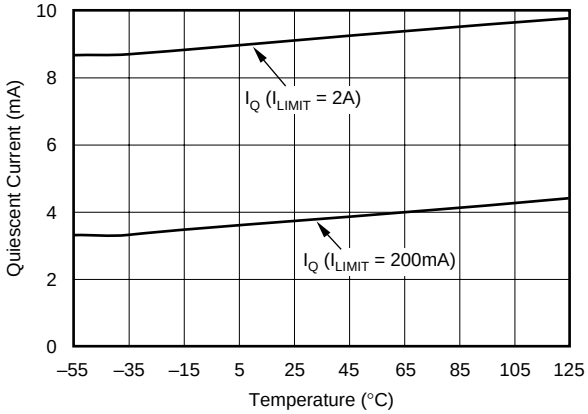
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



QUIESCENT CURRENT vs SUPPLY VOLTAGE



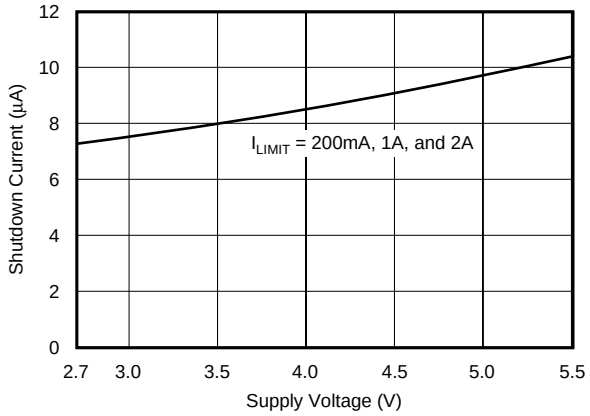
QUIESCENT CURRENT vs TEMPERATURE



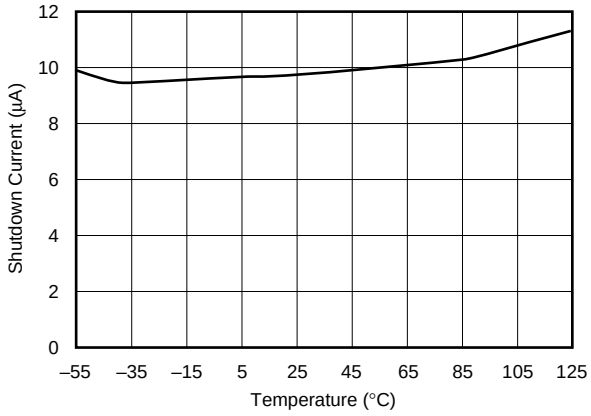
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

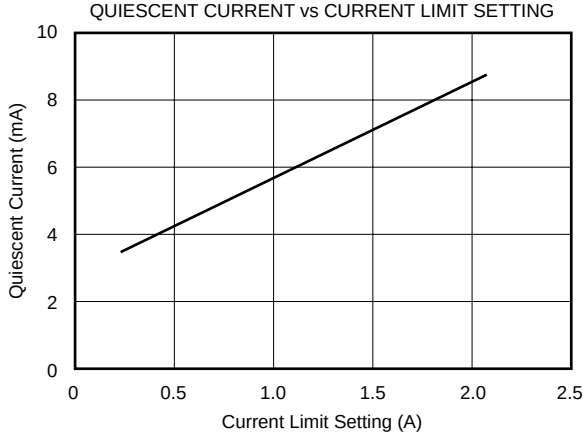
SHUTDOWN CURRENT vs SUPPLY VOLTAGE



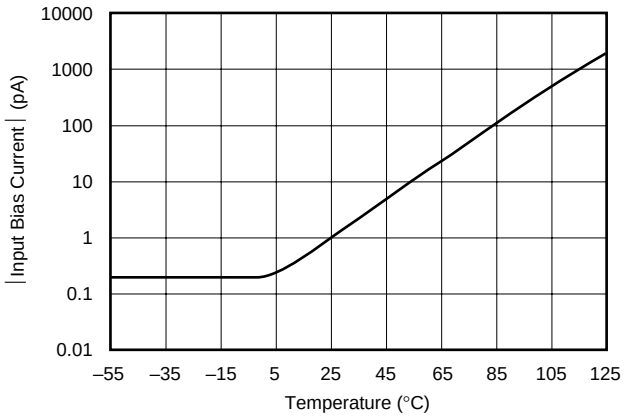
SHUTDOWN CURRENT vs TEMPERATURE



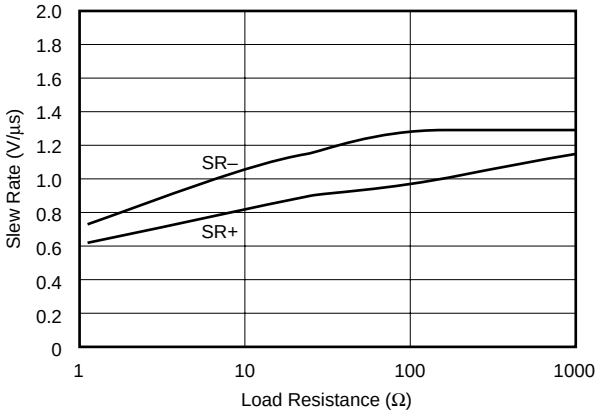
QUIESCENT CURRENT vs CURRENT LIMIT SETTING



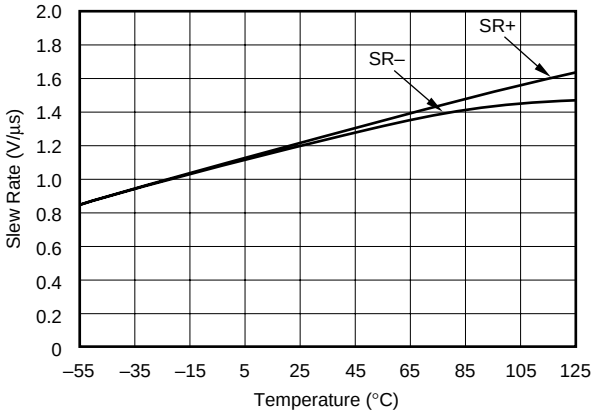
INPUT BIAS CURRENT vs TEMPERATURE



SLEW RATE vs LOAD RESISTANCE



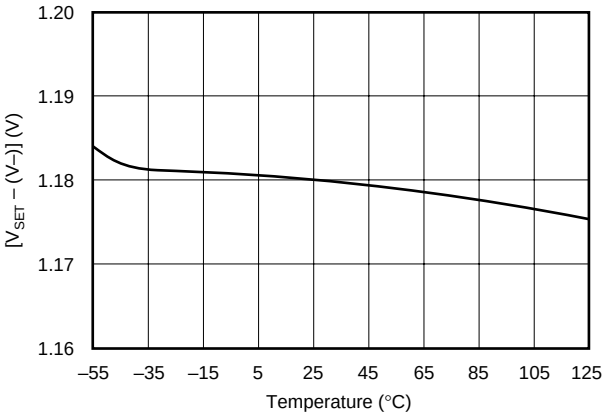
SLEW RATE vs TEMPERATURE



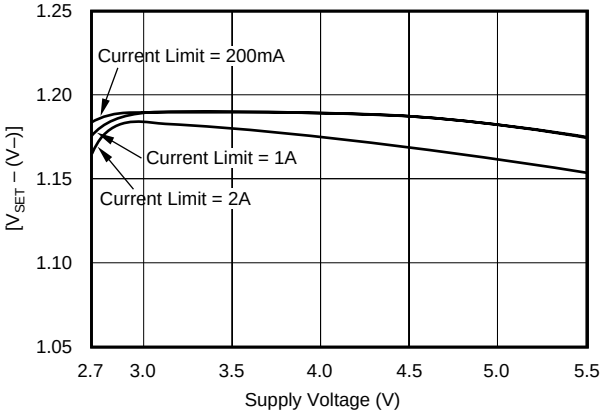
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

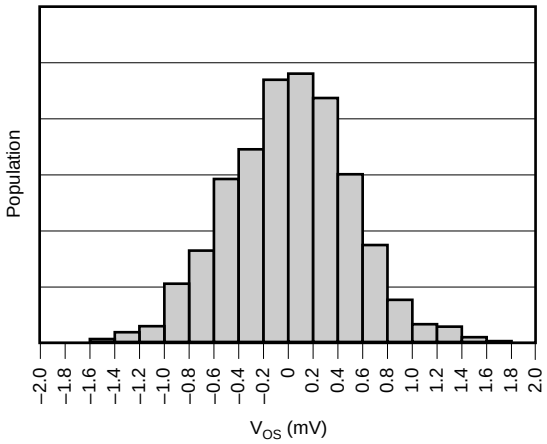
VOLTAGE ON I_{SET} PIN vs TEMPERATURE



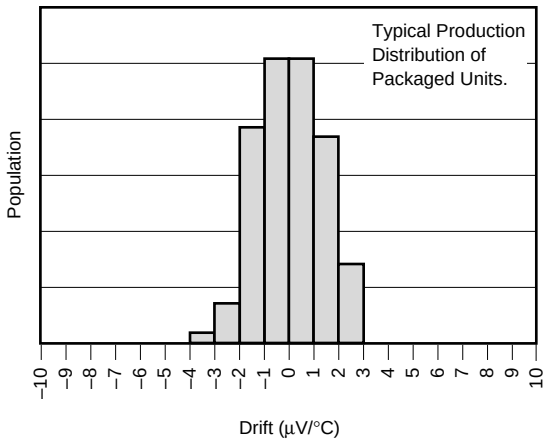
VOLTAGE ON I_{SET} PIN vs SUPPLY VOLTAGE



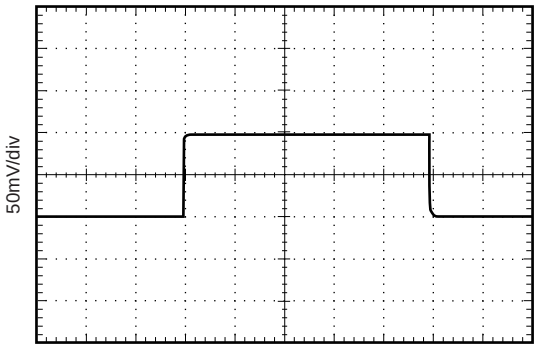
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



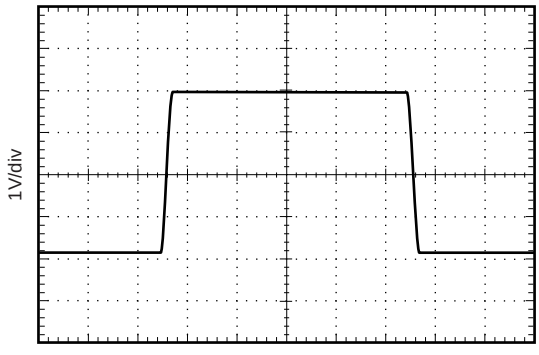
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 1kΩ)



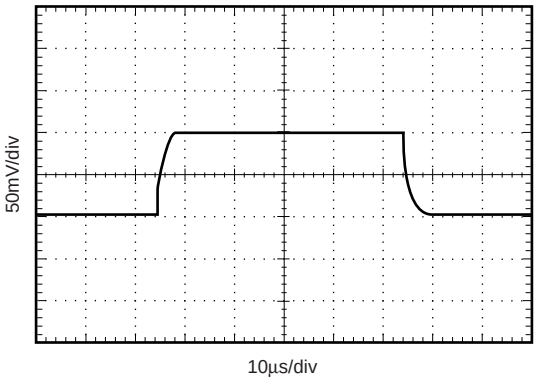
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 1kΩ)



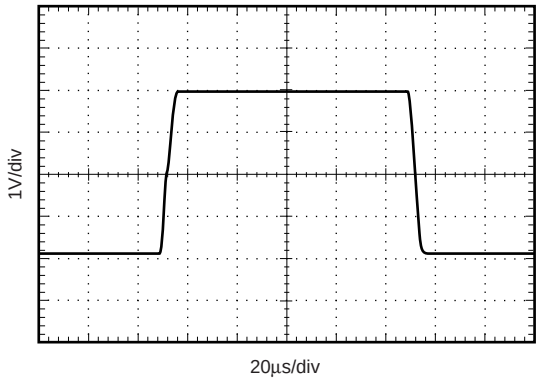
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

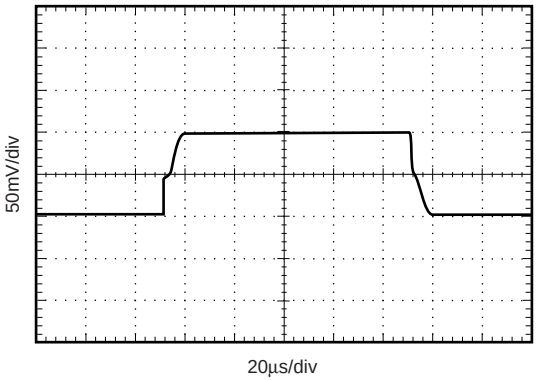
SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 10Ω)



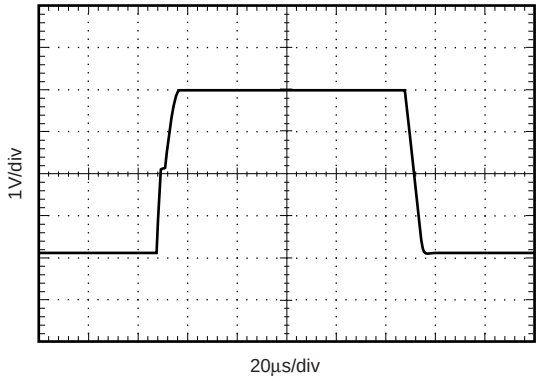
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 10Ω)



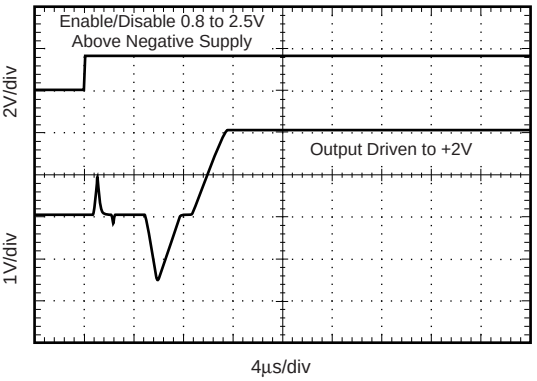
SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 1Ω)



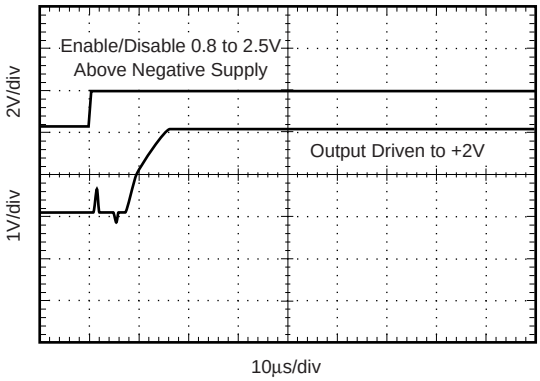
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 1Ω)



ENABLE
(10Ω Load)



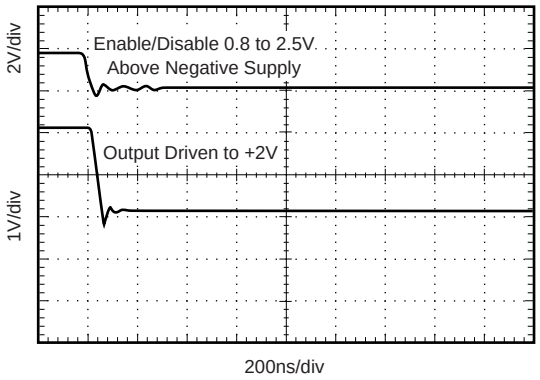
ENABLE
(1Ω Load)



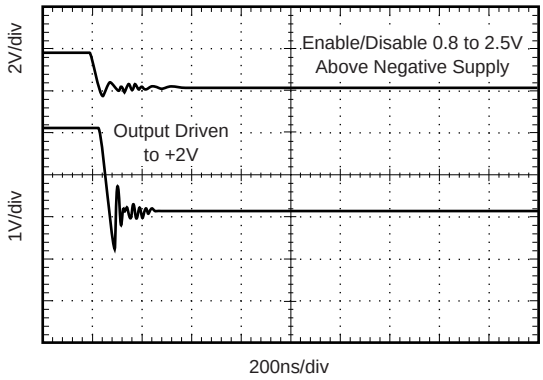
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

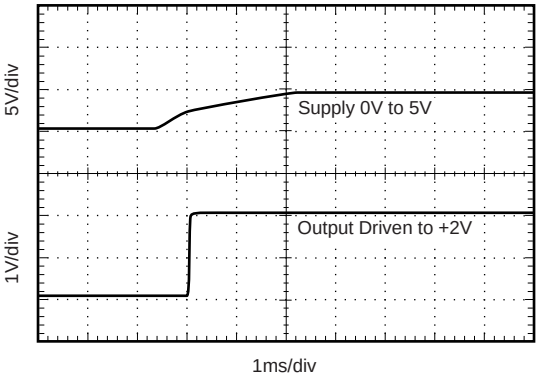
DISABLE
(10Ω Load)



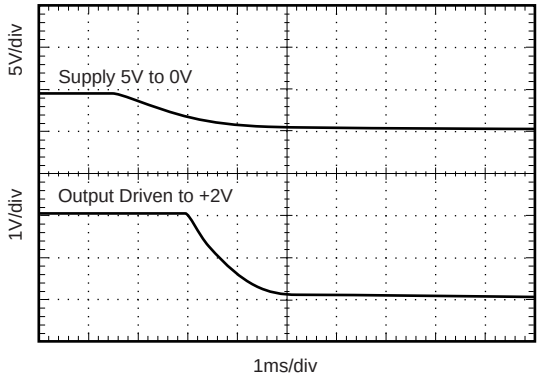
DISABLE
(1Ω Load)



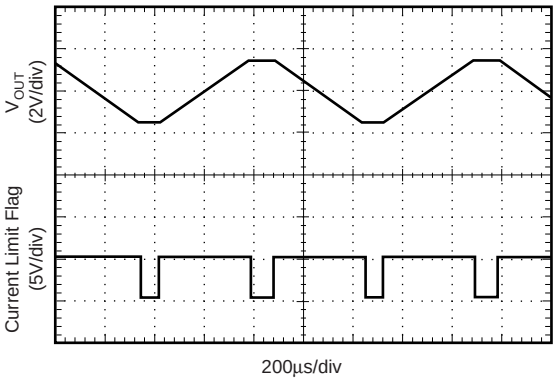
POWER ON
(1Ω Load)



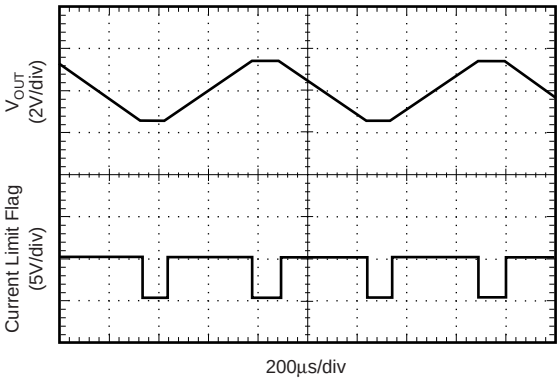
POWER OFF
(1Ω Load)



IN AND OUT OF CURRENT LIMIT TRANSIENT
(R_L = 0.75Ω, Current Limit = 2A)



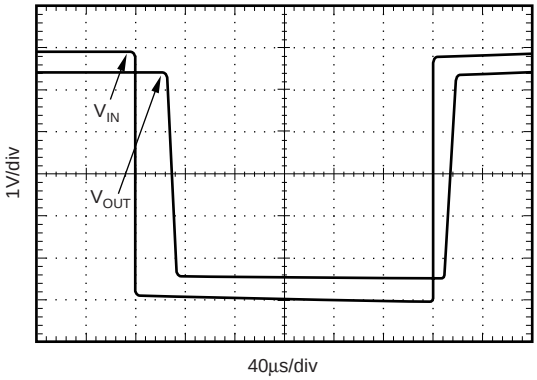
IN AND OUT OF CURRENT LIMIT TRANSIENT
(R_L = 7.5Ω, Current Limit = 200mA)



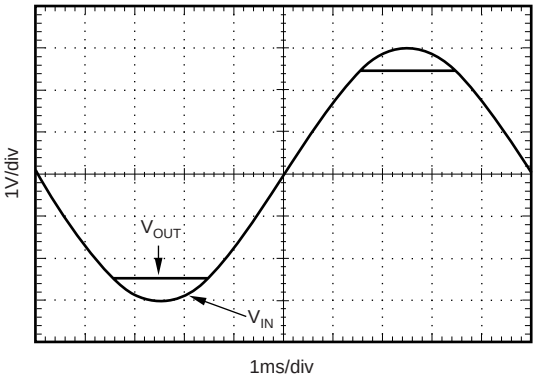
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

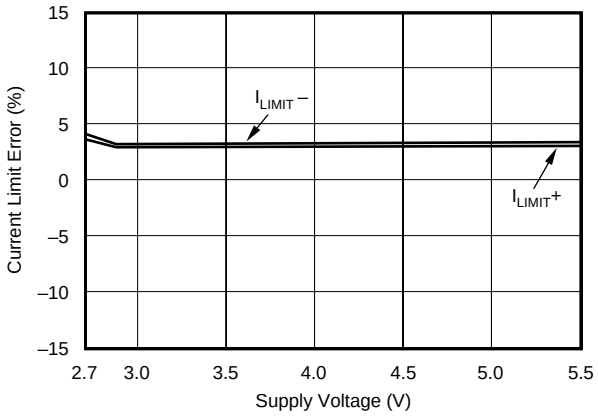
OVERLOAD RECOVERY
(G = +1)



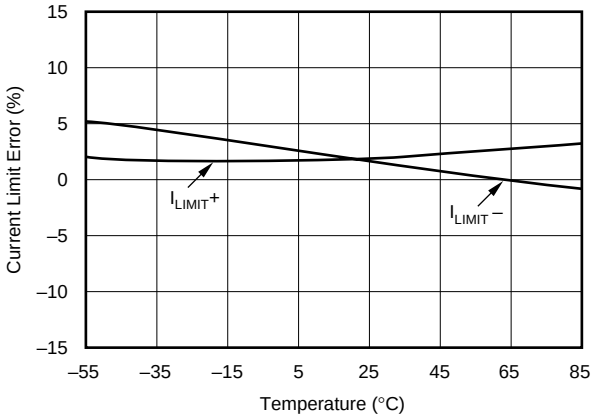
NO PHASE INVERSION WITH INPUTS
LARGER THAN SUPPLY VOLTAGE
(G = +1, R_L = 10Ω)



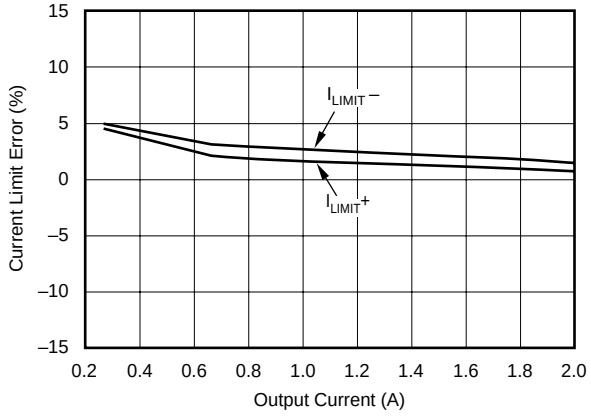
CURRENT LIMIT ERROR vs SUPPLY VOLTAGE



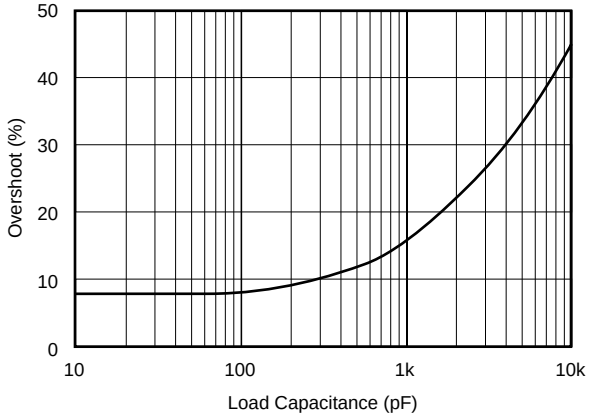
CURRENT LIMIT ERROR vs TEMPERATURE



CURRENT LIMIT ERROR vs OUTPUT CURRENT



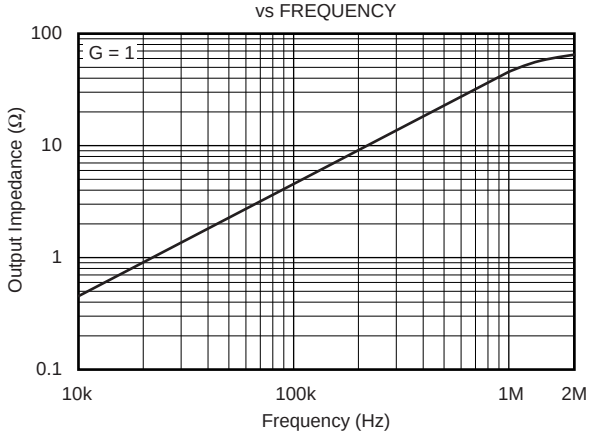
OVERSHOOT vs LOAD CAPACITANCE
(G = +1, R_L = 1kΩ)



TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

CLOSED-LOOP OUTPUT IMPEDANCE
vs FREQUENCY



APPLICATIONS INFORMATION

BASIC CONFIGURATION

Figure 1 shows the OPA567 connected as a basic non-inverting amplifier. However, the OPA567 can be used in virtually any op amp configuration. A current limit setting resistor (R_{SET}, in Figure 1) is essential to the OPA567 operation, and cannot be omitted.

Power-supply terminals should be bypassed with low series impedance capacitors. Using larger tantalum and smaller ceramic type capacitors in parallel is recommended. Power-supply wiring should have low series impedance.

POWER SUPPLIES

The OPA567 operates with excellent performance from a single (+2.7V to +5.5V) supply or from dual supplies. Power supply voltages do not need to be equal as long as the total voltage remains below 5.5V. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics* section.

ADJUSTABLE CURRENT LIMIT AND CURRENT LIMIT FLAG PIN

The OPA567 provides over-current protection to the load through its accurate, user-adjustable current limit (pin 6). The current limit value, I_{LIMIT}, can be set from 0.2A to 2.2A by controlling the current to the I_{SET} pin. The current limit, I_{LIMIT}, will be 9800 • I_{SET}, where I_{SET} is the current through the I_{SET} pin. Setting the current limit requires no special power resistors. The output current does not flow through this pin.

Setting the current limit

As illustrated in Figure 2, the simplest method of setting the current limit is to connect a resistor or potentiometer between the I_{SET} pin and V–, the negative supply, according to the formula:

$$I_{LIMIT} = 9800 \bullet (1.18V/R_{SET})$$

Alternatively, the output current limit can be set by applying a voltage source in series with a resistance using the equation:

$$I_{LIMIT} = 9800 \bullet [(1.18V - V_{ADJUST})/R_{SET}]$$

The voltage source must be referenced to V–.

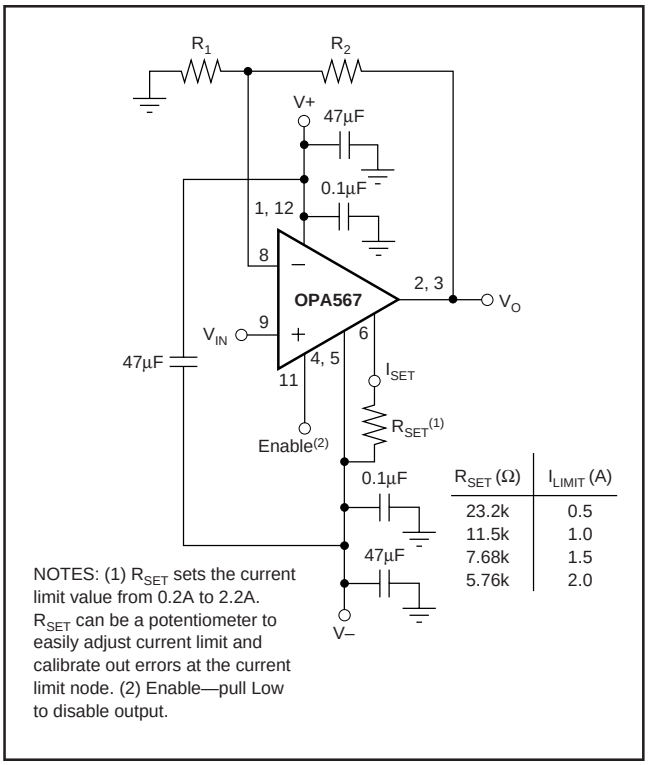


FIGURE 1. Basic Connections.

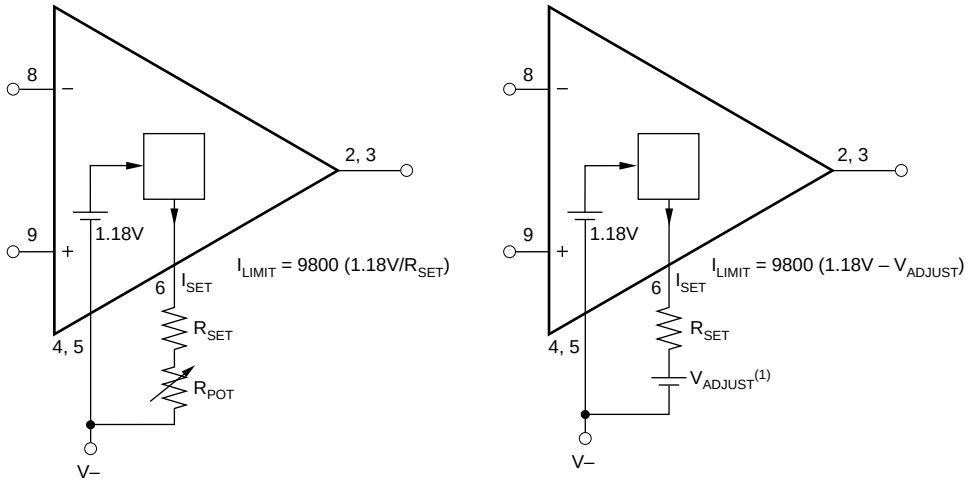


FIGURE 2. Setting the Current Limit—Resistor Method.

Current Limit Accuracy

Internally separate circuits monitor the positive and negative current limits. Each circuit output is compared to a single internal reference that is set by the user with an external resistor or a resistor/voltage source combination. The OPA567 employs a patented circuit technique to achieve an accurate and stable current limit throughout the full output range. The initial accuracy of the current limit is typically within 3%; however, because of internal matching limitations, the error can be as much as 15%. The variation of the current limit with factors such as output current level, output voltage, and temperature is shown in the *Typical Characteristics* section.

When the accuracy of one current limit (sourcing or sinking) is more important than the other, it is possible to set its accuracy to better than 1% by adjusting the external resistor or the applied voltage. The accuracy of the other current limit will still be affected by internal matching.

Current Limit Flag Pin

The OPA567 features an I_{FLAG} pin (pin 7) that can be monitored to determine when the part is in current limit. The output signal of the I_{FLAG} pin is compatible to standard logic in single-supply applications. The output signal is a CMOS logic gate that switches from V+ to V– to indicate that the amplifier is in current limit. The I_{FLAG} pin can source and sink up to 25µA. Additional parasitic capacitance between pins 6 and 7 can cause instability at the edge of the current limit. Avoid routing these traces in parallel close to each other.

Quiescent Current Dependence on the Current Limit Setting

The OPA567 is a low-power amplifier, with a typical 3.4mA quiescent current (with the current limit configured for 200mA). The quiescent current varies with the current limit setting—it increases 0.5mA for each additional 200mA increase in the current limit, as shown in Figure 3.

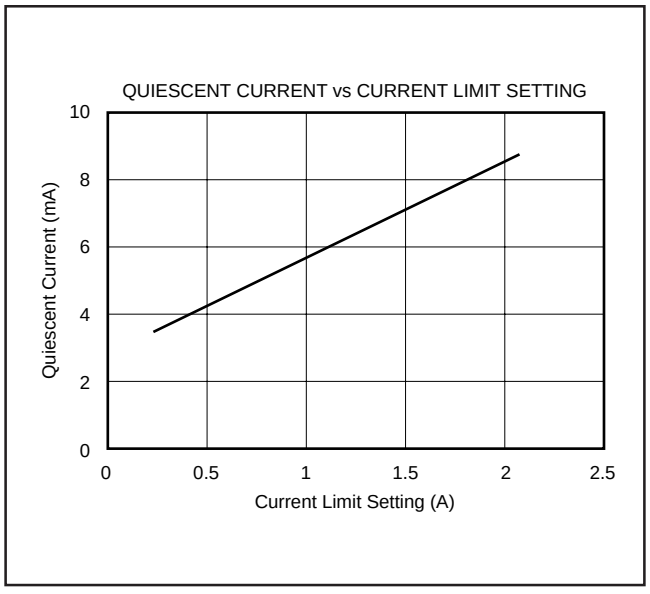


FIGURE 3. Quiescent Current vs Current Limit Setting.

ENABLE PIN—OUTPUT DISABLE

The Enable pin can disable the OPA567 within microseconds. When disabled, the amplifier draws less than 10µA and its output enters a high-impedance state that allows multiplexing. It is important to note that when the amplifier is disabled, the Thermal Flag pin (T_{FLAG}) circuitry continues to operate. This feature allows use of the T_{FLAG} pin output to implement thermal protection strategies. For more details, please see the section on thermal protection.

The OPA567 Enable pin has an internal pull-up circuit, so it does not have to be connected to the positive supply for normal operation. To disable the amplifier, the Enable pin must be connected to no more than (V–) + 0.8V. To enable the amplifier, either allow the Enable pin to float or connect it to at least (V–) + 2.5V.

The Enable pin is referenced to the negative supply (V–). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications.

In single-supply operation, V– typically equals common ground; thus, the enable/disable logic signal and the OPA567 Enable pin are referenced to the same potential. In this configuration, the logic level and the OPA567 Enable pin can simply be tied together. Disabling the OPA567 occurs for voltage levels of less than 0.8V. The OPA567 is enabled at logic levels greater than 2.5V.

In dual-supply operation, the logic level is referenced to a logic ground. However, the OPA567 Enable pin is still referenced to V–. To disable the OPA567, the voltage level of the logic signal needs to be level-shifted. This level-shifting can be done using an optocoupler, as shown in Figure 4.

Examples of output behavior during disabled and enabled conditions with various load impedances are shown in the typical characteristics section. Please note that this behavior is a function of board layout, load impedances, and bypass strategies. For sensitive loads, the use of a low-pass filter or other protection strategy is recommended.

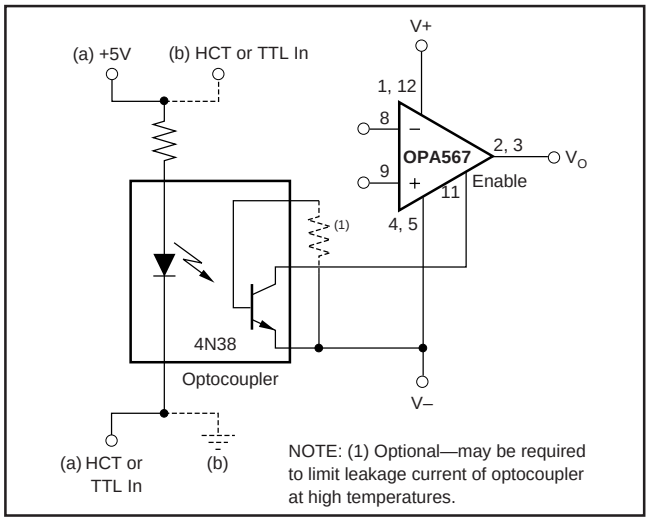


FIGURE 4. OPA567 Shutdown Configuration for Dual Supplies.

ENSURING MICROCONTROLLER COMPATIBILITY

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic High levels on their ports while other models power up with logic Low levels after reset.

In configuration (a) shown in Figure 4, the enable/disable signal is applied on the cathode side of the photodiode within the optocoupler. A logic High level causes the OPA567 to be enabled, and a logic Low level disables the OPA567. In configuration (b) of Figure 4, with the logic signal applied on the anode side, a high level disables the OPA567 and a low level enables the op amp.

RAIL-TO-RAIL OUTPUT RANGE

The OPA567 has a class AB output stage with common source transistors that are used to achieve rail-to-rail output swing. It was designed to be able to swing closer to the rail than other existing linear amplifiers, even with high output current levels. A quick way to estimate the output swing with various output current requirements is by using the equation:

$$V_{SWING}\ [typical] = 0.1 \bullet I_O$$

Plots of the Output Swing vs Output Current, Supply Voltage, and Temperature are provided in the Typical Characteristics section.

RAIL-TO-RAIL INPUT RANGE

The input common-mode voltage range of the OPA567 extends 100mV beyond the supply rails. This is achieved by a complementary input stage with an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel input pair is active for input voltages close to the positive rail while the P-channel input pair is active for input voltages close to the negative rail. The transition point is typically at (V+) – 1.3V, and there is a small transition region around the switching point where both transistors are on. It is important to note that the two input pairs can have offsets of different signs and magnitudes. Therefore, as the transition point is crossed, the offset of the amplifier changes. This offset shift accounts for the reduced common-mode rejection ratio over the full input common-mode range.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 5. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

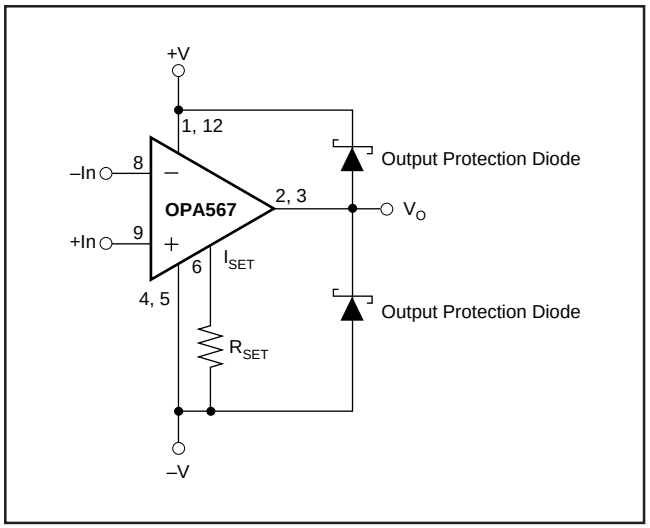


FIGURE 5. Output Protection Diode.

THERMAL FLAG PIN

The OPA567 has thermal sensing circuitry that provides a warning signal when the die temperature exceeds safe limits. Unless the T_{FLAG} pin is connected to the Enable pin, when this flag is triggered, the part continues to operate even though the junction temperature exceeds 150°C. This default operation allows maximum usable operation in very harsh conditions but degrades reliability. The T_{FLAG} pin can be used to provide for orderly system shutdown before failure occurs. It can be also used to evaluate the thermal environment to determine need for and appropriate design of a shutdown mechanism.

The thermal flag output signal is from a CMOS logic gate that switches from V+ to V– to indicate that the amplifier is in thermal limit. This flag output pin can source and sink up to 25µA. The T_{FLAG} pin is HIGH during normal operation. Power dissipated in the amplifier will cause the junction temperature to rise. When the junction temperature exceeds 150°C, the T_{FLAG} pin will go Low, and remain Low until the amplifier has cooled to 130°C. Despite this hysteresis, with a method of orderly shutdown, the T_{FLAG} pin can cycle on and off, depending on load and signal conditions. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

It is possible to connect the T_{FLAG} pin directly to the Enable pin for automatic shutdown protection. When both thermal shutdown and the amplifier enable/disable functions are desired, the externally generated control signal and the T_{FLAG} pin outputs should be combined with an AND gate; see Figure 6. The temperature protection was designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the OPA567 in and out of thermal shutdown will degrade reliability.

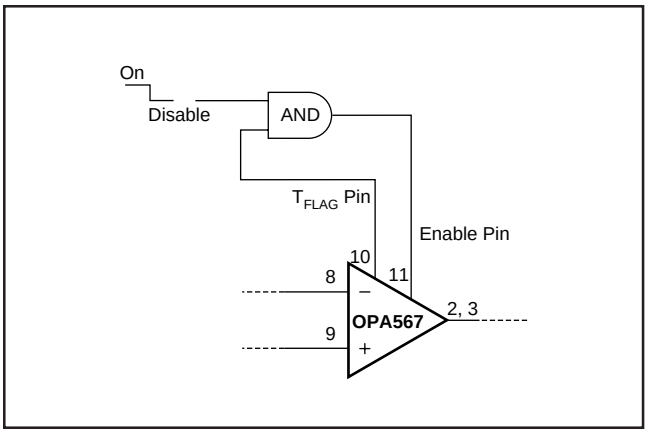


FIGURE 6. Enable/Shutdown Control Using T_{FLAG} Pin and External Control Signal.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable, long term, continuous operation, the junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection should trigger more than 25°C above the maximum expected ambient conditions of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Fast transients of large output current swings (for example, switching quickly from sourcing 2A to sinking 2A) may cause a glitch on the T_{FLAG} pin. When switching large currents is expected, the use of extra bypass between the supplies or a low-pass filter on the T_{FLAG} pin is recommended.

POWER DISSIPATION AND SAFE OPERATING AREA

Power dissipation depends on power supply, signal, and load conditions. It is dominated by the power dissipation of the output transistors. For DC signals, power dissipation is equal to the product of output current, I_{OUT} and the output voltage across the conducting output transistor ($V_S - V_{OUT}$). Dissipation with AC signals is lower. Application Bulletin SBOA022 explains how to calculate or measure power dissipation with unusual signals and loads and can be found at the TI web site (www.ti.com).

Output short-circuits are particularly demanding for the amplifier because the full supply voltage is seen across the conducting transistor. It is very important to note that the temperature protection will not shut the part down in over-temperature conditions, unless the T_{FLAG} pin is connected to the Enable pin; see the section on Thermal Flag.

Figure 7 shows the safe operating area at room temperature with various heatsinking efforts. Note that the safe output current decreases as ($V_S - V_{OUT}$) increases. Figure 8 shows the safe operating area at various temperatures with the metal heatsink being soldered to a 2oz copper pad.

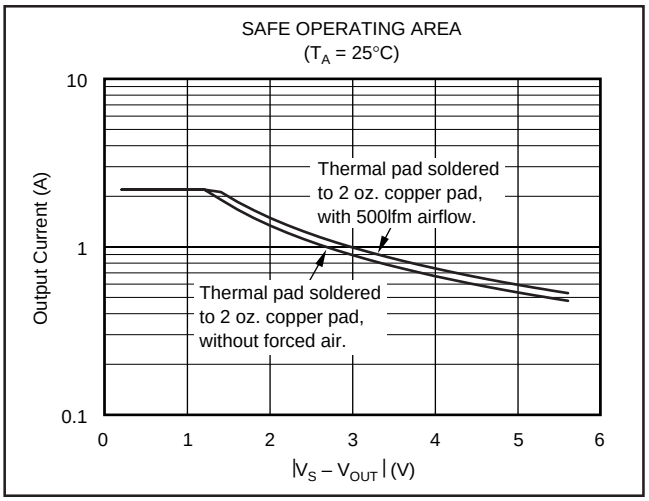


FIGURE 7. Safe Operating Area at Room Temperature.

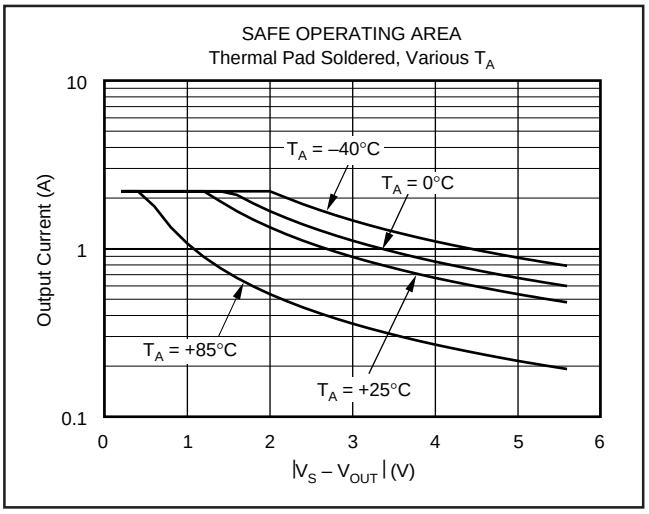


FIGURE 8. Safe Operating Area at Various Ambient Temperatures. Metal heat sink soldered to a 2oz copper pad.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design. The QFN package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. Refer to the QFN Package section for further details.

The OPA567 has a junction-to-ambient thermal resistance (θ_{JA}) value of 38°C/W when soldered to a 2oz copper plane. This value can be further decreased by the addition of forced air. See Figure 9 for the junction-to-ambient thermal resistance of the QFN-12 package.

Junction temperature should be kept below 125°C for reliable operation. The junction temperature can be calculated by:

$$T_J = T_A + P_D\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CA}$

T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
P_D = Power Dissipated (W)
θ_{JA} = Junction-to-Ambient Thermal Resistance
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{CA} = Case-to-Air Thermal Resistance

HEATSINKING METHOD	θ_{JA}
The part is soldered to a 2 oz copper pad under the exposed pad.	38
Soldered to copper pad with forced airflow (150lfm).	36
Soldered to copper pad with forced airflow (250lfm).	35
Soldered to copper pad with forced airflow (500lfm).	34

FIGURE 9. Junction-to-Ambient Thermal Resistance with Various Heatsinking Efforts.

The Maximum Power Dissipation vs Temperature for the heatsinking methods referenced in Figure 9 is shown in Figure 10.

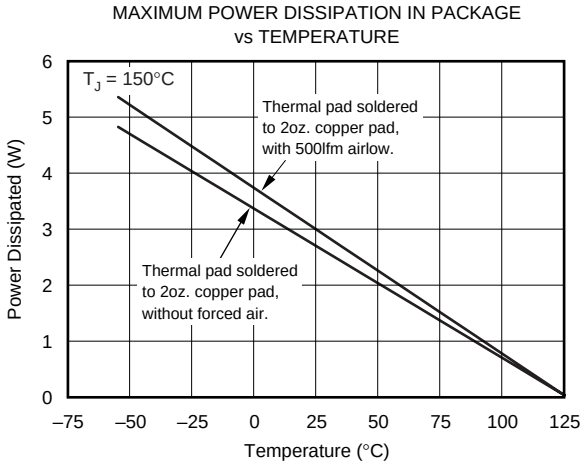


FIGURE 10. Maximum Power Dissipation vs Temperature.

To appropriately determine required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of 125°C). Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

For applications with limited board size, refer to Figure 11 for the approximate thermal resistance relative to the number of thermal vias. The QFN-12 package is well suited for continuous power levels, as shown in Figure 10. Higher power levels may be achieved in applications with a low on/off duty cycle.

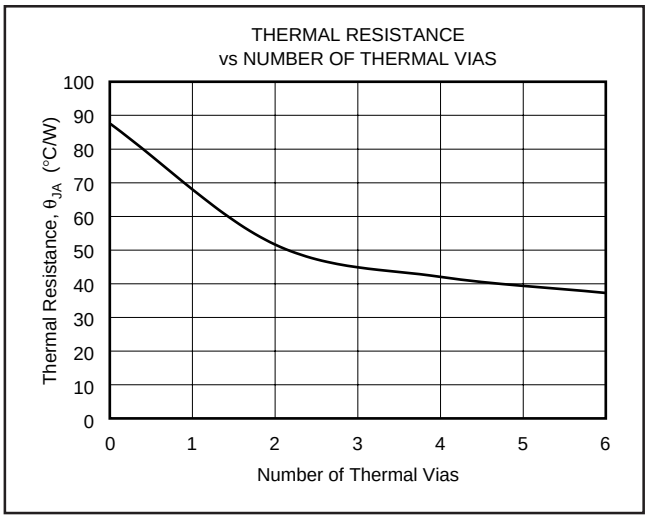


FIGURE 11. Thermal Resistance vs Number of Thermal Vias.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with higher impedance feedback networks (R_F > 50kΩ), it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 12. This capacitor compensates for the zero created by the feedback network impedance and the input capacitance of the OPA567 (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

The size of the capacitor needed is estimated using the equation:

$$R_{IN} \bullet C_{IN} = R_F \bullet C_F$$

where C_{IN} is the sum of the input capacitance of the OPA567 plus the parasitic layout capacitance.

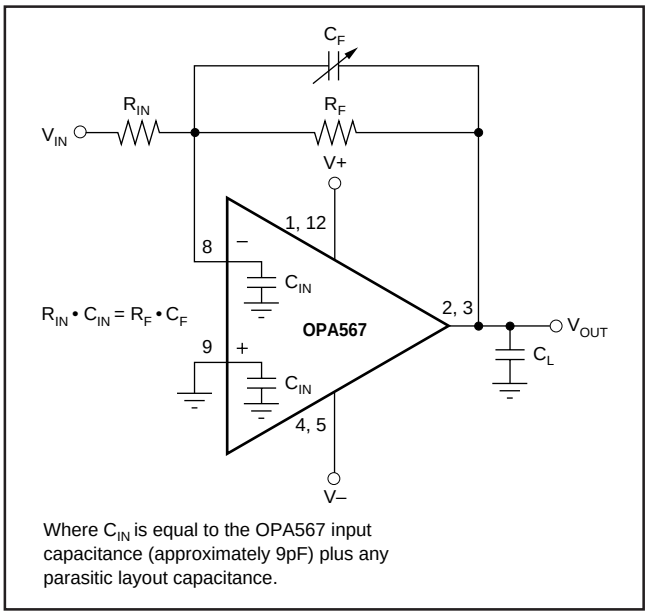


FIGURE 12. Feedback Capacitor for Use with Higher Impedance Networks.

QFN THERMALLY ENHANCED PACKAGE

The OPA567 uses the QFN-12 package, a thermally-enhanced package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See QFN/SON PCB Attachment Application Note (SLUA271) located at www.ti.com.

The thermal resistance junction-to-ambient ($R_{\theta JA}$) of the QFN package depends on the PCB layout. Using thermal vias and wide PCB traces improve thermal resistance. The thermal pad must be soldered to the PCB. The thermal pad should either be left floating or connected to V–.

LAYOUT GUIDELINES

The OPA567 is a power amplifier that requires proper layout for best performance. An example layout is appended to the end of this datasheet. Refinements to this layout may be required based on assembly process requirements.

Keep power-supply leads as short as possible. This practice will keep inductance low and resistive losses at a minimum. A minimum of 18 gauge wire thickness is recommended for power- supply leads. The wire length should be less than 8 inches.

Proper power-supply bypassing with low ESR capacitors is essential to achieve good performance. A parallel combination of 100nF ceramic and 47μF tantalum bypass capacitors will provide low impedance over a wide frequency range. Bypass capacitors should be placed as close as practical to the power-supply pins of the OPA567.

PCB traces conducting high currents, such as from output to load or from the power-supply connector to the power-supply pins of the OPA567 should be kept as wide and short as possible. This practice will keep inductance low and resistive losses to a minimum.

The nine holes in the landing pattern for the OPA567 are for the thermal vias that connect the thermal pad of the OPA567 to the heatsink area on the PCB. All traces conducting high currents are very wide for lowest inductance and minimal resistive losses.

APPLICATION CIRCUITS

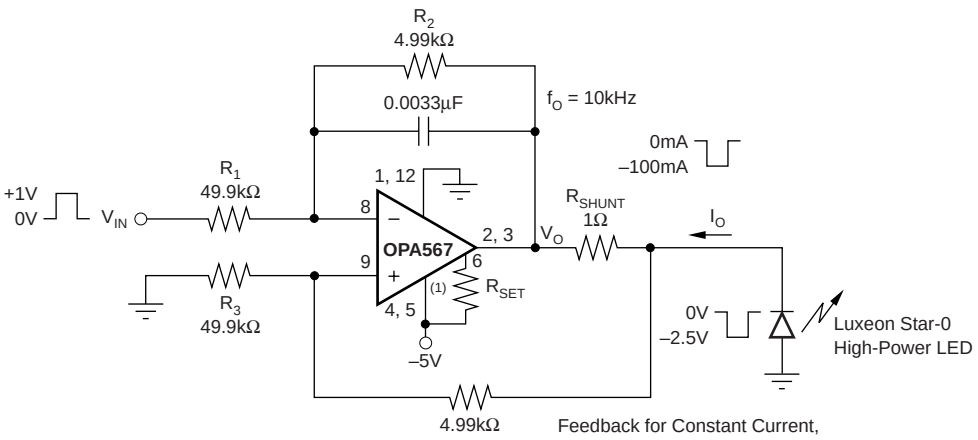


FIGURE 13. Grounded Anode LED Driver.

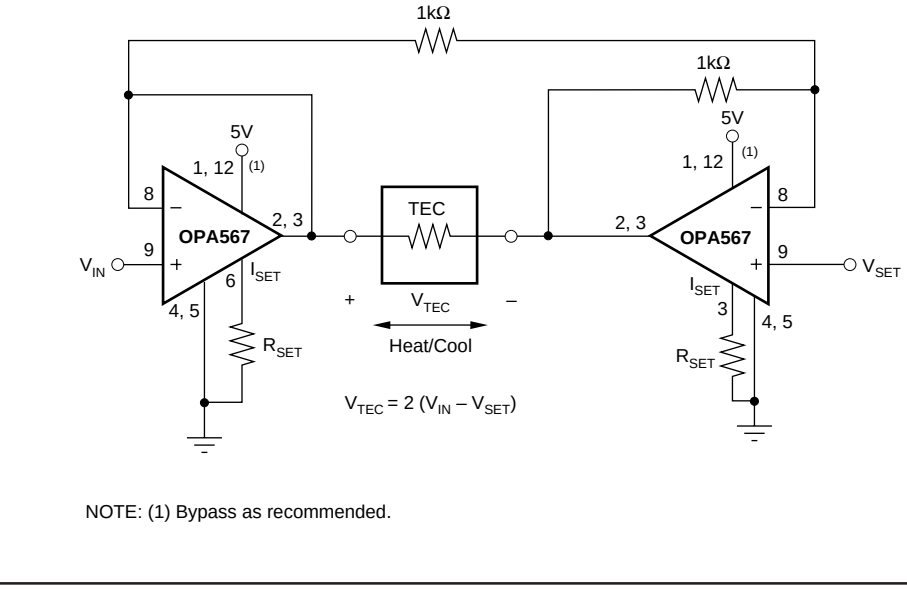


FIGURE 14. Bridge-Tied Load Driver.

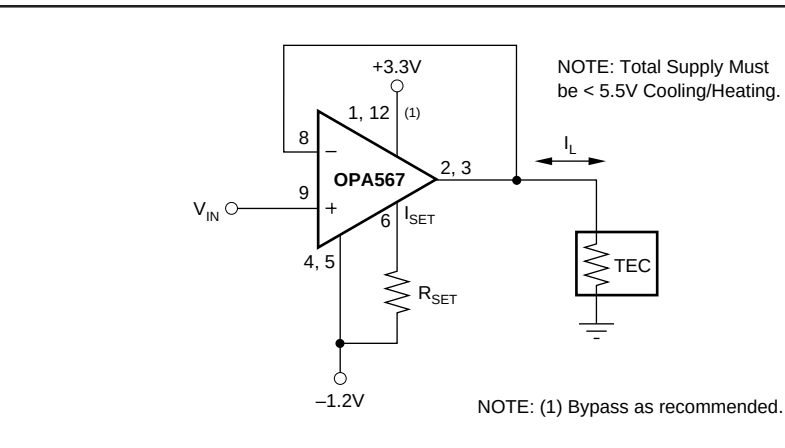


FIGURE 15. Single Power Amplifier Driving Bidirectional Current through a TEC using Asymmetrical Bipolar Power Supplies.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA567AIRHGR	Active	Production	VQFN (RHG) | 12	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 567AI
OPA567AIRHGR.Z	Active	Production	VQFN (RHG) | 12	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 567AI
OPA567AIRHGRG4.Z	Active	Production	VQFN (RHG) | 12	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 567AI
OPA567AIRHGT	Active	Production	VQFN (RHG) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 567AI
OPA567AIRHGT.Z	Active	Production	VQFN (RHG) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 567AI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

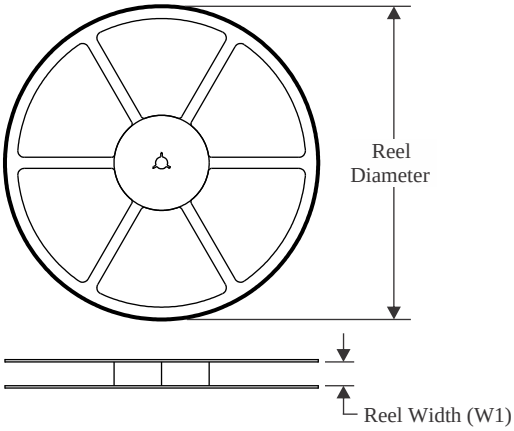
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

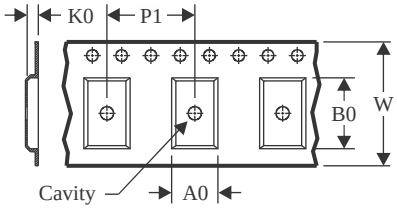
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

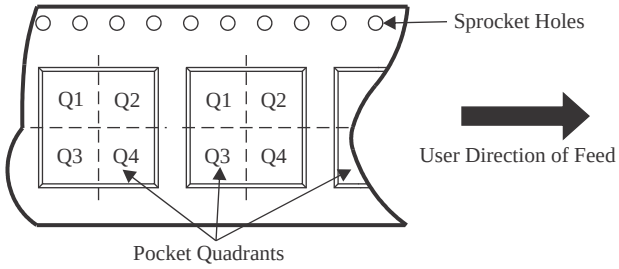


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

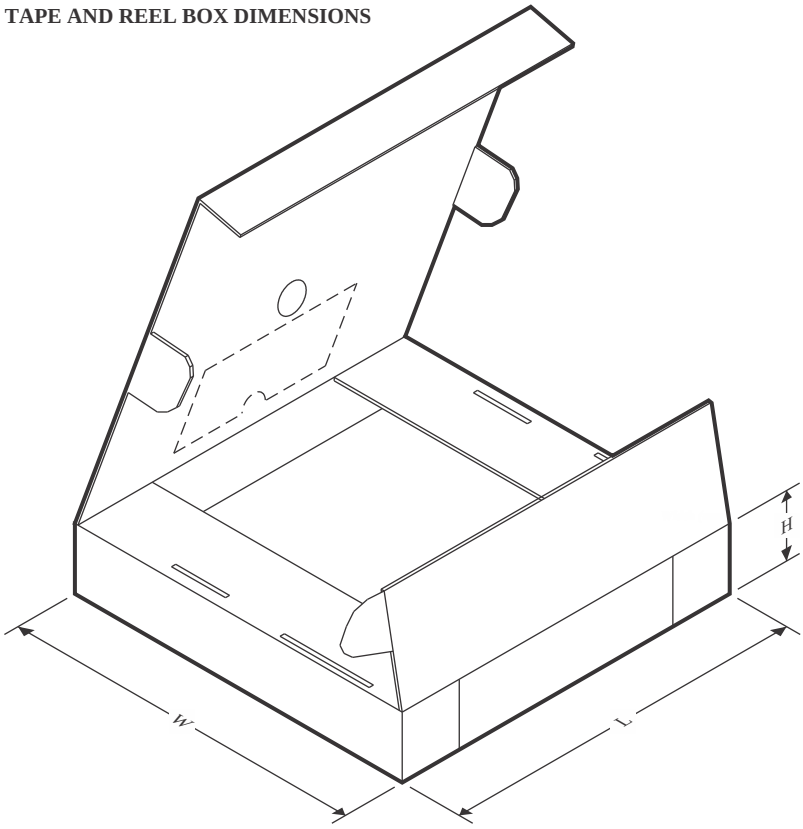
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA567AIRHGR	VQFN	RHG	12	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
OPA567AIRHGT	VQFN	RHG	12	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

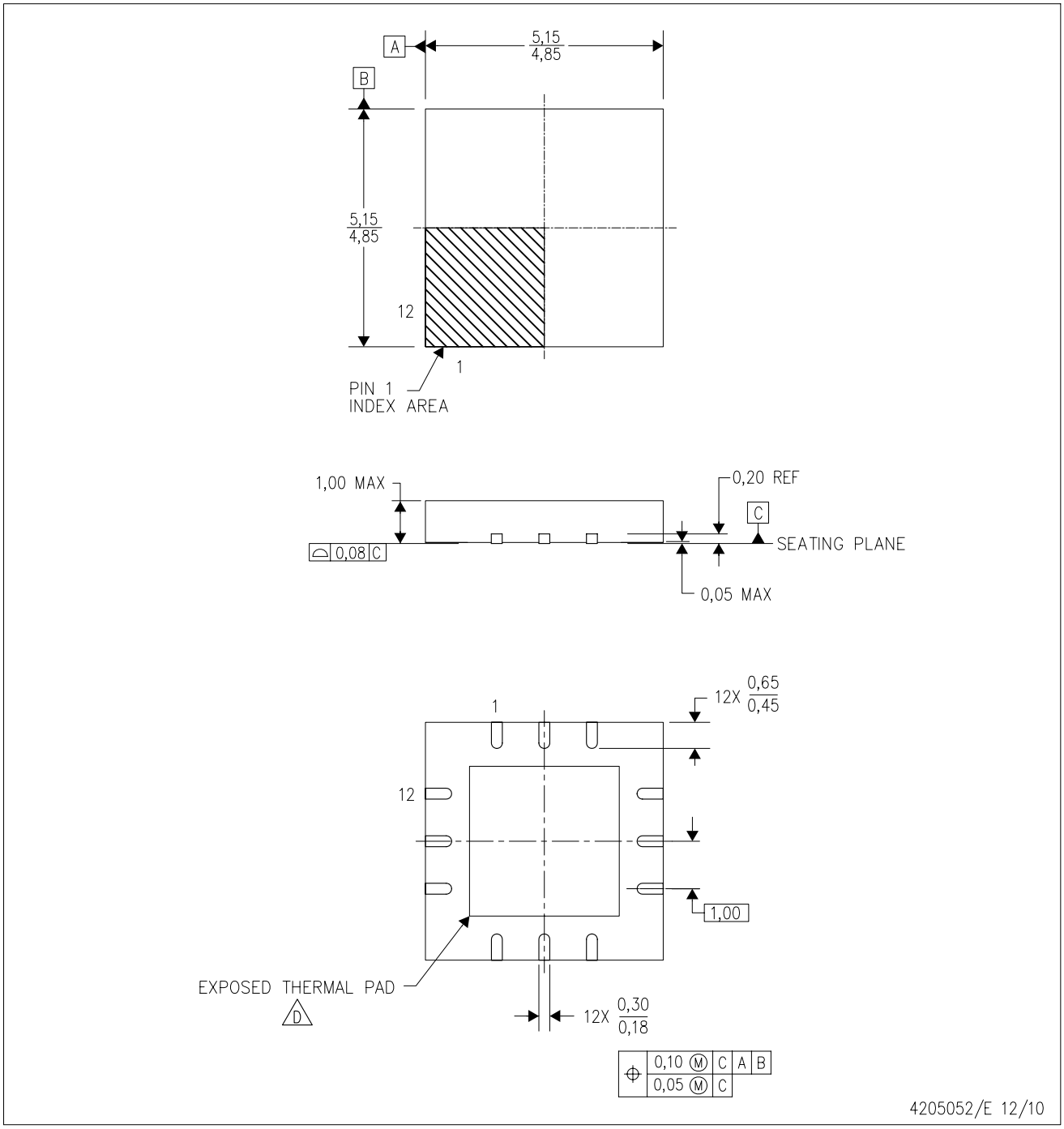
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA567AIRHGR	VQFN	RHG	12	2500	356.0	356.0	35.0
OPA567AIRHGT	VQFN	RHG	12	250	210.0	185.0	35.0

RHG (S–PVQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

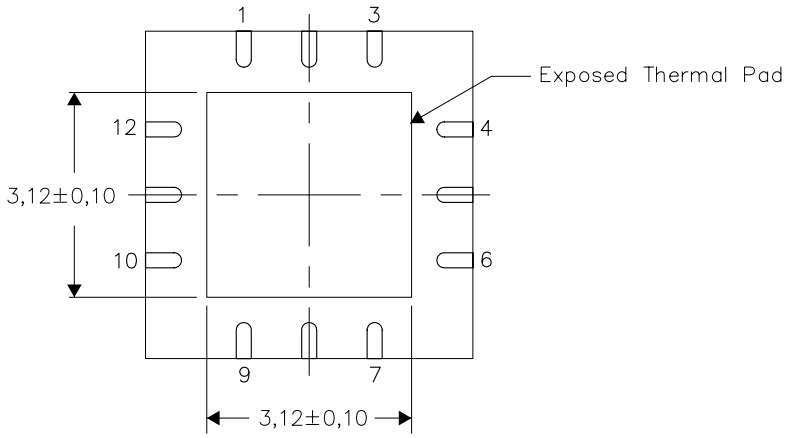
RHG (S–PVQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



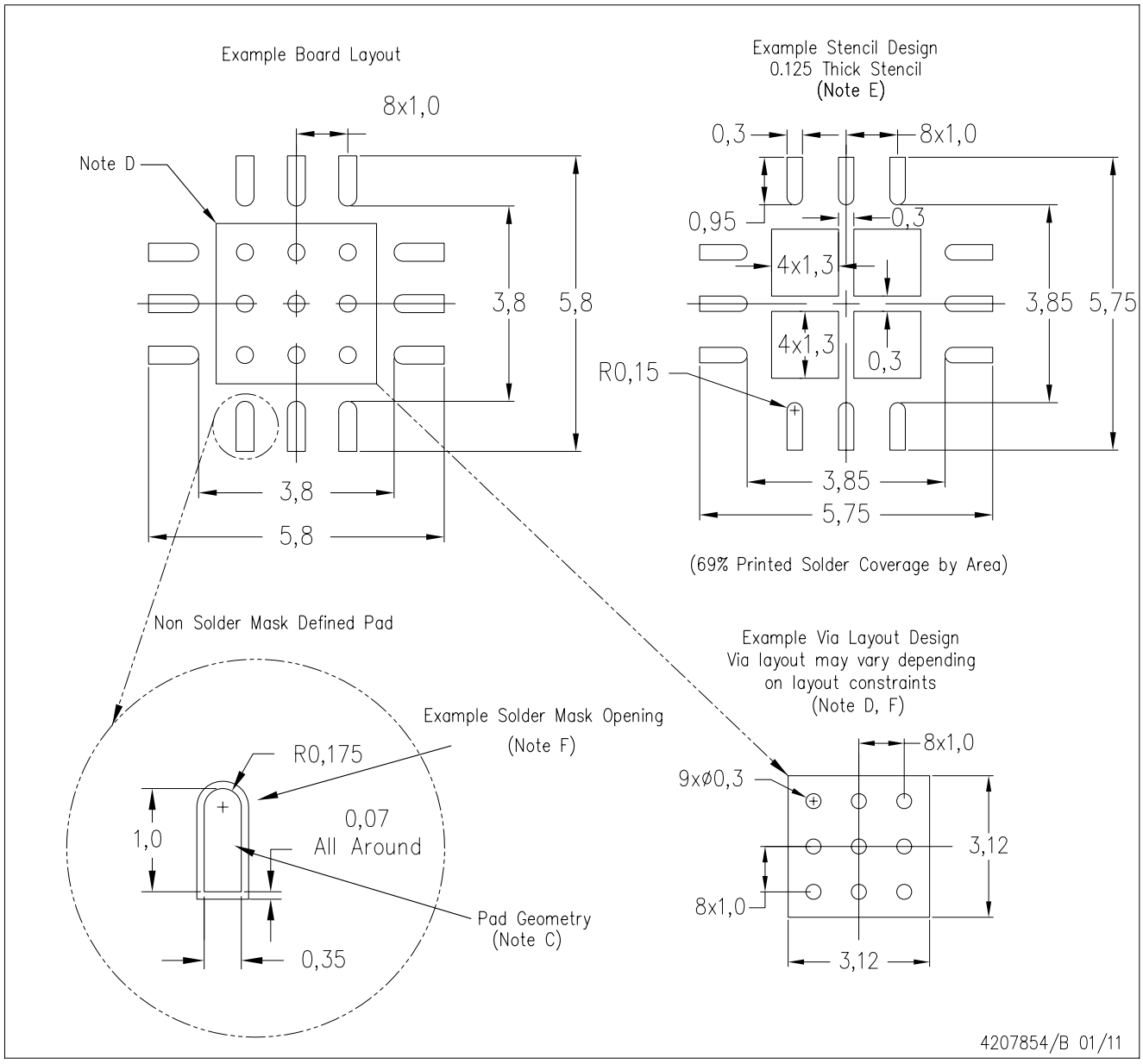
Bottom View

Exposed Thermal Pad Dimensions

4206361/D 01/11

NOTE: A. All linear dimensions are in millimeters

RHG (S–PVQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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