OPAx391 Precision, Ultra-Low I_Q, Low Offset Voltage, e-trim™ Operational Amplifiers

1 Features

- Low I_Q: 24µA
- Gain bandwidth product: 1MHz
- Low input bias current: 10fA
- Low offset voltage: ±45µV (maximum)
- Low drift: ±1.2µV/°C
- Low supply voltage operation: 1.7V to 5.5V
- Input common mode range ±100mV beyond rail
- Fast slew rate: 1V/µs
- High load capacitance drive
- High output current drive: 60mA
- Rail-to-rail output
- EMI and RFI filtered inputs
- Small package options: SC-70, DSBGA

2 Applications

- Portable electronics
- Flow transmitter
- Blood glucose monitor
- Process analytics (pH, gas, force, humidity)
- Temperature transmitter
- Pressure transmitter
- Medical sensor patches
- Building automation
- Wearable fitness and activity monitor
- Gas detector
- Analog security camera

3 Description

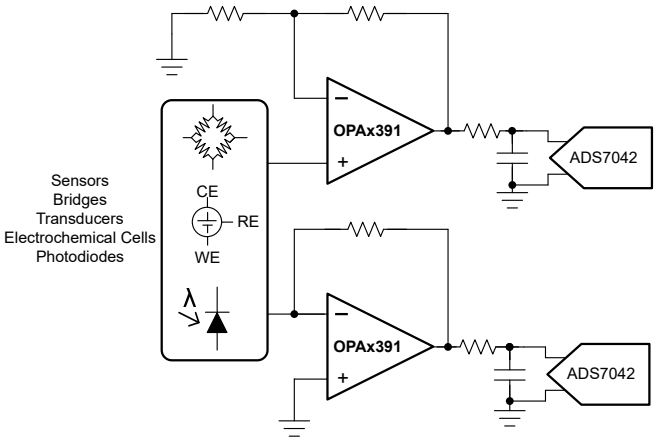
The OPA391, OPA2391, and OPA4391 (OPAx391) devices feature a unique combination of high bandwidth (1MHz) along with very-low quiescent current (24µA) in high-precision amplifiers. These features combined with rail-to-rail input and output make these devices an exceptional choice in high-gain, low-power applications. Ultra-low input bias current of 10fA, only 45µV of offset (maximum), and 1.2µV/°C of drift over temperature help maintain high precision in ratiometric and amperometric sensor front ends that have demanding low-power requirements.

The OPAx391 use Texas Instruments' proprietary e-trim™ operational amplifier technology, enabling a unique combination of ultra-low offset and low input offset drift without the need for any input switching or auto-zero techniques. The CMOS-based technology platform also features a modern, robust output stage design that is tolerant of high output capacitance, alleviating stability problems that are common in typical low-power amplifiers.

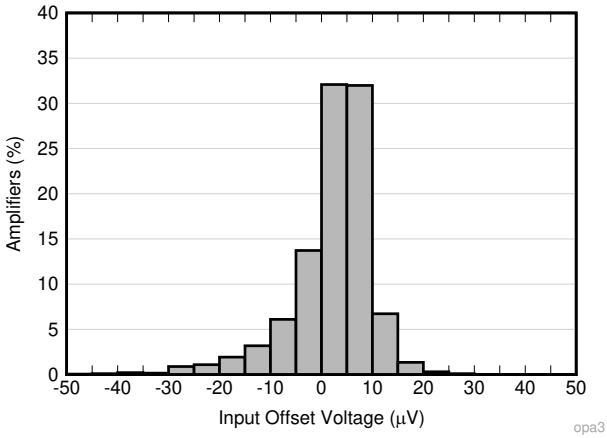
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
OPA391	Single	DBV (SOT-23, 5)(2)
		DCK (SC70, 5)
OPA2391	Dual	D (SOIC, 8)(2)
		DGK (VSSOP, 8)
		YBJ (DSBGA, 9)
OPA4391	Quad	PW (TSSOP, 14)

(1) For more information, see Section 10.
(2) Preview information (not Production Data).



High Input Impedance, Low Offset Buffer



OPA391 Offset Voltage

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....2
5 Specifications....5
5.1 Absolute Maximum Ratings....5
5.2 ESD Ratings....5
5.3 Recommended Operating Conditions....5
5.4 Thermal Information: OPA391....6
5.5 Thermal Information: OPA2391....6
5.6 Thermal Information: OPA4391....6
5.7 Electrical Characteristics: OPA391DCK and OPA2391YBJ....7
5.8 Electrical Characteristics: OPA2391DGK and OPA4391PW....9
5.9 Typical Characteristics....11
6 Detailed Description....18
6.1 Overview....18
6.2 Functional Block Diagram....18
6.3 Feature Description....19
6.4 Device Functional Modes....20
7 Application and Implementation....21
7.1 Application Information....21
7.2 Typical Applications....21
7.3 Power Supply Recommendations....25
7.4 Layout....25
8 Device and Documentation Support....26
8.1 Device Support....26
8.2 Documentation Support....26
8.3 Receiving Notification of Documentation Updates....26
8.4 Support Resources....26
8.5 Trademarks....26
8.6 Electrostatic Discharge Caution....27
8.7 Glossary....27
9 Revision History....27
10 Mechanical, Packaging, and Orderable Information....27

4 Pin Configuration and Functions

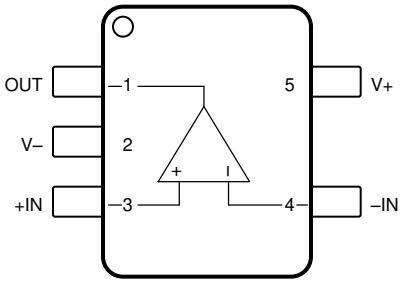


Figure 4-1. OPA391: DBV Package (Preview), 5-Pin SOT-23 (Top View)

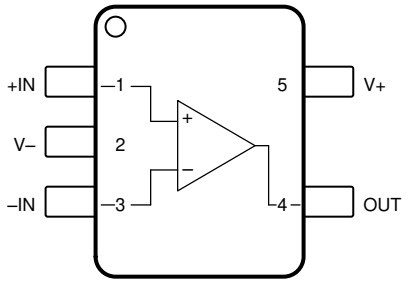


Figure 4-2. OPA391: DCK Package, 5-Pin SC-70 (Top View)

Table 4-1. Pin Functions: OPA391

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DBV (SOT-23)	DCK (SC70)		
–IN	4	3	Input	Inverting input
+IN	3	1	Input	Noninverting input
OUT	1	4	Output	Output
V–	2	2	Power	Negative (lowest) power supply
V+	5	5	Power	Positive (highest) power supply

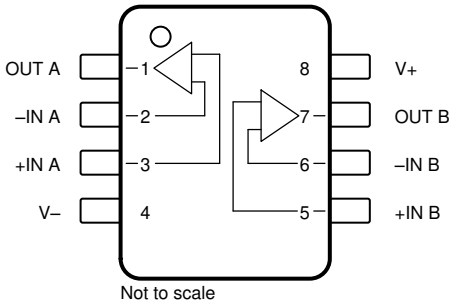


Figure 4-3. OPA2391: D Package (Preview), 8-pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

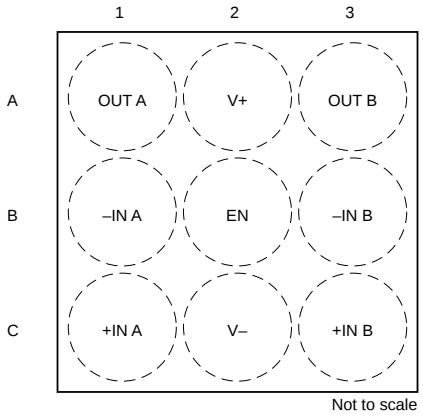


Figure 4-4. OPA2391: YBJ Package, 9-Pin DSBGA (Top View)

Table 4-2. Pin Functions: OPA2391

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	YBJ (DSBGA)		
EN	—	B2	Input	Enable pin. High = both amplifiers enabled.
–IN A	2	B1	Input	Inverting input, channel A
+IN A	3	C1	Input	Noninverting input, channel A
–IN B	6	B3	Input	Inverting input, channel B
+IN B	5	C3	Input	Noninverting input, channel B
OUT A	1	A1	Output	Output, channel A
OUT B	7	A3	Output	Output, channel B
V–	4	C2	Power	Negative (lowest) power supply
V+	8	A2	Power	Positive (highest) power supply

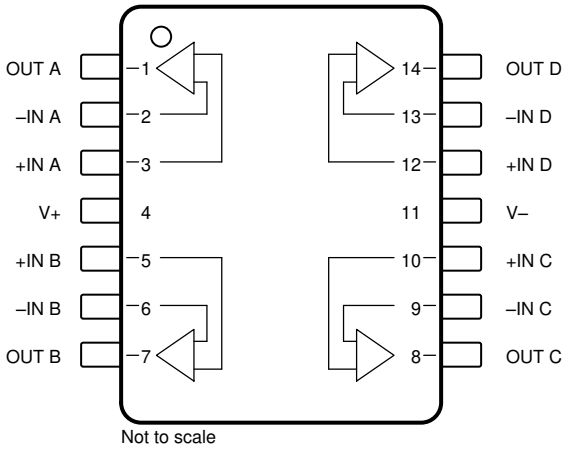


Figure 4-5. OPA4391: PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: OPA4391

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
+IN A	3	Input	Noninverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN B	5	Input	Noninverting input, channel B
–IN C	9	Input	Inverting input, channel C
+IN C	10	Input	Noninverting input, channel C
–IN D	13	Input	Inverting input, channel D
+IN D	12	Input	Noninverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V–	11	Power	Negative (lowest) power supply
V+	4	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.5	
	Input current, all pins			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
OPA391 and OPA2391				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	
OPA4391				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
	Differential input voltage		–0.5		0.5	V
T_A	Specified temperature	OPA391DCK, OPA2391YBJ	–40		125	°C
		OPA2391D, OPA2391DGK, OPA4391PW	–40		85	

5.4 Thermal Information: OPA391

THERMAL METRIC[1]		OPA391 DCK (SC-70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA2391

THERMAL METRIC[1]		OPA2391 D (SOIC) 8 PINS	OPA2391 DGK (VSSOP) 8 PINS	OPA2391 YBJ (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.8	152.1	110.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.7	61.7	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.3	86.8	32.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.6	5.2	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.6	85.5	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information: OPA4391

THERMAL METRIC[1]		OPA4391 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics: OPA391DCK and OPA2391YBJ

at V_S = 1.7 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.0 V			±10	±45	µV
		V_{CM} = (V+) – 0.3 V, V_S = 5.0 V			±60	±750	
		V_{CM} = (V–) – 0.1 V			±15	±80	
			T_A = –40°C to +125°C(1)			±600	
dV_{OS}/dT	Input offset voltage drift	T_A = 0°C to 85°C(1)			±1	±5	µV/°C
		T_A = –40°C to +125°C(1)			±1.2	±6	
PSRR	Power supply rejection ratio	V_{CM} = (V–) – 0.1 V				40	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C(1)			±0.01	0.8	pA
		T_A = 0°C to 85°C(1)				5	
		T_A = –40°C to +125°C(1)	OPA391DCK			30	
			OPA2391YBJ			35	
I_{OS}	Input offset current	T_A = 25°C(1)			±0.01	0.8	pA
		T_A = 0°C to 85°C(1)				5	
		T_A = –40°C to +125°C(1)				30	
NOISE							
	Input voltage noise	*f* = 0.1 Hz to 10 Hz, V_{CM} = (V–)			0.91		$µV_{RMS}$
					6.0		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			130		nV/√Hz
		f = 1 kHz			60		
		f = 10 kHz			55		
i_n	Input current noise density	f = 1 kHz			30		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	T_A = –40°C to +125°C(1)		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 1.5 V	OPA391DCK	89	100		dB
			OPA2391YBJ		100		
		(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 1.5 V, V_S = 5.5 V		100	121		
			T_A = –40°C to +125°C(1)	90	100		
		(V+) – 0.6 V ≤ V_{CM} ≤ (V+) + 0.1 V			69		
INPUT IMPEDANCE							
Z_{id}	Differential input impedance				0.1 || 1		GΩ || pF
Z_{ic}	Common-mode input impedance				1 || 1		TΩ || pF

5.7 Electrical Characteristics: OPA391DCK and OPA2391YBJ (continued)

at V_S = 1.7 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5 V	(V–) + 0.1 V < V_O < (V+) – 0.1 V, V_{CM} = (V–) –100 mV	100	121		dB
			(V–) + 0.45 V < V_O < (V+) – 0.45 V, V_{CM} = (V–) –100 mV, R_L = 2 kΩ	100	121		
		V_S = 1.7 V	(V–) + 0.1 V < V_O < (V+) – 0.1 V, V_{CM} = (V+) – 1.5 V	90	113		
			(V–) + 0.45 V < V_O < (V+) – 0.45 V, V_{CM} = (V+) – 1.5 V, R_L = 2 kΩ	90	107		
FREQUENCY RESPONSE							
UGB	Unity-gain bandwidth	G = 1	I_{OUT} = 0 µA		450		kHz
			I_{OUT} = 0 µA, R_L = 50 kΩ		0.85		MHz
			I_{OUT} = 100 µA		0.75		
GBW	Gain-bandwidth product	No load			1		MHz
SR	Slew rate	G = –1, 4-V step			1		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, G = 1, 1-V step			8		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			15		µs
OUTPUT							
V_O	Voltage output swing from rail	No load				3	mV
						10	
		R_L = 2 kΩ				40	
		T_A = –40°C to +125°C(1)	OPA391DCK			10	
			OPA2391YBJ			12	
I_{SC}	Short-circuit current	V_S = 5.5 V		45	60		mA
Z_O	Open-loop output impedance	f = 1 MHz, no load			1.6		kΩ
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = (V+) – 1.5 V			23.5	30	µA
			T_A = –40°C to +125°C(1)			32	
SHUTDOWN (OPA2391YBJ Only)							
I_{QSD}	Quiescent current per amplifier(2)	All amplifiers disabled, EN = (V–)			3.5		µA
V_{IH}	High-level input voltage(2)	Amplifier enabled		(V+) – 0.5			V
V_{IL}	Low-level input voltage(2)	Amplifier disabled				(V–) + 0.5	V
t_{ON}	Amplifier enable time(2)	G = 1, V_{OUT} = 0.9 × V_S/2(3)			75		µs
t_{OFF}	Amplifier disable time(2)	G = 1, V_{OUT} = 0.1 × V_S/2(3)			4		µs
	EN pin input leakage current(2)	V_{IH} = (V+)			±0.01		µA
		V_{IL} = (V–)			–0.3		

(1) Specification established from device population bench system measurements across multiple lots.
(2) Specified by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

5.8 Electrical Characteristics: OPA2391DGK and OPA4391PW

at V_S = 1.7 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.0 V	OPA2391DGK		±10	±70	µV
			OPA4391PW		±10	±85	
			V_{CM} = (V+) – 0.3 V		±60	±750	
		V_{CM} = (V–) – 0.1 V	OPA2391DGK		±15	±85	
			OPA4391PW		±15	±80	
dV_{OS}/dT	Input offset voltage drift	T_A = 0°C to 85°C(1)			±1	±5	µV/°C
PSRR	Power supply rejection ratio	V_{CM} = (V–) – 0.1 V				40	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C(1)			±0.01	0.8	pA
		T_A = 0°C to 85°C(1)				5	
I_{OS}	Input offset current	T_A = 25°C(1)			±0.01	0.8	pA
		T_A = 0°C to 85°C(1)				5	
NOISE							
	Input voltage noise	*f* = 0.1 Hz to 10 Hz, V_{CM} = (V–)			0.91		$µV_{RMS}$
					6.0		$µV_{PP}$
e_n	Input voltage noise density	f = 10 Hz			130		nV/√Hz
		f = 1 kHz			60		
		f = 10 kHz			55		
i_n	Input current noise density	f = 1 kHz			30		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	T_A = –40°C to +85°C(1)		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V ≤ V_{CM} ≤ (V+) – 1.5 V		86	100		dB
			V_S = 5.5 V	100	121		
		(V+) – 0.6 V ≤ V_{CM} ≤ (V+) + 0.1 V			69		
INPUT IMPEDANCE							
Z_{id}	Differential input impedance				0.1 || 1		GΩ || pF
Z_{ic}	Common-mode input impedance				1 || 1		TΩ || pF

5.8 Electrical Characteristics: OPA2391DGK and OPA4391PW (continued)

at V_S = 1.7 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5 V	(V–) + 0.1 V < V_O < (V+) – 0.1 V, V_{CM} = (V–) –100 mV	100	121		dB
			(V–) + 0.45 V < V_O < (V+) – 0.45 V, V_{CM} = (V–) –100 mV, R_L = 2 kΩ	100	121		
		V_S = 1.7 V	(V–) + 0.1 V < V_O < (V+) – 0.1 V, V_{CM} = (V+) – 1.5 V	90	113		
			(V–) + 0.45 V < V_O < (V+) – 0.45 V, V_{CM} = (V+) – 1.5 V, R_L = 2 kΩ	86	107		
FREQUENCY RESPONSE							
UGB	Unity-gain bandwidth	G = 1	I_{OUT} = 0 µA		450		kHz
			I_{OUT} = 0 µA, R_L = 50 kΩ		0.85		MHz
			I_{OUT} = 100 µA		0.75		
GBW	Gain-bandwidth product	No load			1		MHz
SR	Slew rate	G = –1, 4-V step			1		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, G = 1, 1-V step			8		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			15		µs
OUTPUT							
V_O	Voltage output swing from rail	No load				3	mV
						10	
		R_L = 2 kΩ				40	
I_{SC}	Short-circuit current	V_S = 5.5 V		45	60		mA
Z_O	Open-loop output impedance	f = 1 MHz, no load			1.6		kΩ
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = (V+) – 1.5 V			23.5	30	µA
			T_A = –40°C to +125°C(1)			32	

(1) Specification established from device population bench system measurements across multiple lots.

5.9 Typical Characteristics

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

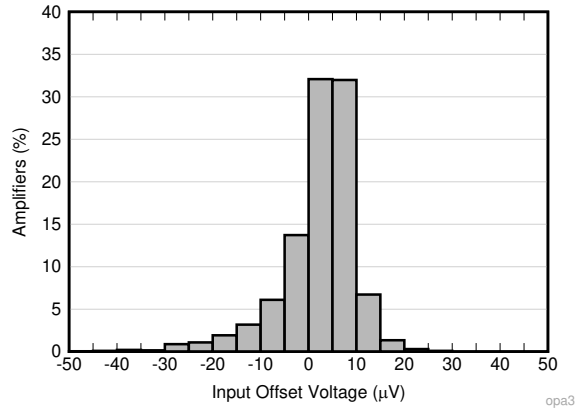
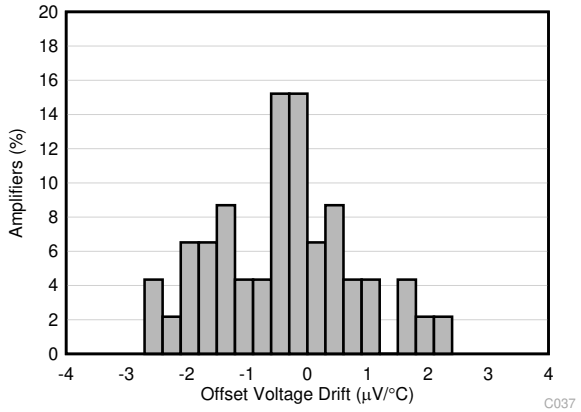
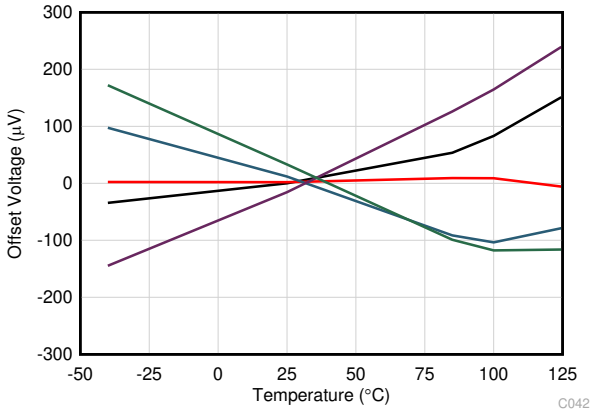


Figure 5-1. Offset Voltage Distribution



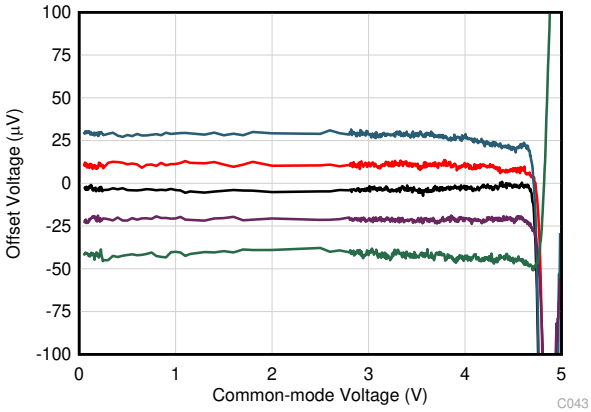
45 units, T_A = –40°C to +125°C

Figure 5-2. Offset Voltage Drift Distribution



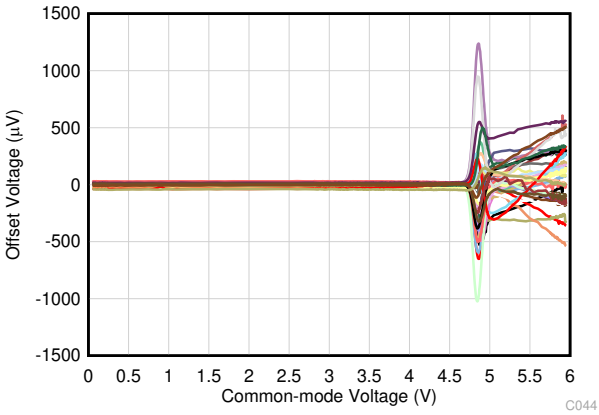
5 units

Figure 5-3. Offset Voltage vs Temperature



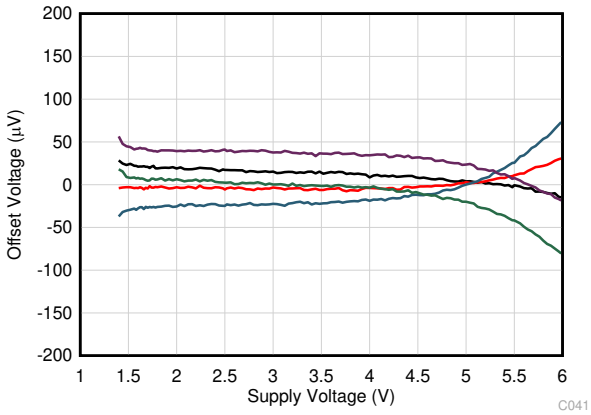
5 units

Figure 5-4. Offset Voltage vs Common-Mode Voltage



30 units, V_S = 5.5 V

Figure 5-5. Offset Voltage vs Common-Mode Voltage

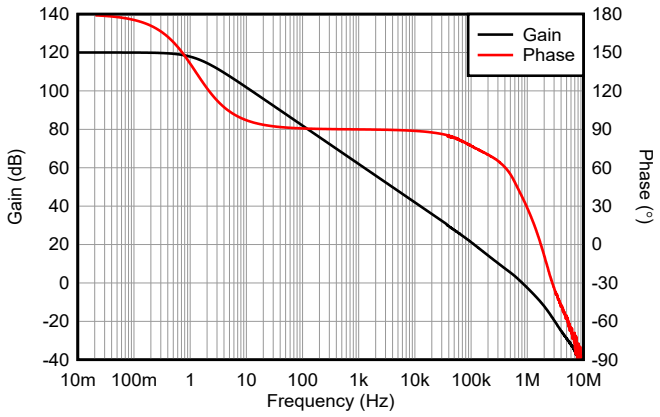


5 units, V_S = 5.5 V

Figure 5-6. Offset Voltage vs Supply Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



R_L = no load

Figure 5-7. Open-Loop Gain and Phase vs Frequency

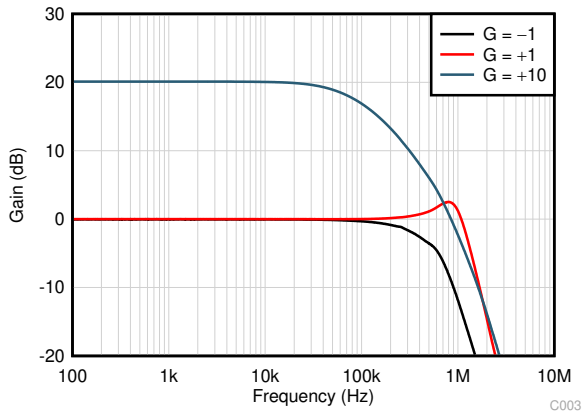
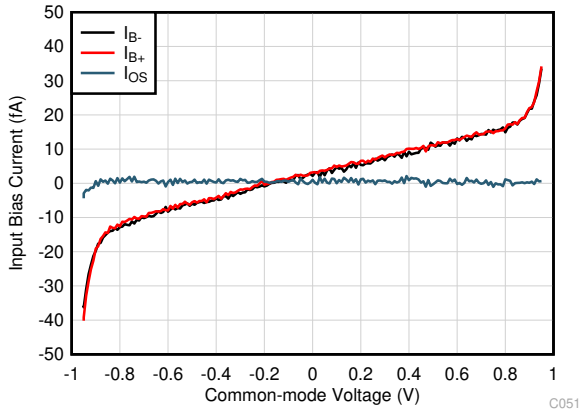
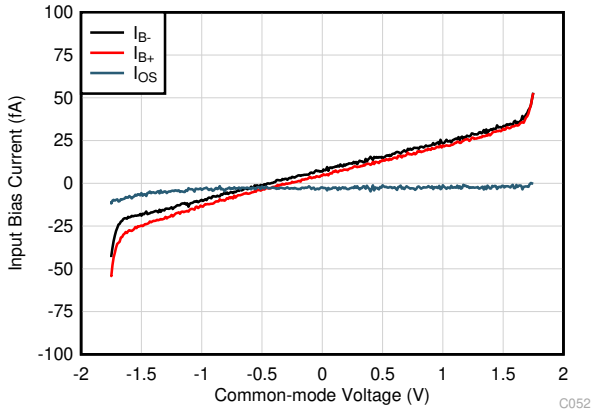


Figure 5-8. Closed-Loop Gain and Phase vs Frequency



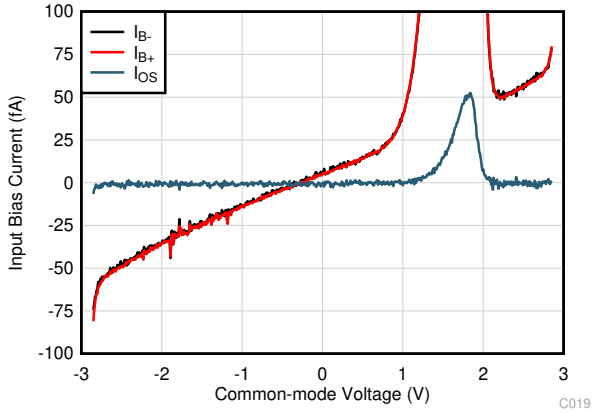
V_S = 1.7 V, common-mode voltage referenced to V_S / 2

Figure 5-9. Input Bias Current vs Common-Mode Voltage



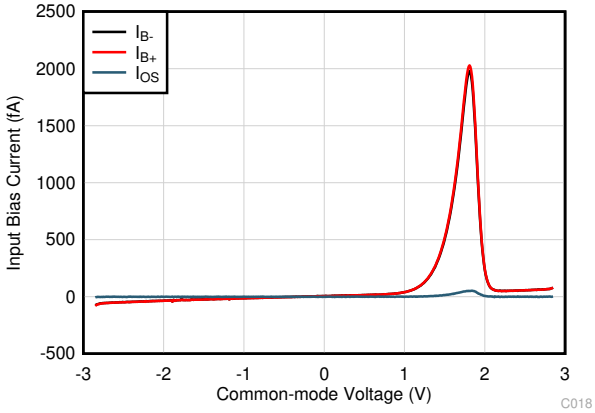
V_S = 3.3 V, common-mode voltage referenced to V_S / 2

Figure 5-10. Input Bias Current vs Common-Mode Voltage



V_S = 5.5 V, common-mode voltage referenced to V_S / 2

Figure 5-11. Input Bias Current vs Common-Mode Voltage



V_S = 5.5 V, common-mode voltage referenced to V_S / 2

Figure 5-12. Input Bias Current vs Common-Mode Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

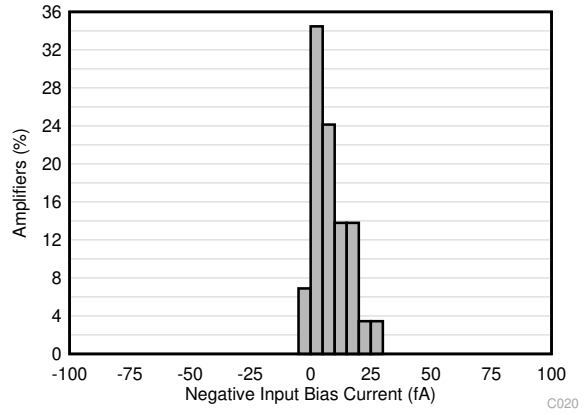


Figure 5-13. Negative Input Bias Current Distribution

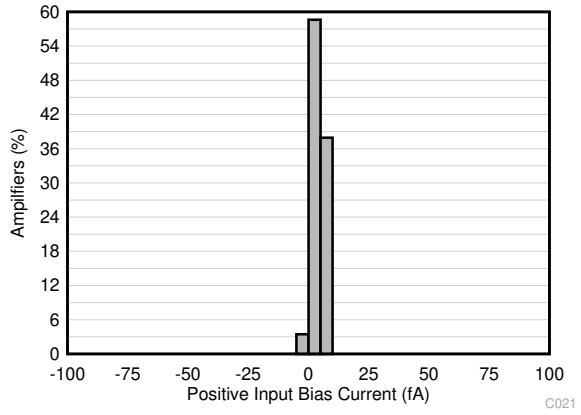


Figure 5-14. Positive Input Bias Current Distribution

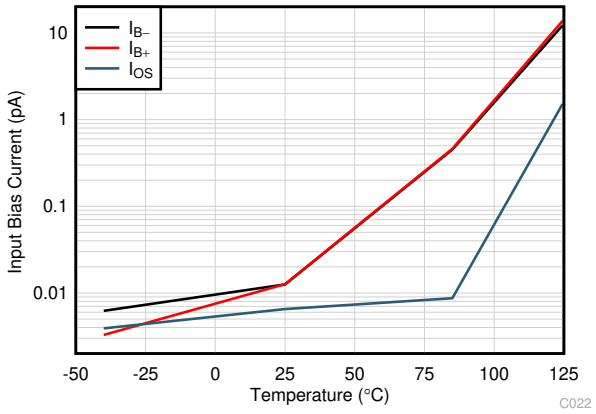


Figure 5-15. Input Bias Current vs Temperature

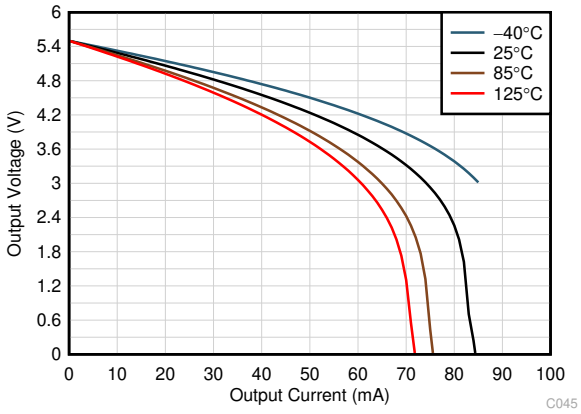


Figure 5-16. Output Voltage Swing vs Output Current (Maximum Supply)

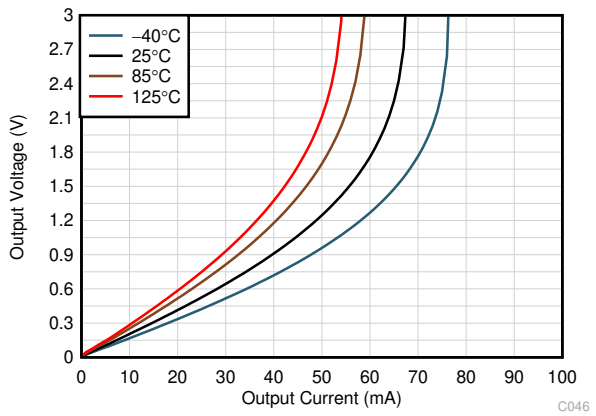


Figure 5-17. Output Voltage Swing vs Output Current (Maximum Supply)

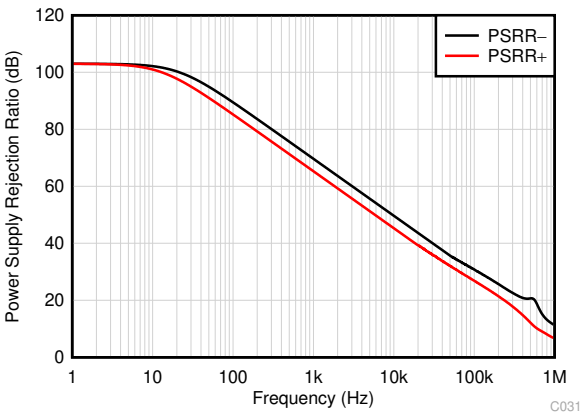
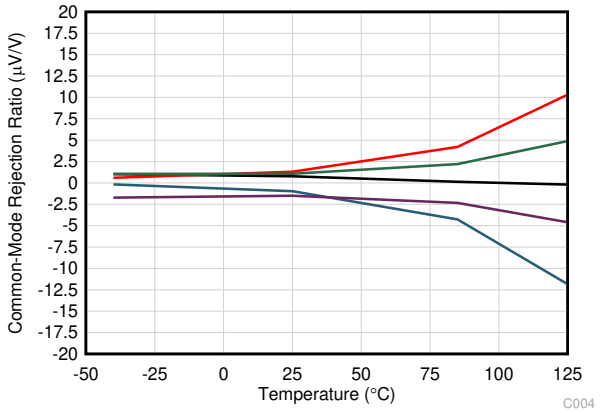


Figure 5-18. PSRR vs Frequency

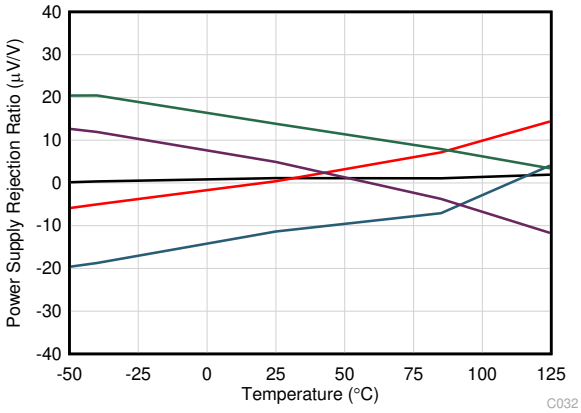
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



5 units

Figure 5-19. CMRR vs Temperature



5 units

Figure 5-20. PSRR vs Temperature

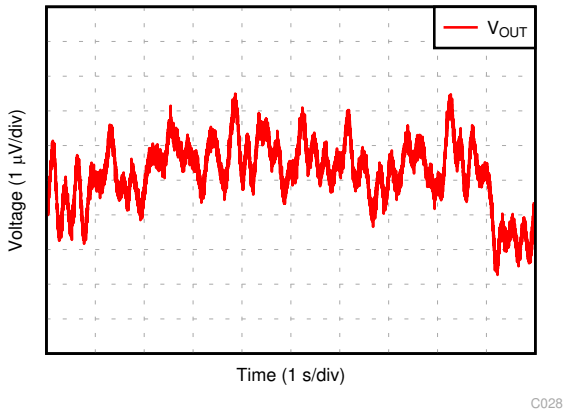


Figure 5-21. 0.1-Hz to 10-Hz Noise

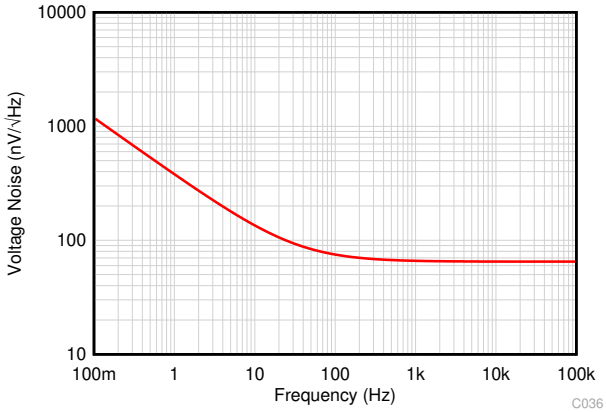
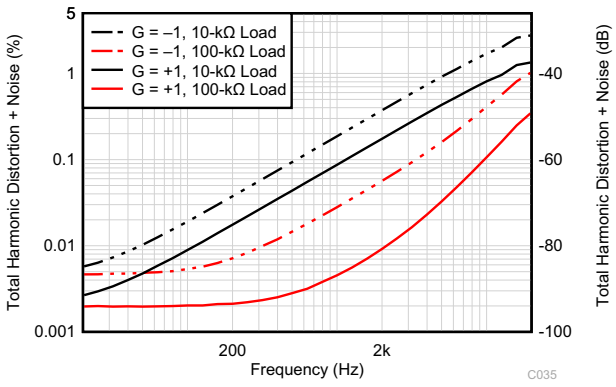
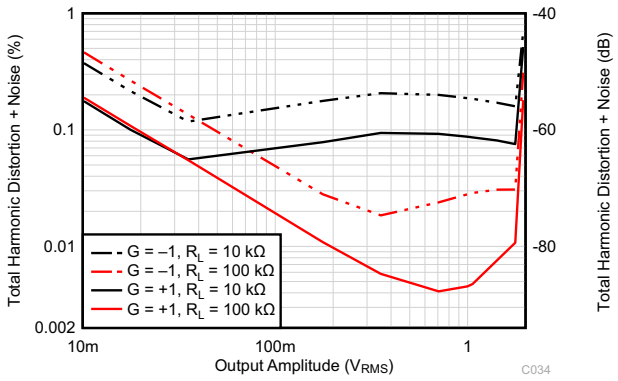


Figure 5-22. Input Voltage Noise Spectral Density vs Frequency



V_{OUT} = 1 V_{RMS}

Figure 5-23. THD+N Ratio vs Frequency



f = 1 kHz, filter BW = 80 kHz

Figure 5-24. THD+N vs Output Amplitude

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

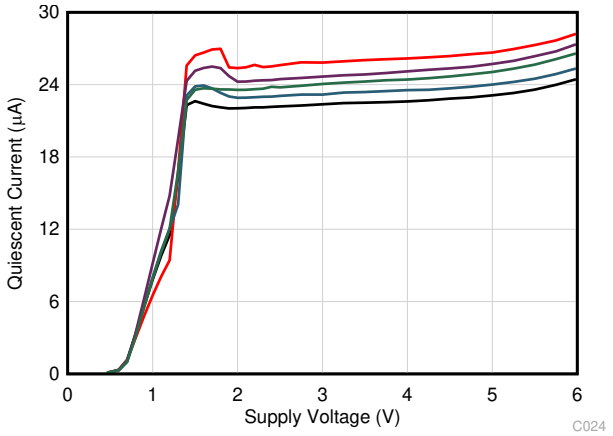


Figure 5-25. Quiescent Current vs Supply Voltage

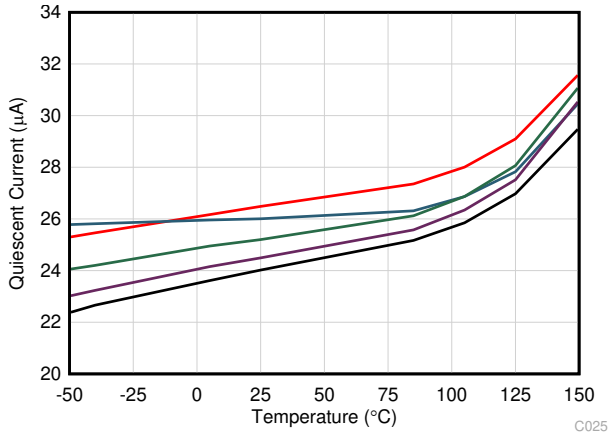


Figure 5-26. Quiescent Current vs Temperature

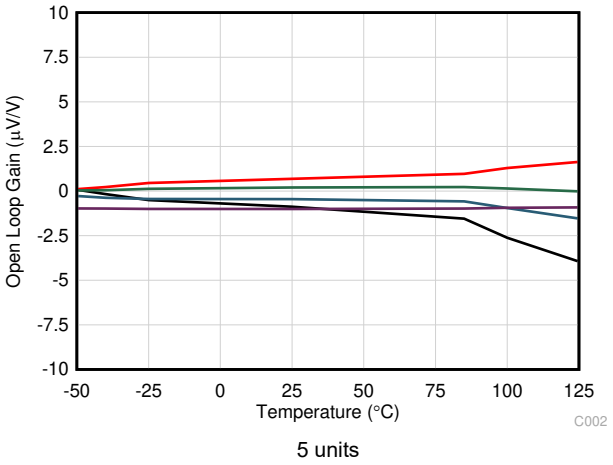


Figure 5-27. Open-Loop Gain vs Temperature

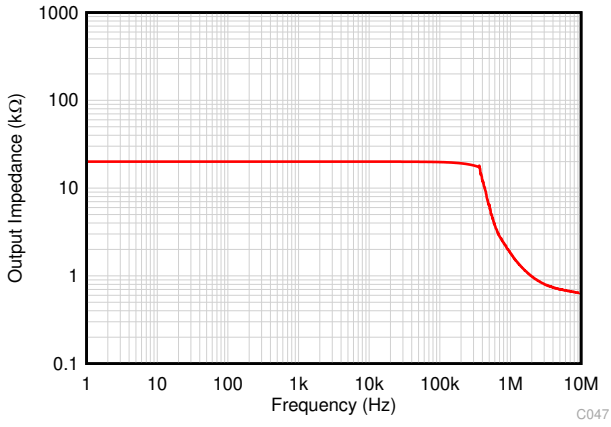


Figure 5-28. Open-Loop Output Impedance vs Frequency

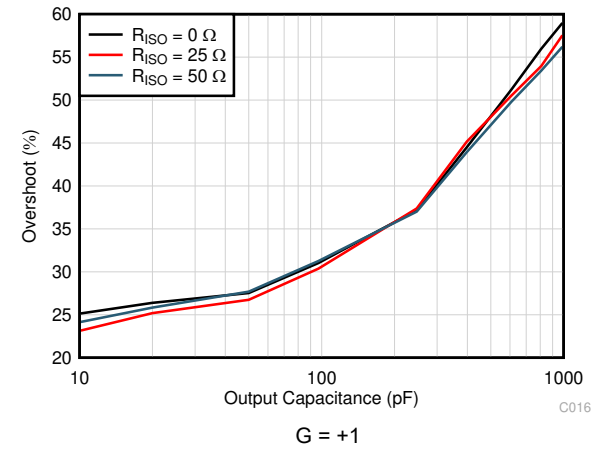


Figure 5-29. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

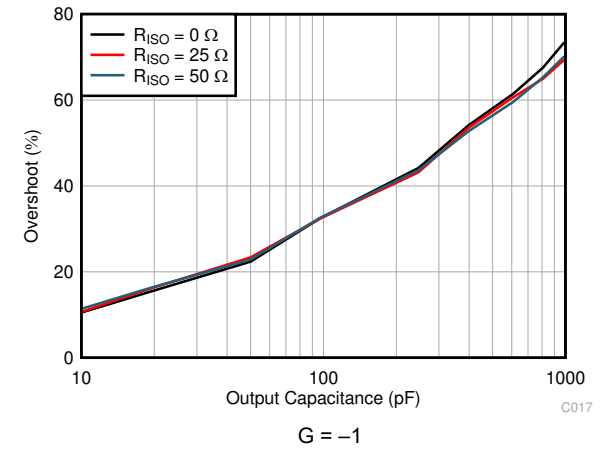


Figure 5-30. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

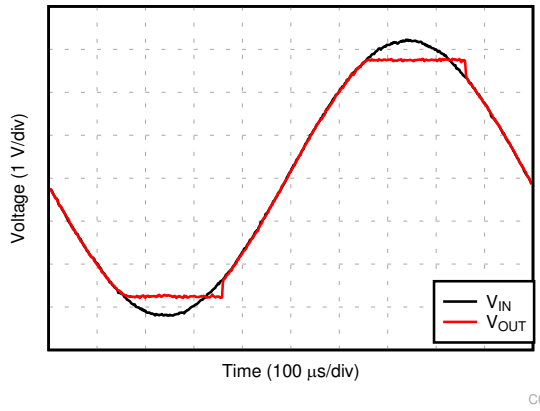


Figure 5-31. No Phase Reversal

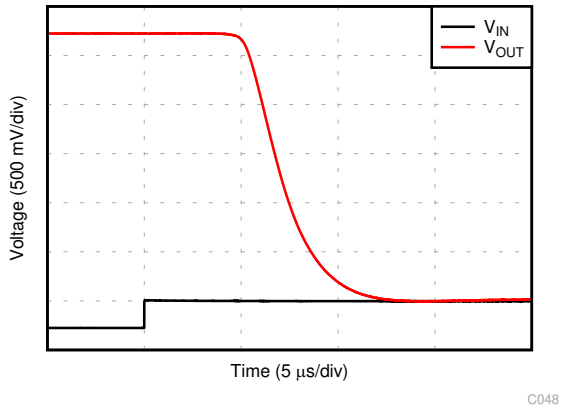


Figure 5-32. Positive Overload Recovery

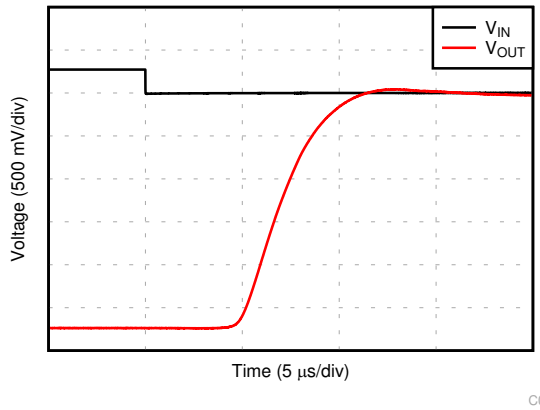
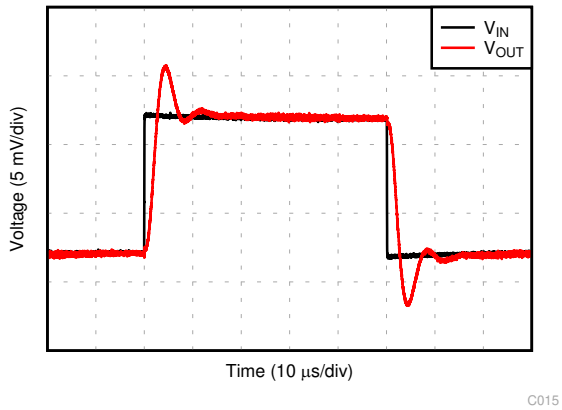
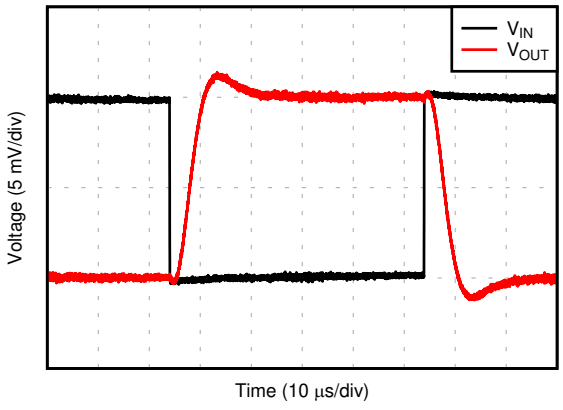


Figure 5-33. Negative Overload Recovery



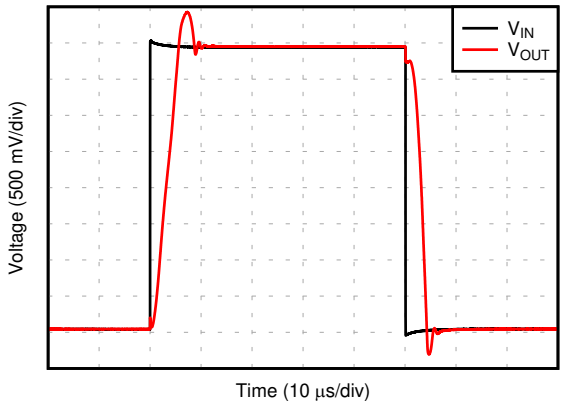
G = +1

Figure 5-34. Small-Signal Step Response (10-mV Step)



G = –1

Figure 5-35. Small-Signal Step Response (10-mV Step)

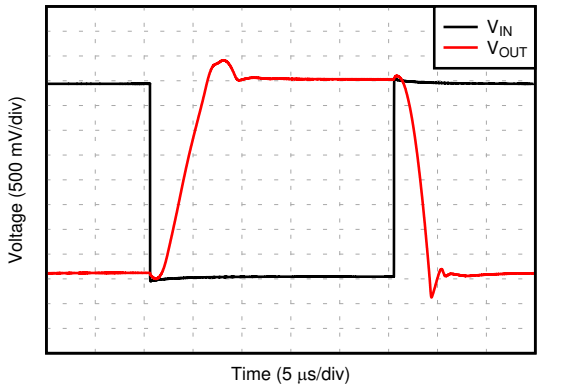


G = +1

Figure 5-36. Large-Signal Step Response (4-V Step)

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.0 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = –1

Figure 5-37. Large-Signal Step Response (4-V Step)

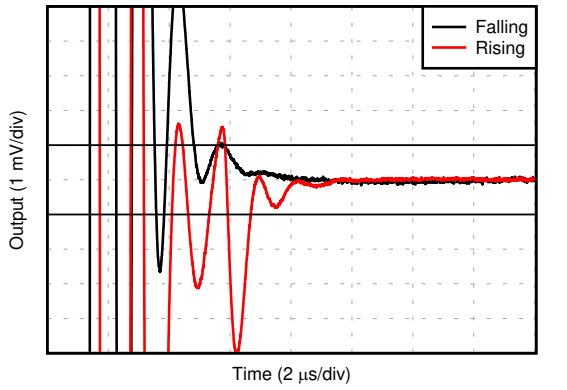


Figure 5-38. Settling Time (1-V Positive Step)

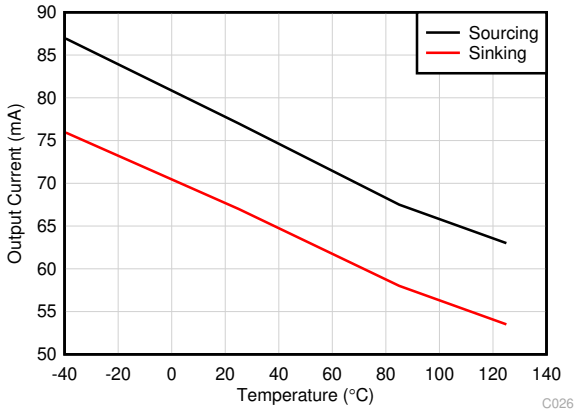


Figure 5-39. Short-Circuit Current vs Temperature

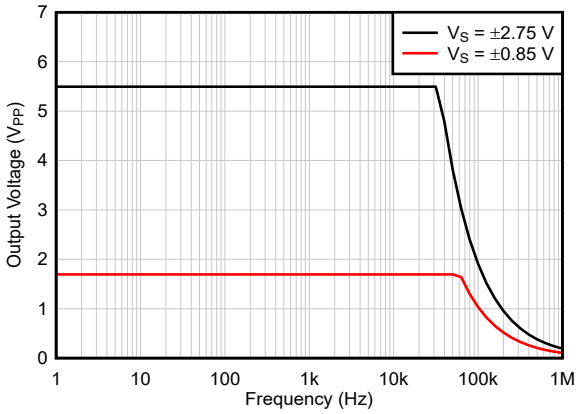
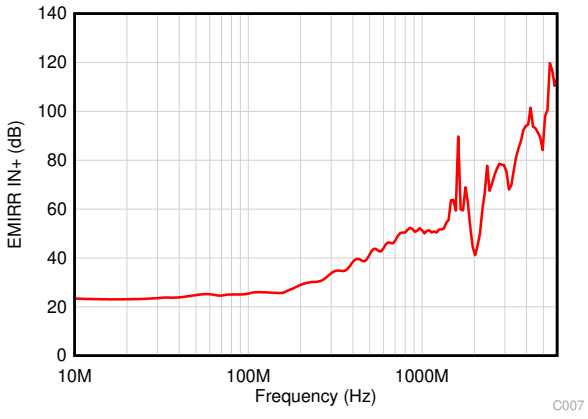


Figure 5-40. Maximum Output Voltage vs Frequency



P_{RF} = –10 dBm

Figure 5-41. EMIRR vs Frequency

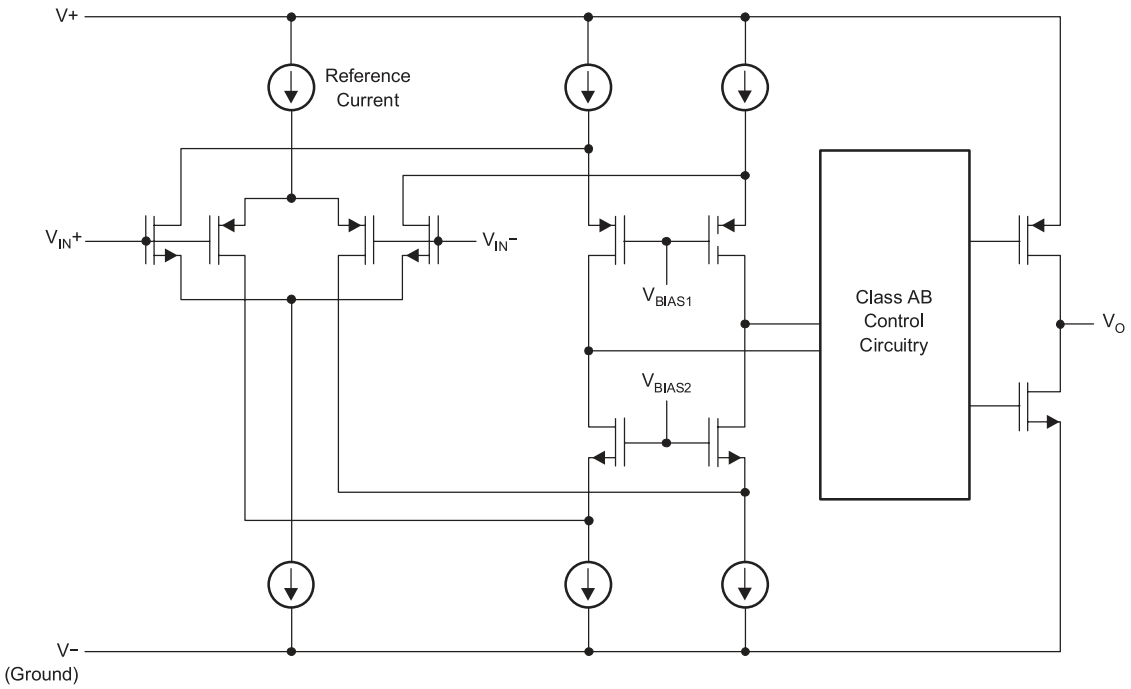
6 Detailed Description

6.1 Overview

The OPAx391 are low-offset, low-power, e-trim operational amplifiers (op amps) that uses a proprietary offset trim technique. These op amps offer ultra-low input offset voltage, drift, and input bias current, while achieving an excellent bandwidth-to-quiescent-current ratio. The OPAx391 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

The output features an advanced output stage that tolerates high capacitive loading for solid and stable performance. The OPAx391 strengths make these devices an excellent amplifier for high-impedance sensors, where input bias current, offset voltage, and power consumption are critical.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Input Bias Current

The OPAx391 achieve very low input bias current as a result of CMOS inputs and advanced electrostatic discharge (ESD) protection circuitry. Input bias current (I_B) is primarily a function of the input protection scheme in CMOS input amplifiers. If careful consideration is not taken with the ESD cells, a CMOS input device can exhibit large input bias currents, especially over temperature. The OPAx391 achieve excellent input bias current ratings of ±30 pA maximum at 125°C.

6.3.2 Input Differential Voltage

The OPAx391 do not have any diodes connected between the input nodes, allowing for input voltages anywhere between the supply voltage. The input structure can be seen in Figure 6-1. Although these devices can tolerate any differential input voltage that does not exceed the supply voltage, do not operate continuously at differential input voltages greater than 0.5 V.

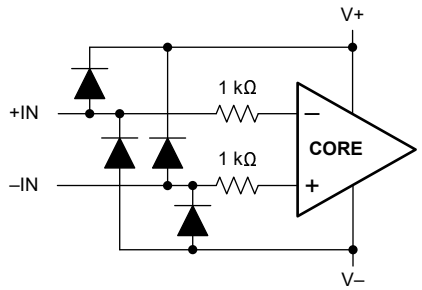


Figure 6-1. Equivalent Input Circuit

6.3.3 Capacitive Load Drive

The OPAx391 feature advanced output drive circuitry that maintain stability even with capacitive loads as high as 1 nF. Many low-quiescent-current amplifiers exhibit poor stability when connected to a capacitive load as a result of the low levels of current used to bias the output stage. The OPAx391 are designed with an output stage that adapts to high capacitive loads without sacrificing additional current consumption. This feature helps produce a highly stable device across all temperature and supply conditions, enabling robust system performance.

6.3.4 EMI Rejection

The OPAx391 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx391 benefit from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 6-2 shows the results of this testing on the OPAx391. Table 6-1 lists the EMIRR +IN values for the OPAx391 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 6-1 can be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects because the amplifier does not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Make sure to properly shield and isolate sensitive analog nodes from noisy radio signals, digital clocks, and interfaces.

The EMIRR +IN of the OPAx391 is plotted versus frequency as shown in Figure 6-2. The OPAx391 unity-gain bandwidth is 1 MHz. EMIRR performance less than this frequency denotes interfering signals that fall within the op amp bandwidth.

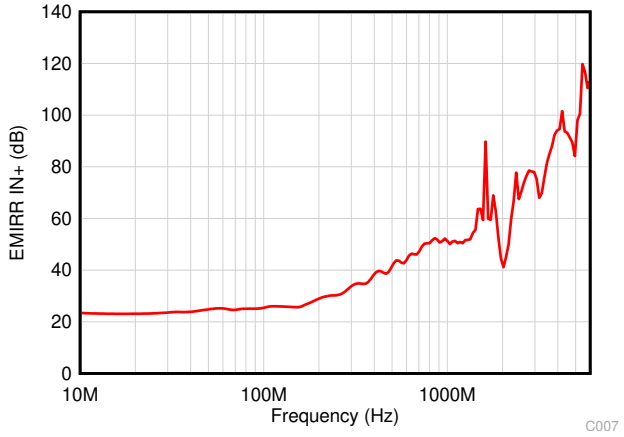


Figure 6-2. EMIRR Testing

Table 6-1. OPAx391 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	39.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	46.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.3 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.8 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	83.6 dB

6.4 Device Functional Modes

The OPAx391 have a single functional mode and are operational when the power-supply voltage is greater than 1.7 V (±0.85 V). The maximum specified power-supply voltage for the OPAx391 is 5.5 V (±2.75 V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx391 are unity-gain stable, precision operational amplifier free from unexpected output and phase reversal. The OPAx391 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies and can tolerate the full supply voltage across the input. The OPAx391 precision amplifier is designed for sensor amplification, low-power analog signal chain applications in low or high gains, as well as a low-power discrete MOSFET or bipolar driver.

7.2 Typical Applications

7.2.1 Three-Terminal CO Gas Sensor

Figure 7-1 shows a simple micropower potentiostat circuit for use with three-terminal unbiased CO sensors. This same design is applicable to many other type of three-terminal gas sensors or electrochemical cells. The basic sensor has three electrodes: the sense or working electrode (WE), counter electrode (CE), and reference electrode (RE). A current flows between CE and WE proportional to the detected concentration. The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE must be maintained at the same potential by adjusting the bias on CE. Through the potentiostat circuit formed by U1, the servo feedback action maintains the RE pin at a potential set by V_{REF}. R1 maintains stability as a result of the large capacitance of the sensor. C1 and R2 form the potentiostat integrator and set the feedback time constant. U2 forms a transimpedance amplifier (TIA) to convert the resulting sensor current into a proportional voltage. Equation 1 calculates the transimpedance gain, and resulting sensitivity, using R_F:

$$V_{TIA} = (-I \times R_F) + V_{REF} \quad (1)$$

R_{Load} is a load resistor with a value that is normally specified by the sensor manufacturer (typically, 10 Ω). The potential at WE is set by the applied V_{REF}.

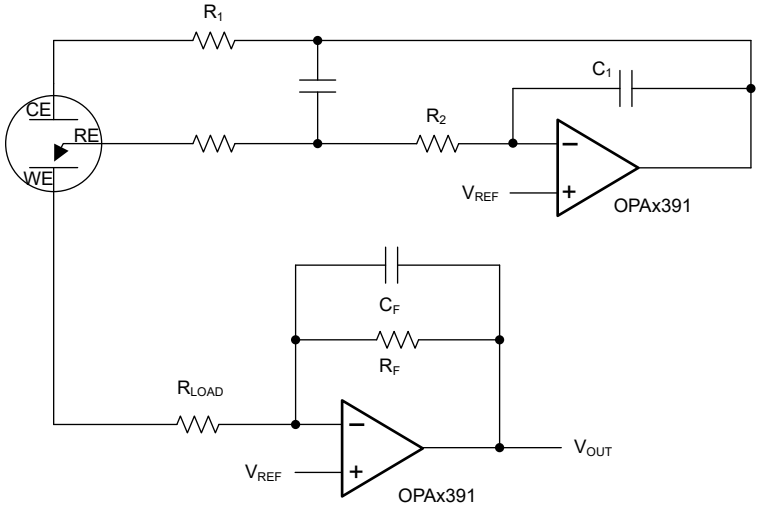


Figure 7-1. Three-Terminal CO Gas Sensor

7.2.1.1 Design Requirements

For this example, Figure 7-2 shows an electrical model of a CO sensor is used to simulate the sensor performance. The simulation is designed to model a CO sensor with a sensitivity of 69 nA/ppm. The supply voltage and maximum analog-to-digital converter (ADC) input voltage is 2.5 V, and the maximum concentration is 300 ppm.

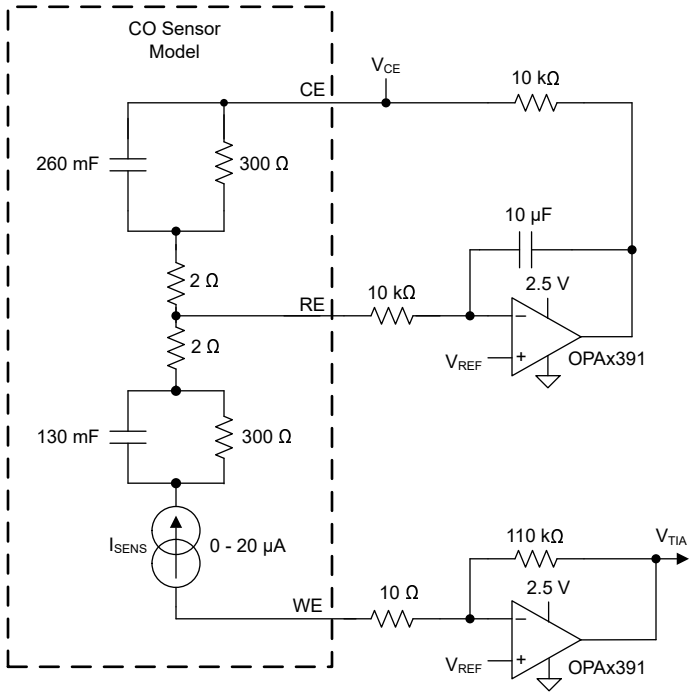


Figure 7-2. CO Sensor Simulation Schematic

7.2.1.2 Detailed Design Procedure

First, determine the V_{REF} voltage. This voltage is a compromise between maximum headroom and resolution, as well as allowance for the minimum swing on the CE terminal because the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180 mV at 300 ppm for this particular sensor. To allow for negative CE swing, footroom, and voltage drop across the 10-kΩ resistor, 300 mV is chosen for V_{REF}.

$$V_{ZERO} = V_{REF} = 300\ mV \tag{2}$$

where

- V_{REF} is the reference voltage (300 mV).
- V_{ZERO} is the concentration voltage (300 mV).

Next, calculate the maximum sensor current at highest expected concentration:

$$I_{SENSMAX} = I_{PERPPM} \times ppmMAX = 69\ nA \times 300\ ppm = 20.7\ \mu A \tag{3}$$

where

- $I_{SENSMAX}$ is the maximum expected sensor current.
- I_{PERPPM} is the manufacturer specified sensor current in amperes per ppm.
- ppmMAX is the maximum required ppm reading.

Then, find the available output swing range greater than the reference voltage available for the measurement:

$$V_{SWING} = V_{OUTMAX} - V_{ZERO} = 2.5\ V - 0.3\ V = 2.2\ V \quad (4)$$

where

- V_{SWING} is the expected change in output voltage.
- V_{OUTMAX} is the maximum amplifier output swing.

Finally, calculate the transimpedance resistor (R_F) value using the maximum swing and the maximum sensor current:

$$R_F = \frac{V_{SWING}}{I_{SENSMAX}} = \frac{2.2\ V}{20.7\ \mu A} = 106.28\ k\Omega\ (\text{use } 110\ k\Omega \text{ for a common value}) \quad (5)$$

7.2.1.3 Application Curve

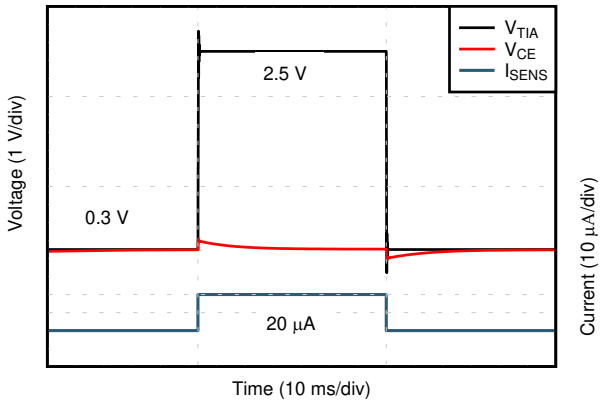


Figure 7-3. Sensor Transient Response to Simulated 300-ppm CO Exposure

7.2.2 4-mA to 20-mA Loop Design

Factory automation systems commonly use the 4-mA to 20-mA (4-20 mA) communication protocol to enable process automation. In typical 2-wire, 4-mA to 20-mA loop applications, power to the remote transmitter is limited to less than 4 mA total consumption. As a result of the power limitations, low power consumption is essential. The OPAx391 solves many design challenges in 4-mA to 20-mA loop applications, where low power, high accuracy, and high bandwidth are required.

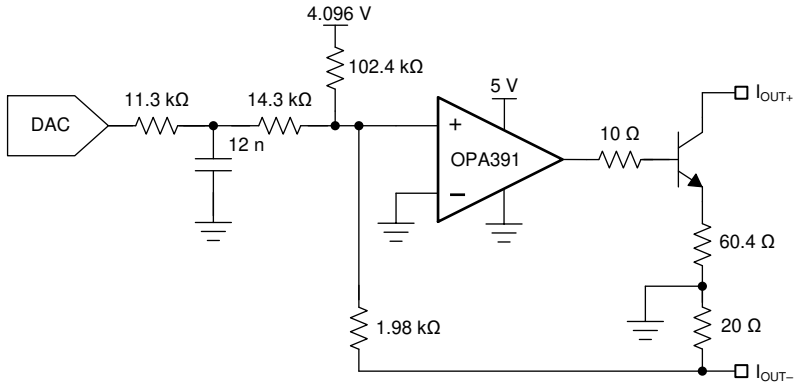


Figure 7-4. 4-20 mA Loop Interface Schematic

7.2.2.1 Application Curve

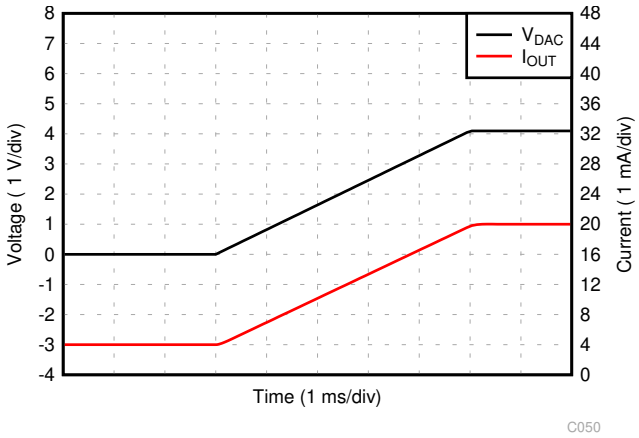


Figure 7-5. 4-mA to 20-mA Loop Response

7.3 Power Supply Recommendations

The OPAx391 devices are specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V).

7.4 Layout

7.4.1 Layout Guidelines

Paying attention to good layout practice is always recommended:

- Keep traces short.
- When possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close as possible to the device pins.
- Place a 0.1-µF capacitor closely across the supply pins.

These guidelines must be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

7.4.2 Layout Example

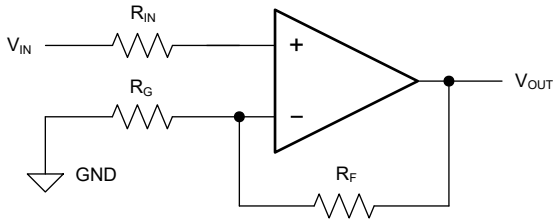


Figure 7-6. Schematic Representation

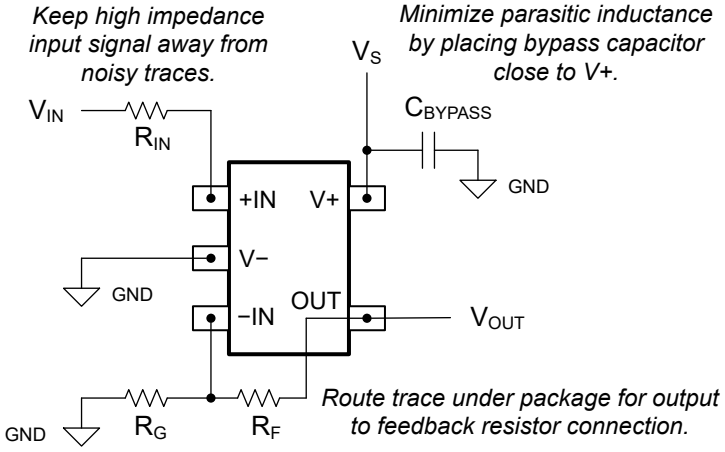


Figure 7-7. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem* reference design
- Texas Instruments, *Micropower Electrochemical Gas Sensor Amplifier* reference design
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively* application report
- Texas Instruments, *Designing With pH Electrodes* application report

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2024) to Revision E (October 2024) — **Page**

- Changed status of OPA2391 in DGK (VSSOP, 8) package from preview to production data (active)..... 1
- Changed the load condition for Gain-bandwidth product from 10kΩ to no load.....7
- Changed the min AOL of OPA4391 for the low supply condition from 90dB to 86dB based on the latest characterization data..... 9
- Changed the load condition for Gain-bandwidth product from 10kΩ to no load.....9

Changes from Revision C (December 2022) to Revision D (April 2024) — **Page**

- Changed status of OPA4391 in PW (TSSOP, 14) package from preview to production data (active)..... 1
- Added minimum value for Short-circuit current..... 7
- Changed the typical value of Open-loop output impedance from 500Ω to 1.6kΩ to match the typical characteristic curve.....7
- Changed I_Q from 24 µA to 23.5 µA based on the latest characterization data.....7

Changes from Revision B (November 2022) to Revision C (December 2022) — **Page**

- Changed status of OPA2391 in YBJ (DSBGA, 9) package from advanced information (preview) to production data (active) and added associated content.....1

Changes from Revision A (January 2021) to Revision B (November 2022) — **Page**

- Added OPA2391 advanced information (preview) device and associated content..... 1
- Added junction temperature to *Absolute Maximum Ratings* 5
- Changed JEDEC specification from JESD22-C101 to ANSI/ESDA/JEDEC JS-002.....5
- Changed input common-mode voltage condition for input voltage noise in the *Electrical Characteristics* 7
- Changed Figure 6-7, *Open-Loop Gain and Phase vs Freq*, Y-axis scale for clarity; no change to data..... 11
- Changed Figure 8-7, *Layout Example*, to show correct pin configuration and names..... 25

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2391DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3BKS
OPA2391YBJR	Active	Production	DSBGA (YBJ) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O91
OPA2391YBJT	Active	Production	DSBGA (YBJ) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O91
OPA391DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EJ
OPA391DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EJ
OPA4391PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4391

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

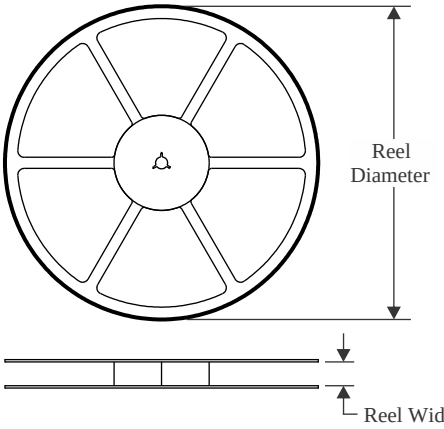
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

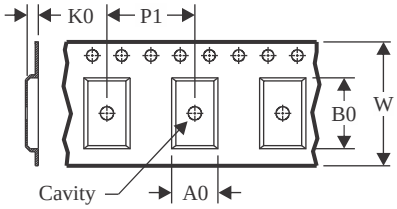
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

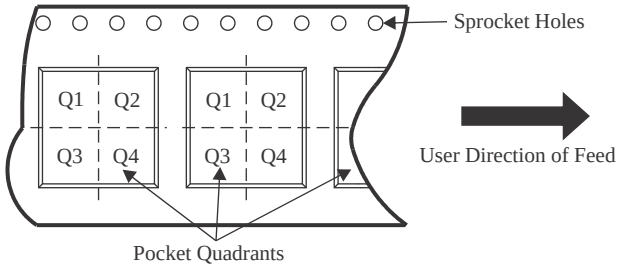


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

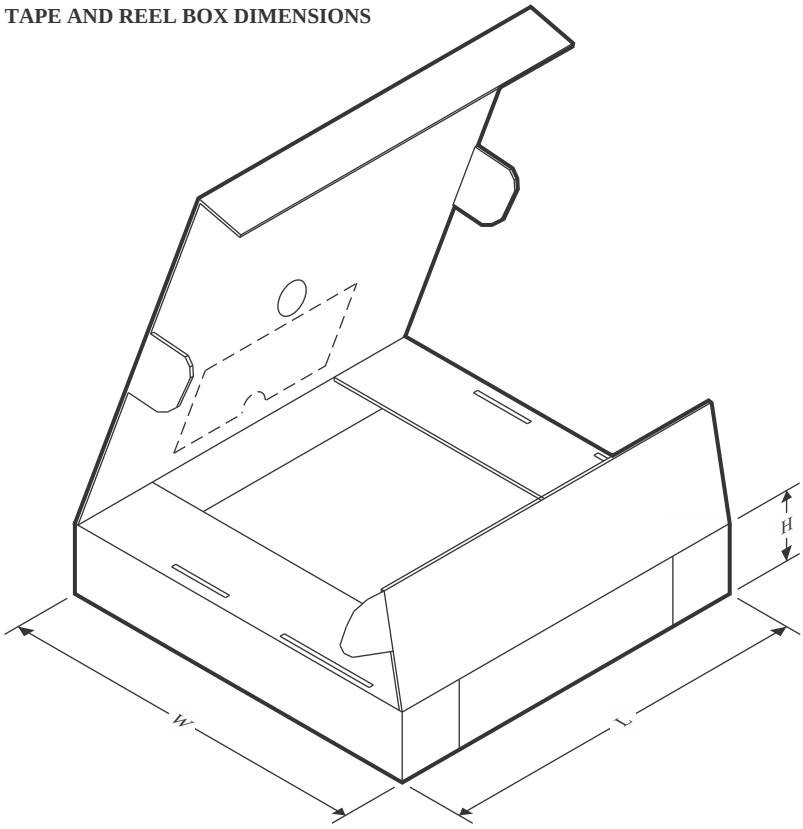
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2391DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2391YBJR	DSBGA	YBJ	9	3000	180.0	8.4	1.26	1.26	0.43	4.0	8.0	Q1
OPA2391YBJT	DSBGA	YBJ	9	250	180.0	8.4	1.26	1.26	0.43	4.0	8.0	Q1
OPA391DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA391DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4391PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

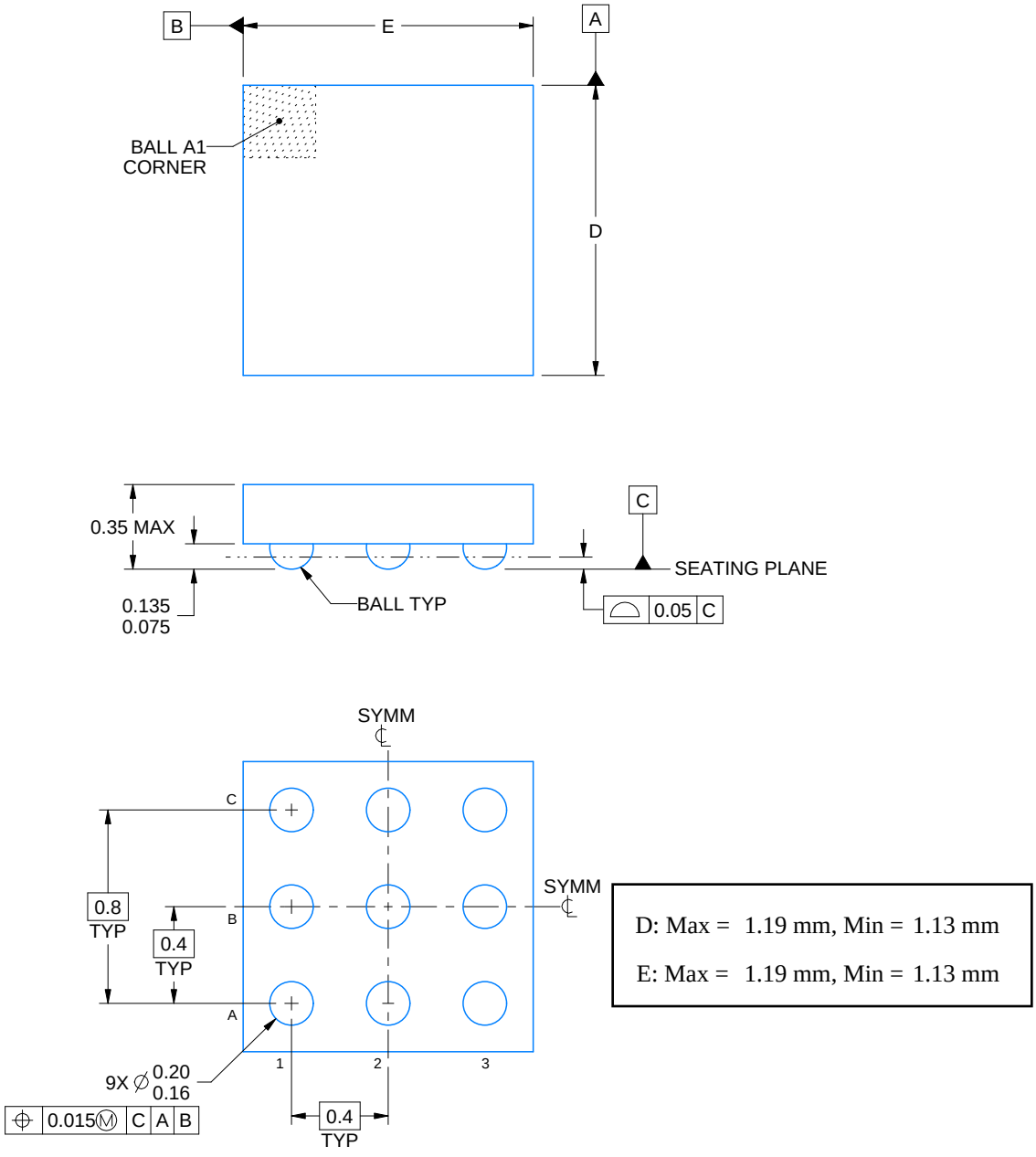
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2391DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2391YBJR	DSBGA	YBJ	9	3000	182.0	182.0	20.0
OPA2391YBJT	DSBGA	YBJ	9	250	182.0	182.0	20.0
OPA391DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA391DCKT	SC70	DCK	5	250	190.0	190.0	30.0
OPA4391PWR	TSSOP	PW	14	3000	356.0	356.0	35.0

YBJ0009

PACKAGE OUTLINE

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



4225688/A 02/2020

NOTES:

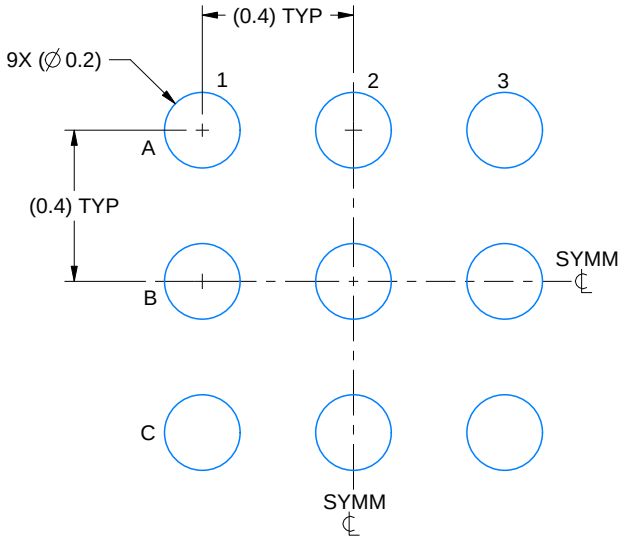
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

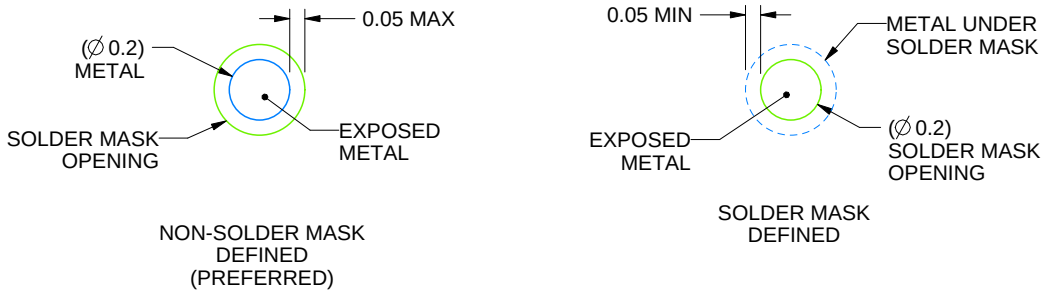
YBJ0009

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225688/A 02/2020

NOTES: (continued)

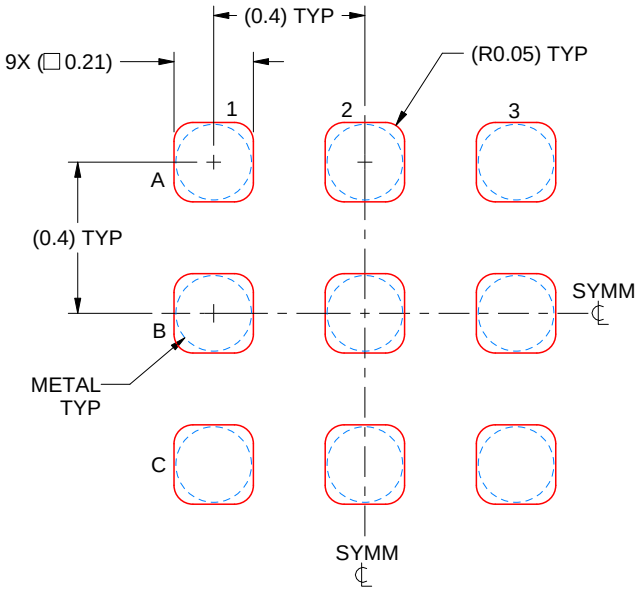
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBJ0009

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4225688/A 02/2020

NOTES: (continued)

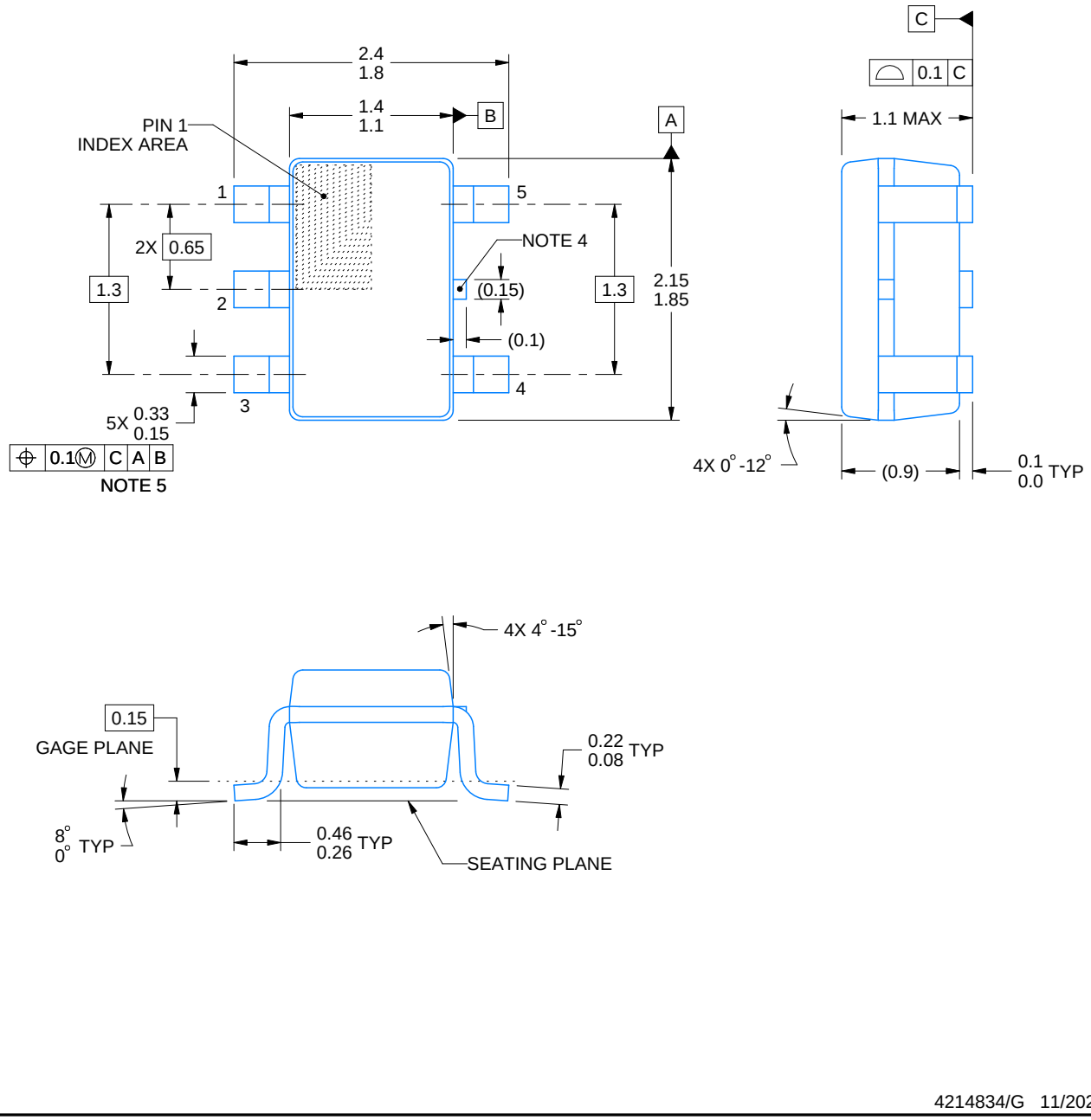
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

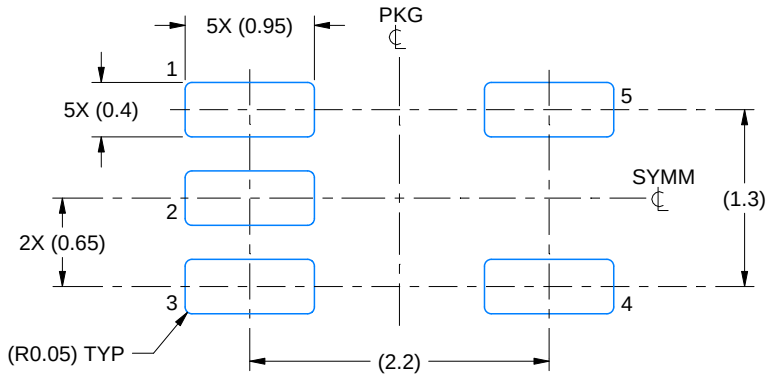
SMALL OUTLINE TRANSISTOR



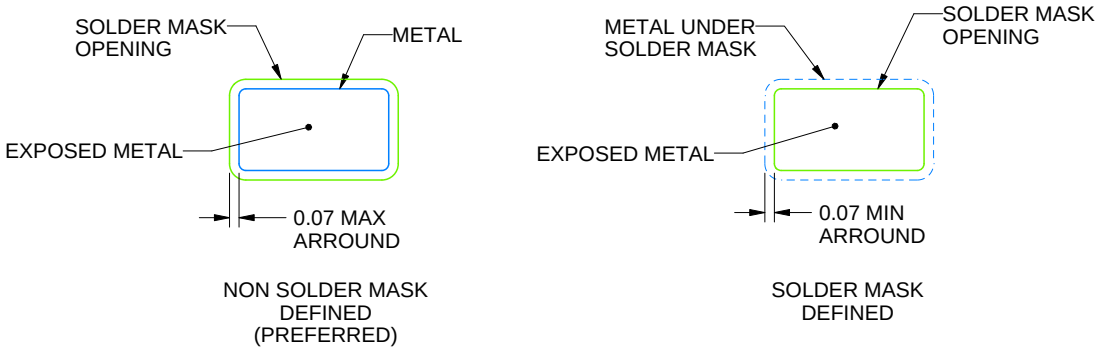
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

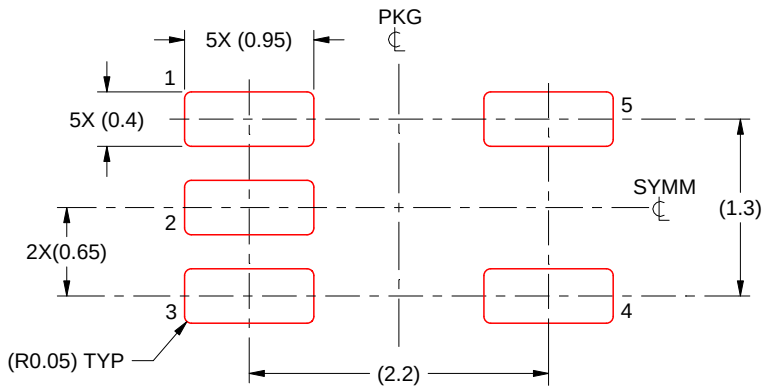


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

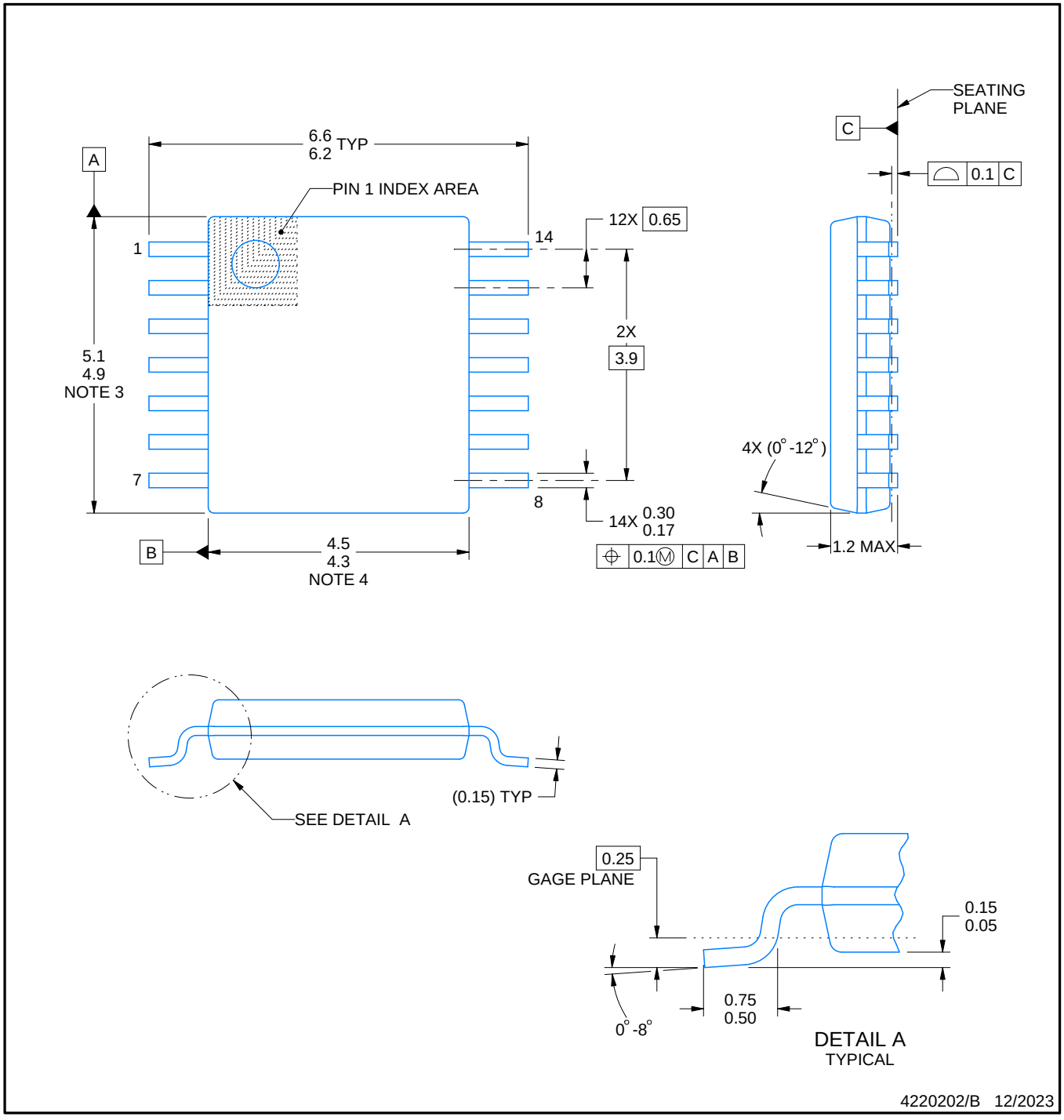
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

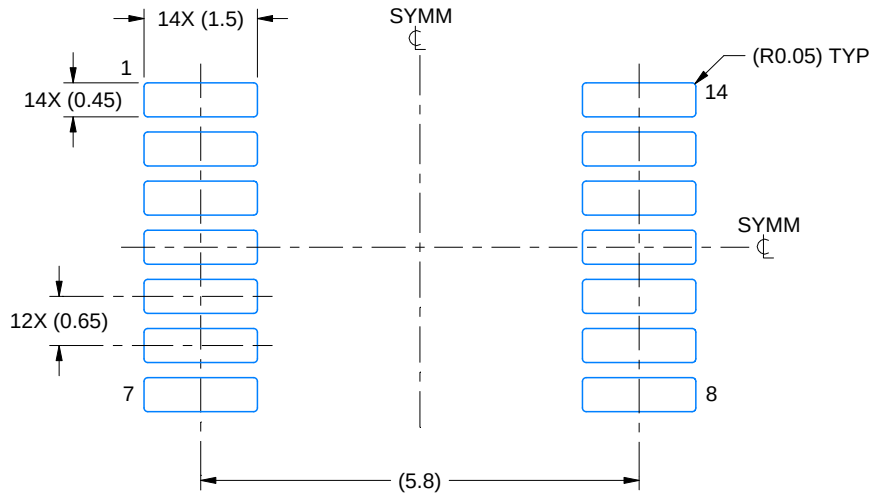
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

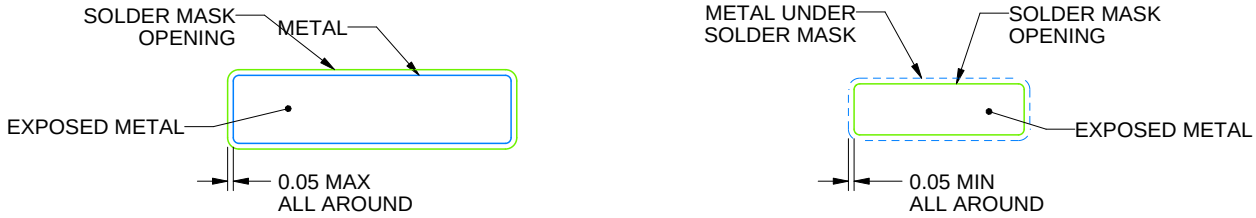


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

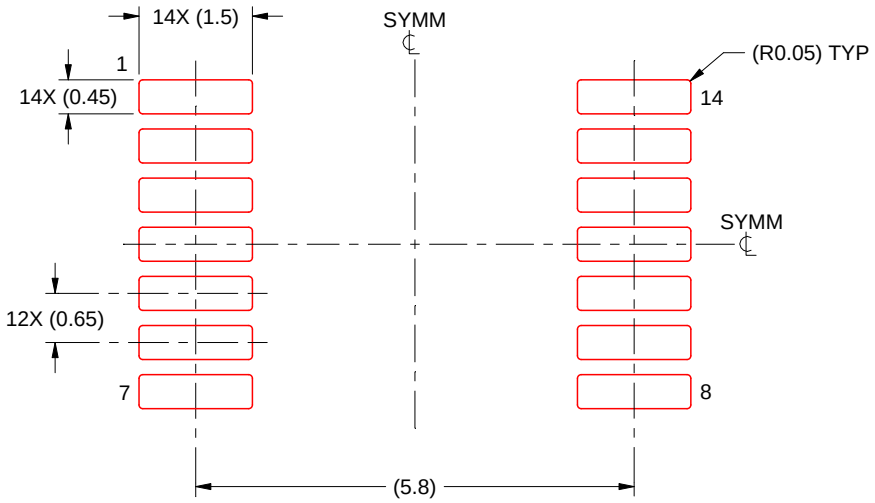


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

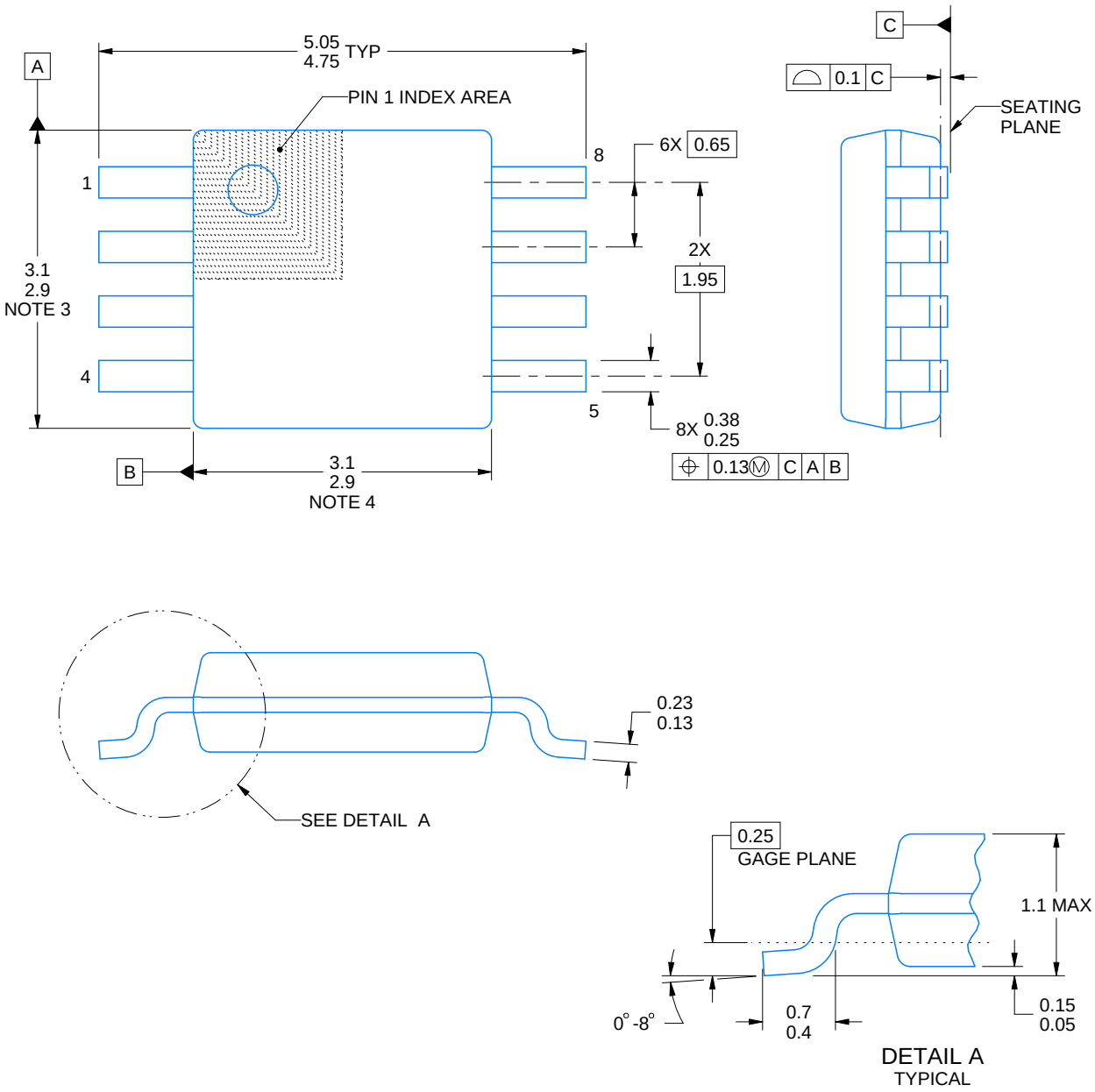
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

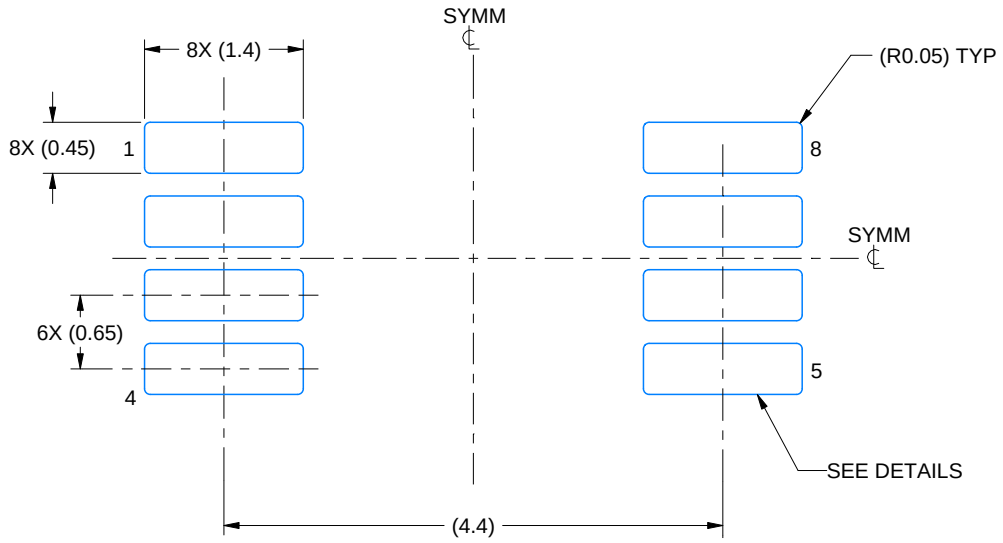
SMALL OUTLINE PACKAGE



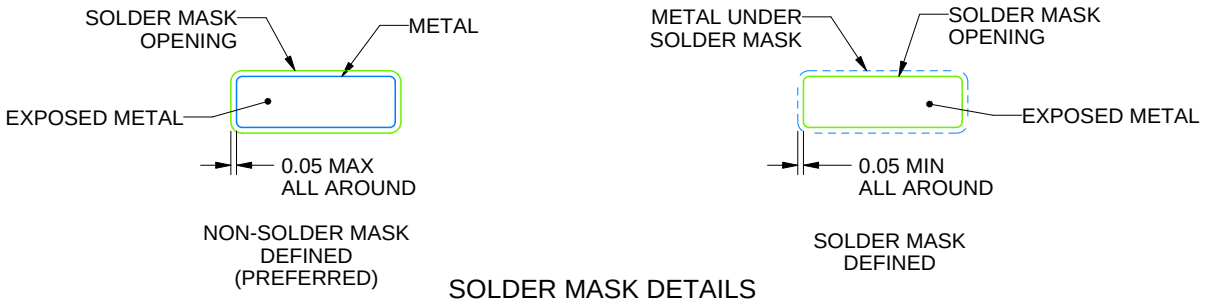
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

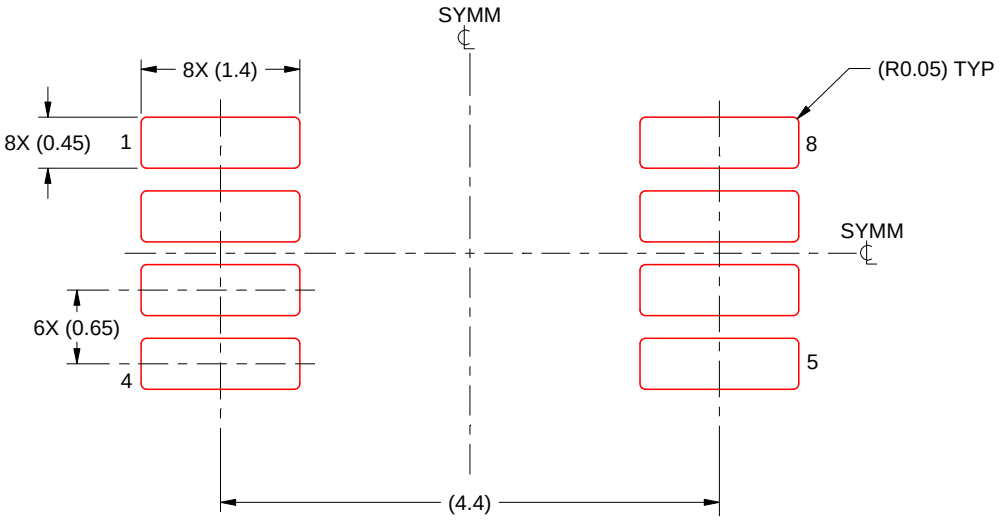


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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