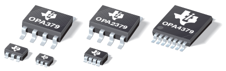


OPA379
OPA2379
OPA4379

1.8V, 2.9μA, 90kHz, Rail-to-Rail I/O OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 2.8μV_{PP} (0.1Hz - 10Hz)
- *micro*Power: 5.5μA (max)
- LOW OFFSET VOLTAGE: 1.5mV (max)
- DC PRECISION:
  - CMRR: 100dB
  - PSRR: 2μV/V
  - A_{OL}: 120dB
- WIDE SUPPLY VOLTAGE RANGE: 1.8V to 5.5V
- *micro*Size PACKAGES:
  - SC70-5, SOT23-5, SOT23-8, SO-8, TSSOP-14

APPLICATIONS

- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- MEDICAL INSTRUMENTS
- HANDHELD TEST EQUIPMENT

DESCRIPTION

The OPA379 family of micropower, low-voltage operational amplifiers is designed for battery-powered applications. These amplifiers operate on a supply voltage as low as 1.8V (±0.9V). High-performance, single-supply operation with rail-to-rail capability (10μV max) makes the OPA379 family useful for a wide range of applications.

In addition to *micro*Size packages, the OPA379 family of op amps features impressive bandwidth (90kHz), low bias current (5pA), and low noise (80nV/$\sqrt{Hz}$) relative to the very low quiescent current (5.5μA max).

The OPA379 (single) is available in SC70-5, SOT23-5, and SO-8 packages. The OPA2379 (dual) comes in SOT23-8 and SO-8 packages. The OPA4379 (quad) is offered in a TSSOP-14 package. All versions are specified from –40°C to +125°C.

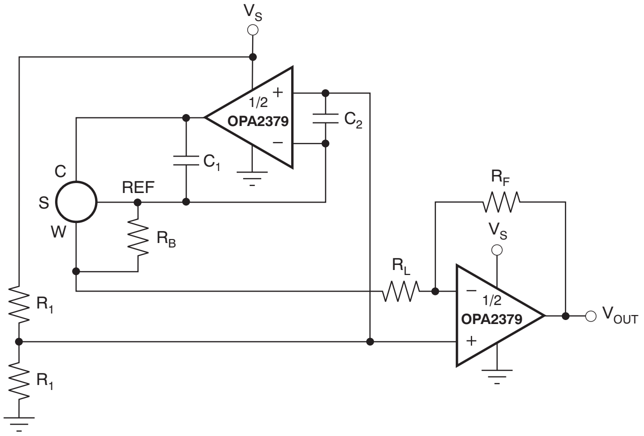


Figure 1. OPA2379 in Portable Gas Meter Application

Table 1. OPAx379 RELATED PRODUCTS

FEATURES	PRODUCT
1μA, 70kHz, 2mV V_{OS}, 1.8V to 5.5V Supply	OPAx349
1μA, 5.5kHz, 390μV V_{OS}, 2.5V to 16V Supply	TLV240x
1μA, 5.5kHz, 0.6mV V_{OS}, 2.5V to 12V Supply	TLV224x
7μA, 160kHz, 0.5mV V_{OS}, 2.7V to 16V Supply	TLV27Lx
7μA, 160kHz, 0.5mV V_{OS}, 2.7V to 16V Supply	TLV238x
20μA, 350kHz, 2mV V_{OS}, 2.3V to 5.5V Supply	OPAx347
20μA, 500kHz, 550μV V_{OS}, 1.8V to 3.6V Supply	TLV276x
45μA, 1MHz, 1mV V_{OS}, 2.1V to 5.5V Supply	OPAx348

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

			OPA379, OPA2379, OPA4379	UNIT
Supply Voltage		$V_S = (V+) – (V–)$	+7	V
Signal Input Terminals, Voltage[2]			(V–) – 0.5 to (V+) + 0.5	V
Signal Input Terminals, Current[2]			±10	mA
Output Short-Circuit[3]			Continuous	
Operating Temperature		T_A	–40 to +125	°C
Storage Temperature		T_A	–65 to +150	°C
Junction Temperature		T_J	+150	°C
ESD Rating	Human Body Model	(HBM)	2000	V
	Charged Device Model	(CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

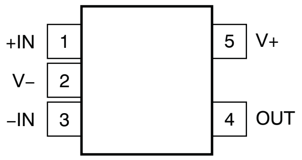
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA379	SC70−5	DCK	AYR
	SOT23−5	DBV	B53
	SO−8	D	OPA379A
OPA2379	SOT23−8	DCN	B61
	SO−8	D	OPA2379A
OPA4379	TSSOP−14	PW	OPA4379A

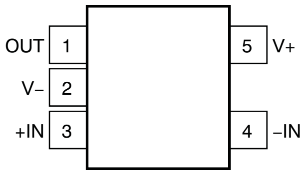
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

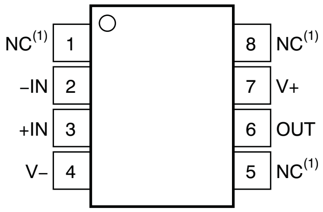
OPA379
SC70-5
(TOP VIEW)



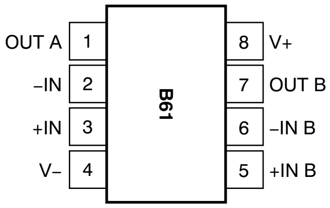
OPA379
SOT23-5
(TOP VIEW)



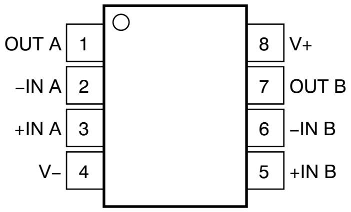
OPA379
SO-8
(TOP VIEW)



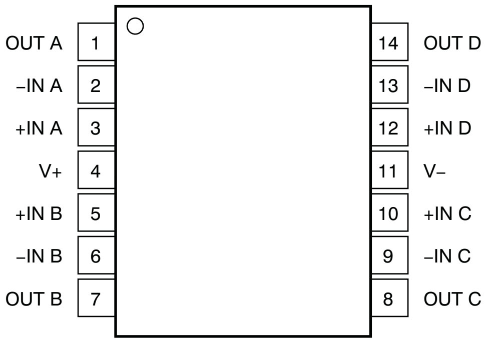
OPA2379(2)
SOT23-8
(TOP VIEW)



OPA2379
SO-8
(TOP VIEW)



OPA4379
TSSOP-14
(TOP VIEW)



(1) NC denotes no internal connection.

(2) Pin 1 of the SOT23−8 package is determined by orienting the package marking as shown.

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range indicated.
At T_A = +25°C, R_L = 25kΩ connected to V_S/2, and V_{CM} < (V+) – 1V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA379, OPA2379, OPA4379			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Initial Offset Voltage V_{OS}	V_S = 5V		0.4	1.5	mV
Over –40°C to +125°C				**2**	**mV**
Drift, –40°C to +85°C **dV_{OS}/dT**			**1.5**		**µV/°C**
Drift, –40°C to +125°C			**2.7**		**µV/°C**
vs Power Supply PSRR			2	10	µV/V
Over –40°C to +125°C				**20**	**µV/V**
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		(V–) – 0.1 to (V+) + 0.1			V
Common-Mode Rejection Ratio(1) CMRR	(V–) < V_{CM} < (V+) – 1V	90	100		dB
Over –40°C to +85°C	**(V–) < V_{CM} < (V+) – 1V**	**80**			**dB**
Over –40°C to +125°C	**(V–) < V_{CM} < (V+) – 1V**	**62**			**dB**
INPUT BIAS CURRENT					
Input Bias Current I_B	V_S = 5V, $V_{CM} \leq V_S/2$		±5	±50	pA
Input Offset Current I_{OS}	V_S = 5V		±5	±50	pA
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 3$		Ω ∥ pF
Common-Mode			$10^{13} \parallel 6$		Ω ∥ pF
NOISE					
Input Voltage Noise	f = 0.1Hz to 10Hz		2.8		μV_{PP}
Input Voltage Noise Density e_n	f = 1kHz		80		nV/√Hz
Input Current Noise Density i_n	f = 1kHz		1		fA/√Hz
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}	V_S = 5V, R_L = 25kΩ, 100mV < V_O < (V+) – 100mV	100	120		dB
Over –40°C to +125°C	**V_S = 5V, R_L = 25kΩ, 100mV < V_O < (V+) – 100mV**	**80**			**dB**
	V_S = 5V, R_L = 5kΩ, 500mV < V_O < (V+) – 500mV	100	120		dB
Over –40°C to +125°C	**V_S = 5V, R_L = 5kΩ, 500mV < V_O < (V+) – 500mV**	**80**			**dB**
OUTPUT					
Voltage Output Swing from Rail	R_L = 25kΩ		5	10	mV
Over –40°C to +125°C	**R_L = 25kΩ**			**15**	**mV**
	R_L = 5kΩ		25	50	mV
Over –40°C to +125°C	**R_L = 5kΩ**			**75**	**mV**
Short-Circuit Current I_{SC}			±5		mA
Capacitive Load Drive C_{LOAD}		See Typical Characteristics			
Closed-Loop Output Impedance R_{OUT}	G = 1, f = 1kHz, I_O = 0		10		Ω
Open-Loop Output Impedance R_O	f = 100kHz, I_O = 0		28		kΩ
FREQUENCY RESPONSE	C_{LOAD} = 30pF				
Gain Bandwidth Product GBW			90		kHz
Slew Rate SR	G = +1		0.03		V/µs
Overload Recovery Time	V_{IN} × GAIN > V_S		25		µs
Turn-On Time t_{ON}			1		ms

(1) See Typical Characteristic gragh, *Common-Mode Rejection Ratio vs Frequency* (Figure 3).

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V (continued)

Boldface limits apply over the specified temperature range indicated.
At T_A = +25°C, R_L = 25kΩ connected to V_S/2, and V_{CM} < (V+) – 1V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA379, OPA2379, OPA4379			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Specified/Operating Voltage Range	V_S		1.8		5.5	V
Quiescent Current per Amplifier	I_Q	V_S = 5.5V, I_O = 0		2.9	5.5	μA
Over –40°C to +125°C					**10**	**μA**
TEMPERATURE						
Specified/Operating Range	T_A		–40		+125	°C
Storage Range	T_J		–65		+150	°C
Thermal Resistance	θ_{JA}					
SC70−5				250		°C/W
SOT23−5				200		°C/W
SOT23−8, TSSOP−14, SO−8				150		°C/W

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, and R_L = 25kΩ connected to $V_S/2$, unless otherwise noted.

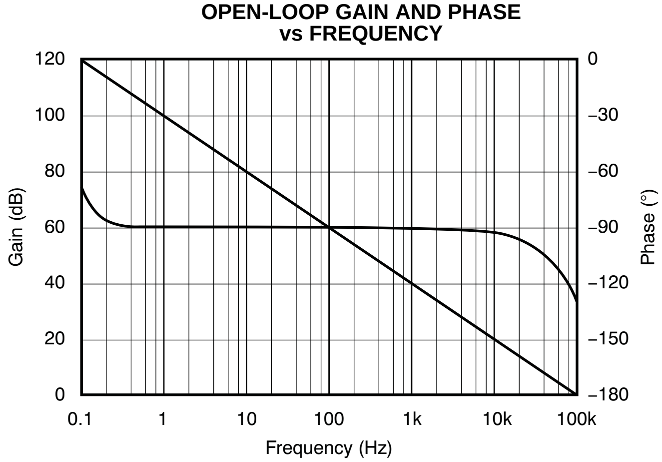


Figure 2.

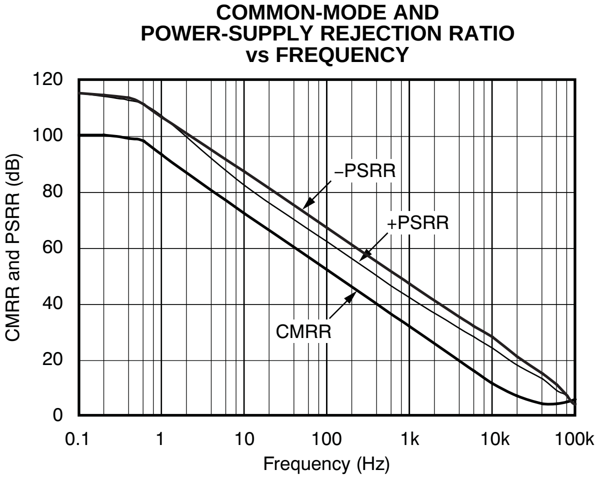


Figure 3.

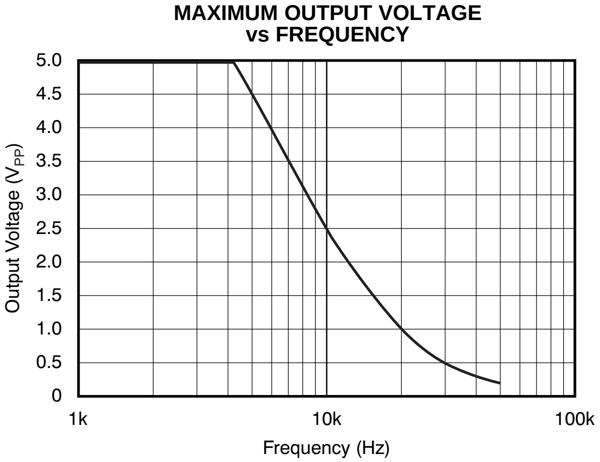


Figure 4.

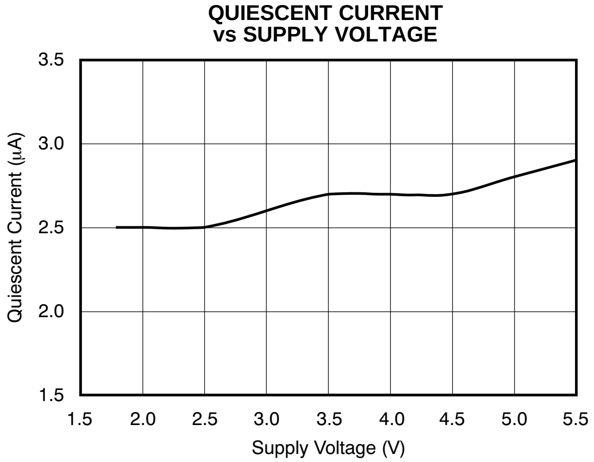


Figure 5.

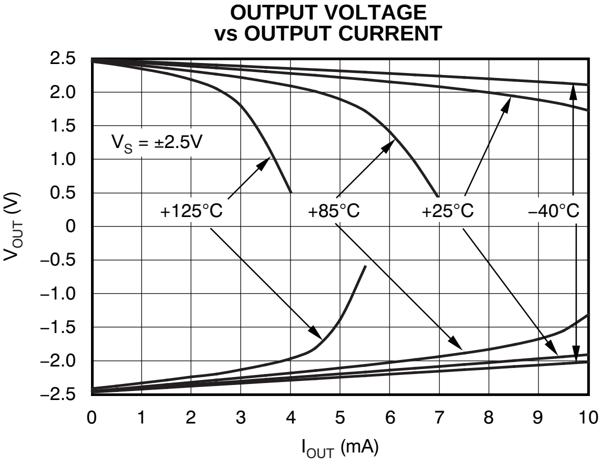


Figure 6.

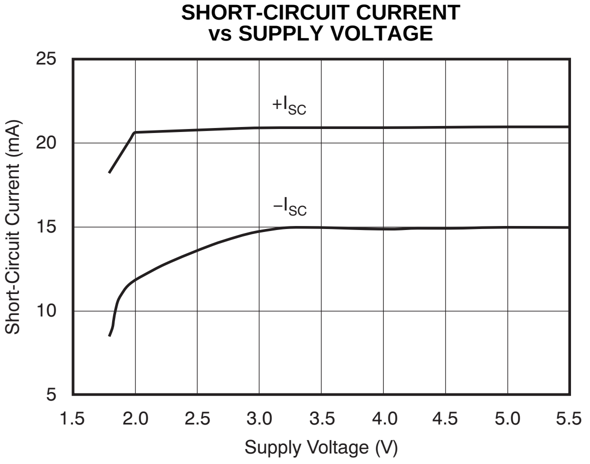


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, and R_L = 25kΩ connected to $V_S/2$, unless otherwise noted.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE vs TEMPERATURE

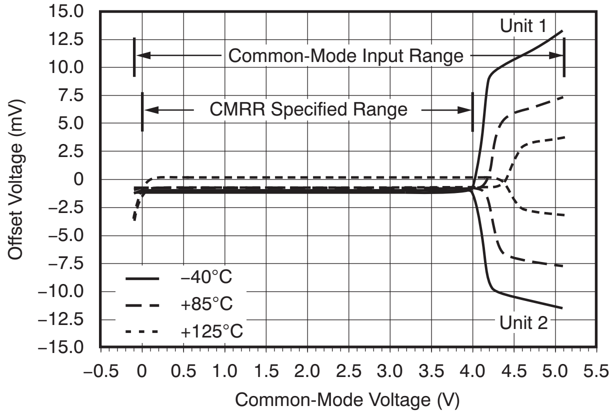


Figure 8.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

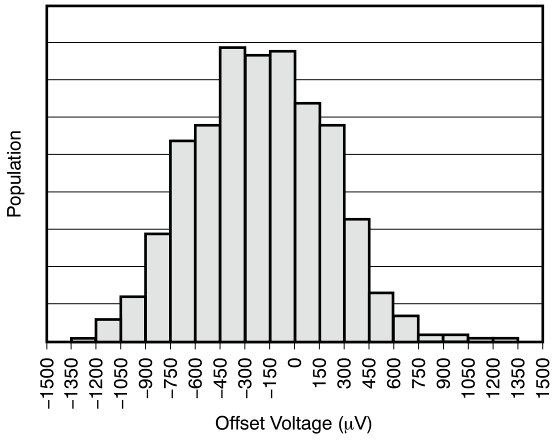


Figure 9.

OFFSET VOLTAGE DRIFT DISTRIBUTION (–40°C to +85°C)

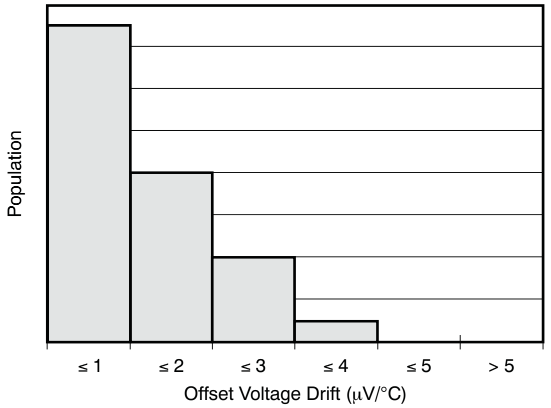


Figure 10.

OFFSET VOLTAGE DRIFT DISTRIBUTION (–40°C to +125°C)

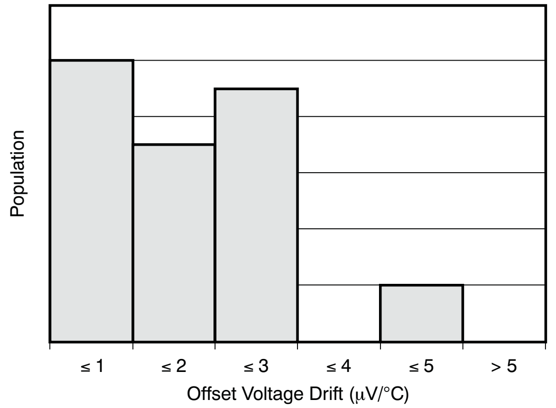


Figure 11.

QUIESCENT CURRENT vs TEMPERATURE

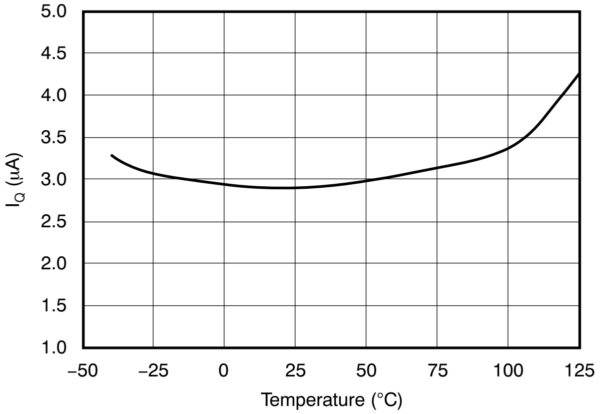


Figure 12.

QUIESCENT CURRENT PRODUCTION DISTRIBUTION

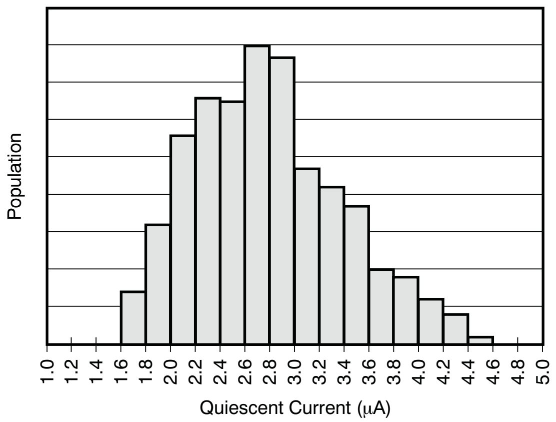


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, and R_L = 25kΩ connected to $V_S/2$, unless otherwise noted.

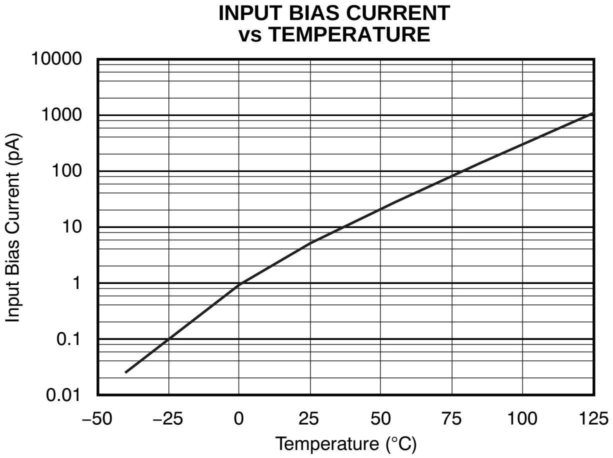


Figure 14.

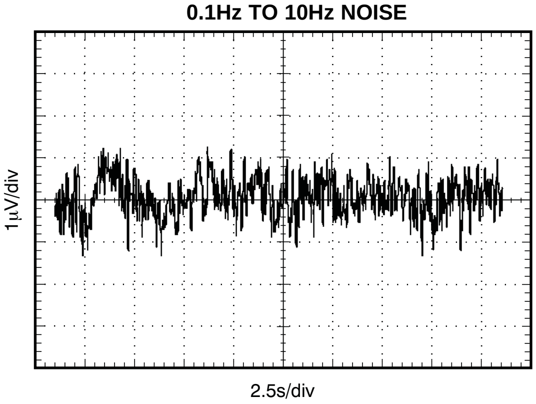


Figure 15.

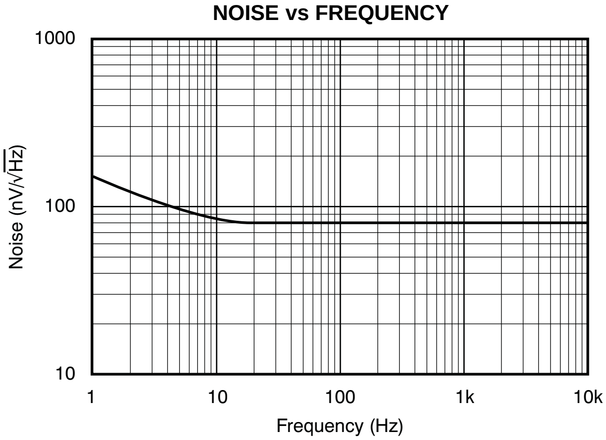


Figure 16.

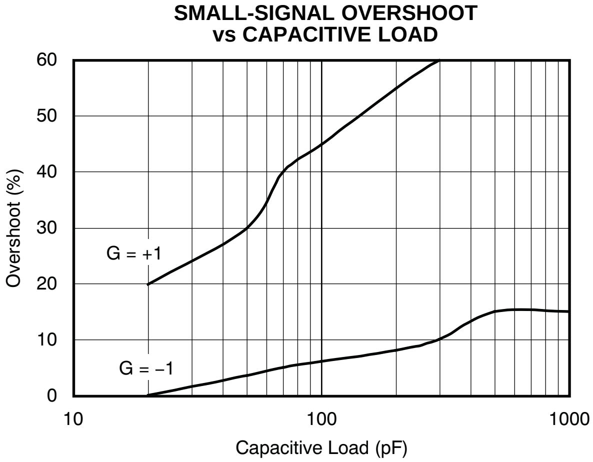


Figure 17.

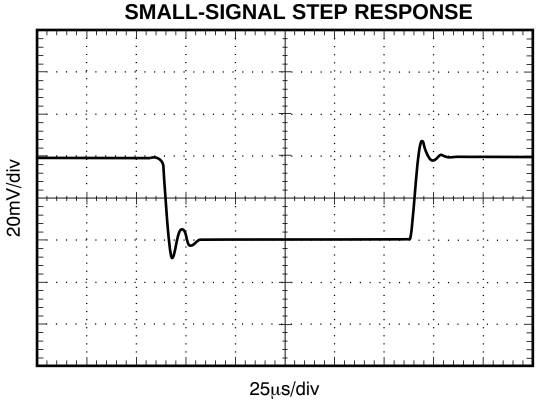


Figure 18.

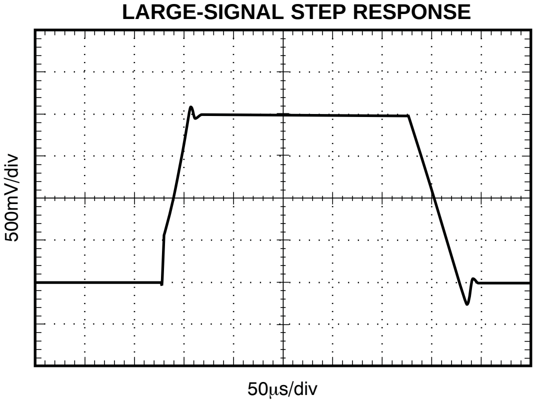


Figure 19.

APPLICATION INFORMATION

The OPA379 family of operational amplifiers minimizes power consumption without compromising bandwidth or noise. Power-supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and open-loop gain (A_{OL}) typical values are 100dB or better.

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

Good layout practice mandates the use of a 0.1µF bypass capacitor placed closely across the supply pins.

OPERATING VOLTAGE

OPA379 series op amps are fully specified and tested from +1.8V to +5.5V (±0.9V to ±2.75V). Parameters that will vary with supply voltage are shown in the Typical Characteristics curves.

INPUT COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA379 family typically extends 100mV beyond each supply rail. This rail-to-rail input is achieved using a complementary input stage. CMRR is specified from the negative rail to 1V below the positive rail. Between (V+) – 1V and (V+) + 0.1V, the amplifier operates with higher offset voltage because of the transition region of the input stage. See the typical characteristic, *Offset Voltage vs Common-Mode Voltage vs Temperature* (Figure 8).

PROTECTING INPUTS FROM OVER-VOLTAGE

Normally, input currents are 5pA. However, a large voltage input (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This limiting is easily accomplished with an input voltage resistor, as shown in Figure 20.

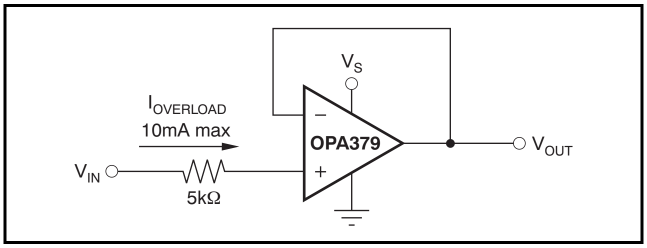


Figure 20. Input Current Protection for Voltages Exceeding the Supply Voltage

NOISE

Although micropower amplifiers frequently have high wideband noise, the OPA379 series offer excellent noise performance. Resistors should be chosen carefully because the OPA379 has only 2.8µV_{PP} of 0.1Hz to 10Hz noise, and 80nV/$\sqrt{Hz}$ of wideband noise; otherwise, they can become the dominant source of noise.

CAPACITIVE LOAD AND STABILITY

Follower configurations with load capacitance in excess of 30pF can produce extra overshoot (see typical characteristic *Small-Signal Overshoot vs Capacitive Load*, Figure 17) and ringing in the output signal. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 21. This resistor significantly reduces ringing while maintaining direct current (dc) performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible.

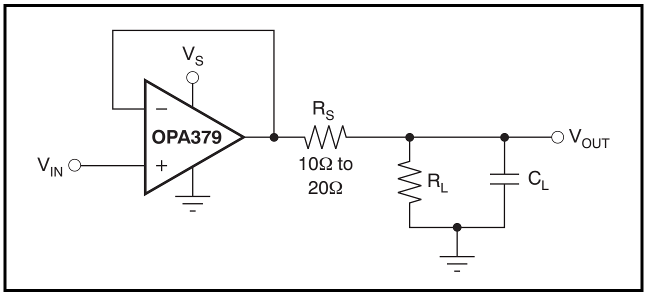


Figure 21. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors. Best performance is achieved by using smaller valued resistors. However, when large valued resistors cannot be avoided, a small (4pF to 6pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 22. This configuration significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance (3pf) and printed circuit board (PC) parasitic capacitance.

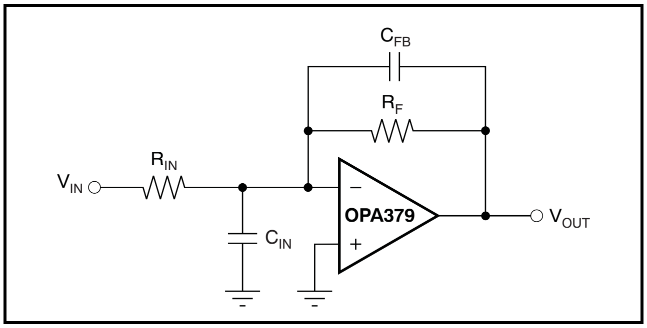


Figure 22. Improving Stability for Large R_F and R_{IN}

BATTERY MONITORING

The low operating voltage and quiescent current of the OPA379 series make it an excellent choice for battery monitoring applications, as shown in Figure 23. In this circuit, V_{STATUS} is high as long as the battery voltage remains above 2V. A low-power reference is used to set the trip point. Resistor values are selected as follows:

1. R_F Selecting: Select R_F such that the current through R_F is approximately 1000x larger than the maximum bias current over temperature:

$$R_F = \frac{V_{REF}}{1000(I_{BMAX})} = \frac{1.2V}{1000(100pA)} = 12M\Omega \approx 10M\Omega \quad (1)$$

2. Choose the hysteresis voltage, V_{HYST}. For battery monitoring applications, 50mV is adequate.
3. Calculate R_1 as follows:

$$R_1 = R_F\left(\frac{V_{HYST}}{V_{BATT}}\right) = 10M\Omega\left(\frac{50mW}{2.4V}\right) = 210k\Omega \quad (2)$$

4. Select a threshold voltage for V_{IN} rising (V_{THRS}) = 2.0V
5. Calculate R_2 as follows:

$$R_2 = \frac{1}{\left[\left(\frac{V_{THRS}}{V_{REF} \times R_1}\right) - \frac{1}{R_1} - \frac{1}{R_F}\right]} = \frac{1}{\left[\left(\frac{2V}{1.2V \times 210k\Omega}\right) - \frac{1}{210k\Omega} - \frac{1}{10M\Omega}\right]} = 325k\Omega \quad (3)$$

6. Calculate R_{BIAS}: The minimum supply voltage for this circuit is 1.8V. The REF1112 has a current requirement of 1.2µA (max). Providing 2µA of supply current assures proper operation. Therefore:

$$R_{BIAS} = \frac{(V_{BATTMIN} - V_{REF})}{I_{BIAS}} = \frac{(1.8V - 1.2V)}{2\mu A} = 0.3M\Omega \quad (4)$$

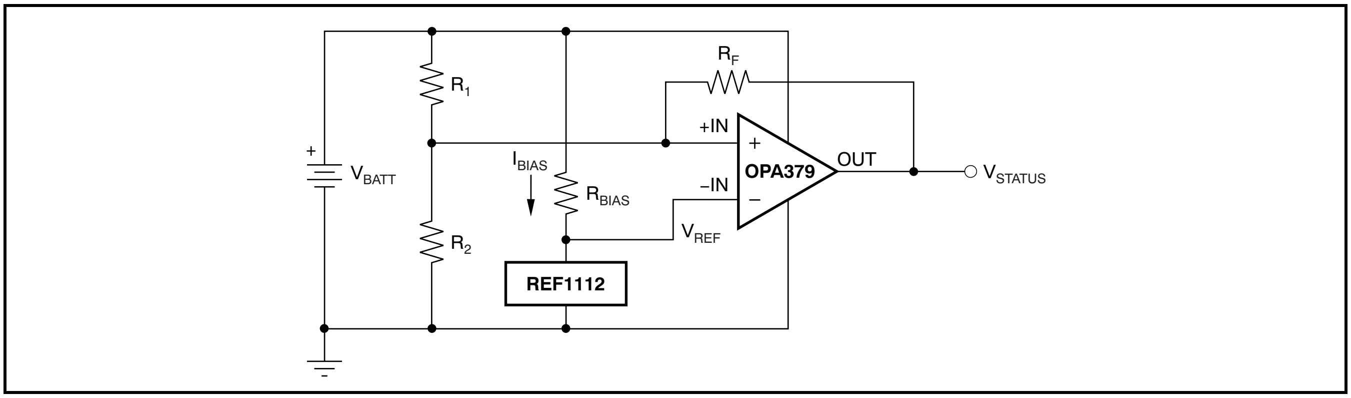


Figure 23. Battery Monitor

WINDOW COMPARATOR

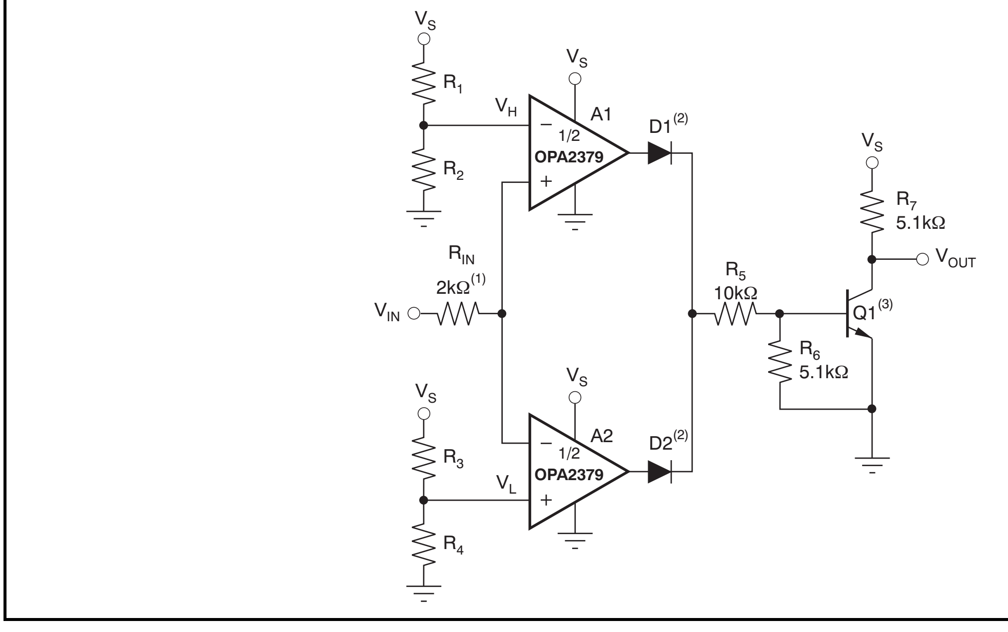
Figure 24 shows the OPA2379 used as a window comparator. The threshold limits are set by V_H and V_L, with $V_H > V_L$. When $V_{IN} < V_H$, the output of A1 is low. When $V_{IN} > V_L$, the output of A2 is low. Therefore, both op amp outputs are at 0V as long as V_{IN} is between V_H and V_L. This architecture results in no current flowing through either diode, Q1 in cutoff, with the base voltage at 0V, and V_{OUT} forced high.

If V_{IN} falls below V_L, the output of A2 is high, current flows through D2, and V_{OUT} is low. Likewise, if V_{IN} rises above V_H, the output of A1 is high, current flows through D1, and V_{OUT} is low.

The window comparator threshold voltages are set as follows:

$$V_H = \frac{R_2}{R_1 + R_2} \times V_S \tag{5}$$

$$V_L = \frac{R_4}{R_3 + R_4} \times V_S \tag{6}$$



(1) R_{IN} protects A1 and A2 from possible excess current flow.

(2) IN4446 or equivalent diodes.

(3) 2N2222 or equivalent NPN transistor.

Figure 24. OPA2379 as a Window Comparator

ADDITIONAL APPLICATION EXAMPLES

Figure 25 through Figure 29 illustrate additional application examples.

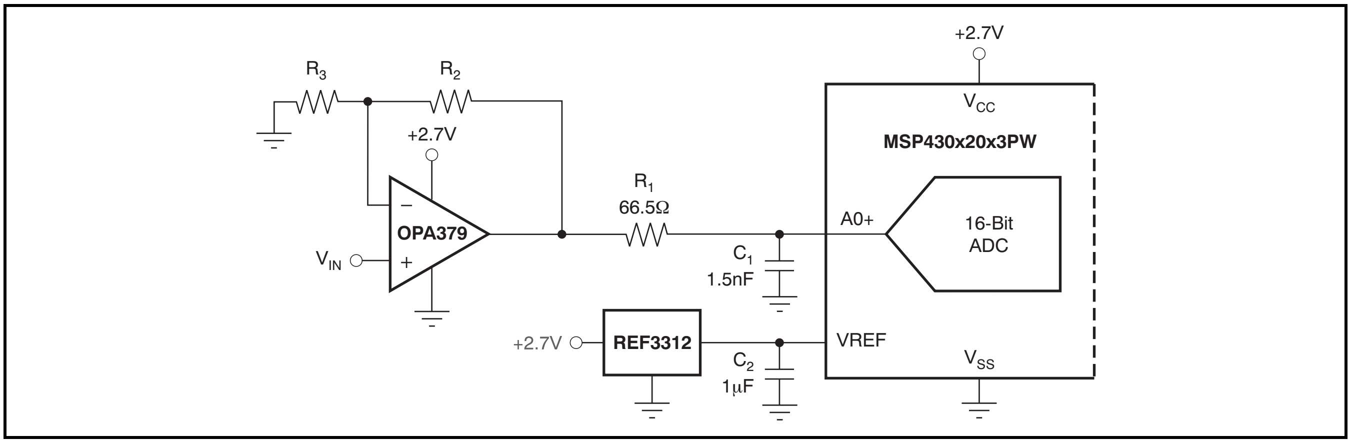


Figure 25. Unipolar Signal Chain Configuration

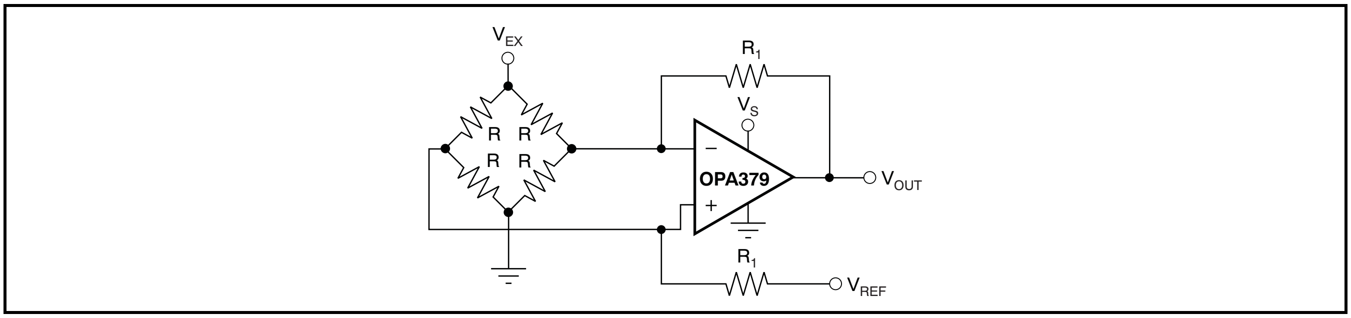
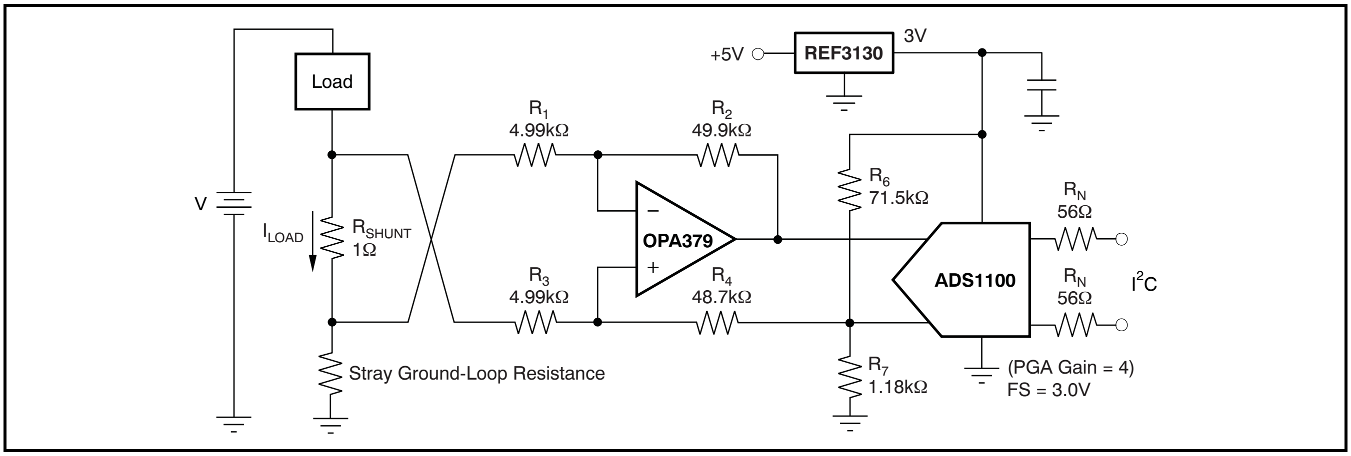
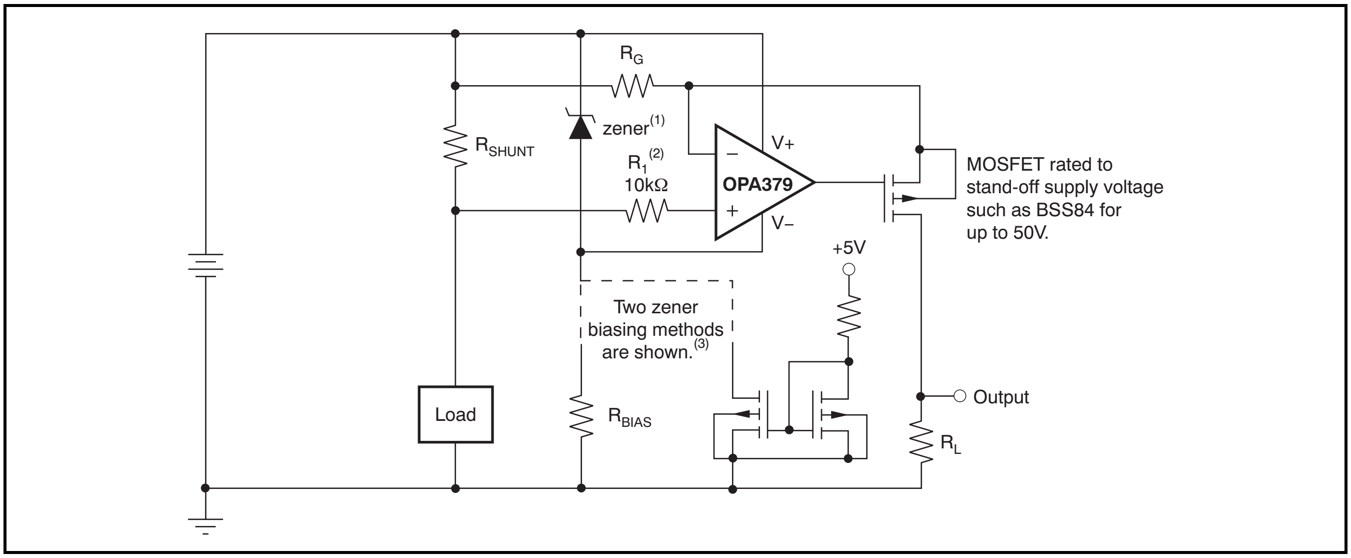


Figure 26. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 27. Low-Side Current Monitor

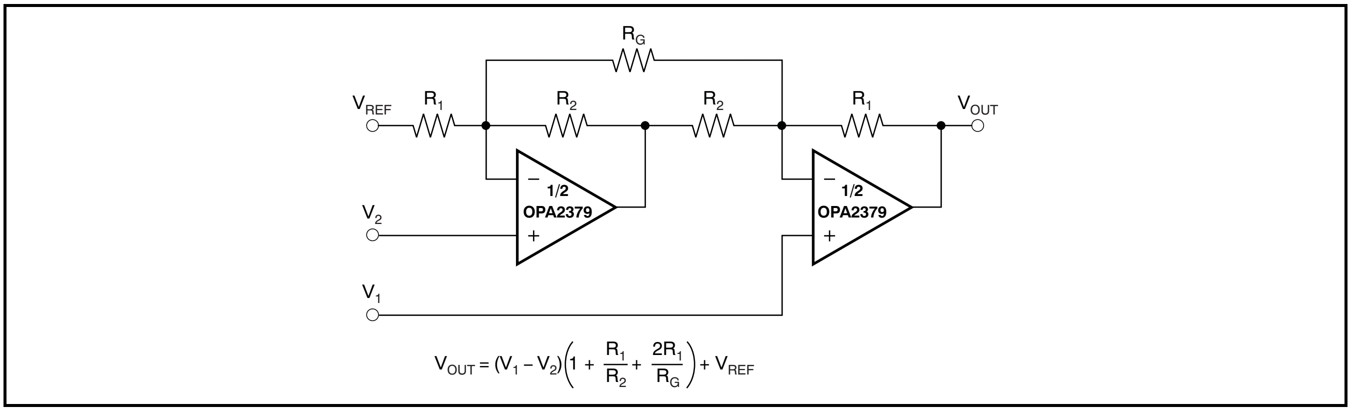


(1) Zener rated for op amp supply capability (that is, 5.1V for OPA379).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual NMOSMETs (FDG6301N, NTJD4001N, or Si1034).

Figure 28. High-Side Current Monitor



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

Figure 29. Two Op Amp Instrumentation Amplifier

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2379AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2379A
OPA2379AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2379A
OPA2379AIDCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDCNT	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDCNT.A	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDCNTG4	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDCNTG4.A	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BPK
OPA2379AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2379A
OPA2379AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2379A
OPA2379AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2379A
OPA379AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 379A
OPA379AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 379A
OPA379AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B53
OPA379AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B53
OPA379AIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B53
OPA379AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B53
OPA379AIDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B53
OPA379AIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B54
OPA379AIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B54
OPA379AIDCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B54
OPA379AIDCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B54
OPA379AIDCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B54
OPA379AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 379A
OPA379AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 379A

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA379AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 379A
OPA4379AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4379A
OPA4379AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4379A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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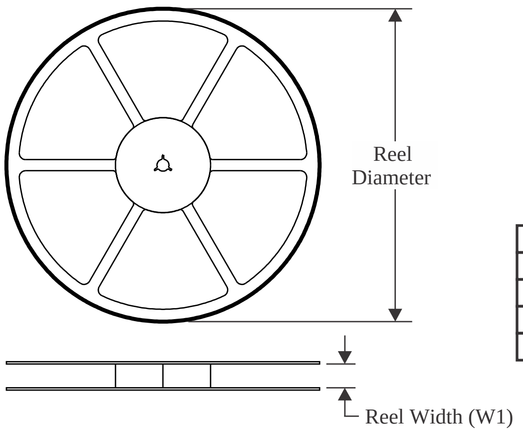
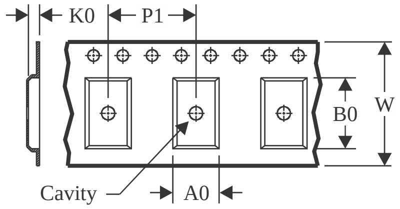
TAPE AND REEL INFORMATION

REEL DIMENSIONS

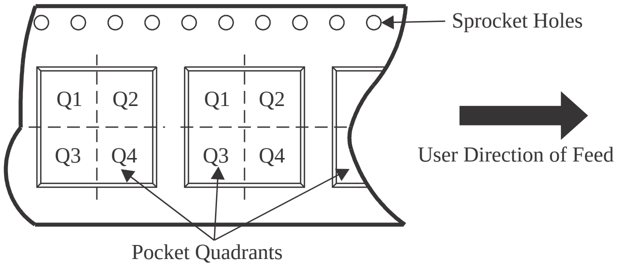


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

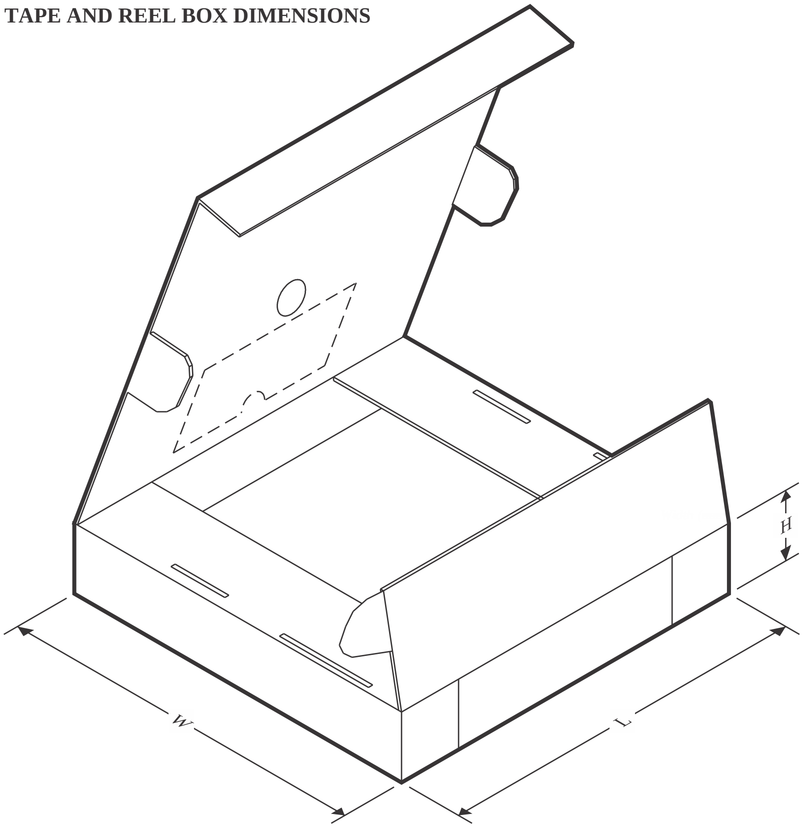
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2379AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2379AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2379AIDCNTG4	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2379AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA379AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA379AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA379AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA379AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA379AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA379AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4379AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

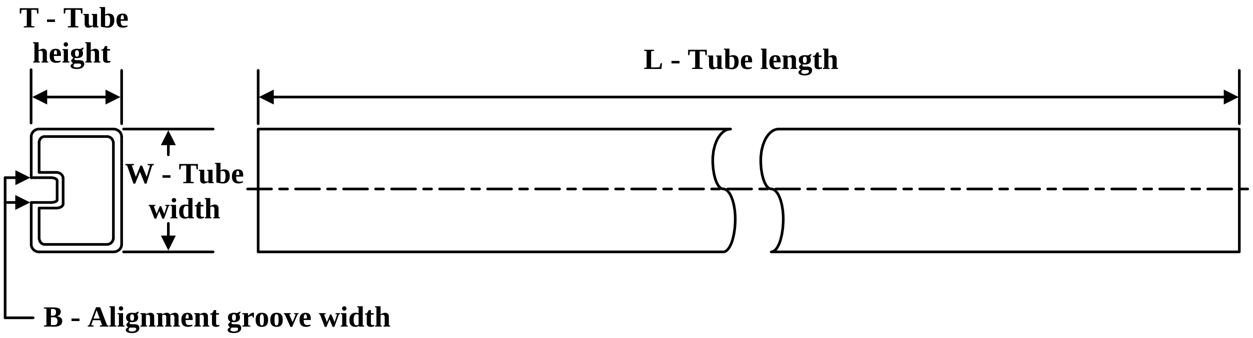
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

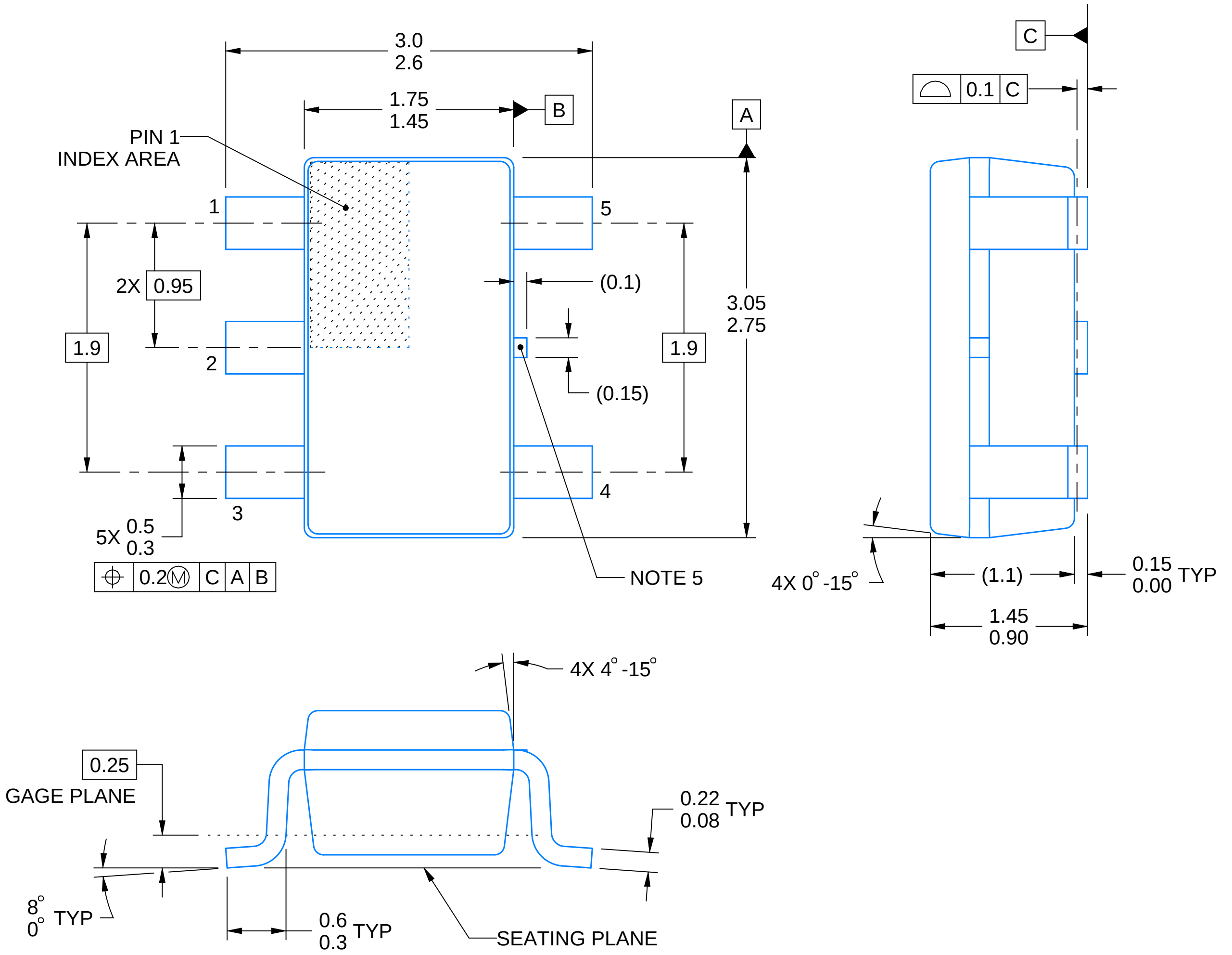
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2379AIDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
OPA2379AIDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2379AIDCNTG4	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2379AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA379AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA379AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA379AIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA379AIDCKT	SC70	DCK	5	250	213.0	191.0	35.0
OPA379AIDCKT	SC70	DCK	5	250	190.0	190.0	30.0
OPA379AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA4379AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

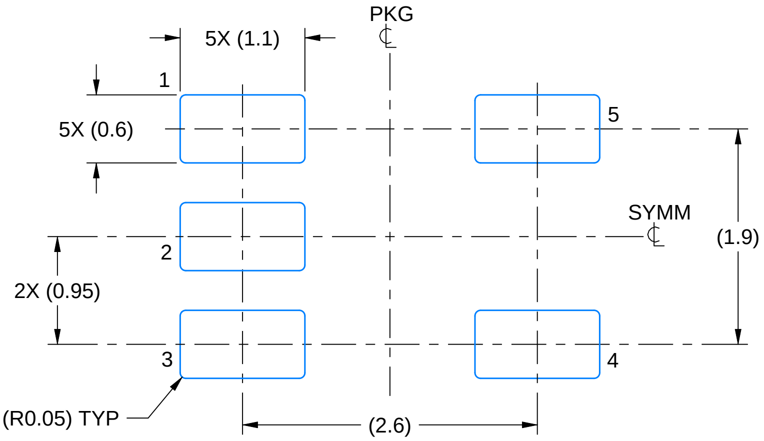
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2379AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2379AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2379AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA379AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA379AID.A	D	SOIC	8	75	506.6	8	3940	4.32



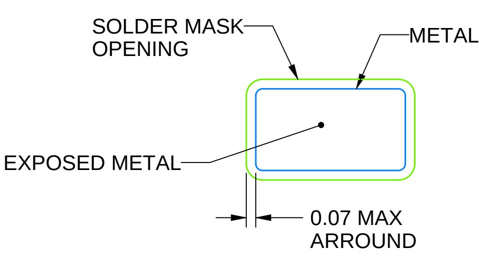
4214839/K 08/2024

NOTES:

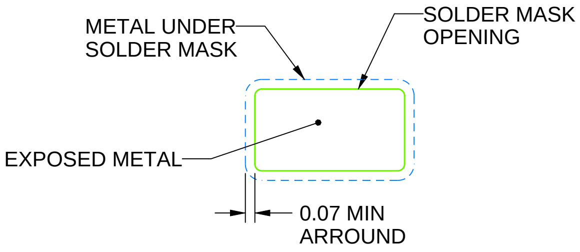
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

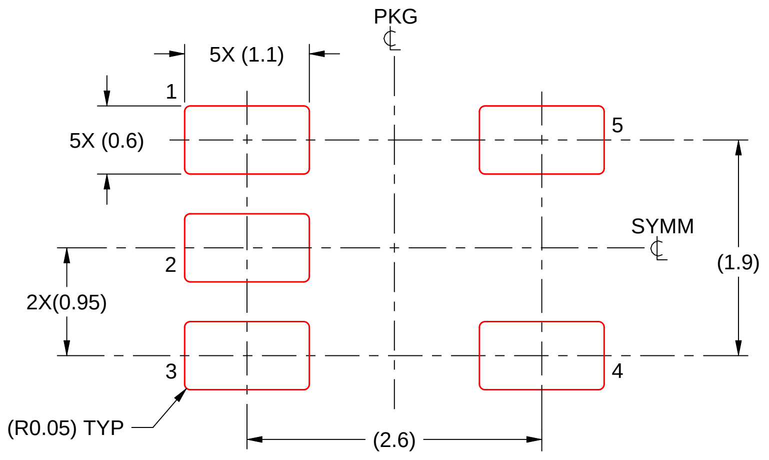


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



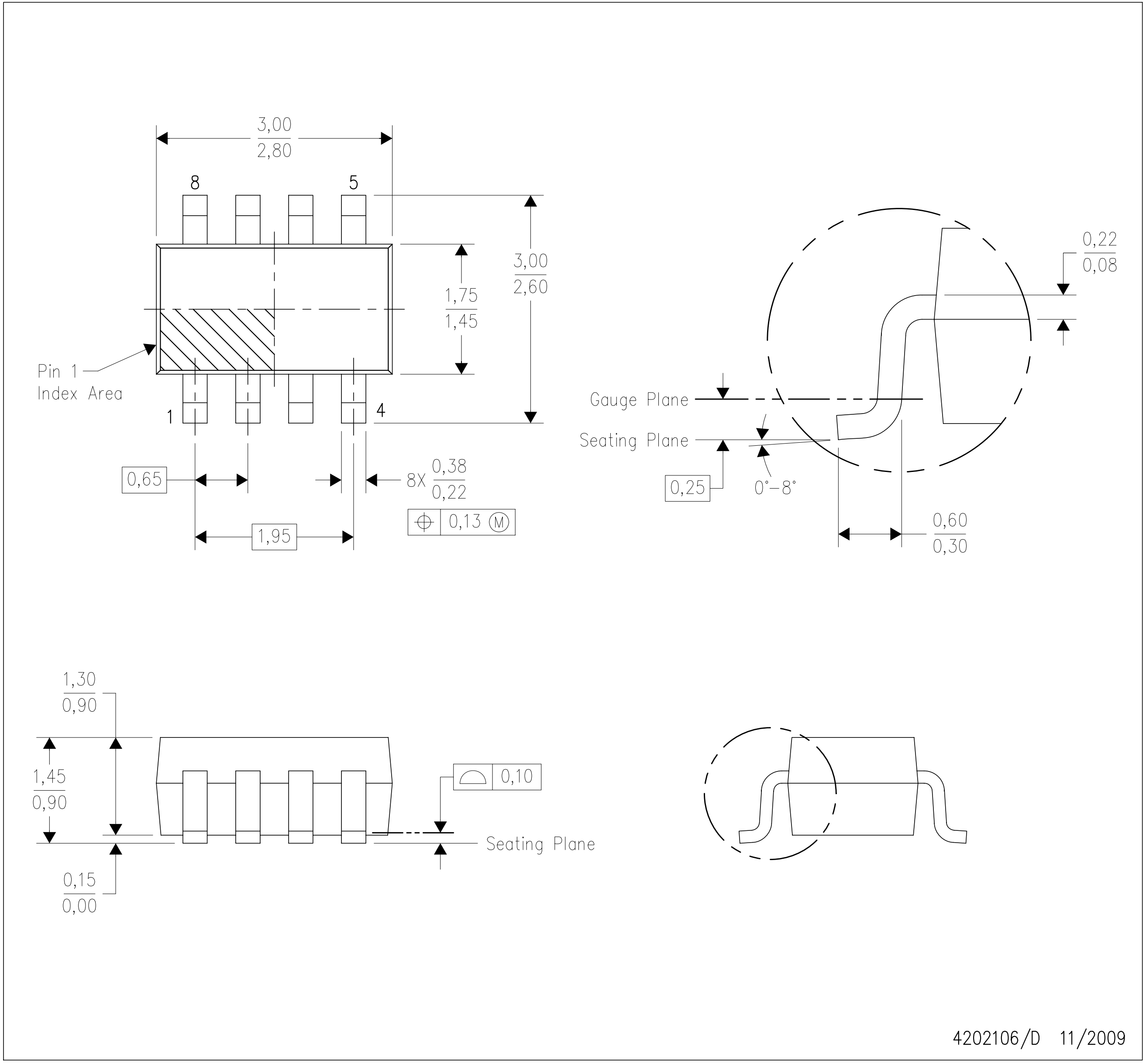
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

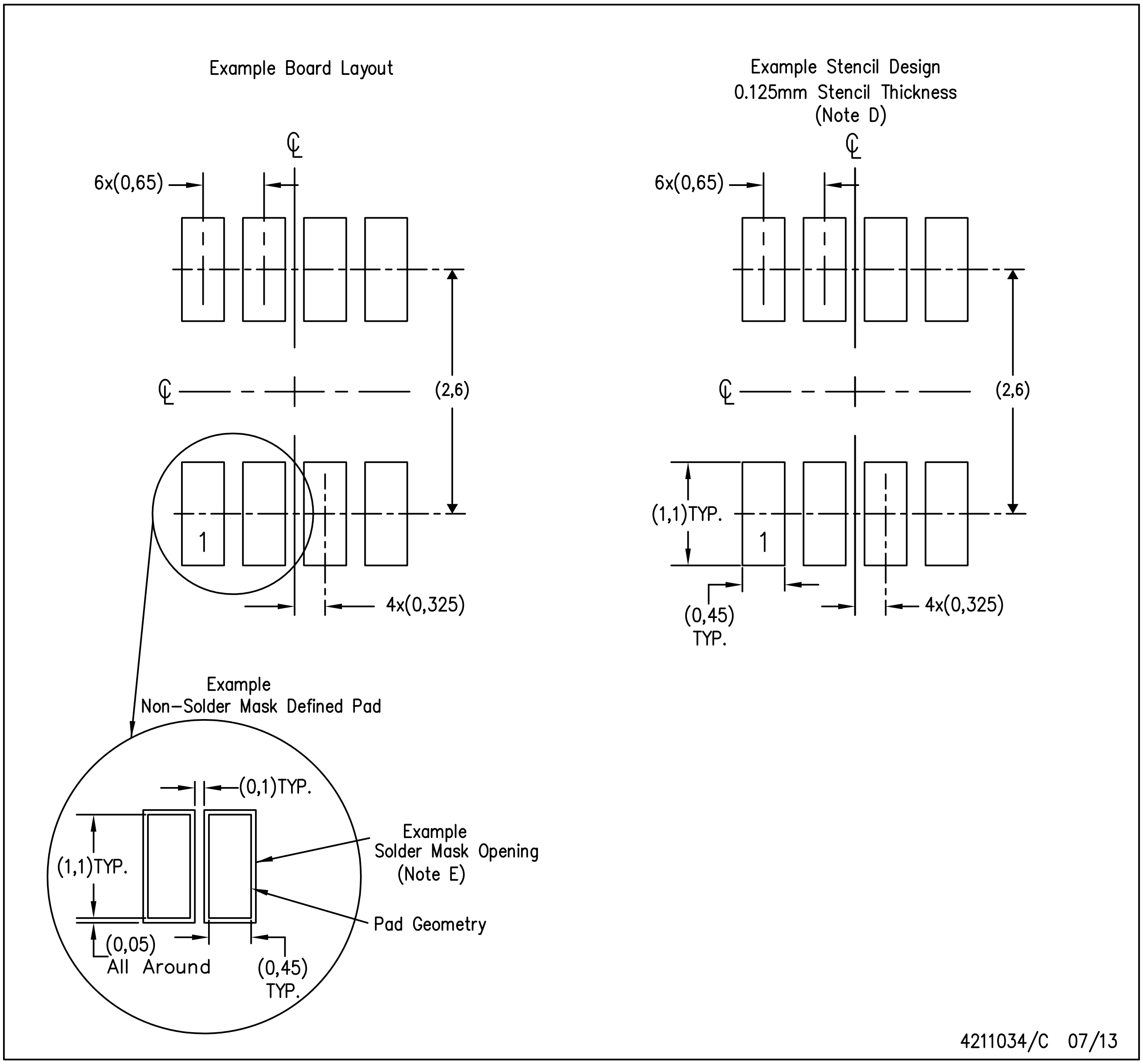
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



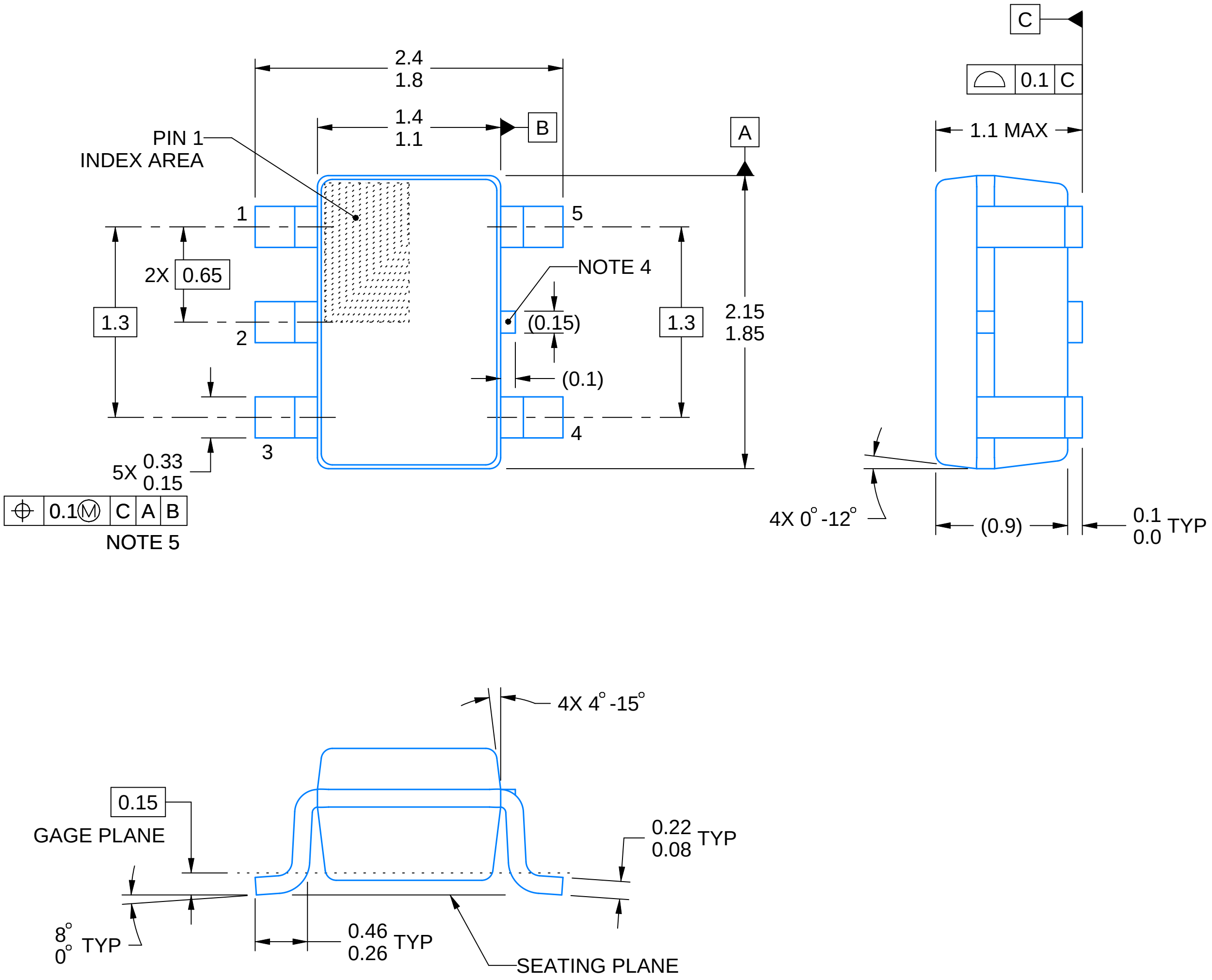
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

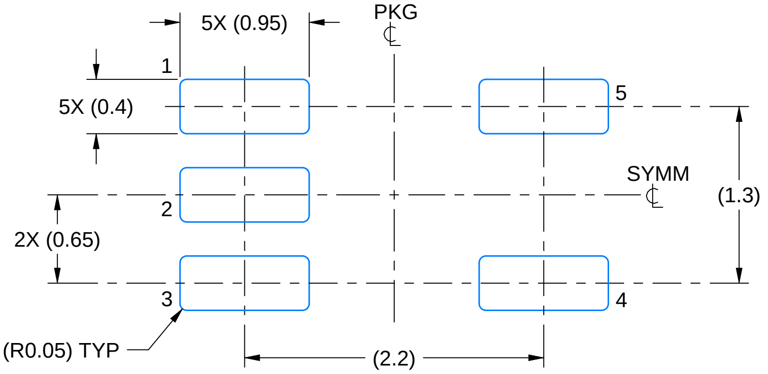
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



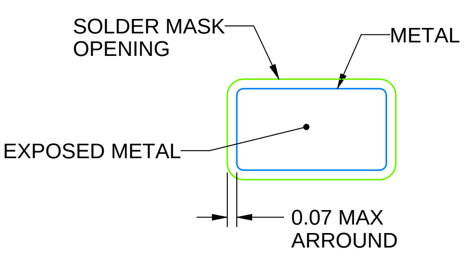
4214834/G 11/2024

NOTES:

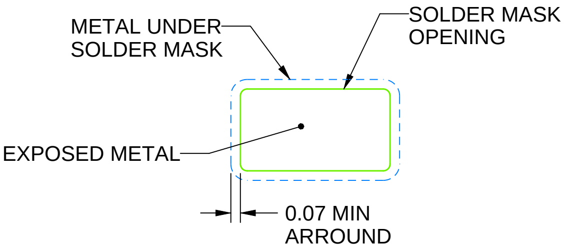
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

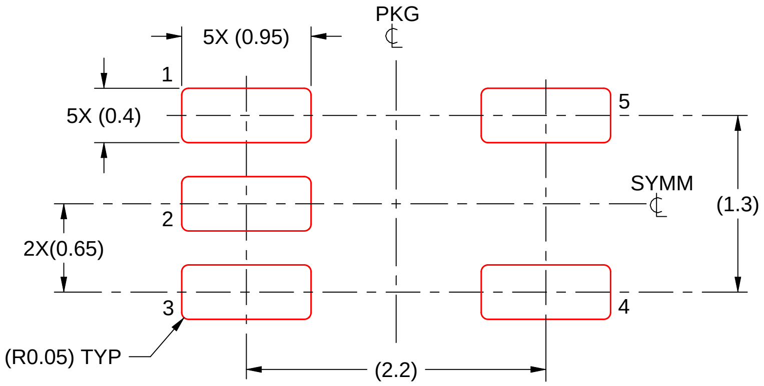


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



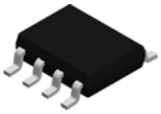
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G   11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

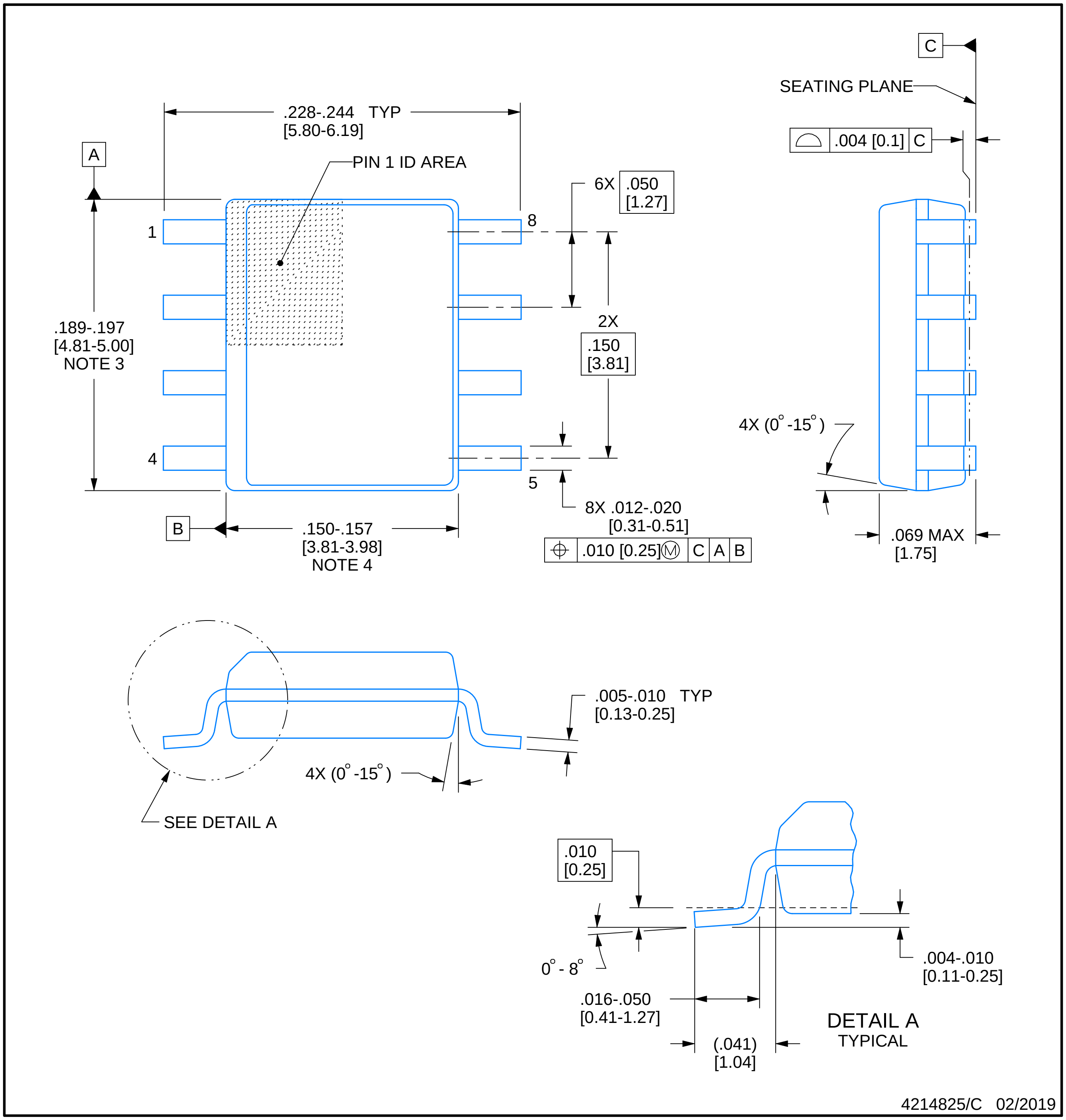
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

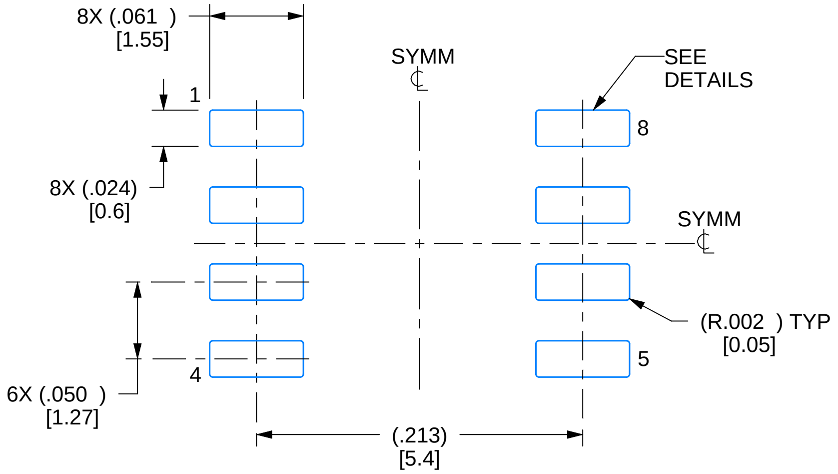
SMALL OUTLINE INTEGRATED CIRCUIT



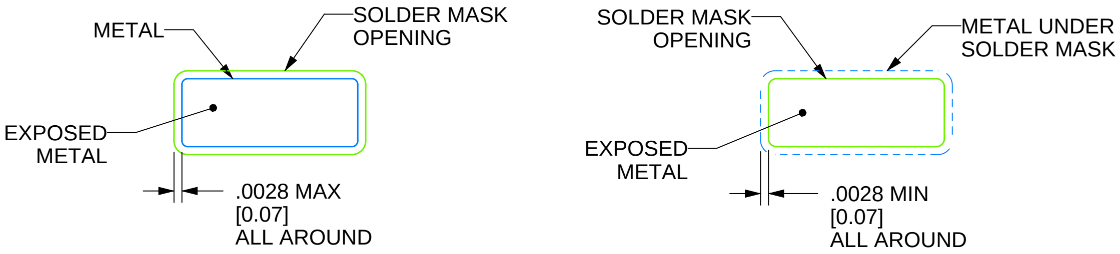
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



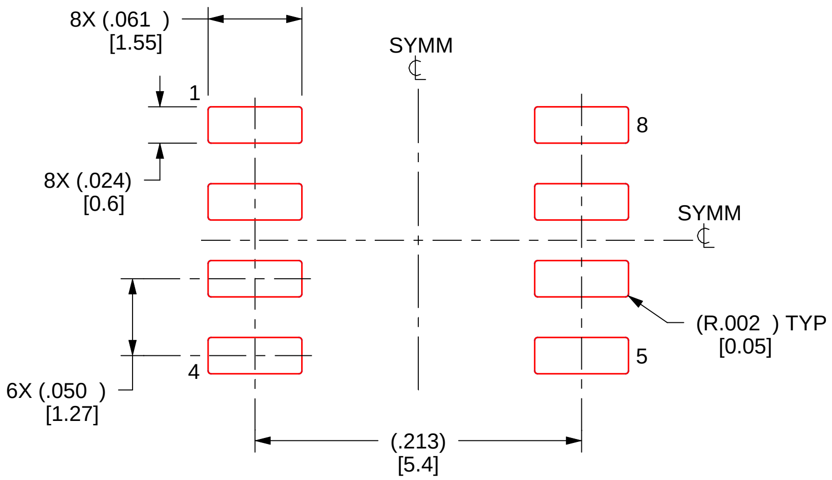
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

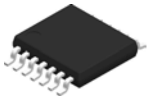


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

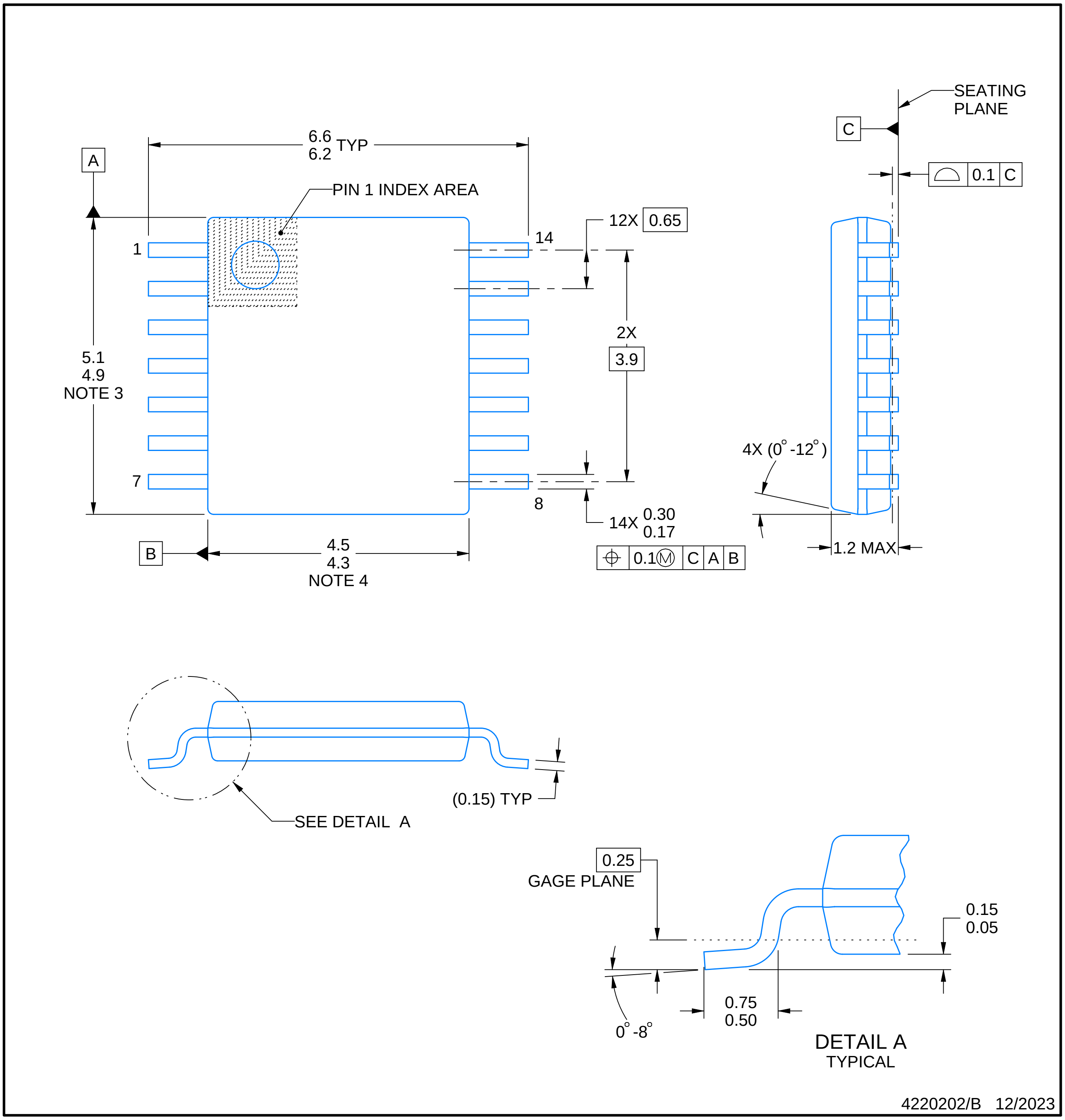
PACKAGE OUTLINE



PW0014A

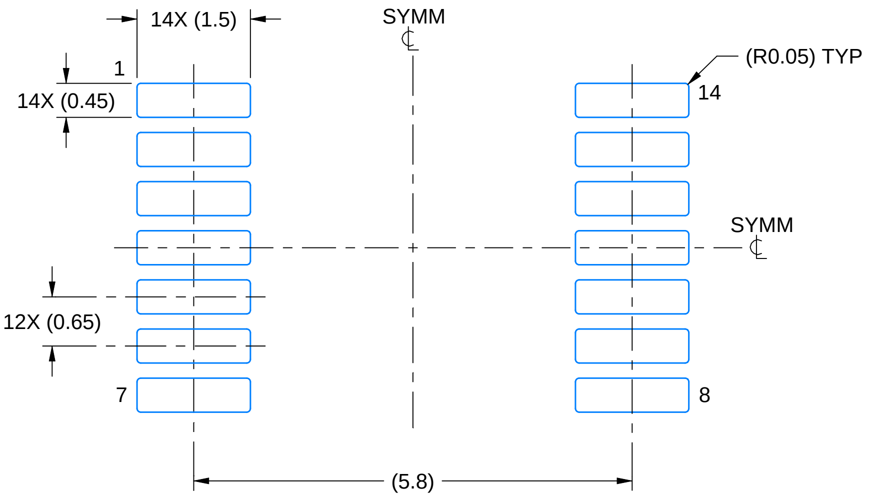
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

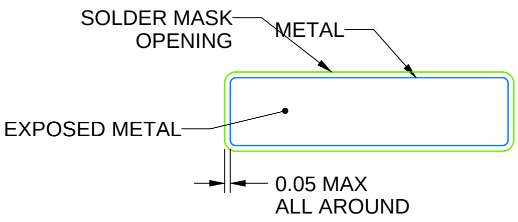


NOTES:

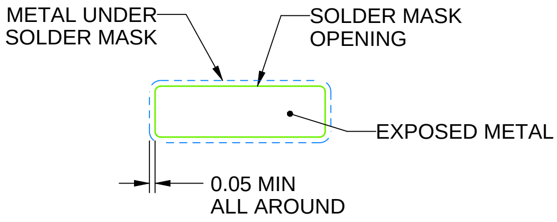
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

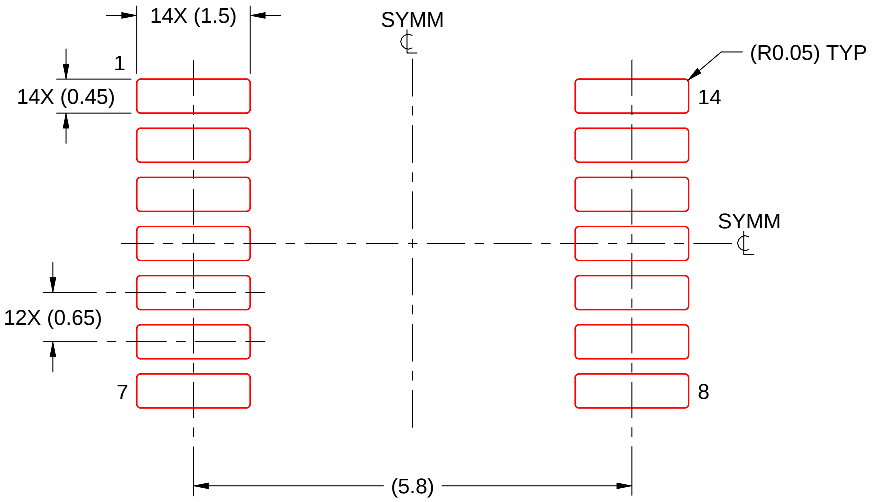


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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