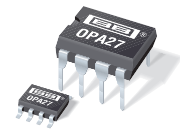
Burr-Brown Products
from Texas Instruments




# OPA27
# OPA37

SBOS135C – JANUARY 1984 – REVISED AUGUST 2005

# Ultra-Low Noise, Precision OPERATIONAL AMPLIFIERS

## FEATURES

- **LOW NOISE: 4.5nV/√Hz max at 1kHz**
- **LOW OFFSET: 100μV max**
- **LOW DRIFT: 0.4μV/°C**
- **HIGH OPEN-LOOP GAIN: 117dB min**
- **HIGH COMMON-MODE REJECTION: 100dB min**
- **HIGH POWER-SUPPLY REJECTION: 94dB min**
- **FITS OP-07, OP-05, AD510, AND AD517 SOCKETS**

## APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **TRANSDUCER AMPLIFIERS**
- **RADIATION HARD EQUIPMENT**

## DESCRIPTION

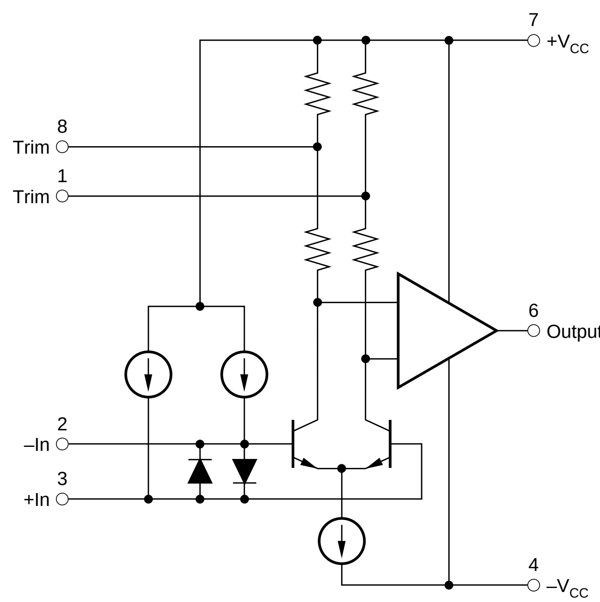
The OPA27 and OPA37 are ultra-low noise, high-precision monolithic operational amplifiers.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –40°C to +85°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Texas Instruments' OPA27 and OPA37 are improved replacements for the industry-standard OP-27 and OP-37.



## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | ±22V |
| Internal Power Dissipation [2] | 500mW |
| Input Voltage | $\pm V_{CC}$ |
| Output Short-Circuit Duration [3] | Indefinite |
| Differential Input Voltage [4] | ±0.7V |
| Differential Input Current [4] | ±25mA |
| Storage Temperature Range | –55°C to +125°C |
| Operating Temperature Range | –40°C to +85°C |
| Lead Temperature: | |
| P (soldering, 10s) | +300°C |
| U (soldering, 3s) | +260°C |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Maximum package power dissipation versus ambient temperature. (2) To common with $\pm V_{CC}$ = 15V. (4) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

## PACKAGE/ORDERING INFORMATION[1]

| PRODUCT | PACKAGE-LEAD | $\theta_{JA}$ | PACKAGE DRAWING | PACKAGE MARKING |
|---|---|---|---|---|
| OPA27 | DIP-8 | 100°C/W | P | OPA27GP |
| OPA27 | SO-8 | 160°C/W | D | OPA27U |
| OPA37 | DIP-8 | 100°C/W | P | OPA37GP |
| OPA37 | SO-8 | 160°C/W | D | OPA37U |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

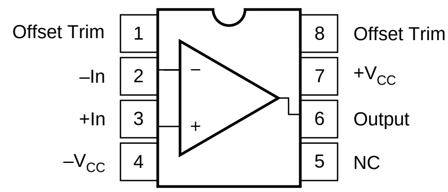
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION

**Top View**




NC = No Connection

# ELECTRICAL CHARACTERISTICS

At $V_{CC} = \pm15V$ and $T_A = +25°C$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA27 OPA37 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT NOISE** (6) | | | | | |
| Voltage, $f_O$ = 10Hz | | | 3.8 | 8.0 | nV/√Hz |
| $f_O$ = 30Hz | | | 3.3 | 5.6 | nV/√Hz |
| $f_O$ = 1kHz | | | 3.2 | 4.5 | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.09 | 0.25 | $\mu V_{PP}$ |
| Current,(1) $f_O$ = 10Hz | | | 1.7 | | pA/√Hz |
| $f_O$ = 30Hz | | | 1.0 | | pA/√Hz |
| $f_O$ = 1kHz | | | 0.4 | 0.6 | pA/√Hz |
| **OFFSET VOLTAGE** (2) | | | | | |
| Input Offset Voltage | | | ±25 | ±100 | µV |
| Average Drift (3) | $T_{A\,MIN}$ to $T_{A\,MAX}$ | | ±0.4 | ±1.8 (6) | µV/°C |
| Long Term Stability (4) | | | 0.4 | 2.0 | µV/mo |
| Supply Rejection | $\pm V_{CC}$ = 4 to 18V | 94 | 120 | | dB |
| | $\pm V_{CC}$ = 4 to 18V | | ±1 | ±20 | µV/V |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | | | ±15 | ±80 | nA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | | | 10 | 75 | nA |
| **IMPEDANCE** | | | | | |
| Common-Mode | | | 2 \|\| 2.5 | | GΩ \|\| pF |
| **VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±11 | ±12.3 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±11VDC | 100 | 122 | | dB |
| **OPEN-LOOP VOLTAGE GAIN, DC** | $R_L \geq 2k\Omega$ | 117 | 124 | | dB |
| | $R_L \geq 1k\Omega$ | | 124 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product (5) | OPA27 | 5 (6) | 8 | | MHz |
| | OPA37 | 45 (6) | 63 | | MHz |
| Slew Rate (5) | $V_O$ = ±10V, $R_L$ = 2kΩ | | | | |
| | OPA27, G = +1 | 1.7 (6) | 1.9 | | V/µs |
| | OPA37, G = +5 | 11 (6) | 11.9 | | V/µs |
| Settling Time, 0.01% | OPA27, G = +1 | | 25 | | µs |
| | OPA37, G = +5 | | 25 | | µs |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L \geq 2k\Omega$ | ±12 | ±13.8 | | V |
| | $R_L \geq 600\Omega$ | ±10 | ±12.8 | | V |
| Output Resistance | DC, Open Loop | | 70 | | Ω |
| Short Circuit Current | $R_L$ = 0Ω | | 25 | 60 (6) | mA |
| **POWER SUPPLY** | | | | | |
| Rated Voltage | | | ±15 | | VDC |
| Voltage Range, Derated Performance | | ±4 | | ±22 | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 3.3 | 5.7 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Operating | | –40 | | +85 | °C |

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter specified by design.

# ELECTRICAL CHARACTERISTICS (Cont.)

At $V_{CC} = \pm15V$ and $-40°C \le T_A \le +85°C$, unless otherwise noted.

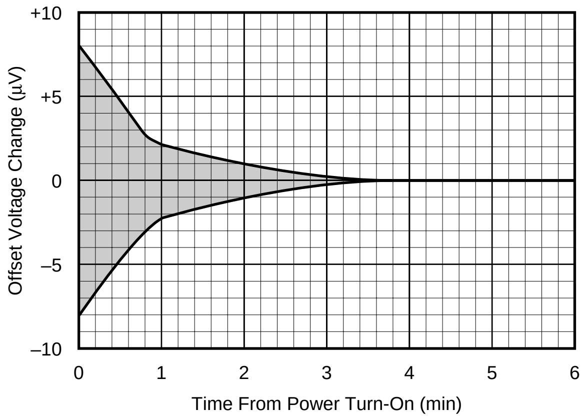
| PARAMETER | CONDITIONS | OPA27 OPA37 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT VOLTAGE**[1] | | | | | |
| Input Offset Voltage | | | ±48 | ±220[3] | µV |
| Average Drift[2] | $T_{A\,MIN}$ to $T_{A\,MAX}$ | | ±0.4 | ±1.8[3] | µV/°C |
| Supply Rejection | $\pm V_{CC}$ = 4.5 to 18V | | | | |
| | $\pm V_{CC}$ = 4.5 to 18V | 90[3] | 122 | | dB |
| **BIAS CURRENT** | | | | | |
| Input Bias Current | | | ±21 | ±150[3] | nA |
| **OFFSET CURRENT** | | | | | |
| Input Offset Current | | | 20 | 135[3] | nA |
| **VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±10.5[3] | ±11.8 | | V |
| Common-Mode Rejection | $V_{IN}$ = ±11VDC | 96[3] | 122 | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | |
| Open-Loop Voltage Gain | $R_L \ge 2k\Omega$ | 113[3] | 120 | | dB |
| **RATED OUTPUT** | | | | | |
| Voltage Output | $R_L = 2k\Omega$ | ±11.0[3] | ±13.4 | | V |
| Short Circuit Current | $V_O$ = 0VDC | | 25 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |

NOTES: (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter specified by design.

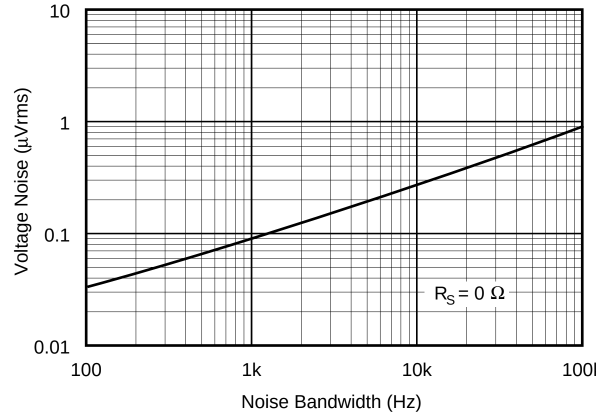
# TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

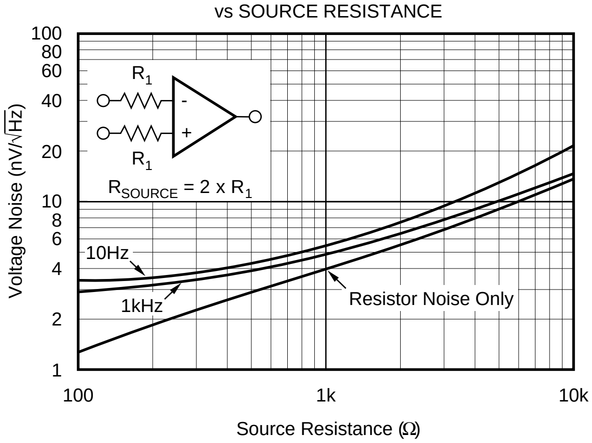
INPUT OFFSET VOLTAGE WARM-UP DRIFT



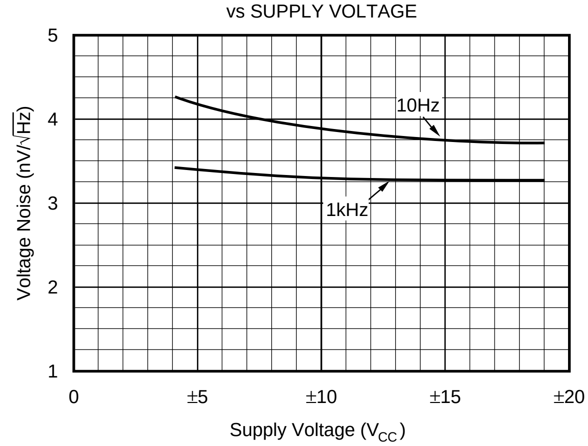

INPUT VOLTAGE NOISE vs NOISE BANDWIDTH
(0.1Hz to Indicated Frequency)



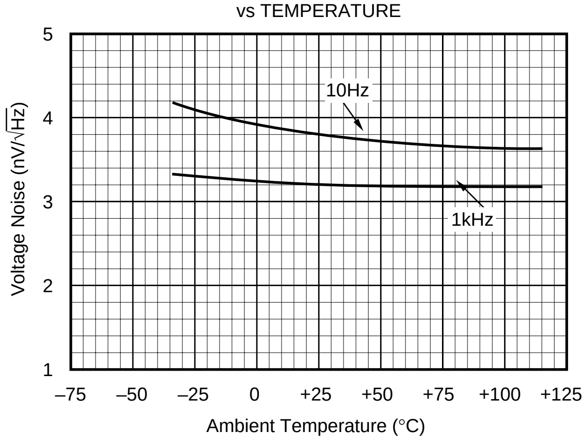

TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



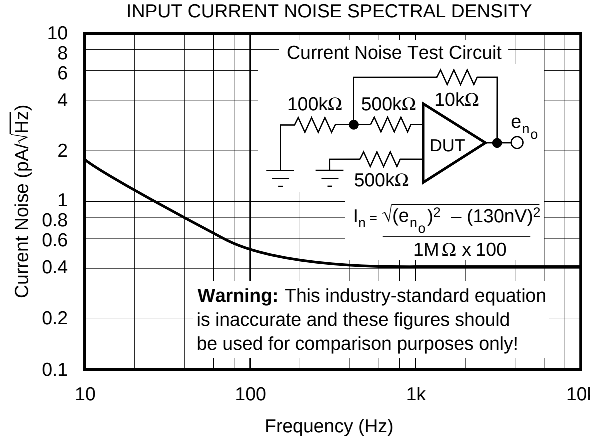

VOLTAGE NOISE SPECTRAL DENSITY
vs SUPPLY VOLTAGE




VOLTAGE NOISE SPECTRAL DENSITY
vs TEMPERATURE

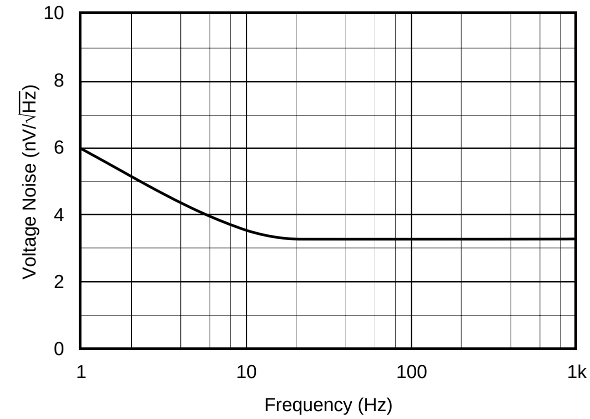



INPUT CURRENT NOISE SPECTRAL DENSITY

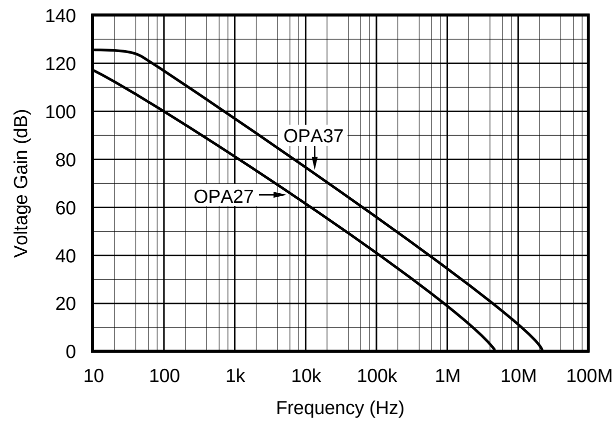


At $T_A$ = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

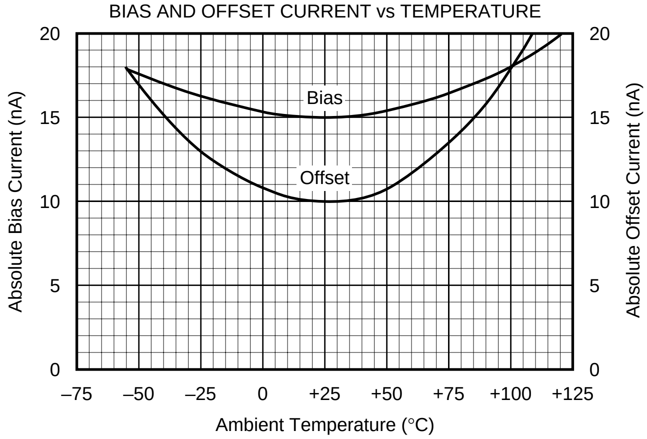
INPUT VOLTAGE NOISE SPECTRAL DENSITY



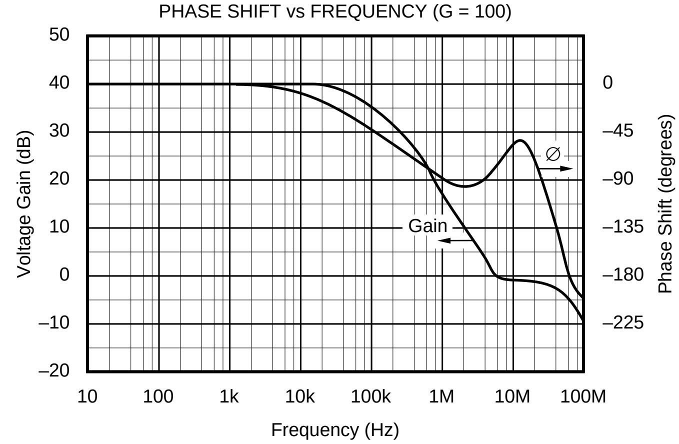

OPEN-LOOP FREQUENCY RESPONSE



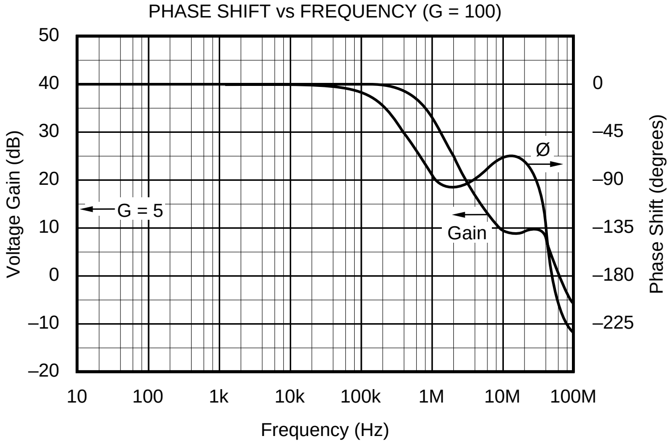

BIAS AND OFFSET CURRENT vs TEMPERATURE



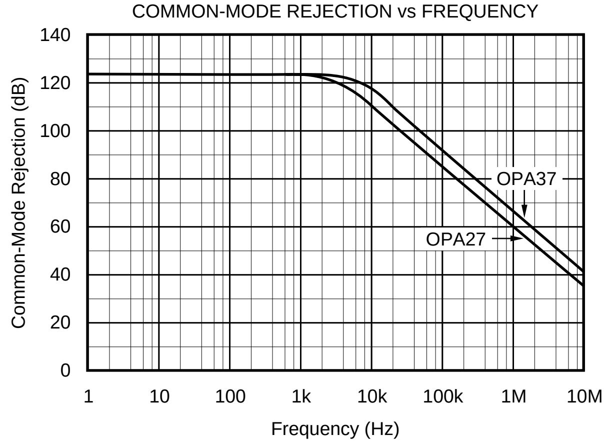

OPA27 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



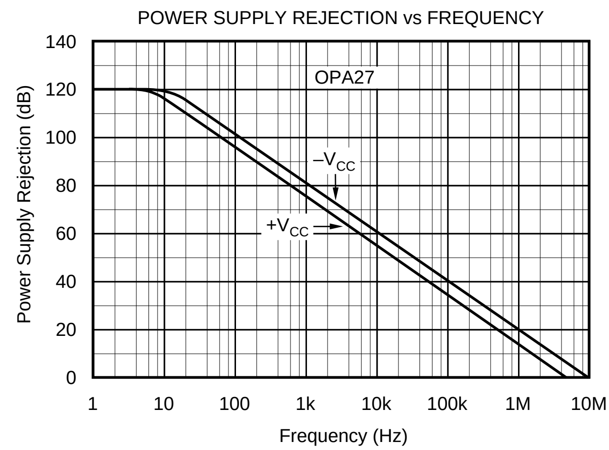

OPA37 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)

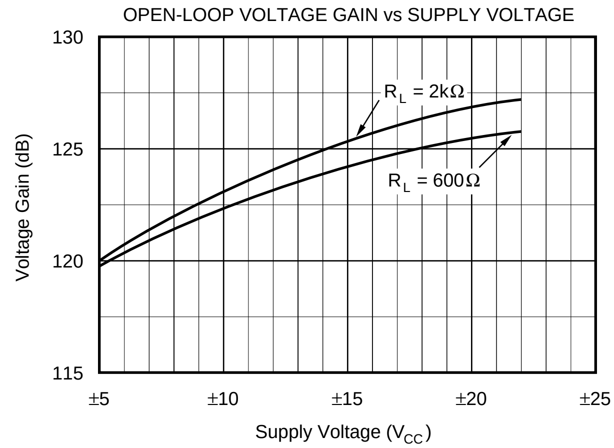


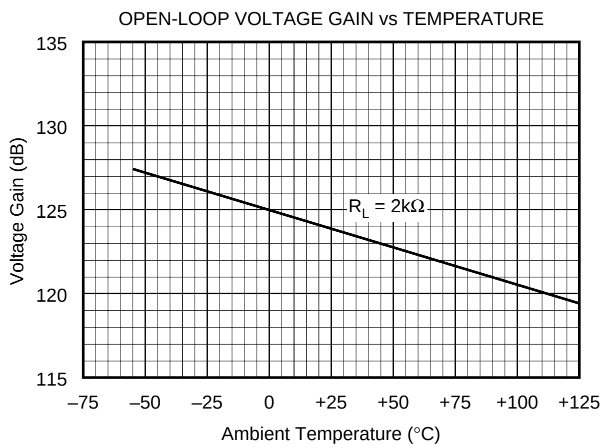

COMMON-MODE REJECTION vs FREQUENCY

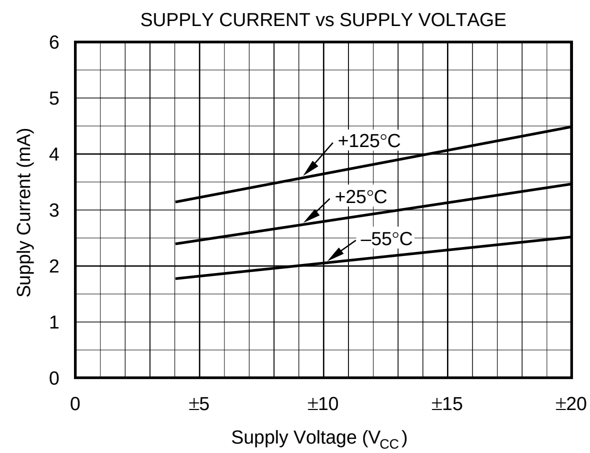


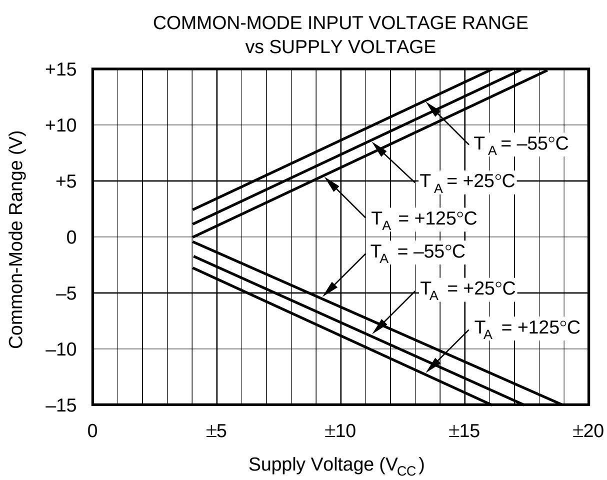
At $T_A = +25°C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

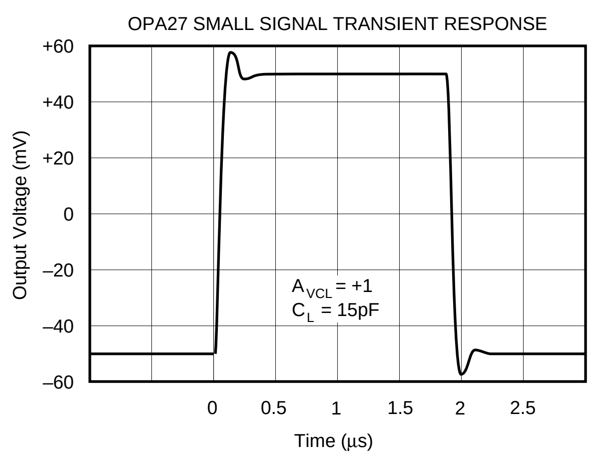


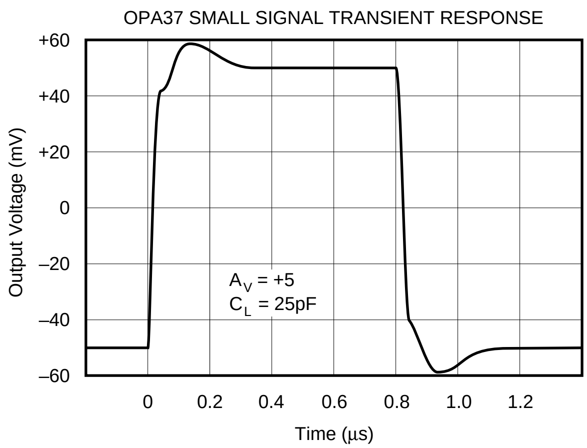



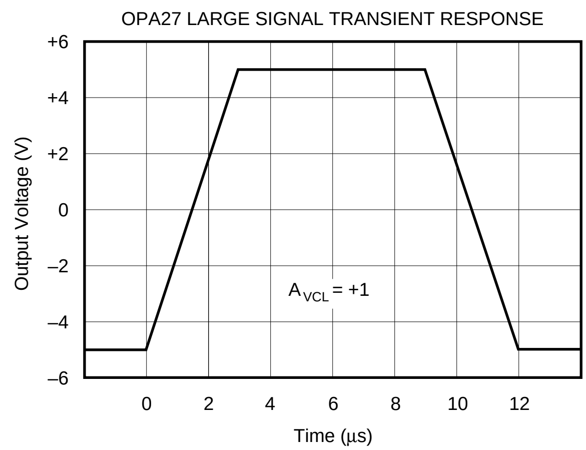



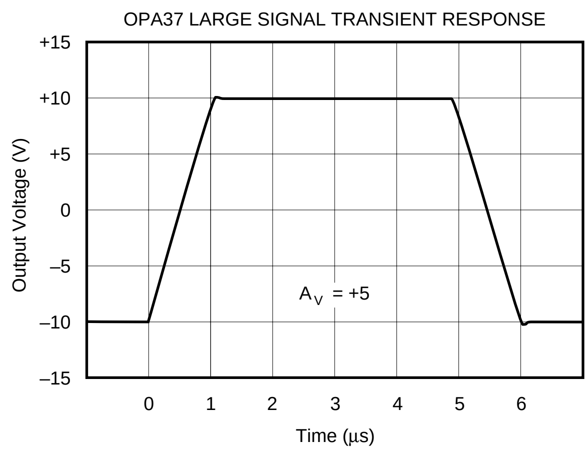



At $T_A$ = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.



# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used, but $V_{OS}$ drift will be degraded by an additional 0.1µV/°C to 0.2µV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3µV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

## THERMOELECTRIC POTENTIALS

The OPA27 and OPA37 are laser-trimmed to microvolt-level input offset voltages, and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference (see Figure 11).

Short, direct mounting of the OPA27 and OPA37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

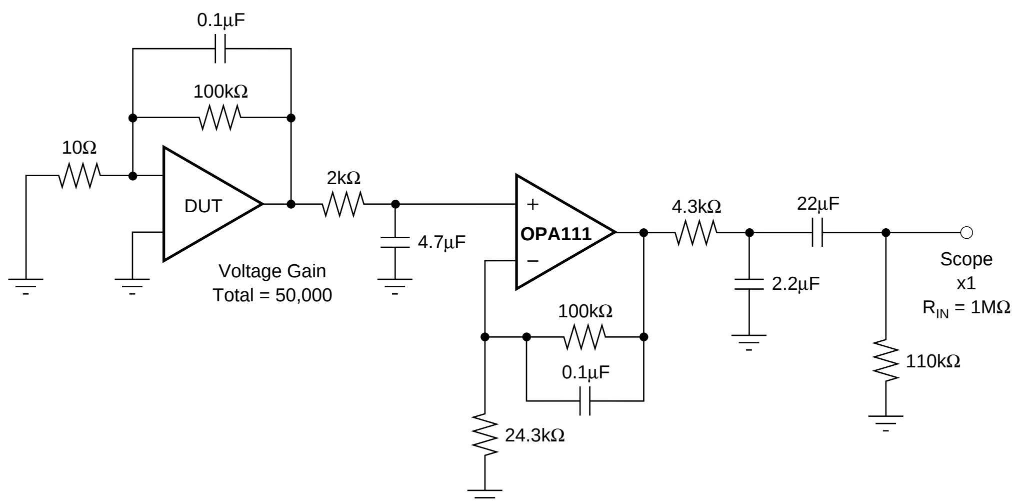



FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

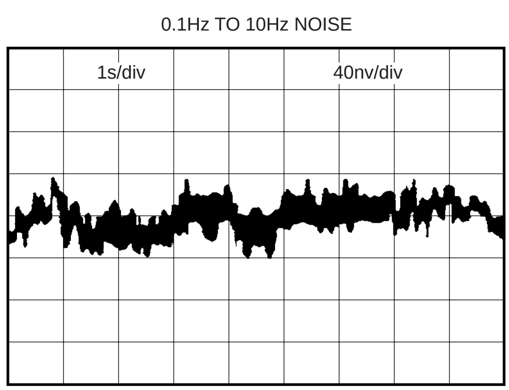



FIGURE 2. Low Frequency Noise.

## NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 5.

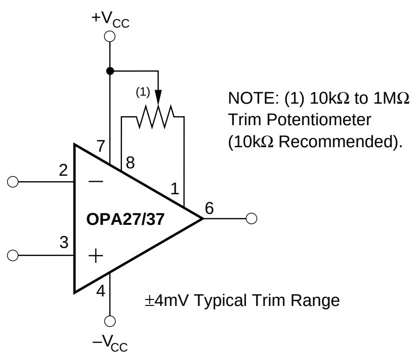



FIGURE 3. Offset Voltage Trim.

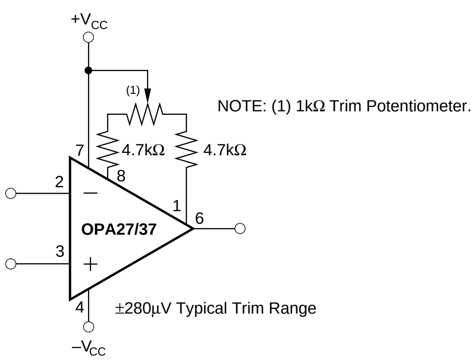



FIGURE 4. High Resolution Offset Voltage Trim.

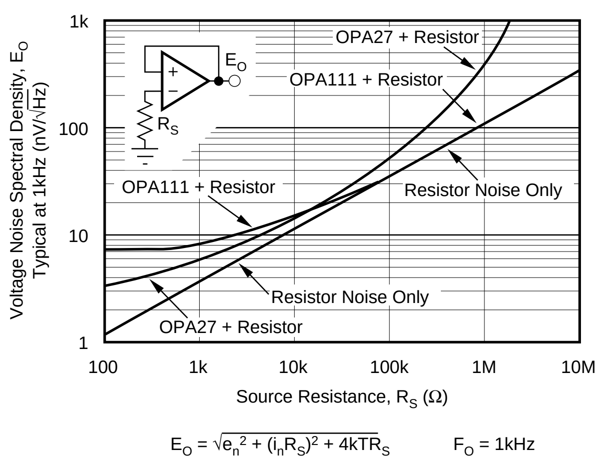



FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

## COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor ($R_F$) which is greater than 2kΩ. This capacitor will compensate the pole generated by $R_F$ and $C_{IN}$ and eliminate peaking or oscillation.

## INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27 and OPA37. Exceeding a few hundred millivolts differential input signal will cause current to flow, and without external current limiting resistors, the input will be destroyed.

Accidental static discharge, as well as high current, can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged, as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OPA27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended, as shown in Figure 6.

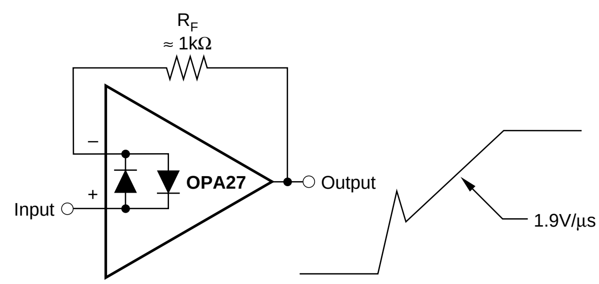



FIGURE 6. Pulsed Operation.

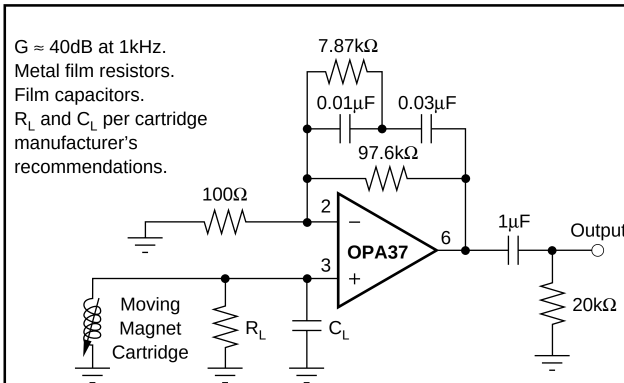



FIGURE 7. Low-Noise RIAA Preamplifier.

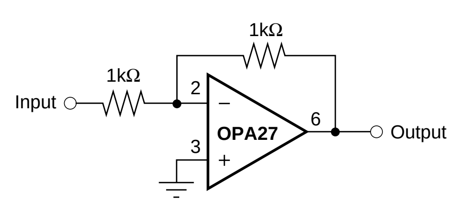



FIGURE 8. Unity-Gain Inverting Amplifier.

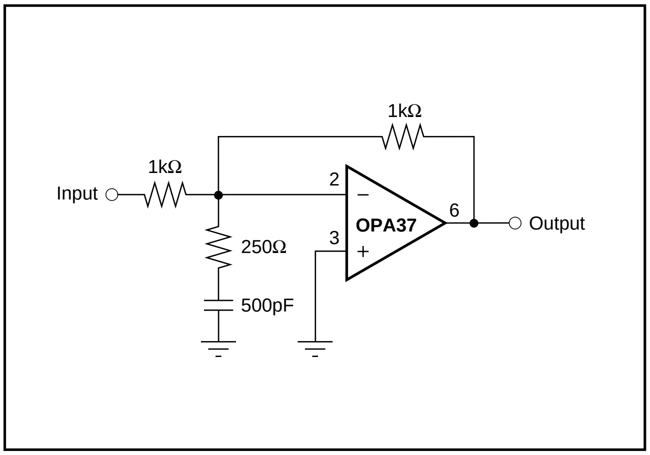



FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

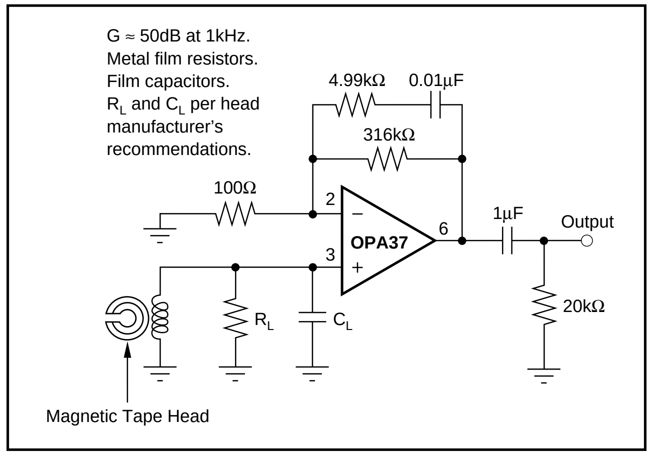



FIGURE 10. NAB Tape Head Preamplifier.

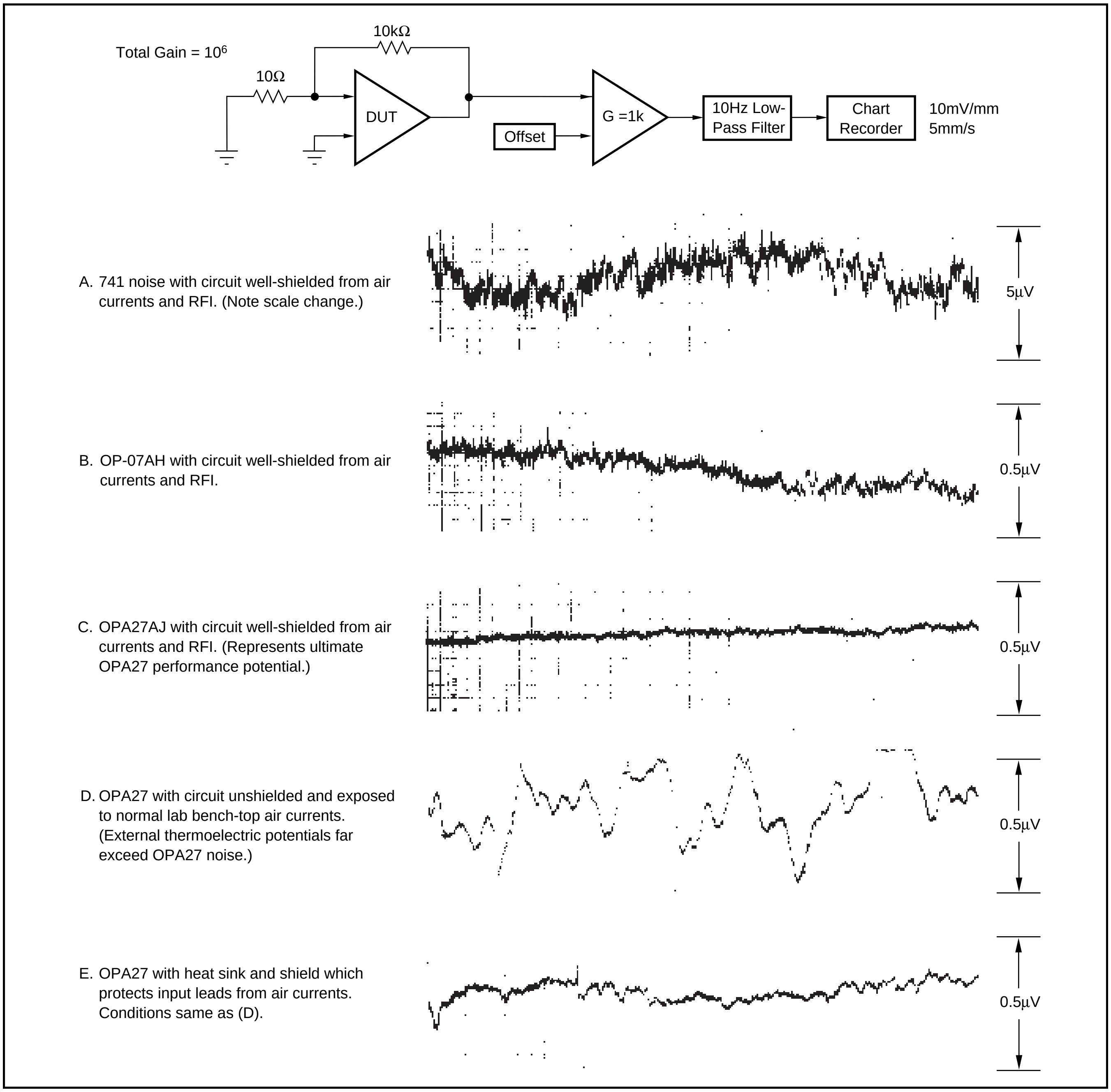



FIGURE 11. Low Frequency Noise Comparison.

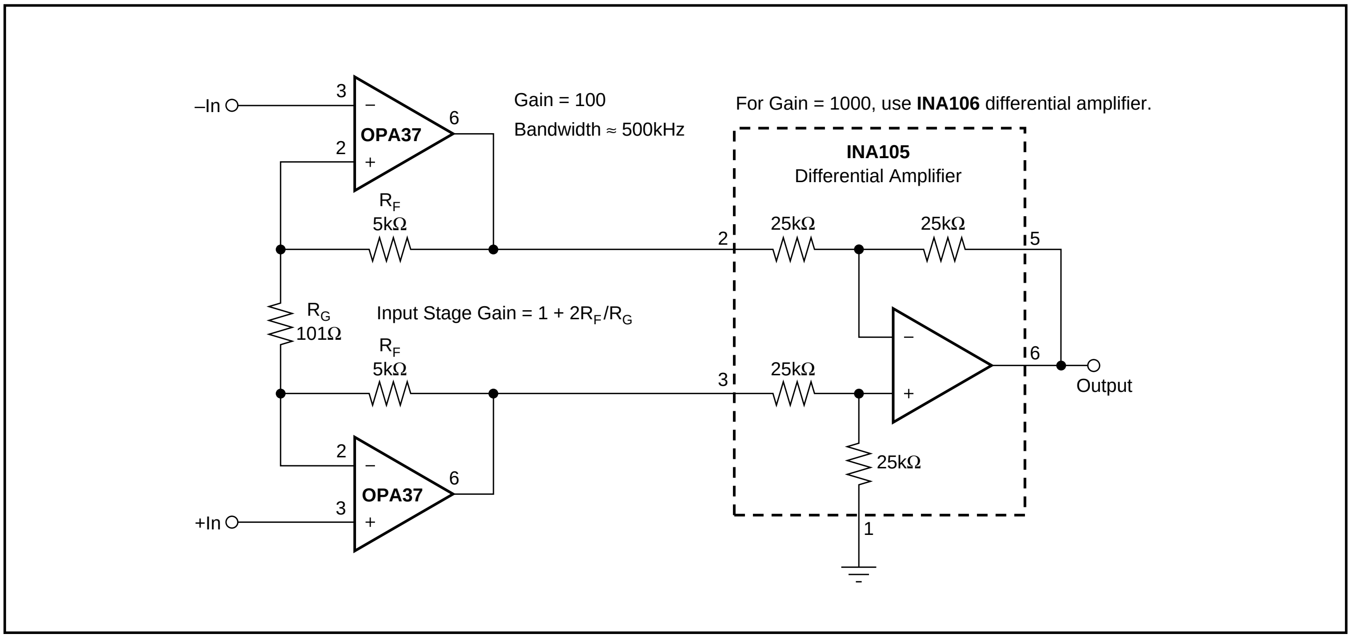



FIGURE 12. Low Noise Instrumentation Amplifier.

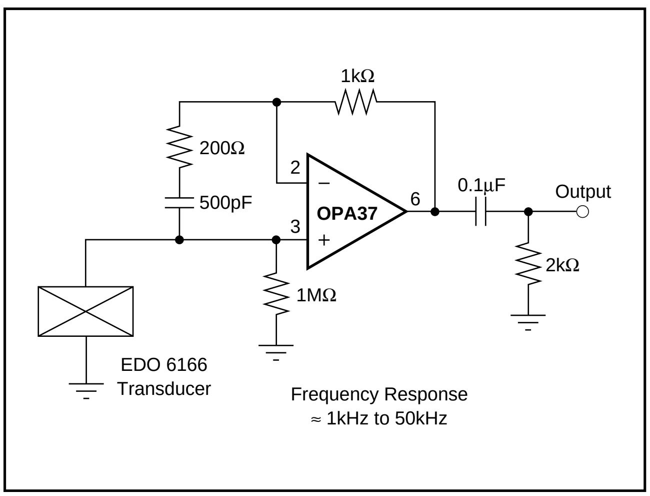



FIGURE 13. Hydrophone Preamplifier.

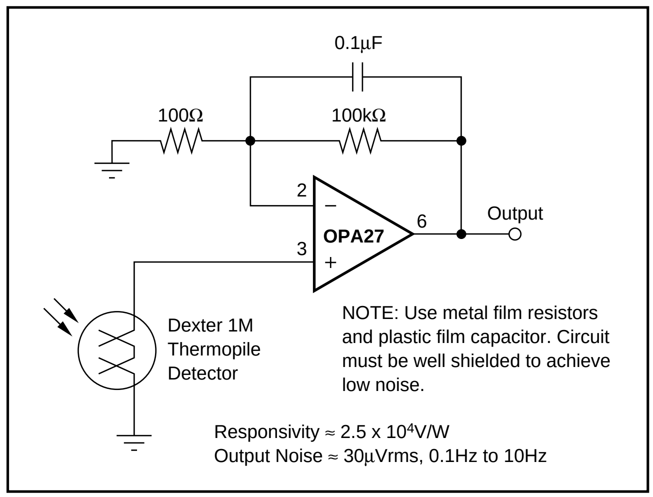
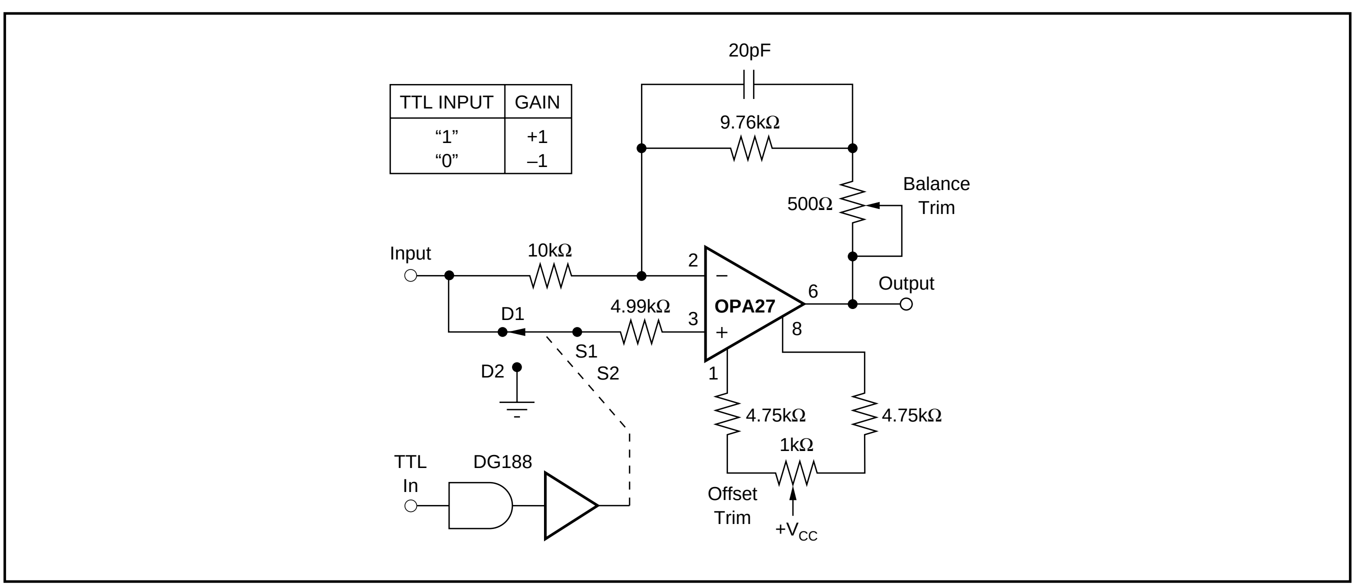



FIGURE 14. Long-Wavelength Infrared Detector Amplifier.




| TTL INPUT | GAIN |
|---|---|
| "1" | +1 |
| "0" | –1 |

FIGURE 15. High Performance Synchronous Demodulator.

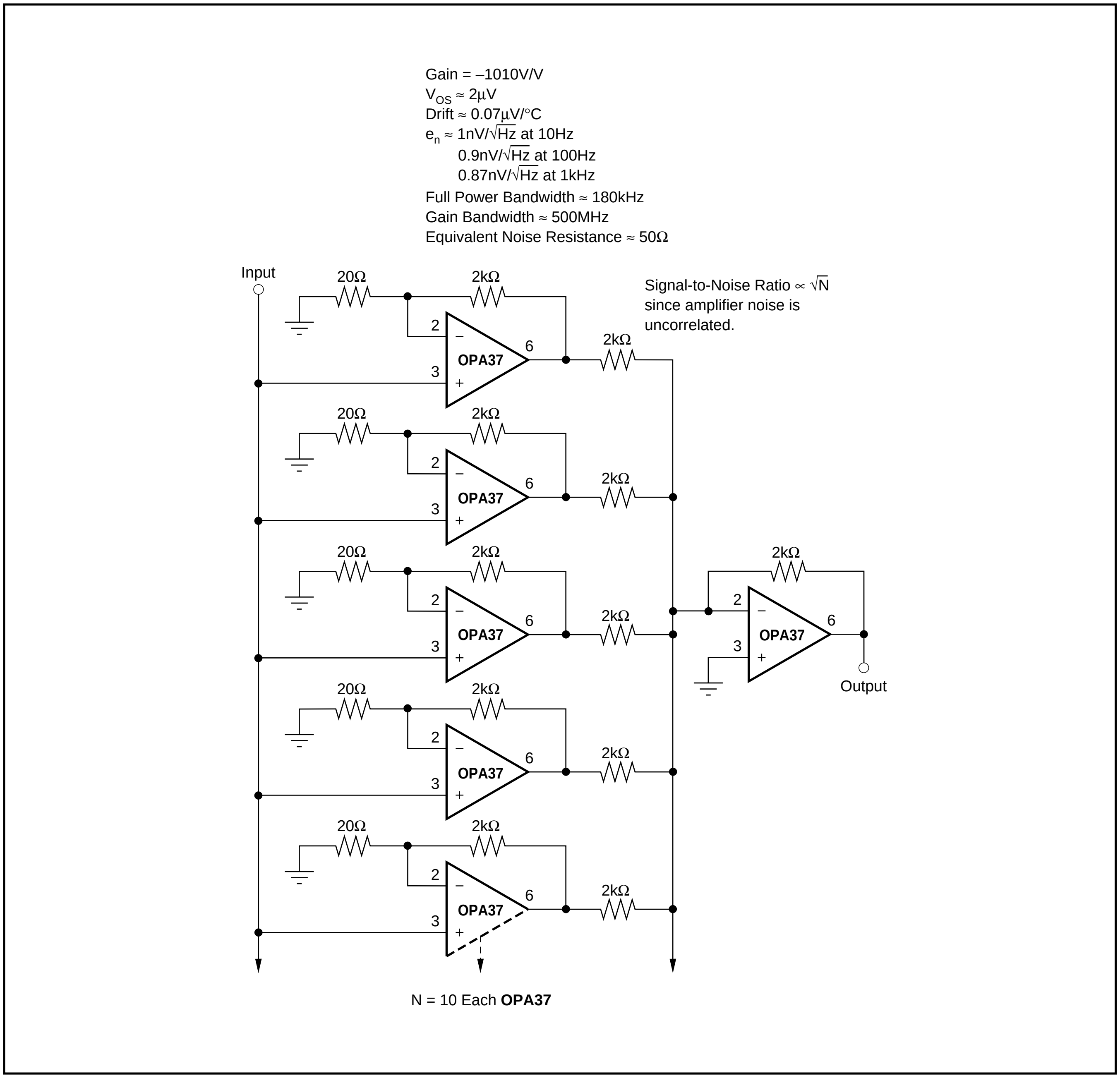



FIGURE 16. Ultra-Low Noise "N"-Stage Parallel Amplifier.

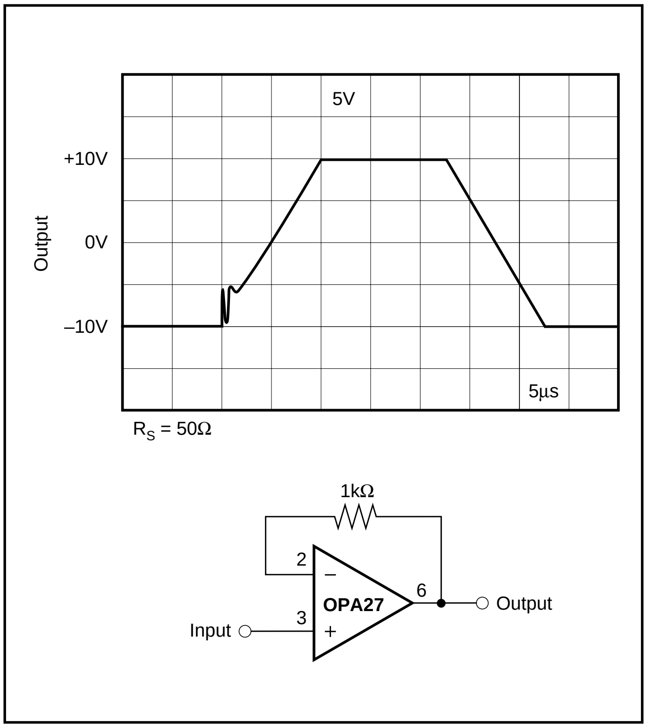



FIGURE 17. Unity-Gain Buffer.

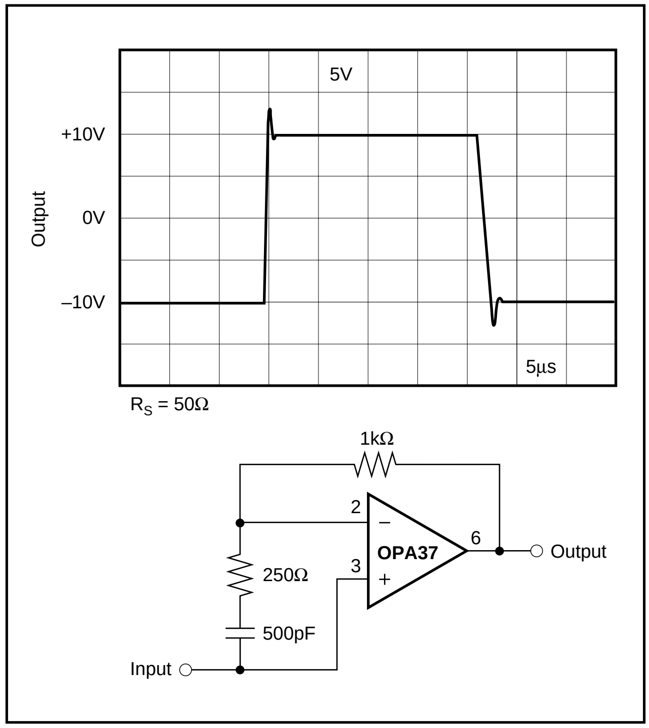



FIGURE 18. High Slew Rate Unity-Gain Buffer.

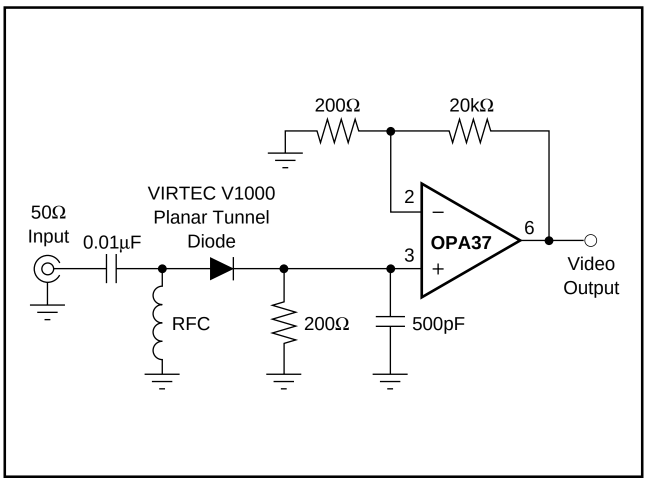



FIGURE 19. RF Detector and Video Amplifier.

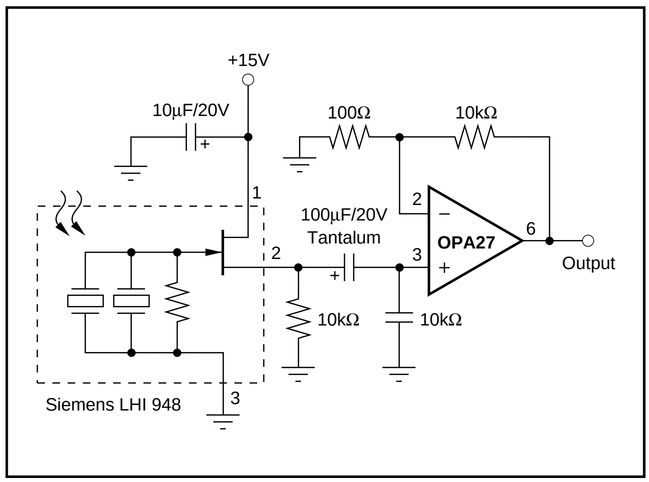



FIGURE 20. Balanced Pyroelectric Infrared Detector.

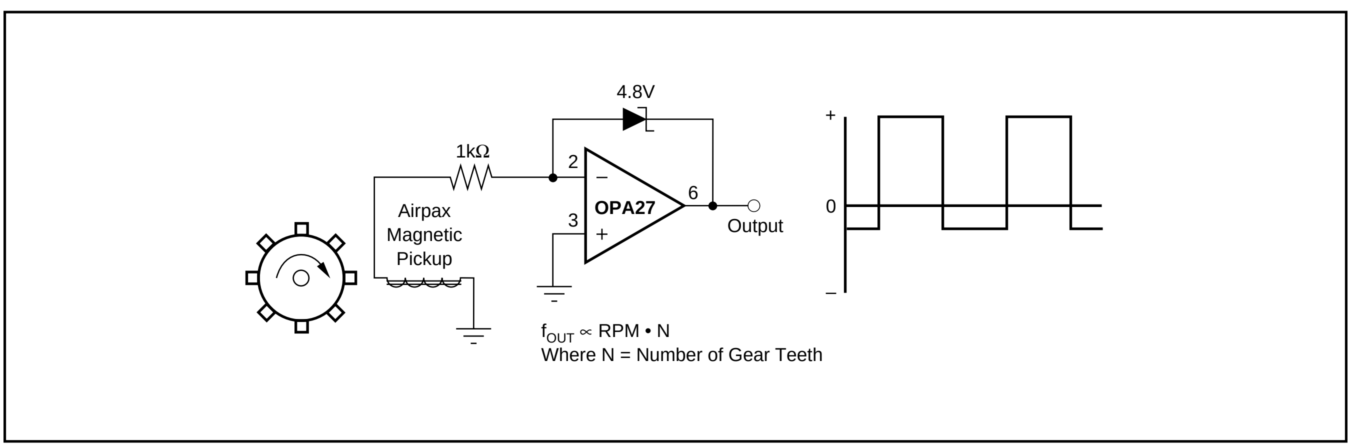



FIGURE 21. Magnetic Tachometer.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA27GP | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA27GP |
| OPA27GP.A | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA27GP |
| OPA27GU | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 27U |
| OPA27GU.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 27U |
| OPA27GU/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 27U |
| OPA27GU/2K5.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 27U |
| OPA37GP | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA37GP |
| OPA37GP.A | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA37GP |
| OPA37GPG4 | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA37GP |
| OPA37GU | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 37U |
| OPA37GU.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 37U |
| OPA37GU/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 37U |
| OPA37GU/2K5.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | OPA 37U |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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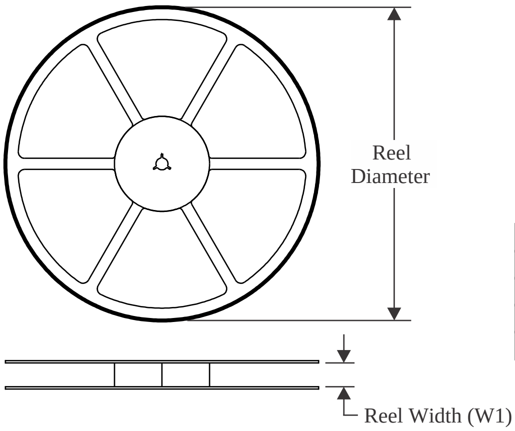
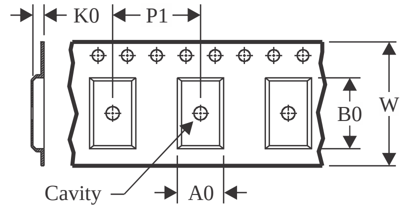
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

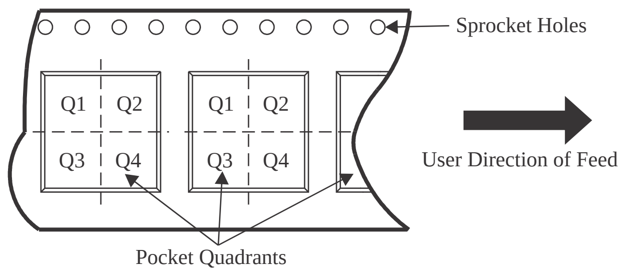



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

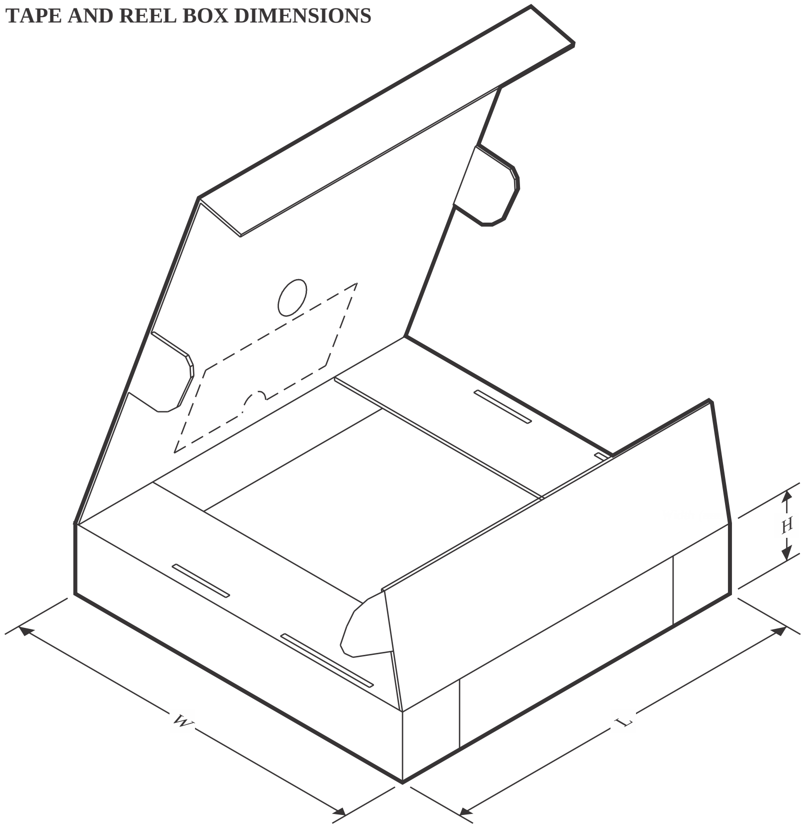
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA27GU/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA27GU/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA37GU/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

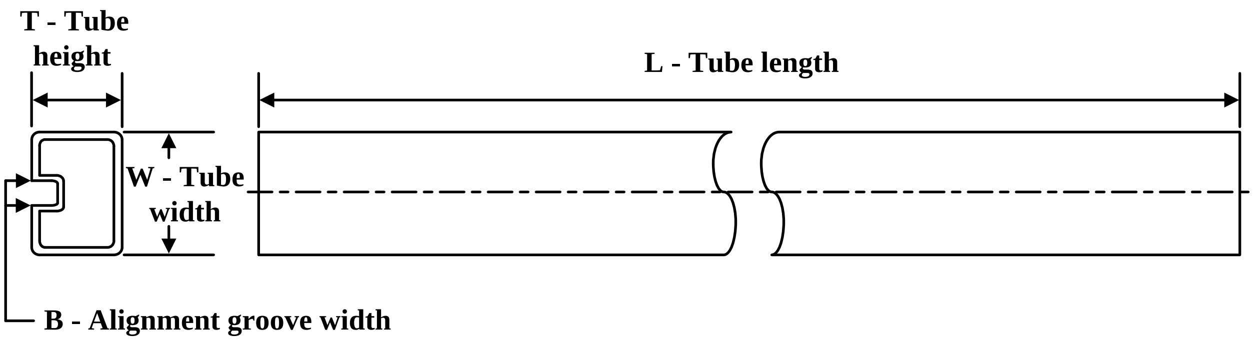
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

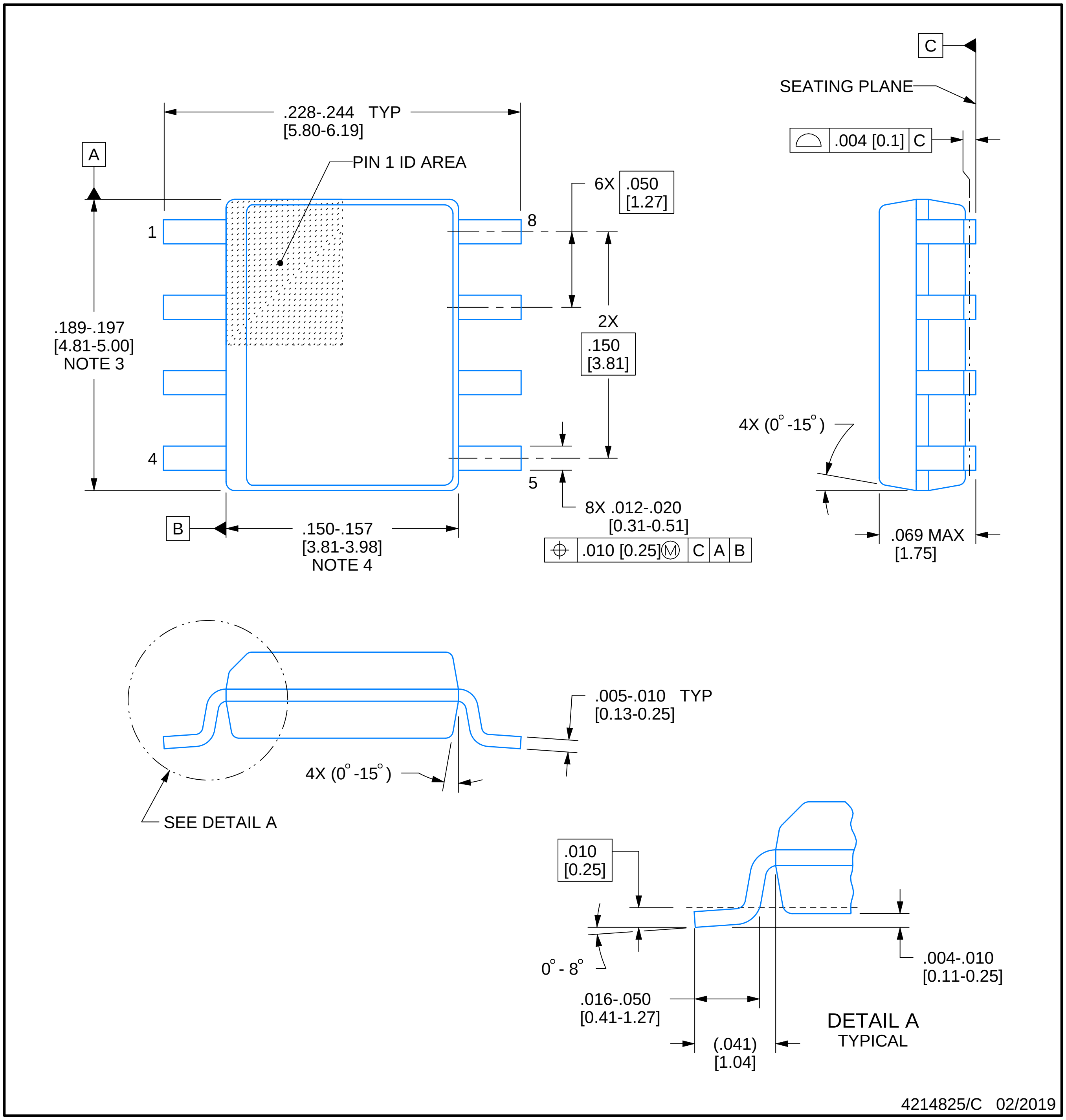
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA27GU/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA27GU/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA37GU/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE



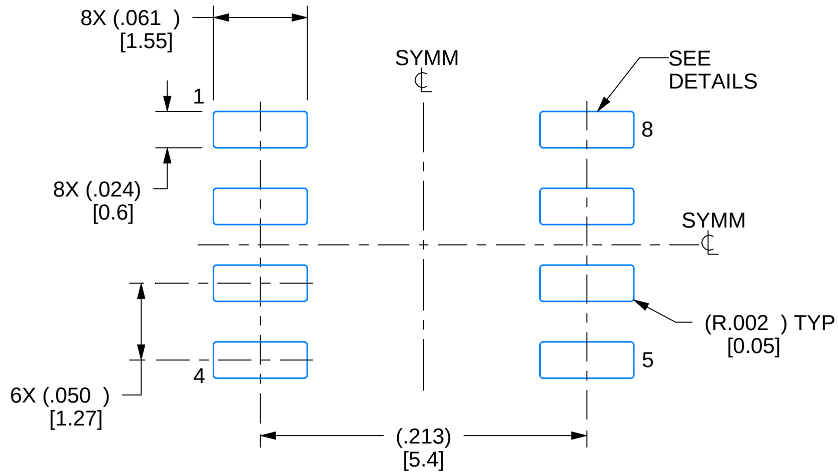

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA27GP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA27GP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA27GU | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA27GU.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA37GP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA37GP.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA37GPG4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA37GU | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA37GU.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

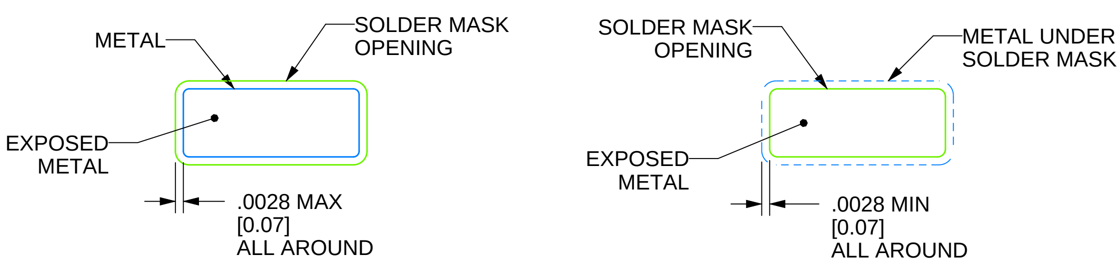



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




NON SOLDER MASK DEFINED

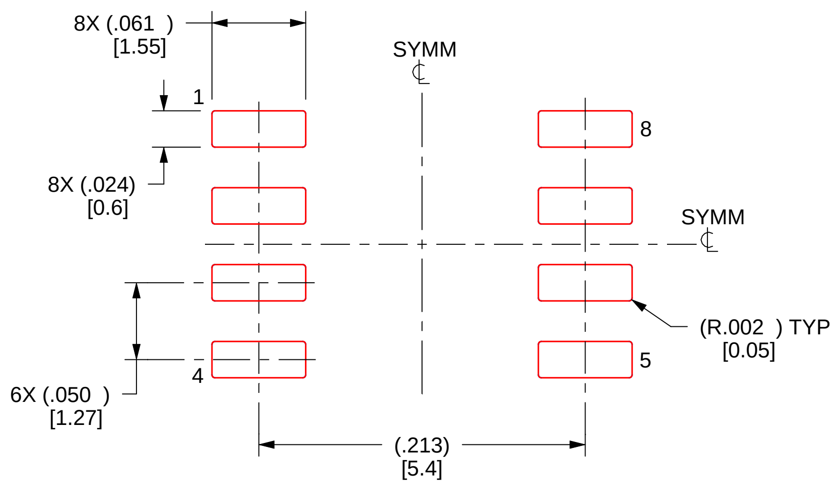
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



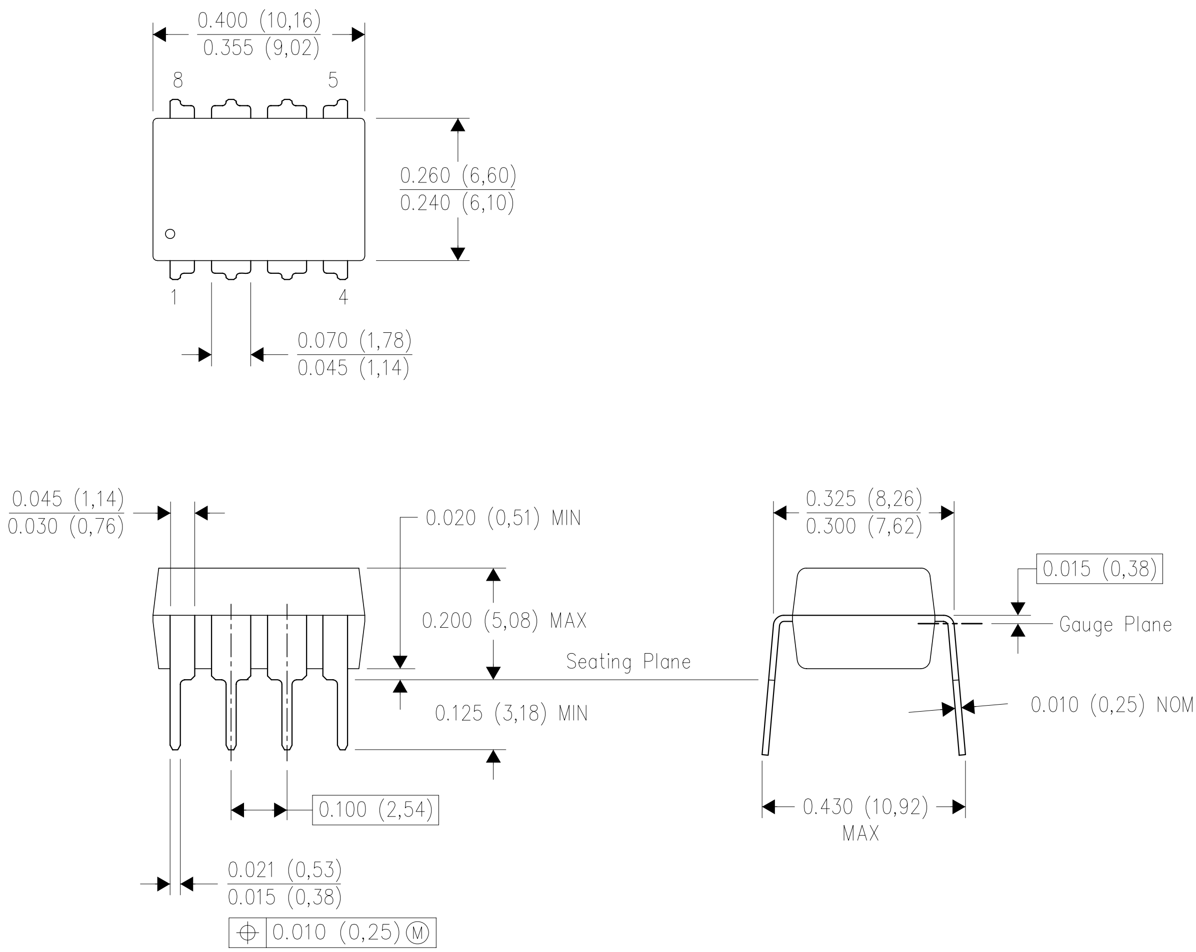

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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