











OPA356-Q1

SBOS479A - MARCH 2009-REVISED APRIL 2018

## **OPA356-Q1 200-MHz CMOS Operational Amplifier**

#### **Features**

- **Qualified For Automotive Applications**
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Unity-Gain Bandwidth: 450 MHz Wide Bandwidth: 200-MHz GBW
- High Slew Rate: 360 V/µs Low Noise: 5.8 nV/√Hz
- **Excellent Video Performance:** 
  - Differential Gain: 0.02%
  - Differential Phase: 0.05°
- 0.1-dB Gain Flatness: 75 MHz Input Range Includes Ground
- Rail-To-Rail Output (Within 100 mV)
- Low Input Bias Current: 3 pA
- Thermal Shutdown
- Single-Supply Operating Range: 2.5 V to 5.5 V

## 2 Applications

- Infotainment Systems
- **ADAS Systems**
- Radar
- Dynamic Stability Controls (DSC)

## 3 Description

The OPA356-Q1 is a high-speed voltage-feedback CMOS operational amplifier designed for video and other applications requiring wide bandwidth. The OPA356-Q1 is unity-gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.05°. Quiescent current is only 8.3 mA.

The OPA356-Q1 is optimized for operation on single or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). The common-mode input range for the OPA356-Q1 extends 100 mV below ground and up to 1.5 V from V+. The output swing is within 100 mV of the rails, supporting wide dynamic range.

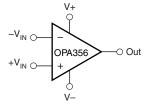
The OPA356-Q1 is available in the SOT23-5 package and is specified over the -40°C to 125°C range.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA356-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### **Simplified Schematic**





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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

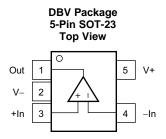
## Changes from Original (March 2009) to Revision A

Page

•	Added Device Information table, ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes section, Application and Implementation section, Power Supply Recommendations section,	
	Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	. 1
•	Added AEC-Q100 Qualification Features bullet	. 1
•	Deleted Ordering Information table	. 3
•	Deleted footnote 2 from Absolute Maximum Ratings table	. 4
•	Deleted the SR, t <sub>r</sub> , t <sub>f</sub> , t <sub>settle</sub> , and Overload recovery time rows from the <i>Electrical Characteristics</i> table and moved to the <i>Timing Requirements</i> table	. 5
•	Changed Layout Guidelines title from PCB Layout	19



## 5 Pin Configuration and Functions



## **Pin Functions**

	PIN	I/O	DESCRIPTION					
NO.	NAME	1/0	DESCRIPTION					
1	Out	0	Output pin					
2	V-		Negative power supply					
3	+In	1	Noninverting input pin					
4	–In	1	Inverting input pin					
5	V+		Positive power supply					

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## 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Vs	Supply voltage, V+ to V-		7.5	V
$V_{IN}$	Signal input pins voltage range	-0.5	(V+) + 0.5	V
	V– current		10	mA
	Output short-circuit duration <sup>(2)</sup>	Con	tinuous	
T <sub>A</sub>	Operating free-air temperature range	-40	125	°C
TJ	Junction temperature		160	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Clastrostatia dia sharea	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	\/
	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	V

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		,		
		M	IN MAX	UNIT
Vs	Supply voltage, V- to V+	2	2.7 5.5	V
T <sub>A</sub>	Operating free-air temperature	_	40 125	°C

#### 6.4 Thermal Information

		OPA356-Q1	
	THERMAL METRIC <sup>(1)</sup>	DBV (SOT-23)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.0	°C/W
R <sub>0</sub> JC(top)	Junction-to-case (top) thermal resistance	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	18.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

<sup>(2)</sup> Short-circuit to ground one amplifier per package.



## 6.5 Electrical Characteristics

 $V_S = 2.7 \text{ V}$  to 5.5 V,  $R_F = 604 \Omega$ ,  $R_L = 150 \Omega$  connected to  $V_S / 2$  (unless otherwise noted)

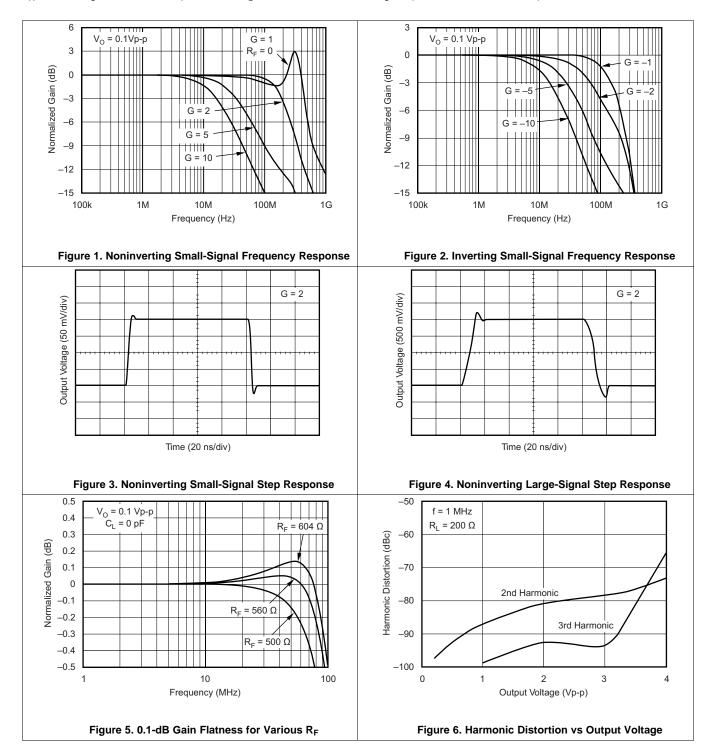
	PARAMETER		TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP	MAX	UNIT
\/	lanut offeet voltege		V 5VV V .09V	25°C		±2	±9	\/
V <sub>OS</sub>	Input offset voltage		$V_S = 5 \text{ V}, V_{CM} = V - + 0.8 \text{ V}$	Full range			±15	mV
ΔV <sub>OS</sub> /ΔT	Offset voltage drift over	r temperature		Full range		±7		μV/°C
PSRR	Offset voltage drift vs p	ower supply	$V_S = 2.7 \text{ V to } 5.5 \text{ V},$ $V_{CM} = V_S / 2 - 0.15 \text{ V}$	25°C		±80	±350	μV/V
l <sub>B</sub>	Input bias current			25°C		3	±50	pA
los	Input offset current			25°C		±1	±50	pА
V <sub>n</sub>	Input voltage noise den	nsity	f = 1 MHz	25°C		5.8		nV/√Hz
n	Input current noise den	sity	f = 1 MHz	25°C		50		fA/√Hz
V <sub>CM</sub>	Input common-mode vo	oltage range		25°C	V 0.1		V+ - 1.5	V
OMBB			V 55V 04V V 4V	25°C	66	80		in.
CMRR	Input common-mode rejection ratio		$V_S = 5.5 \text{ V}, -0.1 \text{ V} < V_{CM} < 4 \text{ V}$	Full range	66			dB
Z <sub>ID</sub>	Differential input imped	ance		25°C		10 <sup>13</sup>    1.5		Ω    pF
Z <sub>ICM</sub>	Common-mode input in	npedance		25°C		10 <sup>13</sup>    1.5		Ω    pF
				25°C	84	92		
A <sub>OL</sub>	Open-loop gain		$V_S = 5 \text{ V}, 0.3 \text{ V} < V_O < 4.7 \text{ V}$	Full range	80			dB
			G = 1, $V_O = 100 \text{ mVp-p}$ , $R_F = 0 \Omega$			450		
			$G = 2$ , $V_O = 100 \text{ mVp-p}$ , $R_L = 50 \Omega$			100		Ì
f_ <sub>3dB</sub>	Small-signal bandwidth		$G = 2$ , $V_O = 100 \text{ mVp-p}$ , $R_L = 150 \Omega$	25°C		170		MHz
			$G = 2$ , $V_0 = 100 \text{ mVp-p}$ , $R_L = 1 \text{ k}\Omega$			200		
GBW	Gain-bandwidth produc	·+	$G = 10, R_1 = 1 k\Omega$	25°C		200		MHz
0.1dB	Bandwidth for 0.1-dB g		$G = 2$ , $V_O = 100 \text{ mVp-p}$ , $R_F = 560 \Omega$	25°C		75		MHz
0.108	Dandwidth for 0.1-db gain namess		2, 10 100 111 111 111	200		+300		141112
SR	Slew rate		$V_S = 5 \text{ V}, G = 2, 4-V \text{ output step}$	25°C		-360		V/µs
$t_r$ , $t_f$	Rise and fall times		$G = 2$ , $V_0 = 200 \text{ mVp-p}$ , 10% to 90%	25°C		2.4		ns
ч, ч	Trisc and fair times		G = 2, V <sub>O</sub> = 2 Vp-p, 10% to 90%	200		8		
١	Settling time	0.1%	V <sub>S</sub> = 5 V, G = 2, 2-V output step	25°C		30		ns
settle	Jetting time	0.01%	vg = 5 v, G = 2, 2-v output step	25 0		120		113
	Overload recovery time	•	$V_{IN} \times Gain = V_{S}$	25°C		8		ns
	Harmonic distortion	Second harmonic	G = 2, f = 1 MHz, V <sub>O</sub> = 2 Vp-p,	25°C		-81		dBc
	Harmonic distortion	Third harmonic	$R_L = 200 \Omega$	25°C		-93		ubc
	Differential gain error	1	NTSC, $R_L = 150 \Omega$	25°C		0.02%		
	Differential phase error		NTSC, $R_L = 150 \Omega$	25°C		0.05		0
			$V_S = 5 \text{ V}, R_L = 150 \Omega, A_{OL} > 84 \text{ dB}$			0.2	0.3	
	Voltage output swing fr	om rail	$V_S = 5 \text{ V}, R_L = 1 \text{ k}\Omega$	25°C		0.1		V
			$V_S = 5 \text{ V}, R_L = 50 \Omega$	1		0.4	0.6	
		Continuous	0 , 2		±60			
О	Output current <sup>(2)</sup>		V <sub>S</sub> = 5 V	25°C	±100			mA
O		Peak	V <sub>S</sub> = 3 V			±80		1
	<u> </u>		<u> </u>			+250		
	Short-circuit current			25°C		-200		mA
			+	25°C		0.02		Ω
	Closed-loop output imp	edance				U.U_		
	Closed-loop output imp	edance				8.3	11	
la	Closed-loop output imp	edance	V <sub>S</sub> = 5 V, I <sub>O</sub> = 0	25°C		8.3	11	mA
lα	<u> </u>		$V_S = 5 \text{ V}, I_O = 0$ Shutdown			8.3	11	mA

<sup>(1)</sup> Full range T<sub>A</sub> = -40°C to 125°C.
(2) See Figure 20.

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#### 6.6 Typical Characteristics

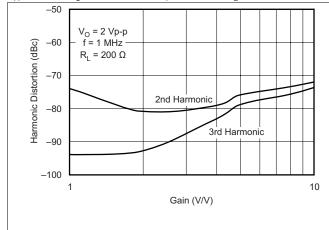
 $T_A = 25$ °C,  $V_S = 5$  V, G = 2,  $R_F = 604$   $\Omega$ ,  $R_L = 150$   $\Omega$  connected to  $V_S$  / 2 (unless otherwise noted)





## **Typical Characteristics (continued)**

 $T_A = 25$ °C,  $V_S = 5$  V, G = 2,  $R_F = 604$   $\Omega$ ,  $R_L = 150$   $\Omega$  connected to  $V_S$  / 2 (unless otherwise noted)



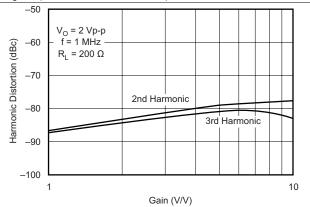
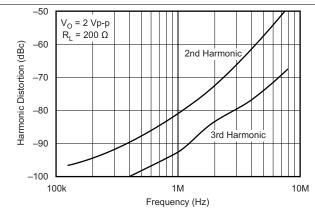


Figure 7. Harmonic Distortion vs Non-Inverting Gain

Figure 8. Harmonic Distortion vs Inverting Gain



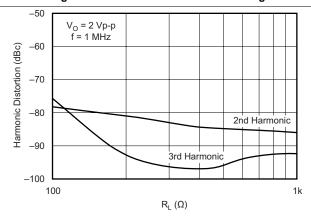
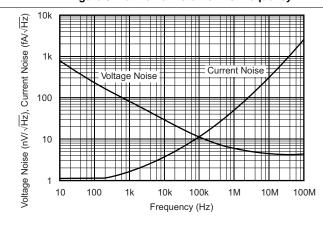


Figure 9. Harmonic Distortion vs Frequency

Figure 10. Harmonic Distortion vs Load Resistance



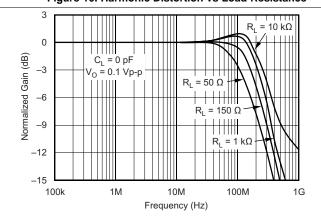


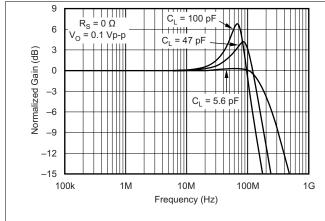
Figure 11. Input Voltage and Current Noise Spectral Density vs Frequency

Figure 12. Frequency Response for Various  $R_{\mathsf{L}}$ 

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## **Typical Characteristics (continued)**

 $T_A$  = 25°C,  $V_S$  = 5 V, G = 2,  $R_F$  = 604  $\Omega$ ,  $R_L$  = 150  $\Omega$  connected to  $V_S$  / 2 (unless otherwise noted)



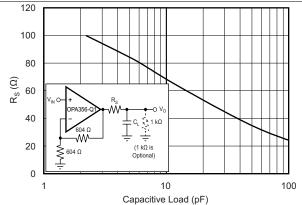
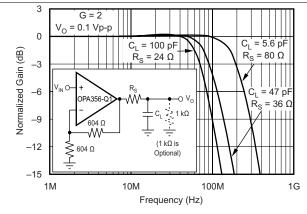


Figure 13. Frequency Response for Various  $C_{\mathsf{L}}$ 

Figure 14. Recommended R<sub>S</sub> vs Capacitive Load



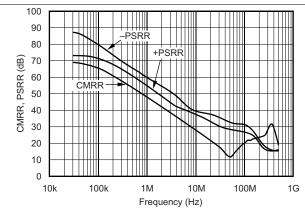
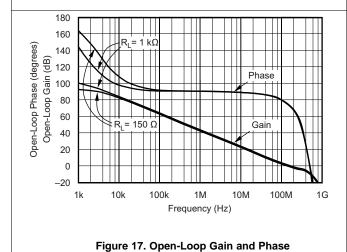


Figure 15. Frequency Response vs Capacitive Load

Figure 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency



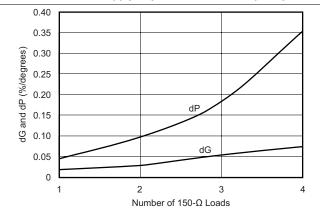


Figure 18. Composite Video Differential Gain and Phase

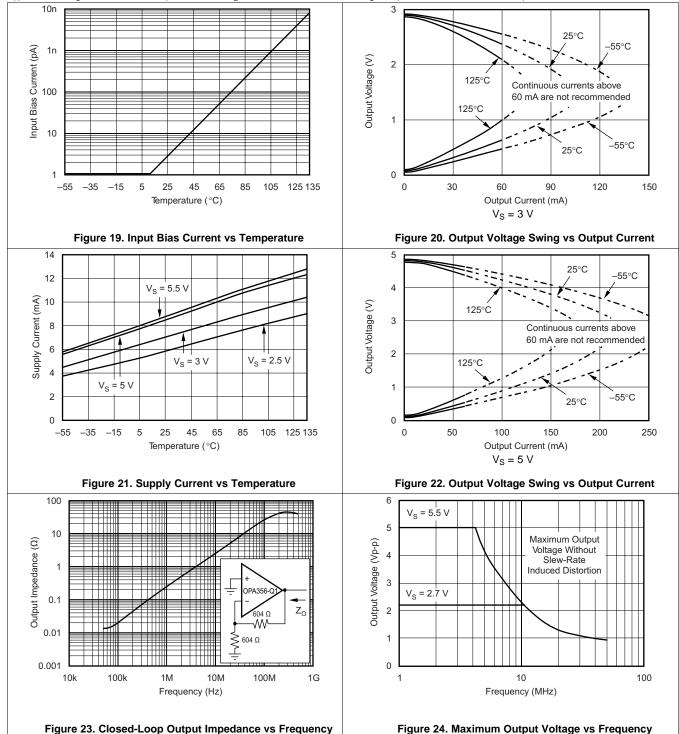
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## **Typical Characteristics (continued)**

 $T_A$  = 25°C,  $V_S$  = 5 V, G = 2,  $R_F$  = 604  $\Omega$ ,  $R_L$  = 150  $\Omega$  connected to  $V_S$  / 2 (unless otherwise noted)

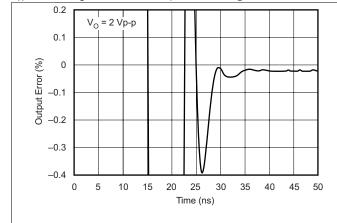


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## **Typical Characteristics (continued)**

 $T_A$  = 25°C,  $V_S$  = 5 V, G = 2,  $R_F$  = 604  $\Omega$ ,  $R_L$  = 150  $\Omega$  connected to  $V_S$  / 2 (unless otherwise noted)



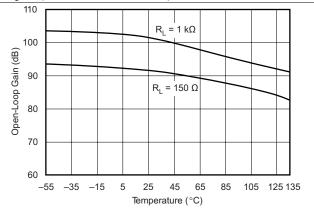
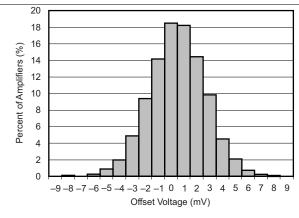


Figure 25. Output Settling Time to 0.1%

Figure 26. Open-Loop Gain vs Temperature

100



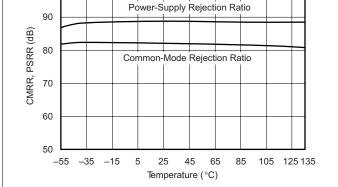


Figure 27. Offset Voltage Production Distribution

Figure 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

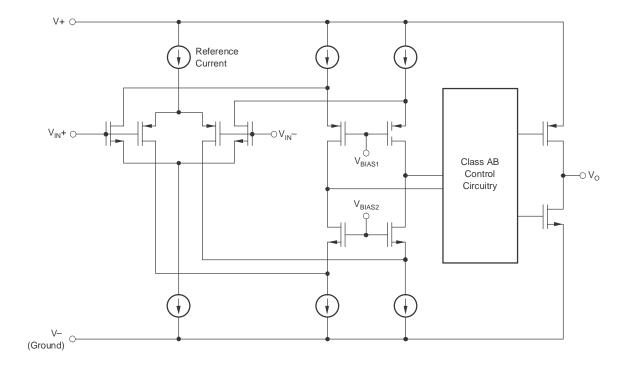


## 7 Detailed Description

#### 7.1 Overview

The OPA356-Q1 operational amplifier is a high-speed, 360-V/μs, amplifier, making the device a great option for transimpedance applications. The device is unity-gain stable and can operate on a single-supply voltage (2.7 V to 5.5 V), or a split-supply voltage ( $\pm 1.35$  V to  $\pm 2.75$  V), making the device highly versatile and simple to use. The OPA356-Q1 amplifier is specified from 2.7 V to 5.5 V and over the automotive temperature range of -40°C to +125°C.

## 7.2 Functional Block Diagram



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Product Folder Links: OPA356-Q1



#### 7.3 Feature Description

#### 7.3.1 Operating Voltage

The OPA356-Q1 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

#### 7.3.2 Output Drive

The output stage of the OPA356-Q1 is capable of driving a standard back-terminated 75- $\Omega$  video cable. A back-terminated transmission line does not exhibit a capacitive load to its driver. A properly back-terminated 75- $\Omega$  cable does not appear as capacitance; the cable presents only a 150- $\Omega$  resistive load to the OPA356-Q1 output.

The output stage can supply high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA356-Q1 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

#### NOTE

TI does not recommend running a continuous dc current in excess of ±60 mA. See Figure 20 in the *Typical Characteristics* section.

#### 7.4 Device Functional Modes

The OPA356-Q1 is powered on when the supply is connected. The device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. The device can also be used with asymmetrical supplies as long as the differential voltage (V- to V+) is at least 1.8 V and no greater than 5.5 V (for example, V- is set to -3.5 V and V+ is set to 1.5 V).



## 8 Application and Implementation

#### 8.1 Application Information

The OPA355-Q1 is a CMOS, high-speed, voltage-feedback, operational amplifier (op-amp) designed for general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 300-V/ $\mu$ s slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

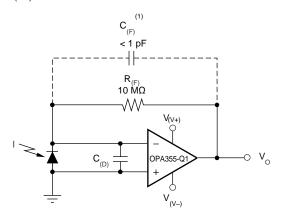
The input common-mode voltage range of the device includes ground, which allows the OPA356-Q1 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

#### 8.2 Typical Applications

#### 8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA356-Q1 a preferred wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 29, are the expected diode capacitance  $(C_{(D)})$ , which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain  $(R_{(FB)})$ , and the gain-bandwidth (GBW) for the OPA356-Q1 (20 MHz). With these three variables set, the feedback capacitor value  $(C_{(FB)})$  is set to control the frequency response.  $C_{(FB)}$  includes the stray capacitance of  $R_{(FB)}$ , which is 0.2 pF for a typical surface-mount resistor.



C<sub>(FB)</sub> is optional to prevent gain peaking. C<sub>(FB)</sub> includes the stray capacitance of R<sub>(FB)</sub>.

Figure 29. Dual-Supply Transimpedance Amplifier

#### 8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage V <sub>(V+)</sub>	2.5 V
Supply voltage V <sub>(V-)</sub>	–2.5 V

#### 8.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole must be set to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \tag{1}$$

Use Equation 2 to calculate the bandwidth.

$$f_{\text{(-3 dB)}} = \sqrt{\frac{\text{GBW}}{2 \times \pi \times \text{R}_{\text{(FB)}} \times \text{C}_{\text{(D)}}}}$$
(2)

For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 30. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

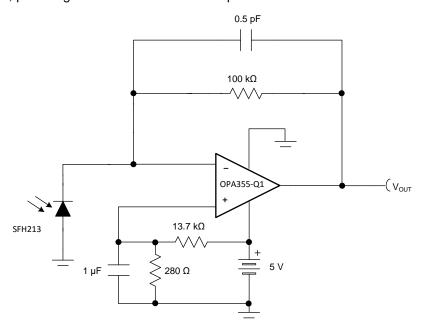


Figure 30. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate Transimpedance Amplifiers Intuitively* application bulletin.

#### 8.2.1.2.1 Optimizing The Transimpedance Circuit

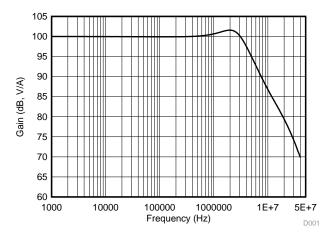
To achieve the best performance, select components according to the following guidelines:

- 1. For lowest noise, select  $R_{(FB)}$  to create the total required gain. Using a lower value for  $R_{(FB)}$  and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by  $R_{(FB)}$  increases with the square-root of  $R_{(FB)}$ , whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
- 2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
- 3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the  $R_{(FB)}$  to limit bandwidth, even if not required for stability.
- 4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, see the *Noise Analysis of FET Transimpedance Amplifiers* and *Noise Analysis for High-Speed Op Amps* application bulletins).



#### 8.2.1.3 Application Curve



-3 dB bandwidth is 4.56 MHz

Figure 31. AC Transfer Function

#### 8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 M $\Omega$ , or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 32, where  $(V_{(+|Nx)} = V_S - I_{(B|AS)} \times R_{(S)})$ . The last term,  $I_{(B|AS)} \times R_{(S)}$ , shows the voltage drop across  $R_{(S)}$ . To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by  $I_{(B|AS)} \times R_{(S)}$  less than the input voltage noise of the amplifier, so that the input voltage noise does not become the dominant noise factor. The OPA356-Q1 op amp features very low input bias current (typically 200 fA), and is therefore a preferred choice for such applications.

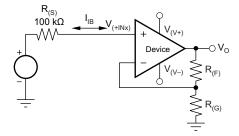


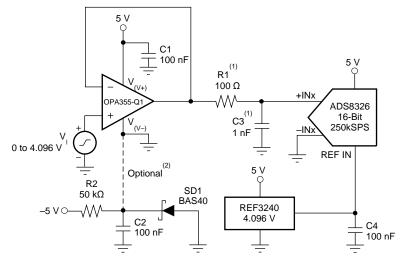
Figure 32. Noise as a Result of I(BIAS)



#### 8.2.3 Driving ADCs

The OPA356-Q1 op amps are designed for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA356-Q1 to drive ADCs without degradation of differential linearity and THD.

The OPA356-Q1 can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 33 shows the OPA356-Q1 configured to drive the ADS8326.



- (1) Suggested value; may require adjustment based on specific application.
- (2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a -0.3-V supply to allow output swing to true ground potential.

Figure 33. Driving the ADS8326

#### 8.2.4 Active Filter

The OPA356-Q1 is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 34 depicts a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is -40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

- 1. Adding an inverting amplifier
- 2. Adding an additional second-order MFB stage
- 3. Using a noninverting filter topology, such as the Sallen-Key (see Figure 35).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.



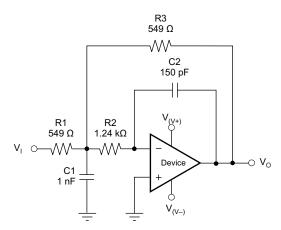


Figure 34. Second-Order Butterworth 500-kHz Low-Pass Filter

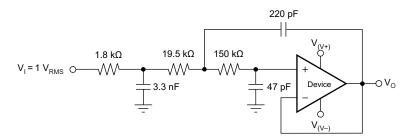


Figure 35. OPA356-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter



## 9 Power Supply Recommendations

The OPA356-Q1 is specified for operation from 2.7 to 5.5 V (±1.35 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or highimpedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, VS – VO. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application bulletin AB-039, *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and is available on www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

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## 10 Layout

#### 10.1 Layout Guidelines

- Good high-frequency PC board layout techniques should be employed for the OPA356-Q1. Generous use of
  ground planes, short direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean,
  stable operation. Large areas of copper also provide a means of dissipating heat that is generated within the
  amplifier in normal operation.
- · Sockets are definitely not recommended for use with any high-speed amplifier.
- A 10-µF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

## 10.2 Layout Example

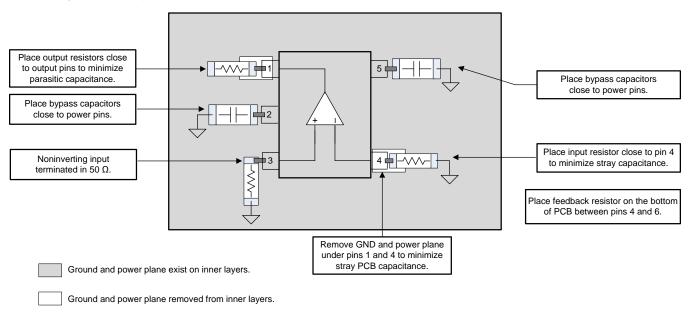


Figure 36. Example Layout

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## 11 Device and Documentation Support

#### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- OPAx380 Precision, High-Speed Transimpedance Amplifier
- OPAx354 250-MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers
- OPAx300 Low-Noise, High-Speed, 16-Bit Accurate, CMOS Operational Amplifier
- OPAx355 200MHz, CMOS Operational Amplifier With Shutdown
- OPA656 Wideband, Unity-Gain Stable, FET-Input Operational Amplifier
- OPA657 1.6-GHz, Low-Noise, FET-Input Operational Amplifier
- Compensate Transimpedance Amplifiers Intuitively
- Noise Analysis of FET Transimpedance Amplifiers
- Noise Analysis for High-Speed Op Amps
- ADS8326 16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling Analog-to-Digital Converter
- FilterPro™

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

FilterPro is a trademark of Texas Instruments Incorporated.

All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: OPA356-Q1

www.ti.com 7-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
OPA356AQDBVRQ1	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOVQ
OPA356AQDBVRQ1.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	OOVQ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF OPA356-Q1:

Catalog: OPA356

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

www.ti.com 7-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 24-Apr-2020

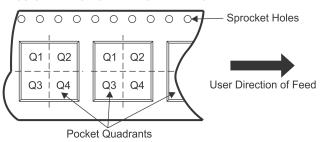
## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA356AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

www.ti.com 24-Apr-2020



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA356AQDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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