OPAx310-Q1 Automotive High Output Current, 5V, RRIO, 3MHz Operational Amplifier with Shutdown

1 Features

- High output current: ±150mA typical I_{SC} at 5.5V
- Fast enable from shutdown: 0.9µs typical
- Wide operational supply voltage: 1.5V to 5.5V
- Low input offset voltage: ±250µV typical
- Fail-safe inputs: No diode from inputs to V+
- Optimized quiescent current: 165µA/ch typical
- Rail-to-rail input and output
- Gain bandwidth product: 3MHz typical at 5.5V
- Thermal noise floor: 16nV/$\sqrt{Hz}$ typical
- Unity-gain stable
- Drives up to 250pF without sustained oscillations
- Internal RFI and EMI filtered input pins
- Operating temperature range: –40°C to 125°C

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Traction inverter
- Battery management systems (BMS)
- On-board charger (OBC) and wireless charger
- HEV/EV DC/DC converter
- Body electronics and lighting

3 Description

The OPAx310-Q1 family of op amps includes single (OPA310-Q1), dual (OPA2310-Q1), and quad-channel (OPA4310-Q1), low-voltage (1.5V to 5.5V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPA310S-Q1 variant also features a very fast shutdown response and has a typical enable time of 0.9µs that allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310-Q1 family has a robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

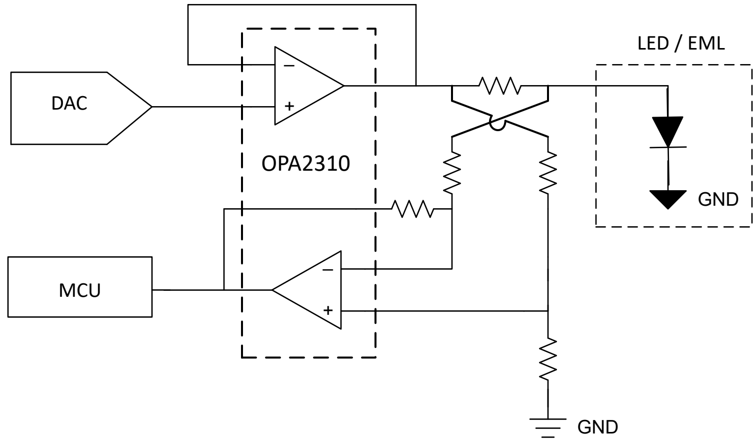
OPAx310-Q1 is offered in power pad, standard, small size package variants and has an internal current limit protection, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310-Q1 can swing very close to the rails and has a short-circuit current of 75mA minimum across temperature at 5.5V power supply. Additional output current capability can be achieved by carefully connecting multiple op amps in parallel. OPAx310-Q1 devices are an excellent choice for LED driver and other high current applications and can also be used as a reference buffer, guard amplifier, or as a discrete LDO.

The robust design of the OPAx310-Q1 family simplifies circuit design. These op amps feature an integrated RFI and EMI rejection filter with no-phase reversal in input overdrive conditions. These devices also deliver excellent AC performance with a gain bandwidth of 3MHz and can drive up to 250pF of capacitor load with no sustained oscillations, enabling designers to achieve both improved performance and a lower-power consumption.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(4)
OPA310-Q1	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
		DCK (SC70, 5)	2mm × 2.1mm
OPA310S-Q1	Single, Shutdown	DBV (SOT-23, 6)	2.9mm × 2.8mm
		DCK (SC70, 6)	2mm × 2.1mm
OPA2310-Q1(2)	Dual	D (SOIC, 8)(3)	4.9mm × 6mm
		DGK (VSSOP, 8)(3)	3mm × 4.9mm
OPA4310-Q1(2)	Quad	D (SOIC, 14)(3)	8.65mm × 6mm
		PW (TSSOP, 14)(3)	5mm × 6.4mm

(1) For more information, Section 10.
(2) Part number is for preview only.
(3) Package is for preview only.
(4) The package size (length × width) is a nominal value and includes pins, where applicable.



LED / EML Biasing With Current Sense

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4 Pin Configuration and Functions

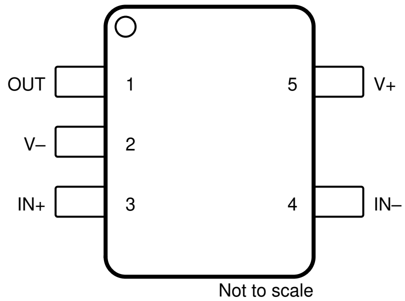


Figure 4-1. OPA310-Q1 DBV Package 5-Pin SOT-23 (Top View)

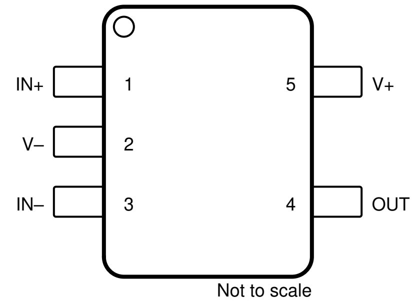


Figure 4-2. OPA310-Q1 DCK Package 5-Pin SC70 (Top View)

Table 4-1. Pin Functions: OPA310-Q1

PIN			TYPE[(1)]	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1) I = input, O = output

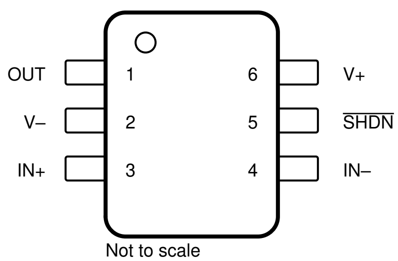


Figure 4-3. OPA310S-Q1 DBV Package 6-Pin SOT-23 (Top View)

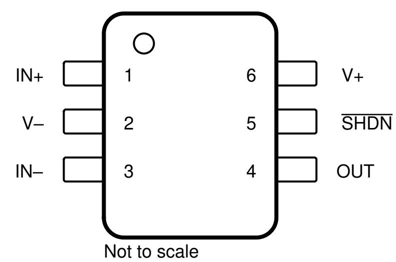


Figure 4-4. OPA310S-Q1 DCK Package 6-Pin SC70 (Top View)

Table 4-2. Pin Functions: OPA310S-Q1

PIN			TYPE[(1)]	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
SHDN	5	5	I	Shutdown: low = amp disabled, high = amp enabled See *Shutdown Function* for more information
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

(1) I = input, O = output

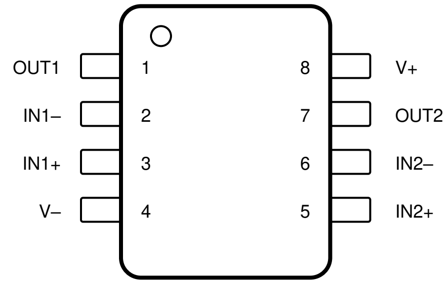


Figure 4-5. OPA2310-Q1 D and DGK Package 8-Pin SOIC and VSSOP (Top View)

Table 4-3. Pin Functions: OPA2310-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

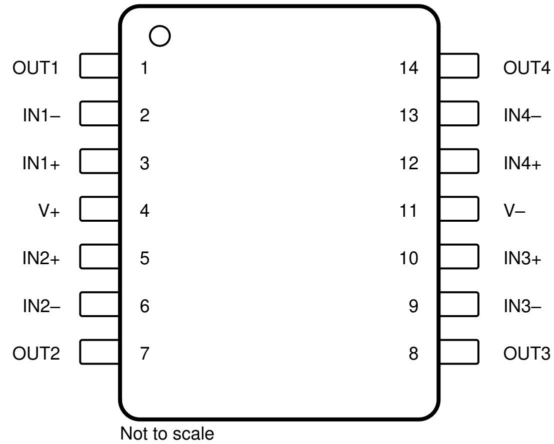


Figure 4-6. OPA4310-Q1 D and PW Package 14-Pin SOIC and TSSOP (Top View)

Table 4-4. Pin Functions: OPA4310-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Supply voltage, V_S = (V+) – (V–)	0	7	V
Signal input pins	Common-mode voltage (2) (3)	– 0.5	6.0	V
	Differential voltage (2) (3)		±6.0	V
	Current (3)	–10	10	mA
Output short-circuit (4)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins can swing beyond (V+) as long as they stay with in 6.0V. No diode structure from input pins to (V+).
(3) Input pins are diode-clamped to (V–). Input signals that 0.3V below (V–) must be current-limited to 10mA or less.
(4) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

PART NUMBER				VALUE	UNIT
OPA310-Q1	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
OPA310-Q1	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JS-002 (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.5	5.5	V
V_I	Input voltage range (Across specified temperature) 1.5V ≤ V_S < 2V	(V–)	(V+)	V
V_I	Input voltage range (Across specified temperature) 2V ≤ V_S ≤ 5.5V	(V–) – 0.1	(V+) + 0.1	V
V_I	Input voltage range	– 0.1	5.6	V
V_{IH}	High level input voltage at shutdown pin (amplifier enabled)	(V-) + 1.2	(V+)	V
V_{IL}	Low level input voltage at shutdown pin (amplifier disabled)	(V–)	(V-) + 0.2	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC [(1)]		OPA310-Q1		OPA310S-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.5	214.6	190.7	195.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.4	110.0	110.5	122.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.8	60.7	70.8	55.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.2	32.1	47.4	38.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.5	60.4	70.5	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC [(1)]		OPA2310-Q1	
		D (SOIC)	DGK (VSSOP)
		8 PINS	8 PINS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.0	187.7
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.2	78.1
$R_{\theta JB}$	Junction-to-board thermal resistance	82.4	109.5
Ψ_{JT}	Junction-to-top characterization parameter	31.3	17.9
Ψ_{JB}	Junction-to-board characterization parameter	81.6	107.9
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC [(1)]		OPA4310-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.5	128.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.8	58.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	71.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.9	13.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.6	70.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.5V to 5.5V (±0.75V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.25	±1.3	mV
		V_{CM} = V–	T_A = –40°C to 125°C			±1.4	mV
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±0.5		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 1.5V to 5.5V , V_{CM} = V–			±10	±50	µV/V
	Channel separation	f = 10kHz			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_S = 1.8V and V_S = 5V			±1	±30	pA
I_{OS}	Input offset current (1)	V_S = 1.8V and V_S = 5V			±0.5	±25	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10Hz			4		$µV_{PP}$
e_N	Input voltage noise density	f = 100Hz			32		nV/√Hz
		f = 1kHz			16		nV/√Hz
		f = 10kHz			13		nV/√Hz
i_N	Input current noise (3)	f = 1kHz			10		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range (1)	V_S = 1.8V	T_A = –40°C to 125°C	(V–)		(V+)	V
	Common-mode voltage range (1)	V_S = 5.5V	T_A = –40°C to 125°C	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8V, (V–) ≤ V_{CM} ≤ (V+) – 0.6V		75	85		dB
		V_S = 1.8V, (V–) ≤ V_{CM} ≤ (V+) – 0.6V	T_A = –40°C to 125°C	65	78		dB
		V_S = 5.5V, (V–) ≤ V_{CM} ≤ (V+) – 0.6V		83	95		dB
		V_S = 5.5V, (V–) ≤ V_{CM} ≤ (V+) – 0.6V	T_A = –40°C to 125°C	75	85		dB
		Full Range: V_S = 1.8V, (V–) ≤ V_{CM} ≤ (V+)	T_A = –40°C to 125°C	57.5	70		dB
		Full Range: V_S = 5.5V (V–) – 0.1V ≤ V_{CM} ≤ (V+) + 0.1V	T_A = –40°C to 125°C	66.5	80		dB
INPUT IMPEDANCE							
Z_{ID}	Differential Input Impedance				80 || 1.4		GΩ ||pF
Z_{ICM}	Common-mode Input Impedance				100 || 0.5		GΩ ||pF

5.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.5V to 5.5V (±0.75V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.8V, (V–) + 0.05V < V_O < (V+) – 0.05V, R_L = 10kΩ to V_S / 2		102	115		dB
	Open-loop voltage gain[2]	V_S = 1.8V, (V–) + 0.10V < V_O < (V+) – 0.10V, R_L = 2kΩ to V_S / 2		95	105		dB
		V_S = 5.5V, (V–) + 0.10V < V_O < (V+) – 0.10V, R_L = 10kΩ to V_S / 2		109	125		dB
	Open-loop voltage gain	V_S = 5.5V, (V–) + 0.15V < V_O < (V+) – 0.15V, R_L = 2kΩ to V_S / 2		105	115		dB
		V_S = 1.8V, (V–) + 0.05V < V_O < (V+) – 0.05V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C	90	100		dB
		V_S = 1.8V, (V–) + 0.10V < V_O < (V+) – 0.10V, R_L = 2kΩ to V_S / 2			90		
		V_S = 5.5V, (V–) + 0.10V < V_O < (V+) – 0.10V, R_L = 10kΩ to V_S / 2			105		
		V_S = 5.5V, (V–) + 0.15V < V_O < (V+) – 0.15V, R_L = 2kΩ to V_S / 2		90	100		
	Open-loop voltage gain [6]	V_S = 3.3V, (V–) + 0.25V < V_O < (V+) – 0.25V, I_L = ±50mA	T_A = 25°C	80	102		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 1.8V, G = +1, R_L = 10kΩ, C_L = 100 pF			2.5		MHz
		V_S = 5.5V, G = +1, R_L = 10kΩ, C_L = 100 pF			3		MHz
SR	Slew rate	V_S = 1.8V, G = +1, R_L = 10kΩ			2.8		V/µs
		V_S = 5.5V, G = +1, R_L = 10kΩ			3		V/µs
THD+N	Total harmonic distortion + noise [4]	V_S = 5.5V, G = +1, V_O = 1V_{RMS}, f = 1kHz, R_L = 10kΩ to V_S / 2			0.0005		%
		V_S = 5.5V, G = +1, V_O = 1V_{RMS}, f = 1kHz, R_L = 2kΩ to V_S / 2			0.0035		%
		V_S = 5.5V, G = +1, V_O = 1V_{RMS}, f = 1kHz, R_L = 600 Ω to V_S / 2			0.0080		%
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 4V, G = +1, C_L = 10 pF			1.8		µs
		To 0.1%, V_S = 5.5V, V_{STEP} = 2V, G = +1, C_L = 10 pF			1.3		
		To 0.01%, V_S = 5.5V, V_{STEP} = 4V, G = +1, C_L = 10 pF			2.3		
		To 0.01%, V_S = 5.5V, V_{STEP} = 2V, G = +1, C_L = 10 pF			1.6		
PM	Phase margin	G = +1, R_L = 10kΩ connected to V_S/2, C_L = 10 pF			60		°
C_L Drive	Cap Load Drive	G = +1, R_L = 10kΩ connected to V_S/2, Phase Margin = 40°			75		pF
		G = +1, R_L = 10kΩ connected to V_S/2, No Sustained Oscillations			250		pF
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S			0.6		µs
EMIRR	Electro-magnetic interference rejection ratio	f = 1.8GHz, V_{IN_EMIRR} = 100mV			75		dB

5.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.5V to 5.5V (±0.75V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 2kΩ to V_S / 2			10	21	mV
		V_S = 1.8V, R_L = 10kΩ to V_S / 2			2	11	mV
		V_S = 1.8V, R_L = 2kΩ to V_S / 2	T_A = –40°C to 125°C			51	mV
		V_S = 1.8V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C			26	mV
		V_S = 5.5V, R_L = 2kΩ to V_S / 2			3.5	20	mV
		V_S = 5.5V, R_L = 10kΩ to V_S / 2			0.75	9	mV
		V_S = 5.5V, R_L = 2kΩ to V_S / 2	T_A = –40°C to 125°C			30	mV
		V_S = 5.5V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C			14	mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 2kΩ to V_S / 2			5.5	15	mV
		V_S = 1.8V, R_L = 10kΩ to V_S / 2			1.2	10	mV
		V_S = 1.8V, R_L = 2kΩ to V_S / 2	T_A = –40°C to 125°C			45	mV
		V_S = 1.8V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C			25	mV
		V_S = 5.5V, R_L = 2kΩ to V_S / 2			3.5	17.5	mV
		V_S = 5.5V, R_L = 10kΩ to V_S / 2			0.75	10	mV
		V_S = 5.5V, R_L = 2kΩ to V_S / 2	T_A = –40°C to 125°C			27.5	mV
		V_S = 5.5V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C			11	mV
I_{SC}	Short-circuit current [(5)]	V_S = 1.8V			±20		mA
	Short-circuit current [(2) (5)]	V_S = 1.8V, T_A = –40℃ to 125℃		±6			mA
	Short-circuit current [(5)]	V_S = 5.5V, OPA2310 -Q1		±75	±150		mA
I_{SC}	Short-circuit current [(5)]	V_S = 5.5V, OPA310-Q1 and OPA4310-Q1		±110			mA
Z_O	Open-loop output impedance	f = 10kHz			1000		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 1.5V, I_O = 0 A, $\overline{SHDN}$ = V+ for shutdown devices			165	190	µA
		V_S = 1.5V, I_O = 0 A, $\overline{SHDN}$ = V+ for shutdown devices	T_A = –40°C to 125°C		165	210	µA
		V_S = 5.5V, I_O = 0 A, $\overline{SHDN}$ = V+ for shutdown devices			165	200	µA
			T_A = –40°C to 125°C			215	µA
	Power-on time	At T_A = 25°C, V_S = 5.5V, V_S ramp rate > 0.3V/µs			125		µs

5.7 Electrical Characteristics (continued)

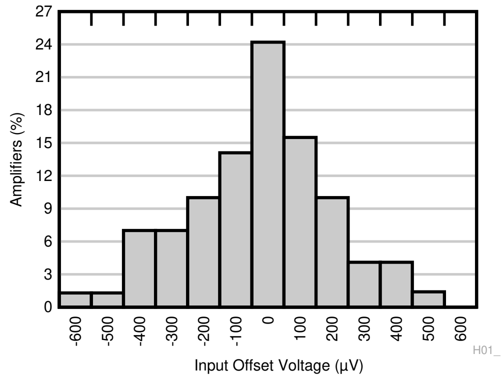
For V_S = (V+) – (V–) = 1.5V to 5.5V (±0.75V to ±2.75V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHUTDOWN						
I_{Q_SHDN}	Shutdown current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–, OPA310S-Q1		0.265	0.475	µA
I_{Q_SHDN}	Shutdown current per amplifier (1)	All amplifiers disabled, $\overline{SHDN}$ = V–, T_A = –40℃ to 85℃, OPA310S-Q1			0.700	µA
Z_{OUT_SHDN}	Output impedance during shutdown	Amplifier disabled		43 || 11.5		GΩ ||pF
V_{SHDN_IH}	Logic high voltage (amplifier enabled)		(V–) + 1.2			V
V_{SHDN_IL}	Logic low voltage (amplifier disabled)				(V–) + 0.2	V
t_{ON}	Amplifier enable time (full shutdown) (7) (1)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–		1	1.6	µs
t_{OFF}	Amplifier disable time (7)	G = +1, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–		1		µs
I_{B_SHDN}	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1V		50		nA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2V		100		

(1) Max data is specified based on characterization results.
(2) Min data is specified based on characterization results.
(3) Typical input current noise data is specified based on design simulation results.
(4) Third-order filter; bandwidth = 80kHz at –3dB.
(5) Short circuit current specified here is the average of sourcing and sinking short circuit currents.
(6) A_{OL} is measured as the difference between (V_{OSA} – V_{OSB}) / (V_{OUTA} – V_{OUTB}). V_{OSA} is the offset measured when the OUT pin is biased at (V+) - 0.25V while the device sources 50mA and VOSB is the offset measured when the OUT pin is biased at (V–) + 0.25V while the device sinks 50mA.
(7) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

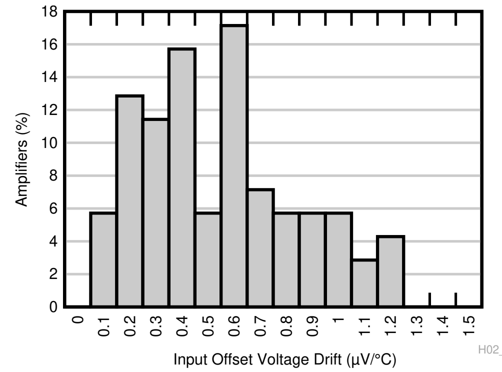
5.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



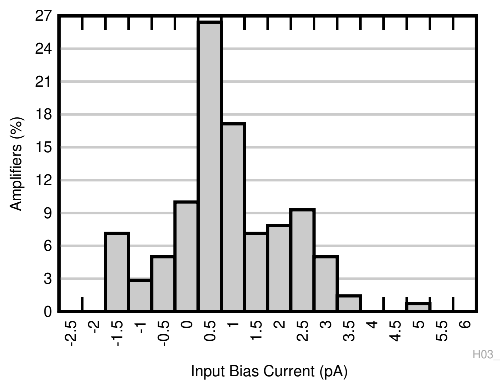
V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 70 Mean = –36µV Sigma = 215µV

Figure 5-1. Offset Voltage Distribution Histogram



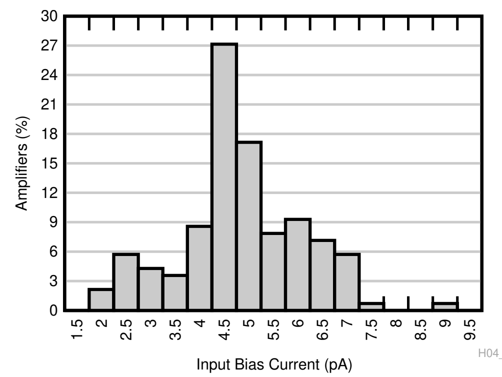
V_S = 5.5V V_{CM} = V_S / 2 T_A = –40°C to +125°C
No. of devices = 70
Mean = 0.5µV/°C Sigma = 0.3µV/°C

Figure 5-2. Offset Voltage Drift Distribution Histogram



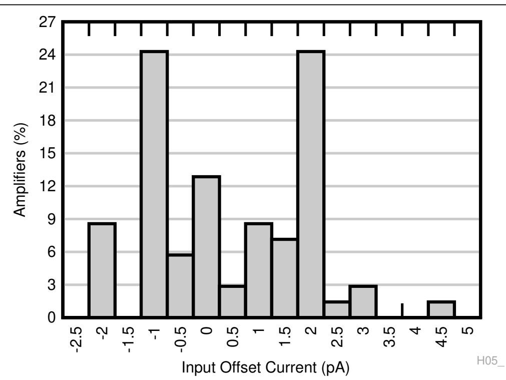
V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 140 Mean = 0.6pA Sigma = 1.2pA

Figure 5-3. Input Bias Current Distribution Histogram



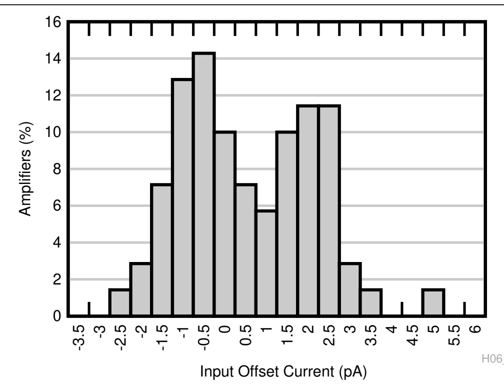
V_S = 5.5V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 140 Mean = 4.6pA Sigma = 1.3pA

Figure 5-4. Input Bias Current Distribution Histogram



V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 140 Mean = 0.2pA Sigma = 1.5pA

Figure 5-5. Input Offset Current Distribution Histogram

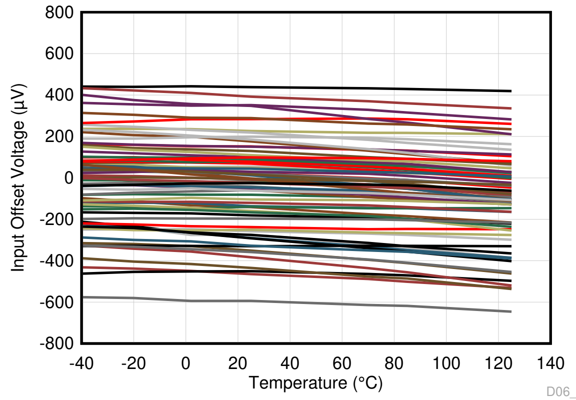


V_S = 5.5V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 70 Mean = 0.3pA Sigma = 1.6pA

Figure 5-6. Input Offset Current Distribution Histogram

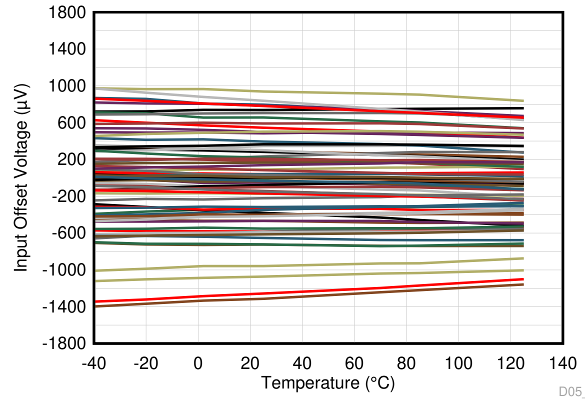
5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



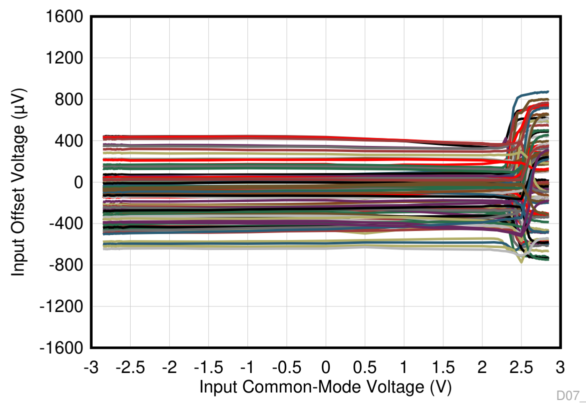
V_S = 5.5V, V_{CM} = V– No. of devices = 72

Figure 5-7. Input Offset Voltage vs Temperature



V_S = 5.5V, V_{CM} = V+ No. of devices = 72

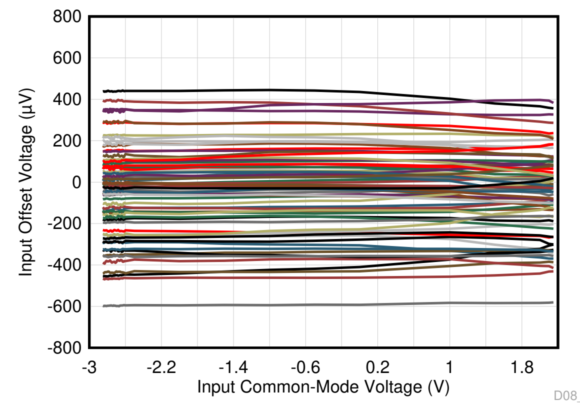
Figure 5-8. Input Offset Voltage vs Temperature



V+ = 2.75V, V– = –2.75V

No. of devices = 72

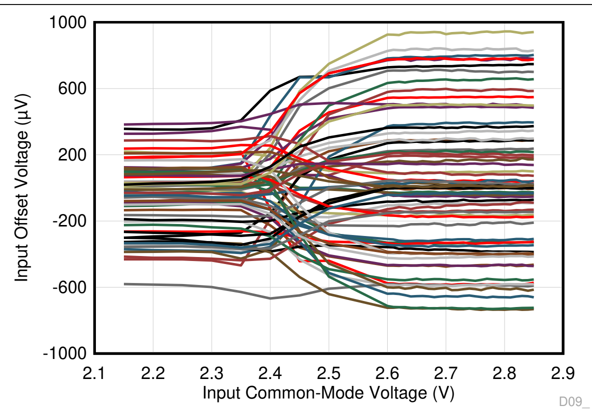
Figure 5-9. Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V, (V–) < V_{CM} < (V+) – 0.6V

No. of devices = 72

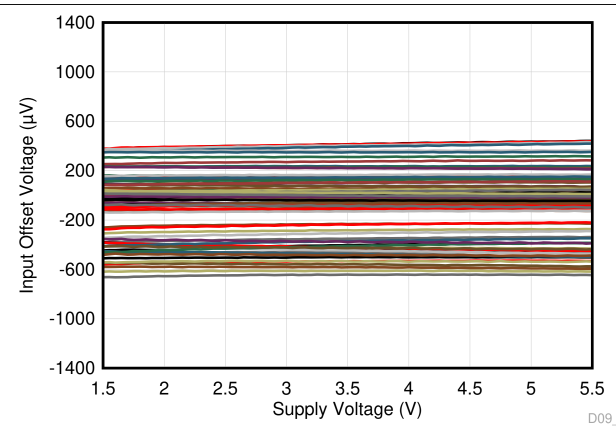
Figure 5-10. Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V, V_{CM} > (V+) – 0.6V

No. of devices = 72

Figure 5-11. Offset Voltage vs Common-Mode

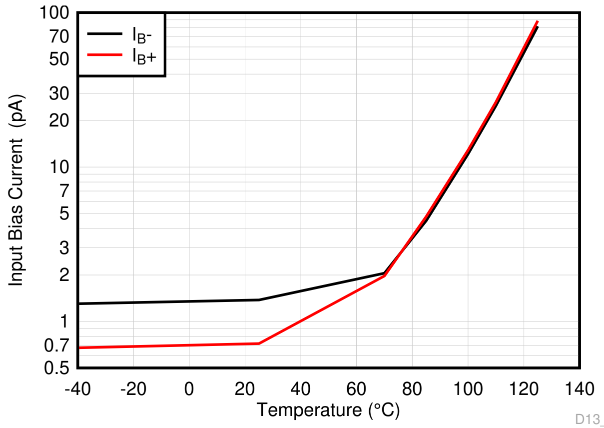


V_{CM} = (V–) No. of devices = 72

Figure 5-12. Offset Voltage vs Supply Voltage

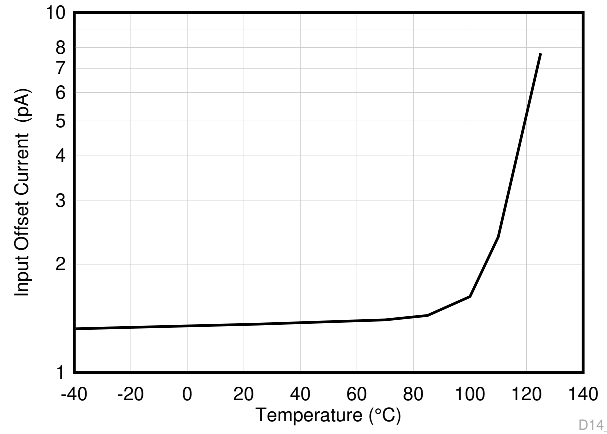
5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



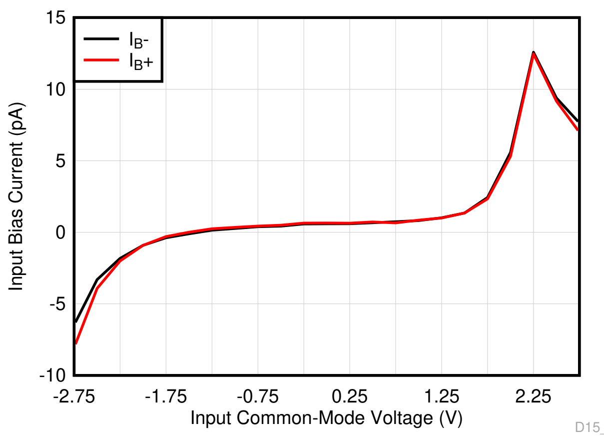
V_S = 5.5V, V_{CM} = V_S/2

Figure 5-13. I_B vs Temperature



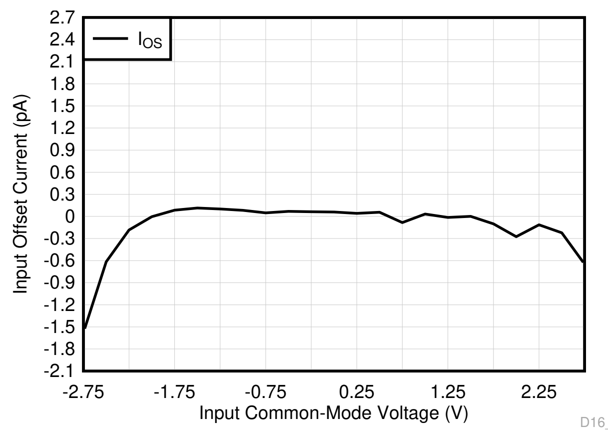
V_S = 5.5V, V_{CM} = V_S/2

Figure 5-14. I_{OS} vs Temperature



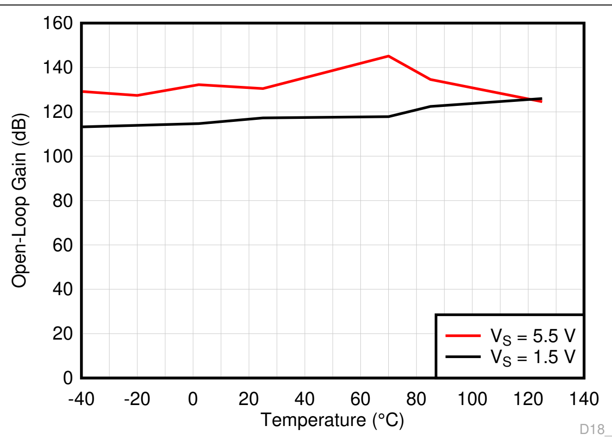
V+ = 2.75V, V– = –2.75V, V_{CM} = V_S/2

Figure 5-15. I_B vs Common-Mode Voltage



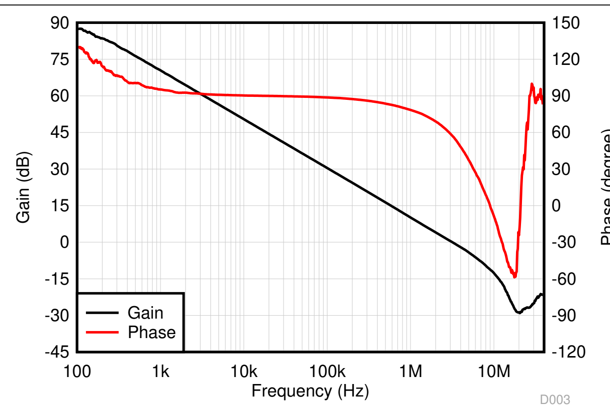
V+ = 2.75V, V– = –2.75V, V_{CM} = V_S/2

Figure 5-16. I_{OS} vs Common-Mode Voltage



R_L = 10kΩ

Figure 5-17. Open-Loop Gain vs Temperature



C_L = 10pF

Figure 5-18. Open-Loop Gain and Phase vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

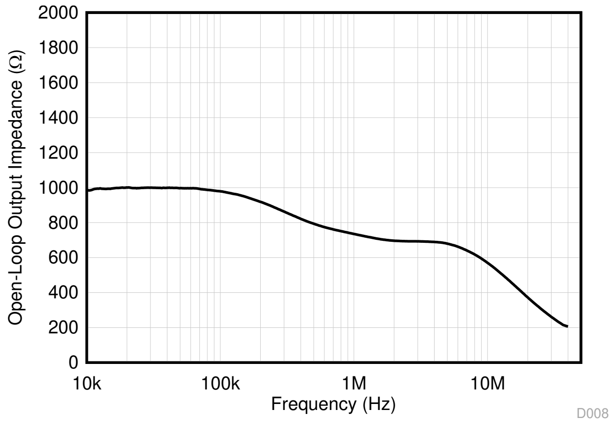
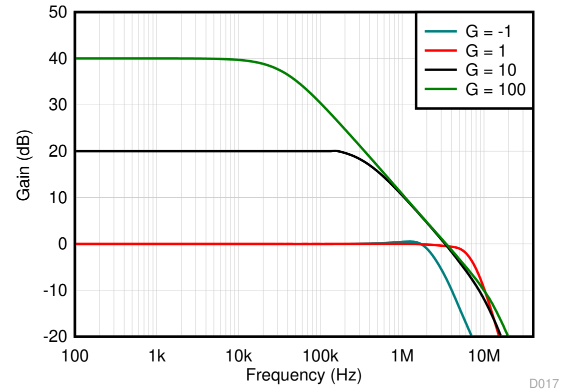
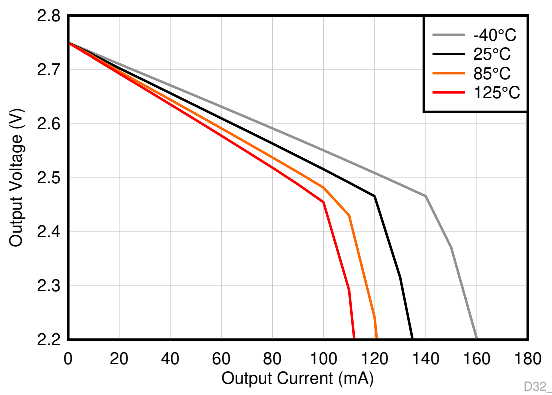


Figure 5-19. Open-Loop Output Impedance vs Frequency



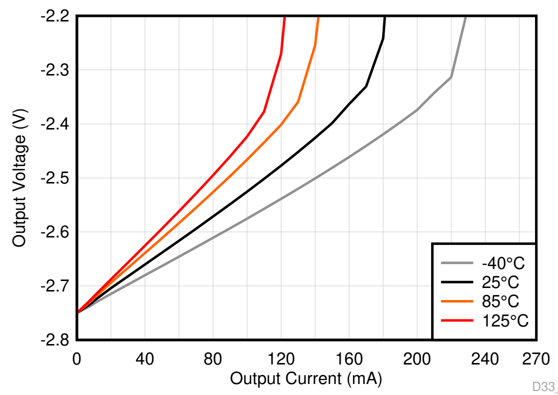
C_L = 10pF

Figure 5-20. Closed-Loop Gain vs Frequency



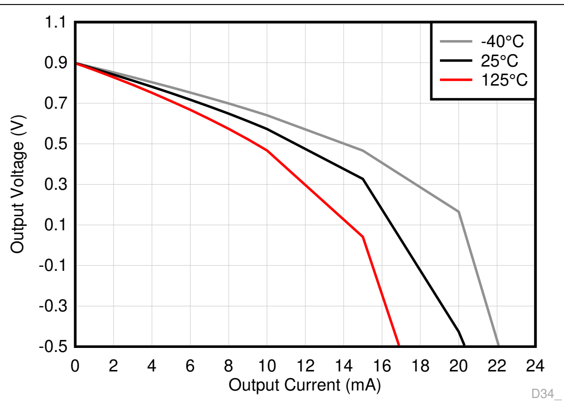
V+ = 2.75V, V– = –2.75 V

Figure 5-21. Output Voltage Swing vs Output Current (Sourcing)



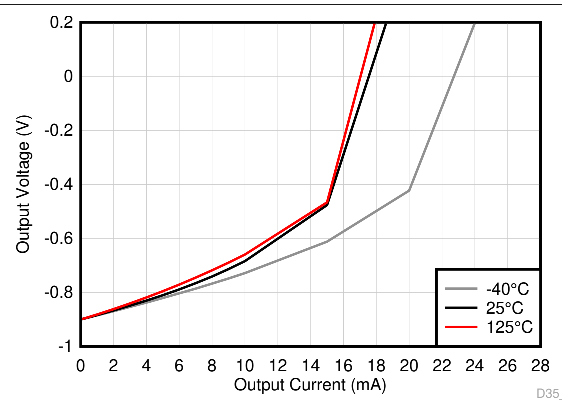
V+ = 2.75V, V– = –2.75V

Figure 5-22. Output Voltage Swing vs Output Current (Sinking)



V+ = 0.9V, V– = –0.9V

Figure 5-23. Output Voltage Swing vs Output Current (Sourcing)



V+ = 0.9V, V– = –0.9V

Figure 5-24. Output Voltage Swing vs Output Current (Sinking)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

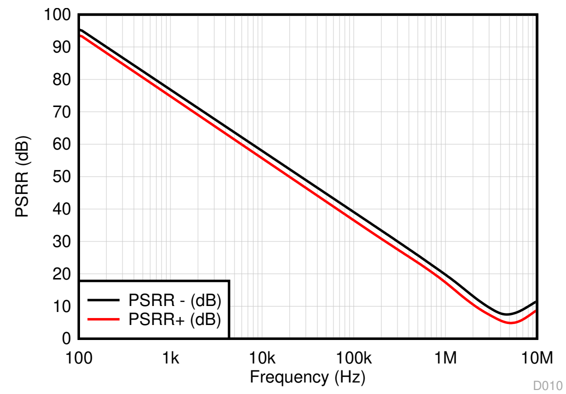
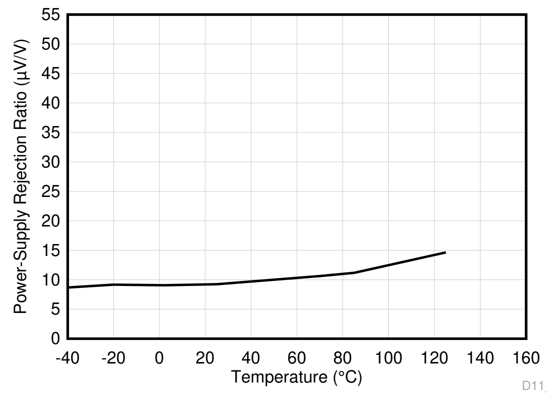


Figure 5-25. PSRR vs Frequency



V_S = 1.5V to 5.5V

Figure 5-26. DC PSRR vs Temperature

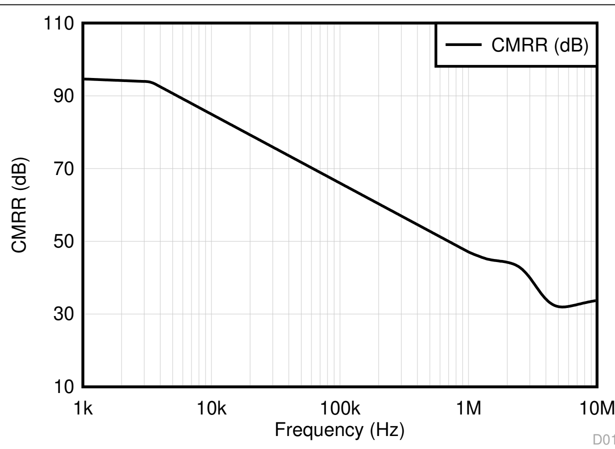
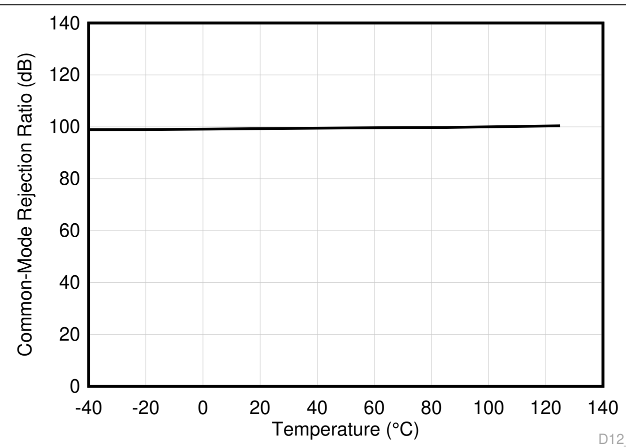


Figure 5-27. CMRR vs Frequency



V_S = 5.5V, (V–) < V_{CM} < (V+) – 0.6V

Figure 5-28. DC CMRR vs Temperature

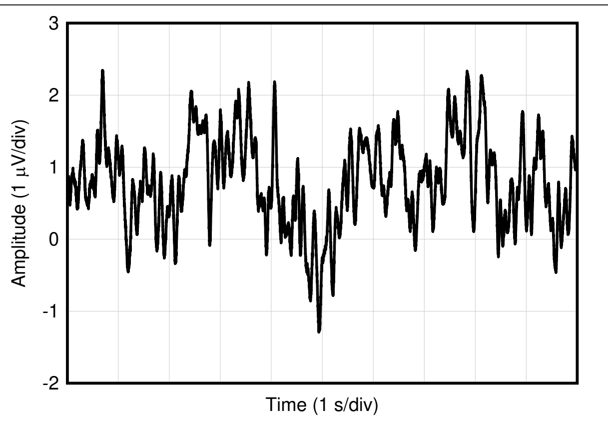


Figure 5-29. 0.1Hz to 10Hz Voltage Noise in Time Domain

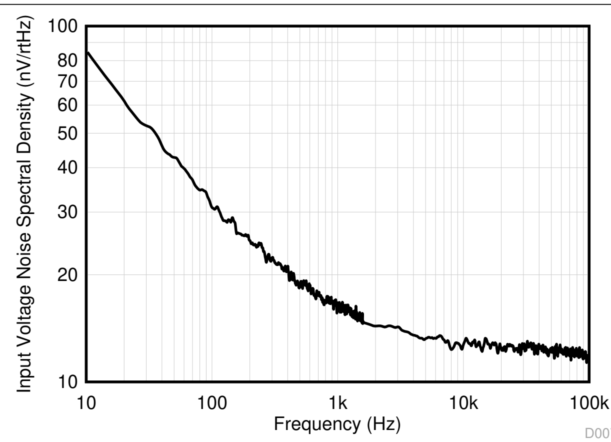
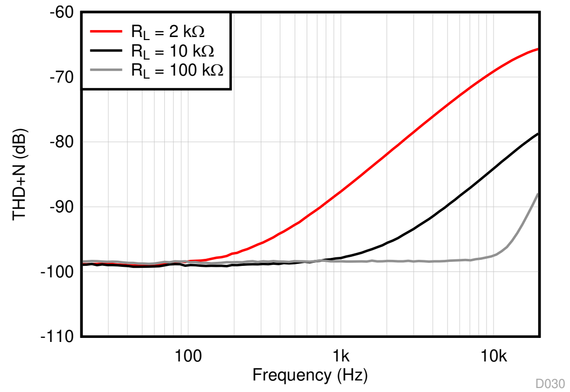


Figure 5-30. Input Voltage Noise Spectral Density

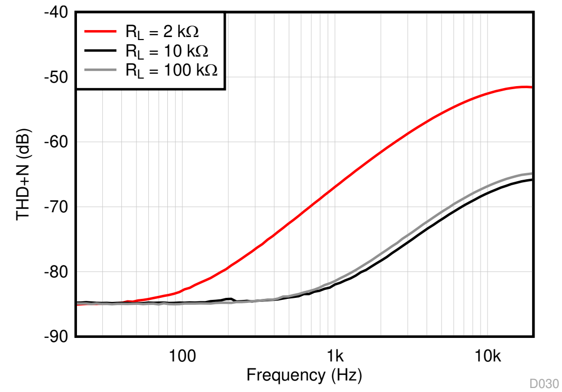
5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



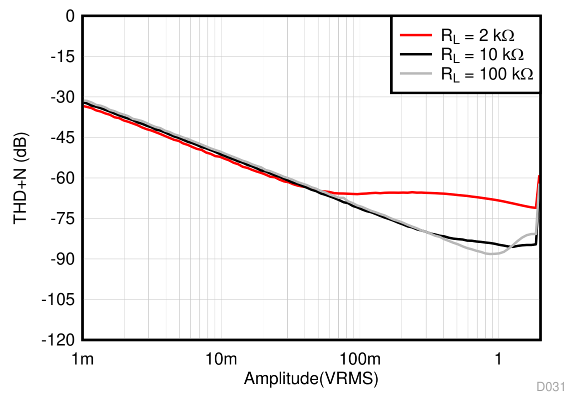
V_S = 5.5V V_{CM} = 2.5V G = 1
BW = 80kHz V_{OUT} = 0.5V_{RMS}

Figure 5-31. THD + N vs Frequency



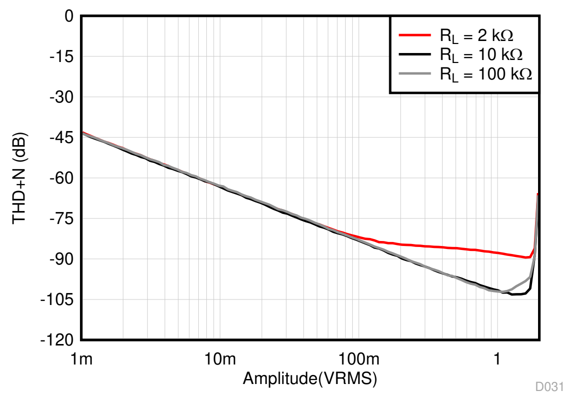
V_S = 5.5V V_{CM} = 2.5V G = –1
BW = 80kHz V_{OUT} = 0.5V_{RMS}

Figure 5-32. THD + N vs Frequency



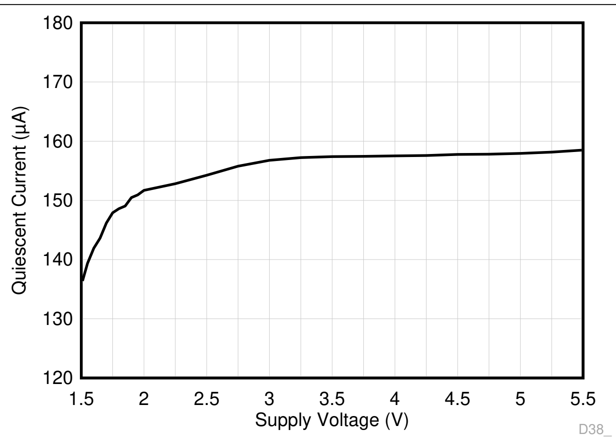
V_S = 5.5V V_{CM} = 2.5V f = 1kHz
G = 1 BW = 80kHz

Figure 5-33. THD + N vs Amplitude



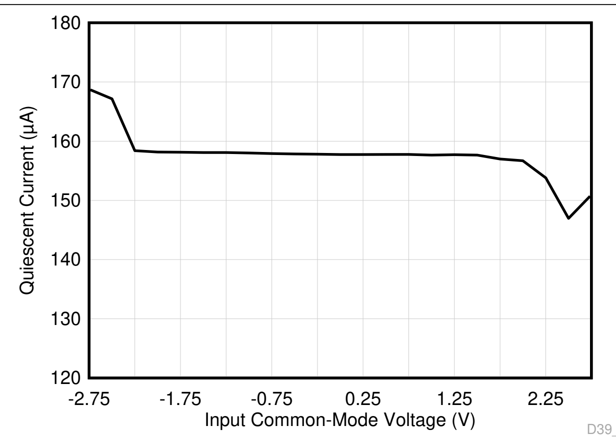
V_S = 5.5V V_{CM} = 2.5V f = 1kHz
G = –1 BW = 80kHz

Figure 5-34. THD + N vs Amplitude



V_{CM} = V_S/2

Figure 5-35. Quiescent Current vs Supply Voltage

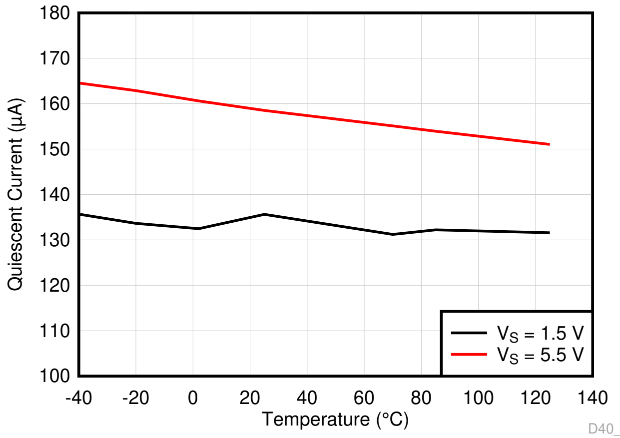


V+ = 2.75V, V– = –2.75V

Figure 5-36. Quiescent Current vs Common-Mode Voltage

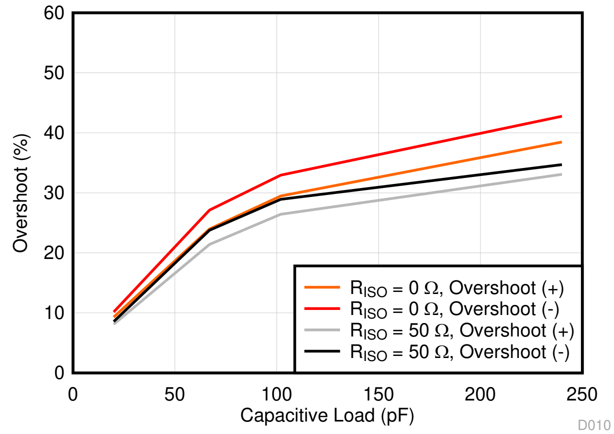
5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



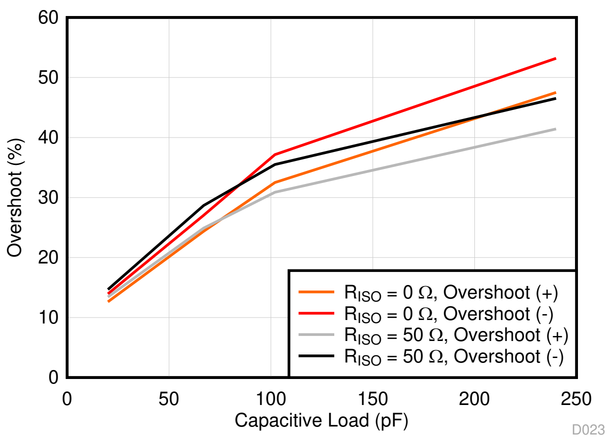
V_{CM} = V_S/2

Figure 5-37. Quiescent Current vs Temperature



G = –1 V_{IN} = 100mVpp

Figure 5-38. Small Signal Overshoot vs Capacitive Load



G = 1 V_{IN} = 100mVpp

Figure 5-39. Small Signal Overshoot vs Capacitive Load

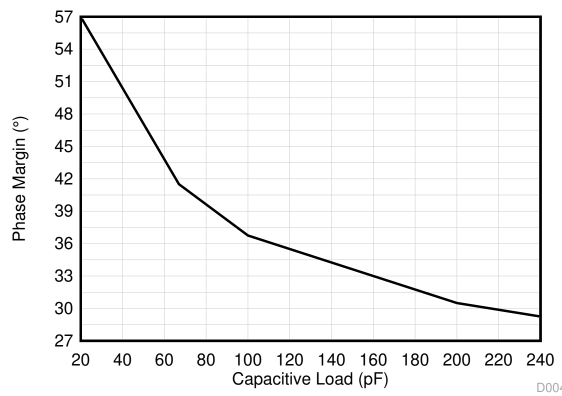
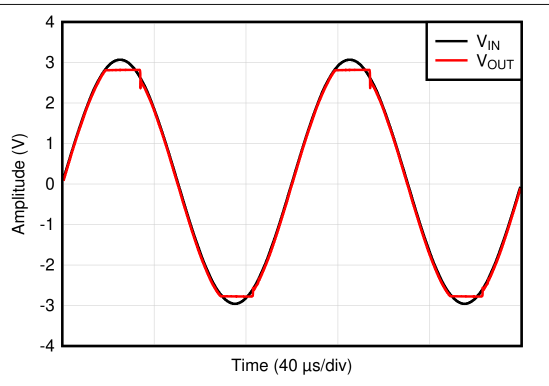
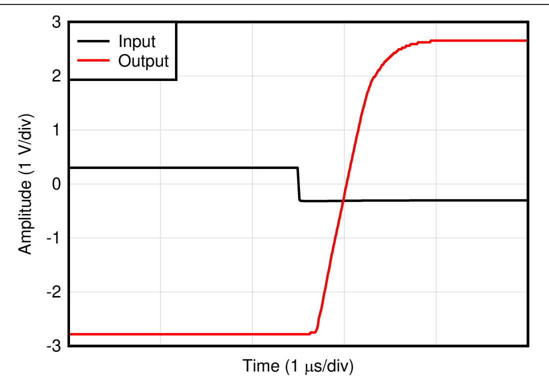


Figure 5-40. Phase Margin vs Capacitive Load



G = 1 V_{IN} = $6V_{PP}$

Figure 5-41. No Phase Reversal

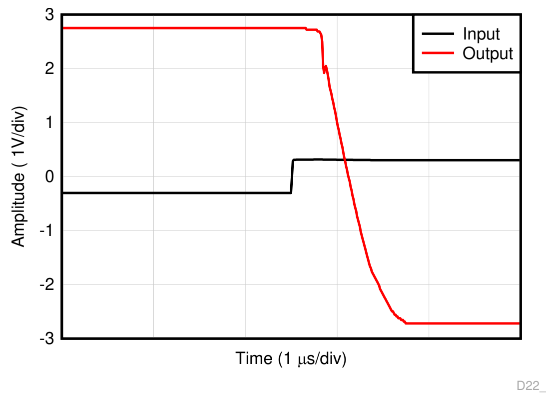


G = –10 V_{IN} = $600mV_{PP}$

Figure 5-42. Overload Recovery

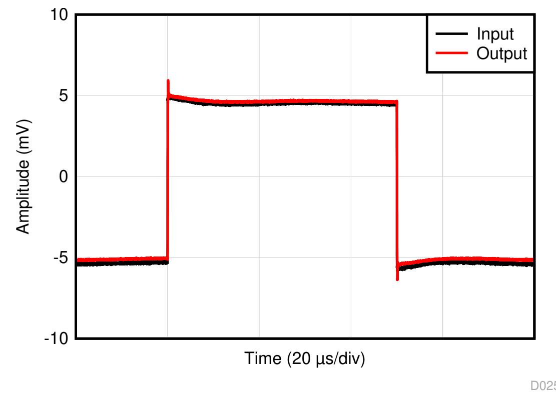
5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



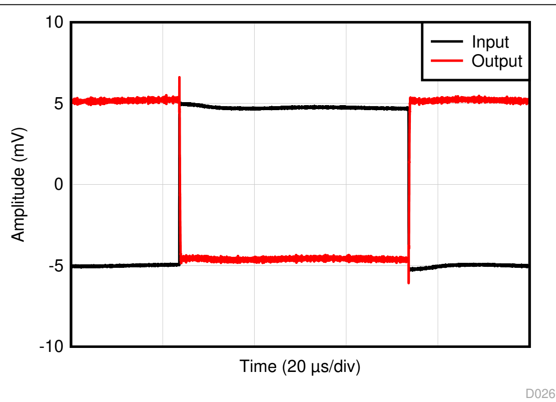
G = –10 V_{IN} = 600mV_{PP}

Figure 5-43. Overload Recovery



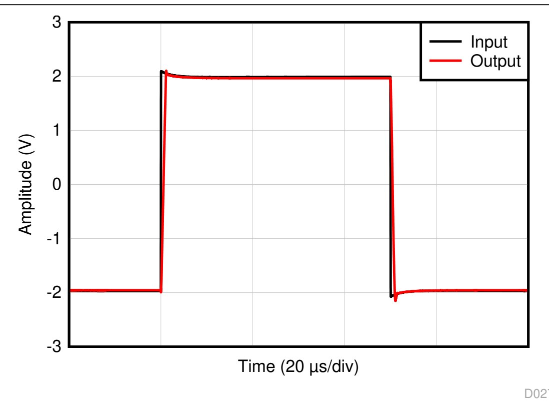
G = 1 V_{IN} = 10mV_{PP} C_L = 10pF

Figure 5-44. Small-Signal Step Response



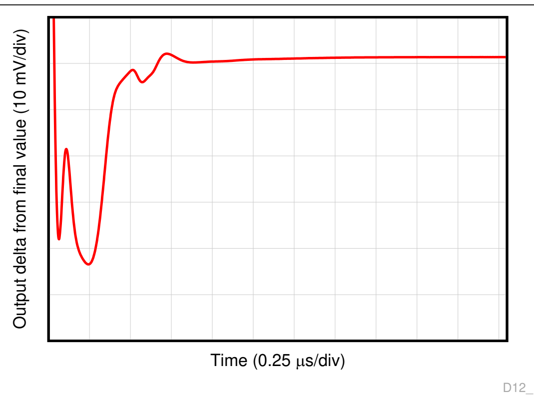
G = –1 V_{IN} = 10mV_{PP} C_L = 10pF

Figure 5-45. Small-Signal Step Response



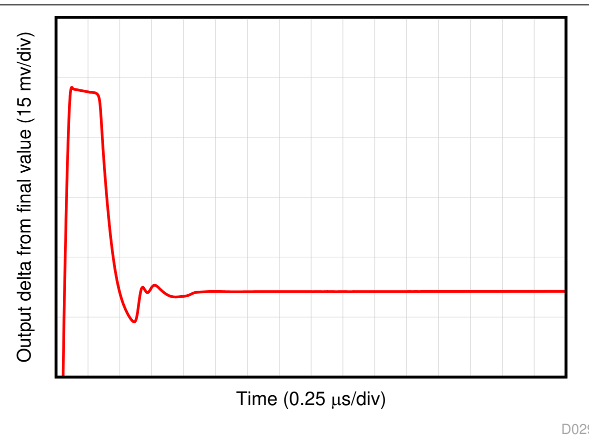
G = 1 V_{IN} = 4V_{PP} C_L = 10pF

Figure 5-46. Large-Signal Step Response



G = 1 V_{IN} = 4V_{PP} C_L = 10pF

Figure 5-47. Large-Signal Settling Time (Negative)

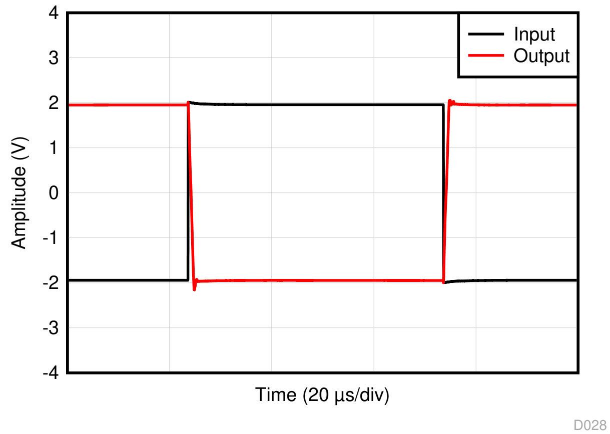


G = 1 V_{IN} = 4V_{PP} C_L = 10pF

Figure 5-48. Large-Signal Settling Time (Positive)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 4V_{PP} C_L = 10pF

Figure 5-49. Large-Signal Step Response

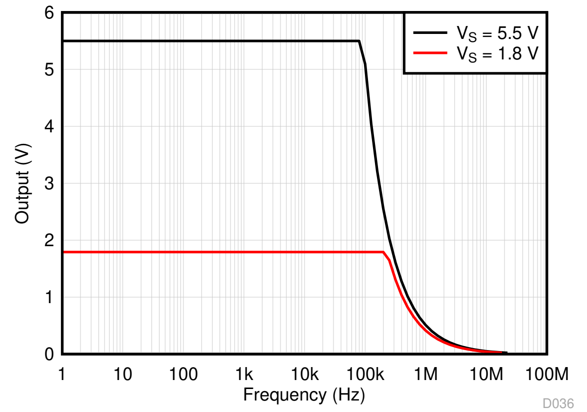
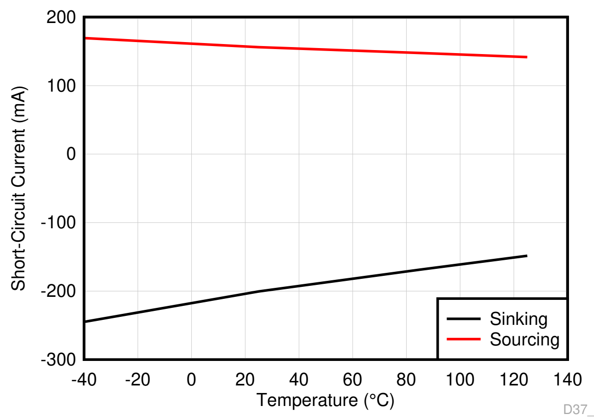


Figure 5-50. Maximum Output Voltage vs Frequency



V_S = 5.5V

Figure 5-51. Short-Circuit Current vs Temperature

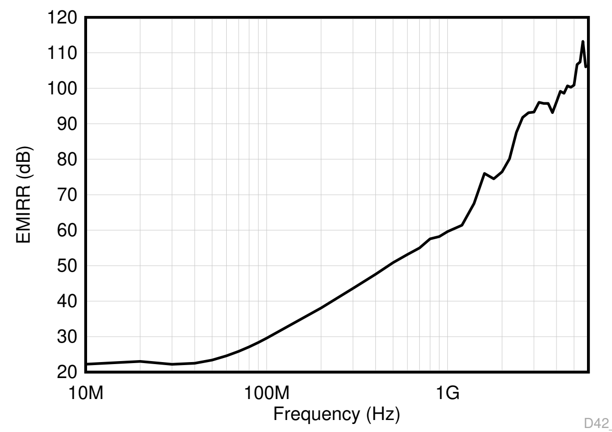


Figure 5-52. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

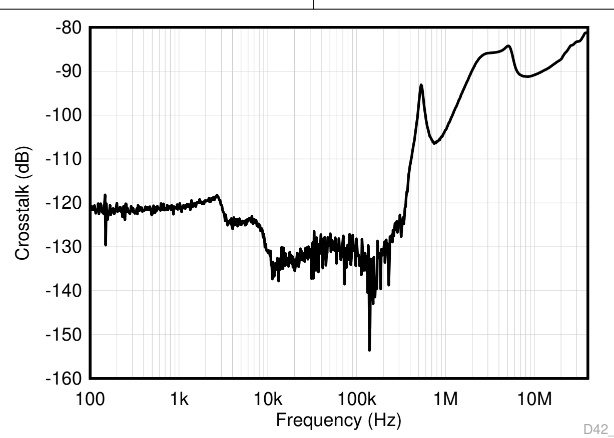


Figure 5-53. Channel Separation

6 Detailed Description

6.1 Overview

The OPAx310-Q1 family of op amps includes single (OPA310-Q1), dual (OPA2310-Q1), and quad-channel (OPA4310-Q1), ultra-low-voltage (1.5V to 5.5V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPAx310-Q1 also features a very fast shutdown response and has an enable time specification of just 0.9µs typical. This feature allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310-Q1 has robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

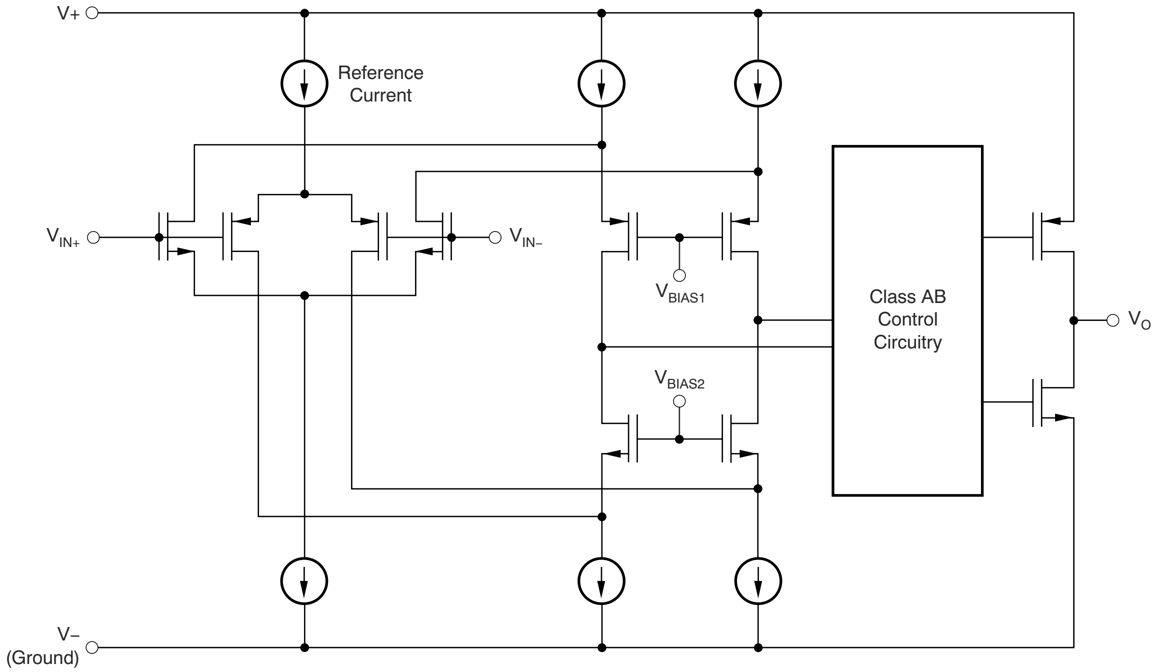
OPAx310-Q1 is offered in standard packages and has an internal current limit, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310-Q1 can swing very close to the rails and has a short circuit current of ±75mA minimum across temperature at 5.5V power supply while consuming just 165µA of quiescent current. This combination of low voltage, low I_Q, and high output current capability makes this device quite unique and an excellent choice for a wide range of general-purpose and high current applications. Additional output current capability can be easily achieved by connecting multiple op amps in parallel. These devices are excellent choice for LED driver and other higher current applications and can also be used as a reference buffer, guard amplifier or as a discrete LDO.

The input common-mode voltage range includes both rails, and allows the OPAx310-Q1 series to be used in many single-supply or dual supply configurations. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices an excellent choice for driving low speed sampling analog-to-digital converters (ADCs). Further, the class AB output stage is capable of driving smaller resistive loads connected to any point between V+ and ground.

The OPAx310-Q1 can drive up to 75pF with a typical phase margin of 40° and features 3MHz gain bandwidth product, 3V/µs slew rate with 4µV_{p-p} integrated noise (0.1Hz to 10Hz) while consuming only 165µA supply current per channel, thus providing a good AC performance at a very low power consumption. DC applications are also well served with a low input bias current (1pA typical), a good input offset voltage (0.25mV typical) and a good PSRR (10µV/V typical), CMRR (80dB typical), and A_{OL} (125dB typical).

The robust design of the OPAx310-Q1 family simplifies circuit design. These op amps feature an integrated radio frequency immunity (RFI) and electro-magnetic interference (EMI) rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The OPAx310-Q1 series of operational amplifiers is fully specified from 1.8V to 5.5V and is tested for amplifier operation from 1.5V to 1.8V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics*. TI highly recommends to bypass power-supply pins with at least 0.01μF ceramic capacitors.

6.3.2 Rail-to-Rail Input

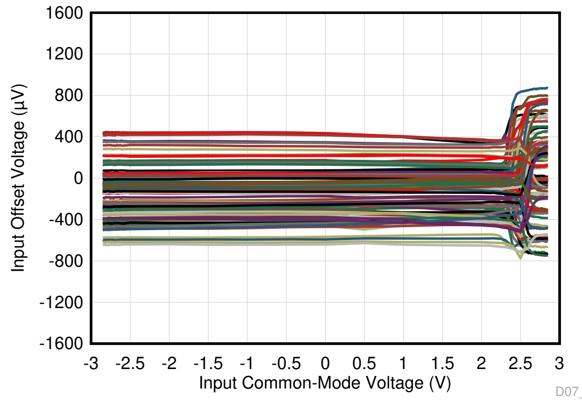
The input common-mode voltage range of the OPAx310-Q1 series extends to either supply rails. This is true even when operating at the ultra-low supply voltage of 1.5V, all the way up to the standard supply voltage of 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to the *Functional Block Diagram* for more details.

For most amplifiers with a complementary input stage, one of the input pairs, usually the P-channel input pair, is designed to deliver slightly better performance in terms of input offset voltage, offset drift over the N-channel pair. Consequently, the P-channel pair is designed to cover the majority of the common mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. Just after the threshold voltage, both the input pairs are in operation for a small range referred to as the transition region. Beyond this region, the N-channel pair completely takes over. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. Hence, most applications generally prefer operating in the P-channel input range where the performance is slightly better.

For the OPAx310-Q1, the P-channel pair is typically active for input voltages from (V–) to (V+) – 0.4V and the N-channel pair is typically active for input voltages from the positive supply to (V+) – 0.4V. The transition region occurs typically from (V+) – 0.5V to (V+) – 0.3V, in which both pairs are on. These voltage levels mentioned above can vary with process variations associated with threshold voltage of transistors. In the OPAx310-Q1, 200mV transition region mentioned above can vary up to 200mV in either direction. Thus, the transition region (both stages on) can range from (V+) – 0.7V to (V+) – 0.5V on the low end, up to (V+) – 0.3V to (V+) – 0.1V on the high end.

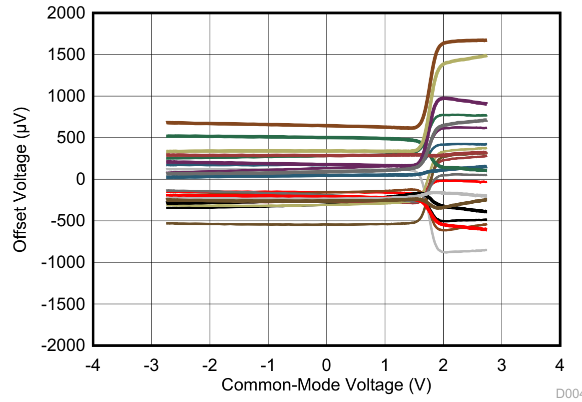
Recollecting the fact that a P-channel input pair usually offers better performance over a N-channel input pair, the OPAx310-Q1 is designed to offer a much wider P-channel input pair range, in comparison to most complimentary input amplifiers in the industry. A side-by-side comparison of the OPAx310-Q1 and the TLV900x is provided below. Note that the TLV900x is designed for P-channel pair operation only until 1.4V from the positive rail, while the OPAx310-Q1 is designed for P-channel pair operation until 0.7V from the positive rail. This additional 700mV of P-channel input pair range for the OPAx310-Q1 is particularly useful when operating at lower supply voltages (1.5V, 1.8V, and so forth) where the P-channel input range usually gets limited to a great extent.

Thus the wide common mode swing of input signal can be accommodated more easily within the P-channel input pair of the OPAx310-Q1, while likely avoiding the transition region, thereby maintaining linearity.



V+ = 2.75V, V– = –2.75V

Figure 6-1. OPAx310-Q1 Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V

Figure 6-2. TLV900x Offset Voltage vs Common-Mode

6.3.3 Rail-to-Rail Output

Designed as a micro-power, high output current operational amplifier, the OPAx310-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. At room temperature and for resistive loads up to 2kΩ, the output swings to within a maximum of 20mV of either supply rail at 5.5V power supply. Different load conditions change the ability of the amplifier to swing close to the rails.

6.3.4 Capacitive Load and Stability

The OPAx310-Q1 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the OPAx310-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the OPAx310-Q1 remains stable with a pure capacitive load up to approximately 75pF with a good phase margin of 40° typical and has no sustained oscillations up to 250pF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10Ω to 20Ω) in series with the output, as shown in Figure 6-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

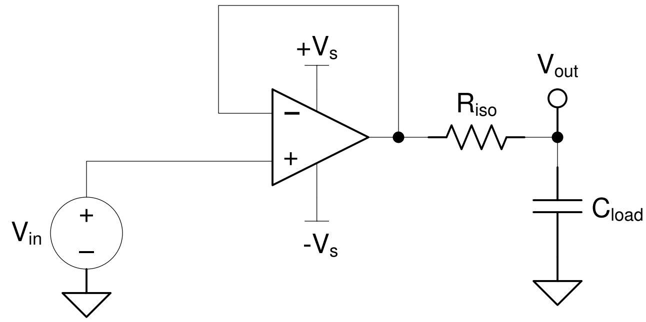


Figure 6-3. Improving Capacitive Load Drive

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time.

The overload recovery time for the OPAx310-Q1 family is approximately 0.75µs typical.

6.3.6 EMI Rejection

The OPAx310-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx310-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-4 shows the results of this testing on the OPAx310-Q1. Table 6-1 shows the EMIRR IN+ values for the OPAx310-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

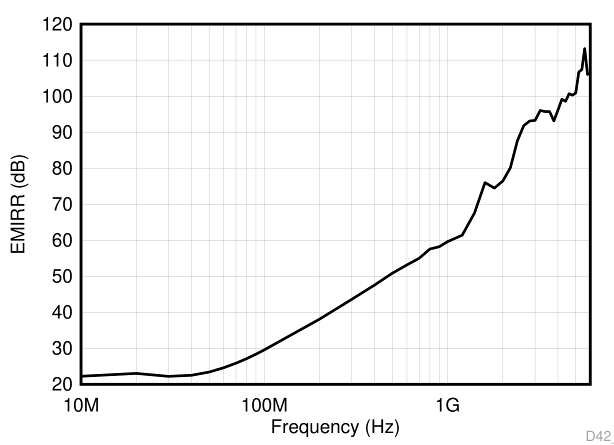


Figure 6-4. EMIRR Testing

Table 6-1. OPAx310-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	58dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	75dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	90dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	102dB

6.3.7 ESD and Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and relevance to an electrical overstress event is helpful. Figure 6-5 shows the ESD circuits contained in the OPAx310-Q1 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the input and output pins meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Note that the OPAx310-Q1 features no current-steering diodes connected between the input and positive power-supply pin.

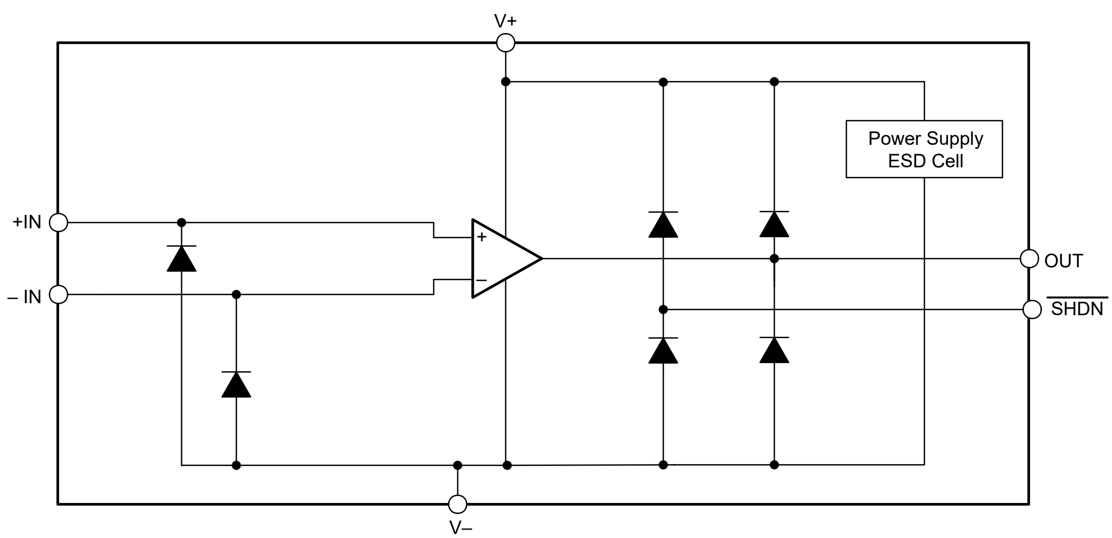


Figure 6-5. Equivalent Internal ESD Circuitry

6.3.8 Input ESD Protection

The OPAx310-Q1 family incorporates internal ESD protection circuits on all pins. For inputs, this protection primarily consists of fail safe ESD input structures which feature no current-steering diodes connected between the input and positive power-supply pin as shown in the Figure 6-5. This feature is very useful during power sequencing scenarios where input signal can be present before the positive power supply rail. A fail safe input ESD structure prevents any short between inputs and positive power supply.

6.3.9 Shutdown Function

The OPAx310-Q1 S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 500nA at room temperature. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to provide for smooth switching characteristics. To make sure of optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and (V–) + 0.2V. A valid logic high is defined as a voltage between (V–) + 1.2V and V+. To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. TI highly recommends that the shutdown pin be connected to a valid high or a low voltage or driven. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5V. Exceeding this voltage level damages the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable and disable time is targeted to be under 1µs for full shutdown of all channels. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx310S-Q1 to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To make sure that shutdown (disable) is within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required.

6.4 Device Functional Modes

The OPAx310-Q1 devices have one functional mode. These devices are powered on as long as the power-supply voltage is between 1.5V (±0.75V) and 5.5V (±2.75V).

The OPAx310-Q1S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See *Shutdown Function* for more information.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx310-Q1 family of rail-to-rail input and output operational amplifiers is specifically designed for high output current applications. The devices operate from 1.5V to 5.5V, are unity-gain stable, and are also an excellent choice for a wide range of general-purpose applications. The class AB output stage is capable of driving small resistive loads connected to any point between V+ and V– as long as the device is not forced into short circuit mode or thermal shutdown mode. The input common-mode voltage range includes both rails and allows the OPAx310-Q1 series to be used in many single-supply or dual supply configurations.

7.2 Typical Application

7.2.1 OPAx310-Q1 Low-Side, Current Sensing Application

Figure 7-1 shows the OPAx310-Q1 configured in a low-side current sensing application.

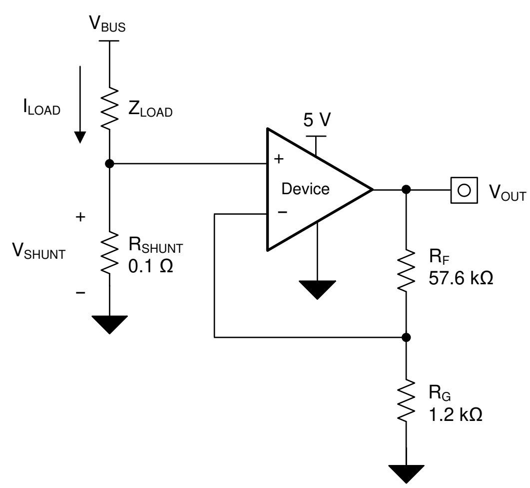


Figure 7-1. OPAx310-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx310-Q1 to produce an output voltage of approximately 0V to 4.9V. The gain needed by the OPAx310-Q1 to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the OPAx310-Q1 to 49V/V.

$$Gain = 1 + \frac{R_F}{R_G} \tag{4}$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49V/V. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; choose an impedance that is best for the system parameters.

7.2.1.3 Application Curve

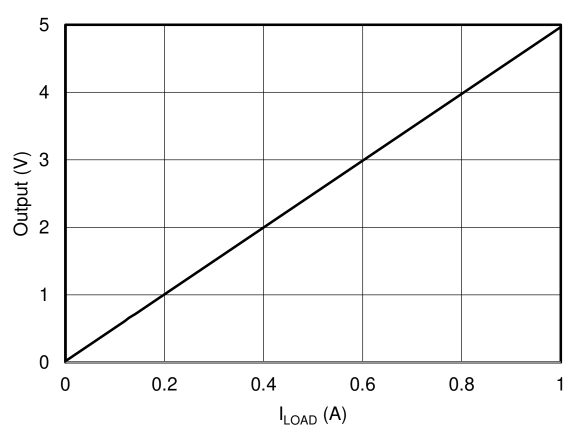


Figure 7-2. Low-Side, Current-Sense Transfer Function

7.3 Power Supply Recommendations

The OPAx310-Q1 family is specified for operation from 1.5V to 5.5V (±0.75V to ±2.75V); many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

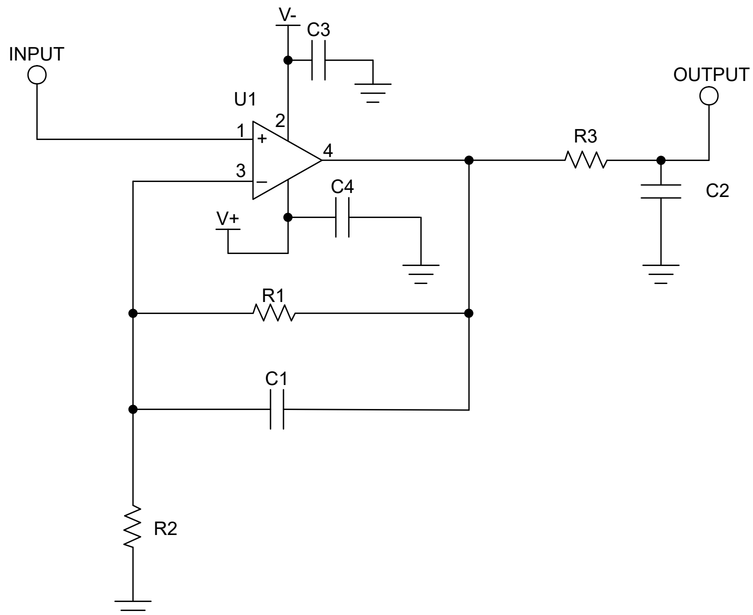


Figure 7-3. Schematic for Noninverting Configuration Layout Example

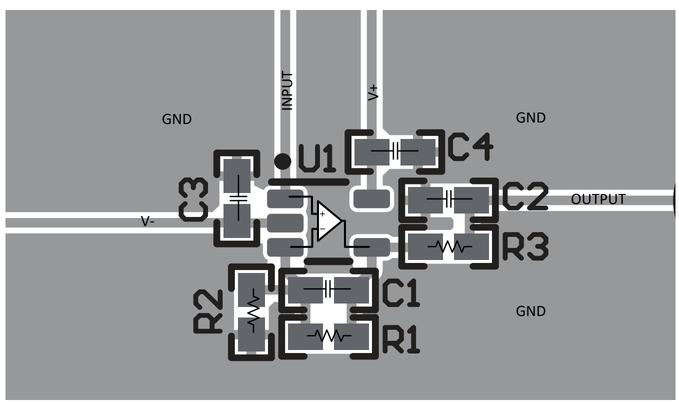


Figure 7-4. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2024) to Revision B (September 2024) **Page**

- Changed the DBV (SOT-23, 5) and DBV (SOT-23, 6) package statuses from: *Advanced Information* to: *Production Data* 1

Changes from Revision * (December 2023) to Revision A (May 2024) **Page**

- Changed the DCK (SC70, 5) and DCK (SC70, 6) package statuses from: *Advanced Information* to: *Production Data* 1
- Changed the data sheet status from: *Advanced Information* to: *Production Mixed* 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA310QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O310Q
OPA310QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O310Q
OPA310QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P1
OPA310QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P1
OPA310SQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O31QS
OPA310SQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O31QS
OPA310SQDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QD
OPA310SQDCKRQ1.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QD
POPA310QDBVRQ1	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
POPA310QDBVRQ1.A	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
POPA310SQDBVRQ1	Active	Preproduction	SOT-23 (DBV) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
POPA310SQDBVRQ1.A	Active	Preproduction	SOT-23 (DBV) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

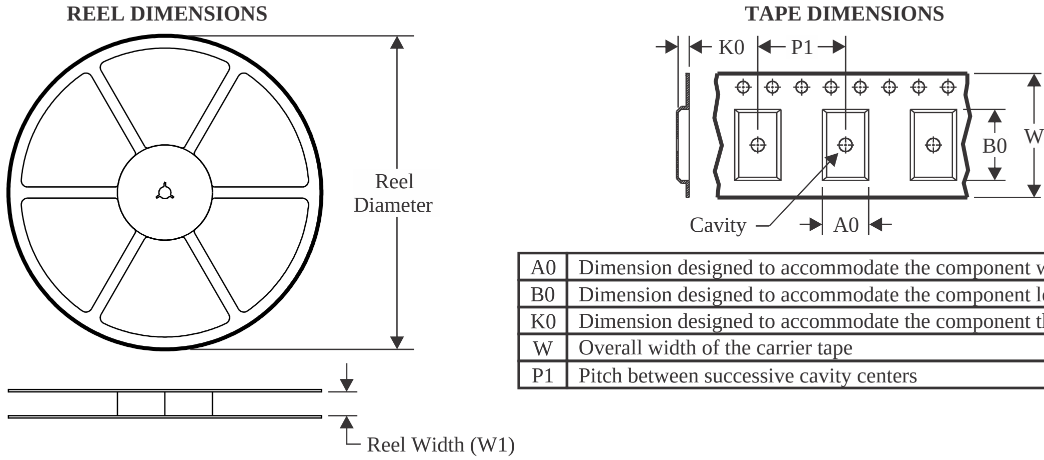
OTHER QUALIFIED VERSIONS OF OPA310-Q1 :

- Catalog : OPA310

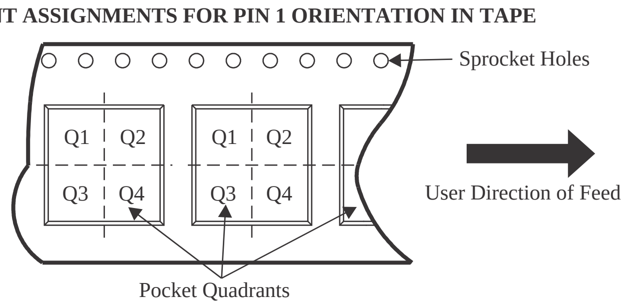
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



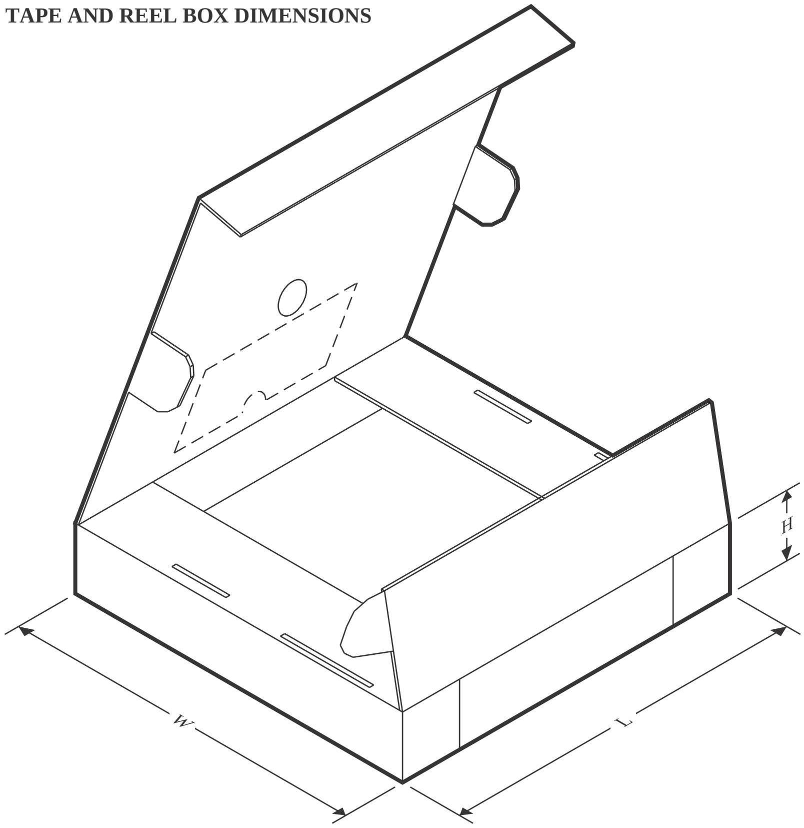
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA310QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA310QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA310SQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA310SQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA310QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA310QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
OPA310SQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA310SQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0

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