OPAx993 32V, Rail-to-Rail Input and Output, 20MHz, Low-Power Op Amp

1 Features

- Rail-to-rail input and output
- Wide supply voltage: 2.7V to 32V
- Wide bandwidth: 20MHz GBW, unity-gain stable
- High slew rate: 40V/µs
- Low quiescent current: 400µA per amplifier
- Low offset voltage: ±1mV (maximum)
- Low offset voltage drift: ±3µV/°C (maximum)
- Low noise: 13nV/√Hz at 1kHz
- Low 1/f noise: 0.5µV (peak-to-peak)
- Low THD+N: 0.00014% (117dB)
- Industry standard packages:
  - Dual in SOIC-8, VSSOP-8, and SOT-23-THIN-8
  - Quad in SOIC-14, TSSOP-14, and SOT-23-THIN-14

2 Applications

- AC charging (pile) station
- GFCI fault detection and test
- Software defined radio
- Display panel for PC and notebooks
- LCD TV
- Wireless control lighting
- Motor drive: power stage and control modules
- Power delivery: UPS, server, and merchant network power
- ADC driver and reference buffer amplifier
- High-side and low-side current sensing

3 Description

The OPA2993 and OPA4993 (OPAx993) are part of a family of high-voltage (32V), rail-to-rail input and output (RRIO) operational amplifiers. These devices offer excellent ac performance, including a wide unity gain bandwidth of 20MHz, and a high slew rate of 40V/µs, while only requiring a quiescent current of 400µA per channel.

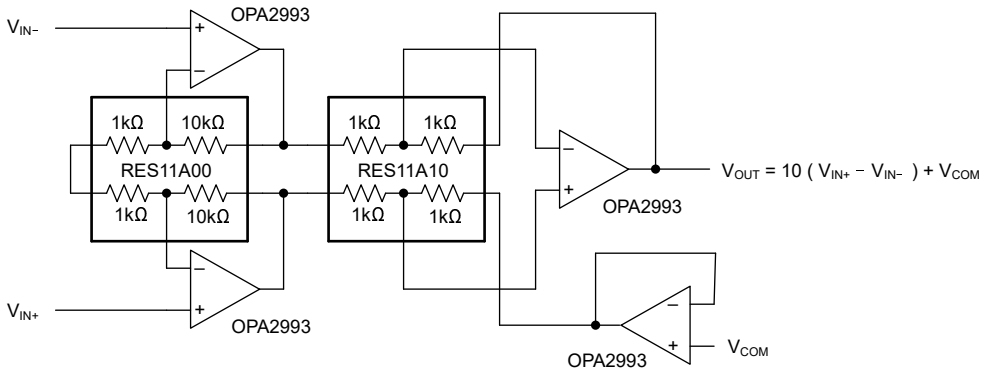
These devices also offer excellent dc precision, low offset voltage (±1mV, maximum), and low offset drift (±3µV/°C, maximum) for high-voltage operation within the main input pair. These features make the OPAx993 a flexible, robust, and high-performance op amp for high-voltage industrial applications.

The OPAx993 family of op amps is available in small-size packages (such as SOT-23-8 and SOT-23-14), as well as standard packages (such as SOIC, and TSSOP), and is specified from –40°C to +125°C.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE	PACKAGE SIZE (3)
OPA2993	Dual	D (SOIC, 8)	4.9mm × 6mm
		DGK (VSSOP, 8)(2)	3mm × 4.9mm
		DDF (SOT-23, 8)(2)	2.9mm × 2.8mm
OPA4993	Quad	D (SOIC, 14)(2)	8.65mm × 6mm
		DYY (SOT-23, 14)(2)	4.2mm × 1.9mm
		PW (TSSOP, 14)(2)	5mm × 6.4mm

(1) For more information, see Section 10.
(2) Preview information (not Production Data).
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



OPAx993 Instrumentation Application With the RES11

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4 Pin Configuration and Functions

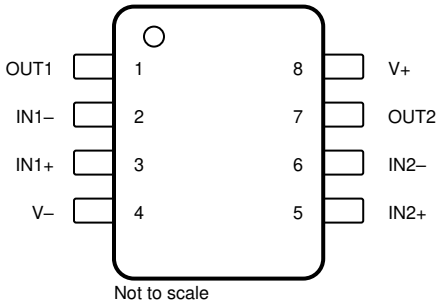


Figure 4-1. OPA2993: D Package, 8-Pin SOIC, DGK (Preview) Package, 8-Pin VSSOP, and DDF (Preview) Package, 8-Pin SOT-23-THN (Top View)

Table 4-1. Pin Functions: OPA2993

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1–	2	Input	Inverting input, channel 1
IN1+	3	Input	Noninverting input, channel 1
IN2–	6	Input	Inverting input, channel 2
IN2+	5	Input	Noninverting input, channel 2
OUT1	1	Output	Output, channel 1
OUT2	7	Output	Output, channel 2
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

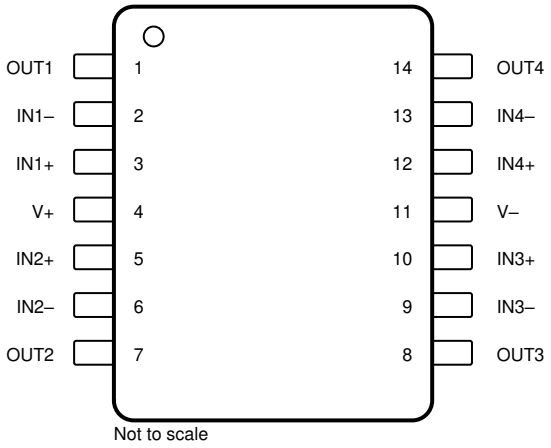


Figure 4-2. OPA4993: D (Preview) Package, 14-Pin SOIC, and PW (Preview) Package, 14-Pin TSSOP (Top View)

Table 4-2. Pin Functions: OPA4993

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1–	2	Input	Inverting input, channel 1
IN1+	3	Input	Noninverting input, channel 1
IN2–	6	Input	Inverting input, channel 2
IN2+	5	Input	Noninverting input, channel 2
IN3–	9	Input	Inverting input, channel 3
IN3+	10	Input	Noninverting input, channel 3
IN4–	13	Input	Inverting input, channel 4
IN4+	12	Input	Noninverting input, channel 4
OUT1	1	Output	Output, channel 1
OUT2	7	Output	Output, channel 2
OUT3	8	Output	Output, channel 3
OUT4	14	Output	Output, channel 4
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	33	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(4)		±15	V
	Current(3)		±10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5 V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	32	V
V_I	Common mode voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information OPA2993

THERMAL METRIC[1]		OPA2993	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.10	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.91	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.54	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 32V (±0.9V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5V to 32V			±0.25	±1	mV
			T_A = –40°C to 125°C			±2	
		V_{CM} = (V–)			±0.2	±0.7	
			T_A = –40°C to 125°C			±0.8	
		V_{CM} = (V+) – 1.35V			±1.2	±1.8	
			T_A = –40°C to 125°C			±4	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C	V_{CM} = (V–)		±0.7	±3[1]	µV/°C
					±0.5	±3[1]	
			V_{CM} = (V+) – 1.35V		±0.5	±3.5[1]	
PSRR	Input offset voltage versus power supply	V_{CM} = (V–), T_A = –40°C to 125°C	V_S = 5V to 32V		±5	±25	µV/V
				92	106		dB
			V_S = 2.7V to 32V			±50[1]	µV/V
				86[1]			dB
INPUT BIAS CURRENT							
I_B	Input bias current				±150	±250	nA
		T_A = –40°C to 85°C				±320	
		T_A = –40°C to 125°C				±403	
I_{OS}	Input offset current				±0.2	±10	
		T_A = –40°C to 125°C				±15	
INPUT VOLTAGE							
V_{CM}	Common-mode input voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 32V, (V–) < V_{CM} < (V+) – 2V		100	130		dB
			T_A = –40°C to 125°C	100	125		
		V_S = 32V, (V–) < V_{CM} < (V+) – 1V[1]		105	120		
			T_A = –40°C to 125°C	100	115		
		V_S = 5V, (V–) < V_{CM} < (V+) – 2V		100	120		
			T_A = –40°C to 125°C	95	105		
		V_S = 5V, (V–) < V_{CM} < (V+) – 1V[1]		90	100		
			T_A = –40°C to 125°C	86	95		
		V_S = 2.7V, (V–) < V_{CM} < (V+) – 2V[1]		90	98		
			T_A = –40°C to 125°C	88	95		
		V_S = 2.7V, (V–) < V_{CM} < (V+) – 1V[1]		77	90		
			T_A = –40°C to 125°C	72	86		
		V_S = 32V, (V–) < V_{CM} < (V+)		83	95		
			T_A = –40°C to 125°C	81	91		
		V_S = 5V, (V–) < V_{CM} < (V+)		68	83		
			T_A = –40°C to 125°C	65	80		
		V_S = 2.7V, (V–) < V_{CM} < (V+)[1]		64	79		
			T_A = –40°C to 125°C	59	75		
		(V+) – 2 V < V_{CM} < (V+) – 1 V					
INPUT IMPEDANCE							
Z_{ID}	Differential				1.1 || 1		MΩ || pF
Z_{ICM}	Common-mode				3.8 || 1.8		GΩ || pF

5.5 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7V to 32V (±0.9V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 32V, (V–) + 1V < V_O < (V+) – 1V		110	136		dB
			T_A = –40°C to 125°C	92			
		V_S = 5V, (V–) + 1V < V_O < (V+) – 1V[1]		100	130		
			T_A = –40°C to 125°C	91	97		
		V_S = 2.7V, (V–) + 1V < V_O < (V+) – 1V[1]		108	126		
			T_A = –40°C to 125°C	85			
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			0.5		μV_{PP}
					0.08		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			13		nV/√Hz
		f = 10kHz			13		
i_N	Input current noise density	f = 1kHz			0.17		pA/√Hz
FREQUENCY RESPONSE							
f_U	Unity-gain bandwidth	R_L = 1MΩ			8		MHz
GBW	Gain-bandwidth product	f = 1kHz to 100kHz			20		MHz
SR	Slew rate	V_S = 32V, V_{STEP} = 10V, R_S < 1kΩ, C_L = 20pF			40		V/µs
t_S	Settling time	To 0.1%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 20pF			0.74		µs
		To 0.01%, V_S = 32V, V_{STEP} = 10V, G = +1, C_L = 20pF			1		
PM	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20pF			60		°
GM	Gain margin	G = +1, R_L = 10 kΩ, C_L = 20pF			12		dB
t_{OR}	Overload recovery time	V_{IN} × gain > V_S			408		ns
THD+N	Total harmonic distortion + noise	V_S = 32V, V_O = 3V_{RMS}, G = 1, f = 1kHz, R_L = 10kΩ			0.00014		%
					117		dB
OUTPUT							
	Voltage output swing from rail	V_S = 32V, Positive and negative rail headroom, R_L = no load			40	140	mV
			T_A = –40°C to 125°C			140	
		V_S = 32V, Positive and negative rail headroom			93	127	
			T_A = –40°C to 125°C			185	
		V_S = 5V, Positive and negative rail headroom, R_L = no load			27	60	
			T_A = –40°C to 125°C			70	
		V_S = 5V, Positive and negative rail headroom			52	71	
			T_A = –40°C to 125°C			90	
		V_S = 5V, Positive and negative rail headroom, R_L = 2kΩ			86	118	
			T_A = –40°C to 125°C			133	
		V_S = 2.7V, Positive and negative rail headroom, R_L = no load			31	94	
			T_A = –40°C to 125°C			112	
		V_S = 2.7V, Positive and negative rail headroom			54	84	
			T_A = –40°C to 125°C			115	
		V_S = 2.7V, Positive and negative rail headroom, R_L = 2kΩ			85	136	
			T_A = –40°C to 125°C			150	

5.5 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7V to 32V (±0.9V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	V_S = 32V			±40	±80	mA
			T_A = –40°C to 125°C			±70	
		V_S = 5V(1)			±30	±60	
			T_A = –40°C to 125°C			±60	
		V_S = 2.7V(1)			±8	±16	
			T_A = –40°C to 125°C			±16	mA
C_{LOAD}	Capacitive load drive						pF
Z_O	Open-loop output impedance	I_O = 0A					Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 32V, I_O = 0A			400	560	µA
			T_A = –40°C to 125°C			560	
		V_S = 5V, I_O = 0A			390	500	
			T_A = –40°C to 125°C			500	
		V_S = 2.7V, I_O = 0A			350	500	
			T_A = –40°C to 125°C			500	

(1) Specified by characterization only.

5.6 Typical Characteristics

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

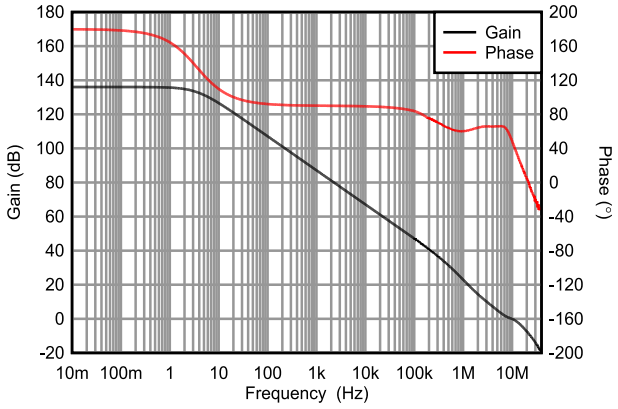


Figure 5-1. Open-Loop Gain and Phase vs Frequency

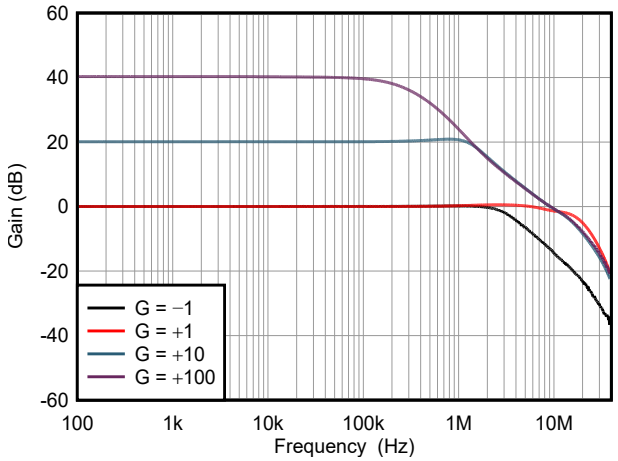


Figure 5-2. Closed-Loop Gain vs Frequency

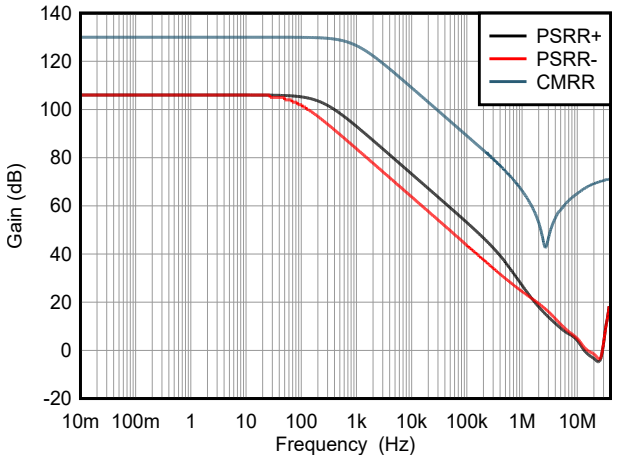


Figure 5-3. CMRR and PSRR vs Frequency

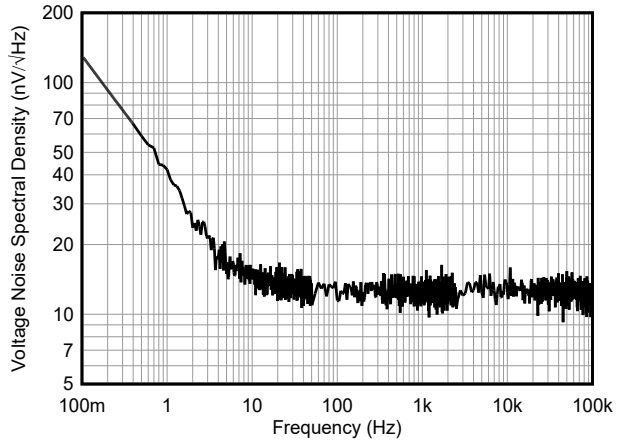


Figure 5-4. Input Voltage Noise Spectral Density vs Frequency

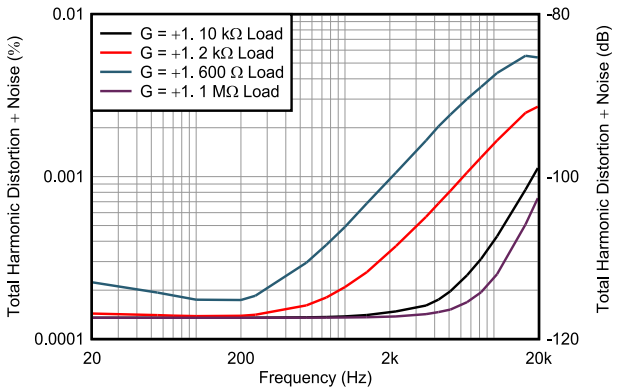


Figure 5-5. THD+N Ratio vs Frequency

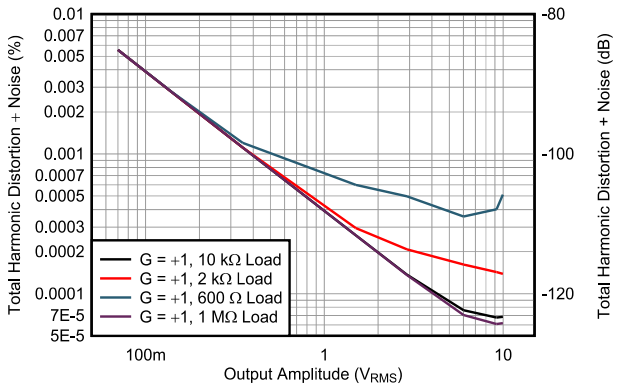


Figure 5-6. THD+N vs Output Amplitude

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

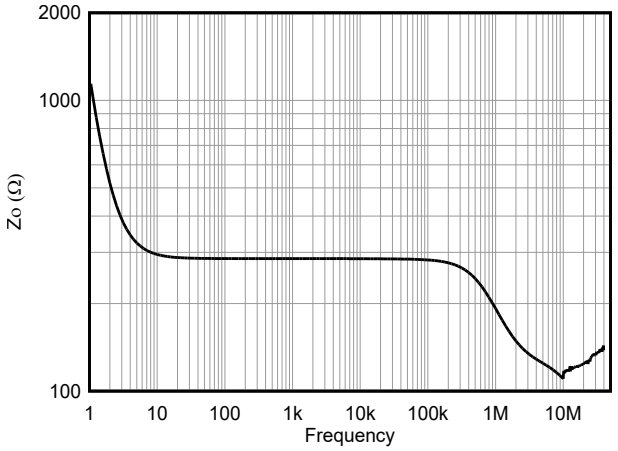


Figure 5-7. Open-Loop Output Impedance vs Frequency

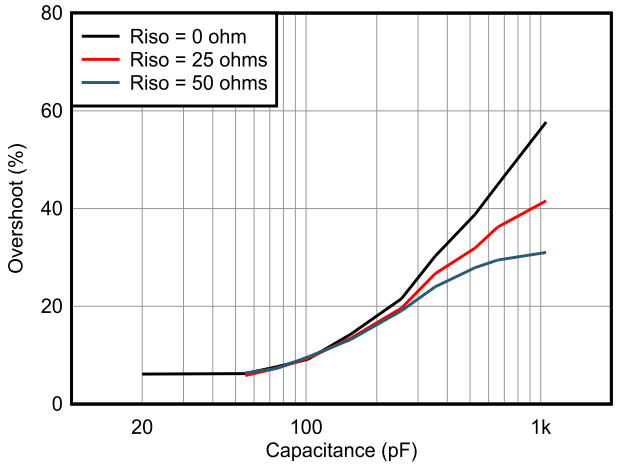


Figure 5-8. Small-Signal Overshoot vs Capacitive Load

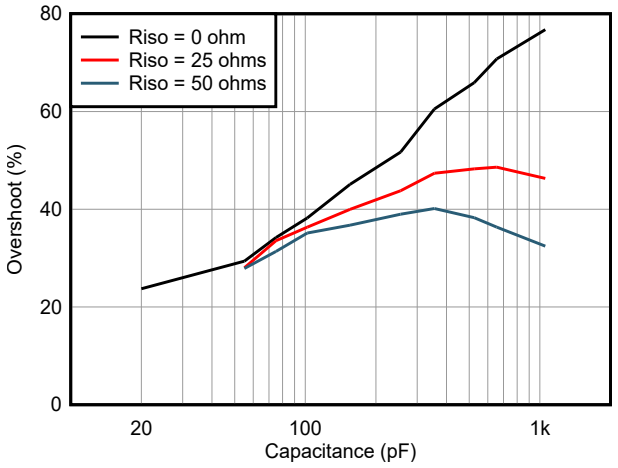


Figure 5-9. Small-Signal Overshoot vs Capacitive Load

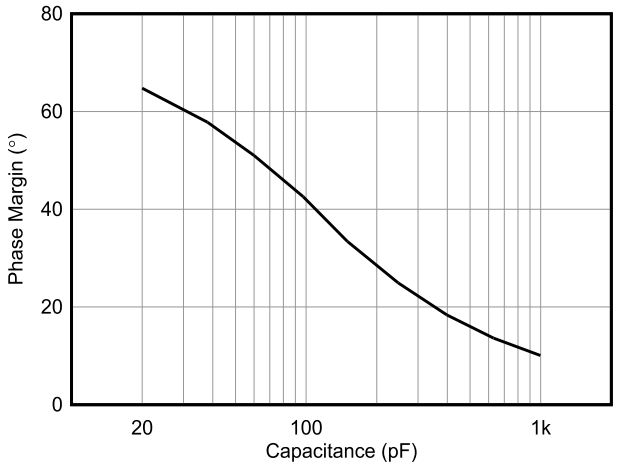


Figure 5-10. Phase Margin vs Capacitive Load

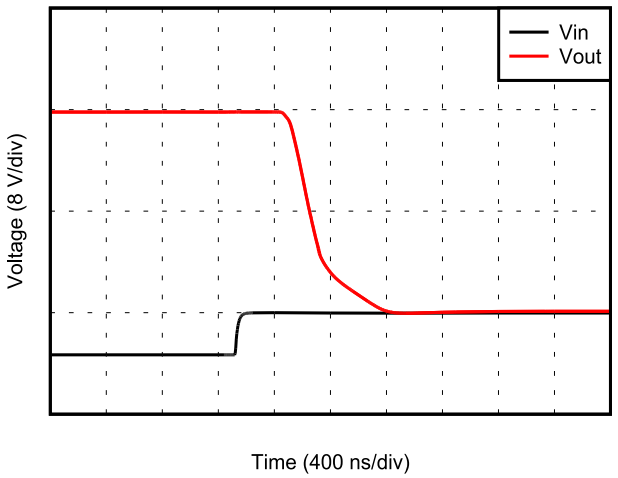


Figure 5-11. Positive Overload Recovery

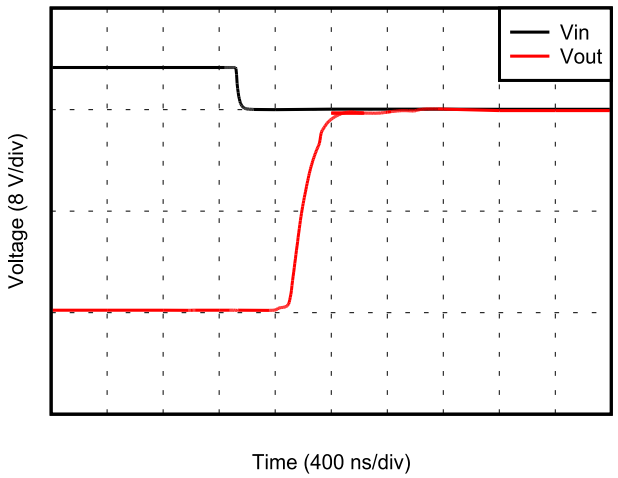


Figure 5-12. Negative Overload Recovery

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±16V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

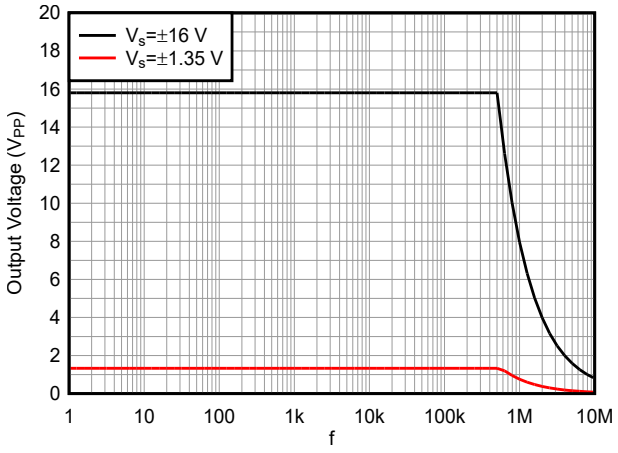


Figure 5-13. Maximum Output Voltage vs Frequency

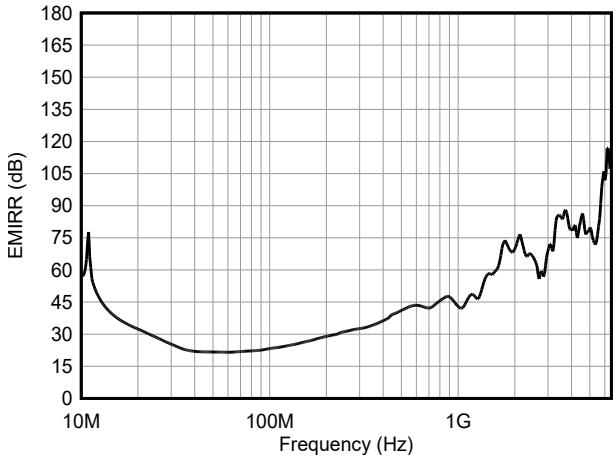


Figure 5-14. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

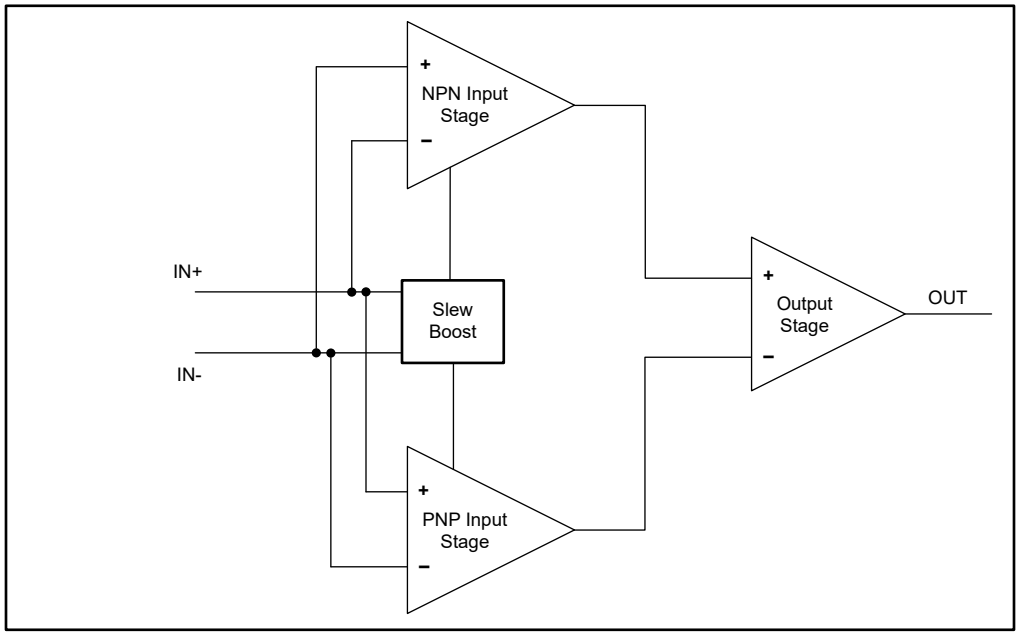
6.1 Overview

The OPAx993 family (OPA2993 and OPA4993) is a family of high voltage (32V) general purpose operational amplifiers.

The OPAx993 family has a wide gain bandwidth of 20MHz and fast slew rate of 40V/µs when no capacitive load is present. These devices require 400uA (typical) at most.

These devices also offer excellent DC precision, including rail-to-rail input/output, low offset (±250µV, typical), and low offset drift (±0.5µV/°C, typical).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Noise Performance

The equation Equation 1 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network; therefore, no additional noise contributions).

$$E_O^2 = e_n^2 + \left(i_n R_S\right)^2 + 4kTR_S \quad (1)$$

The OPAx993 has very low voltage noise, making this device an excellent choice for low source impedances (less than 20kΩ). A similar precision operational amplifier, the OPAx994, has somewhat lower voltage noise but higher current noise. The OPAx993 provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input operational amplifier such as the OPA2156 (very low current noise) can provide improved performance. Use the equation Equation 1 to calculate the total circuit noise, where e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38 × 10^{-23} J/K, and T is temperature in K.

6.3.2 Common-Mode Voltage Range

The OPAx993 is a 32V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary PNP and NPN differential input pairs, as shown in Figure 6-1. The NPN pair is active for input voltages close to the positive rail, typically from (V+) – 1V to the positive supply. The PNP pair is active for inputs from the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region.

For more information on common-mode voltage range and complementary pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

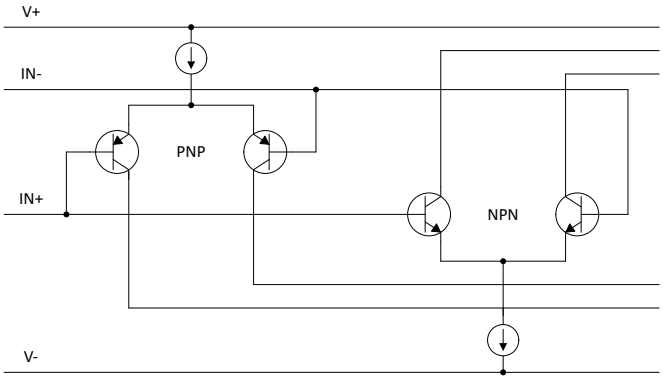


Figure 6-1. Rail-to-Rail Input Stage

6.3.3 Phase Reversal Protection

The OPAx993 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx993 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-2. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

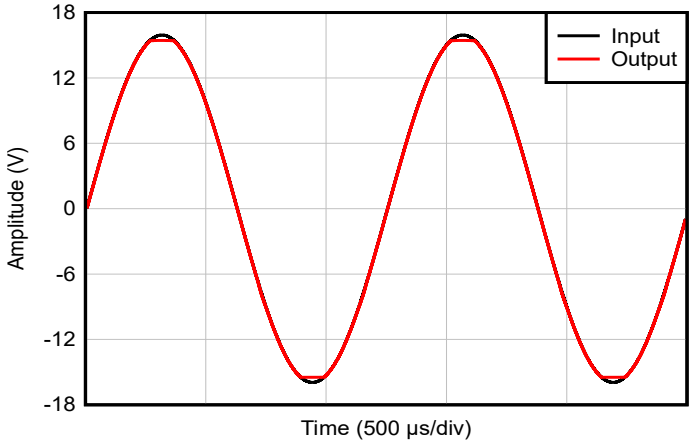


Figure 6-2. No Phase Reversal

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx993 is approximately 408ns.

6.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-3 shows an illustration of the ESD circuits contained in the OPAx993 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

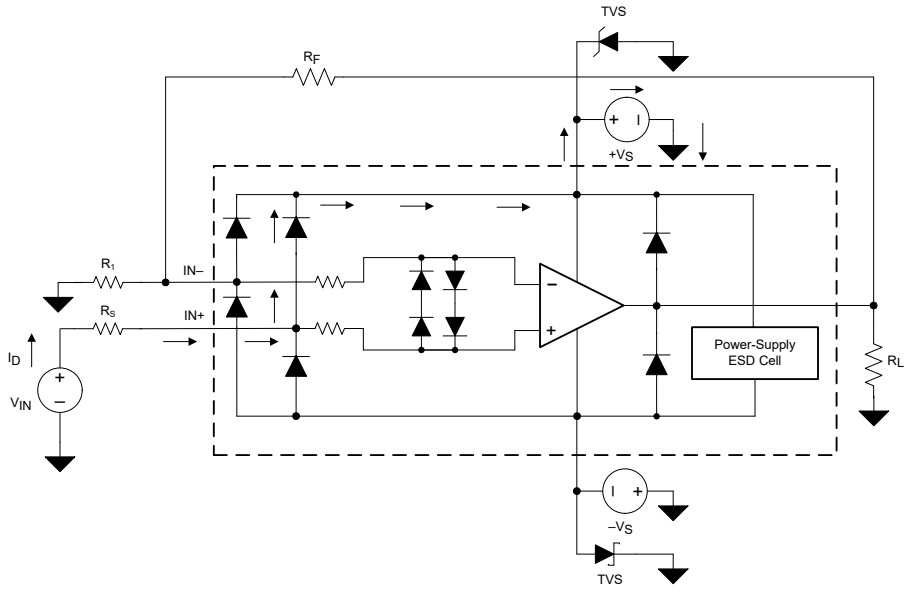


Figure 6-3. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx993 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 6-3), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 6-3 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals; see Figure 6-3. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx993 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 6-3. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx993. Figure 6-3 shows an example configuration that implements a current-limiting feedback resistor.

6.4 Device Functional Modes

The OPAx993 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the OPAx993 is 32V (±16V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx993 family offers excellent DC precision and AC performance. These devices operate up to 32V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 20MHz bandwidth and high slew rate. These features make the OPAx993 a robust, high-performance operational amplifier for high-voltage industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1shows the OPAx993 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

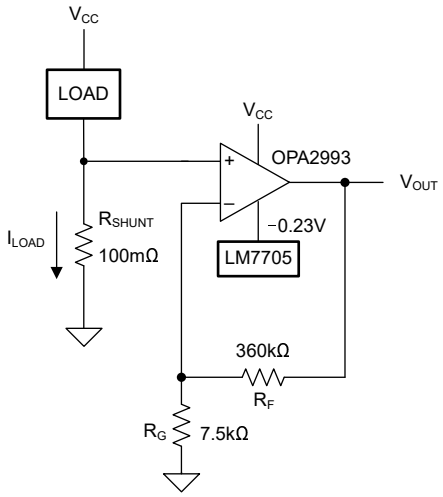


Figure 7-1. OPAx993 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are as follows:

- Load current: 0A to 1A
- Max output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 2:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (2)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 3:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (3)$$

Using Equation 3, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx993 to produce an output voltage of 0V to 4.9V. The gain needed by the OPAx993 to produce the necessary output voltage is calculated using Equation 4:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (4)$$

Using Equation 4, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 5 is used to size the resistors, R_F and R_G, to set the gain of the OPAx993 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (5)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors can generate thermal noise that exceeds the intrinsic noise of the op amp. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curve

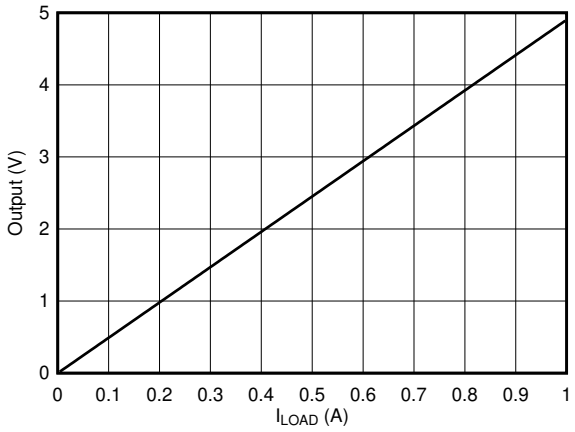


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The OPAx993 is specified for operation from 2.7V to 32V (±1.35V to ±16V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

CAUTION
Supply voltages larger than 33V can permanently damage the device; see *Section 5.1*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

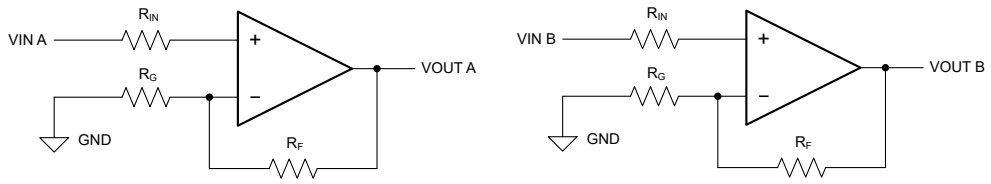


Figure 7-3. Schematic Representation

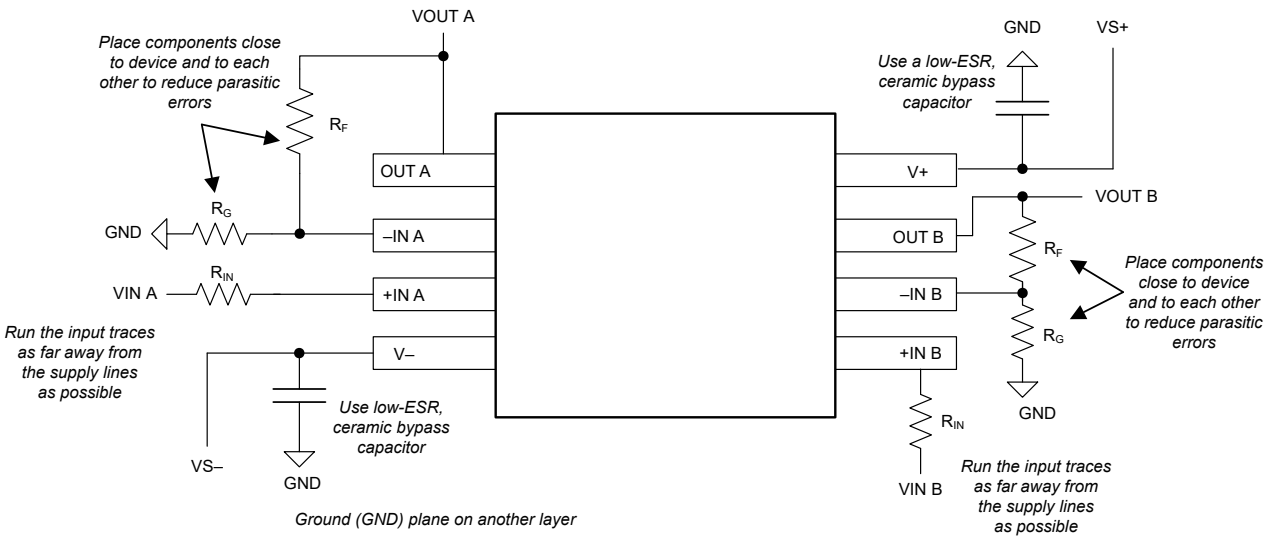


Figure 7-4. Layout Example

Figure 7-5. Schematic for Noninverting Configuration Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note
- Texas Instruments, *0A to 1A, Single-Supply, Low-Side, Current Sensing Solution* design guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2993IDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2993I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

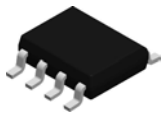
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

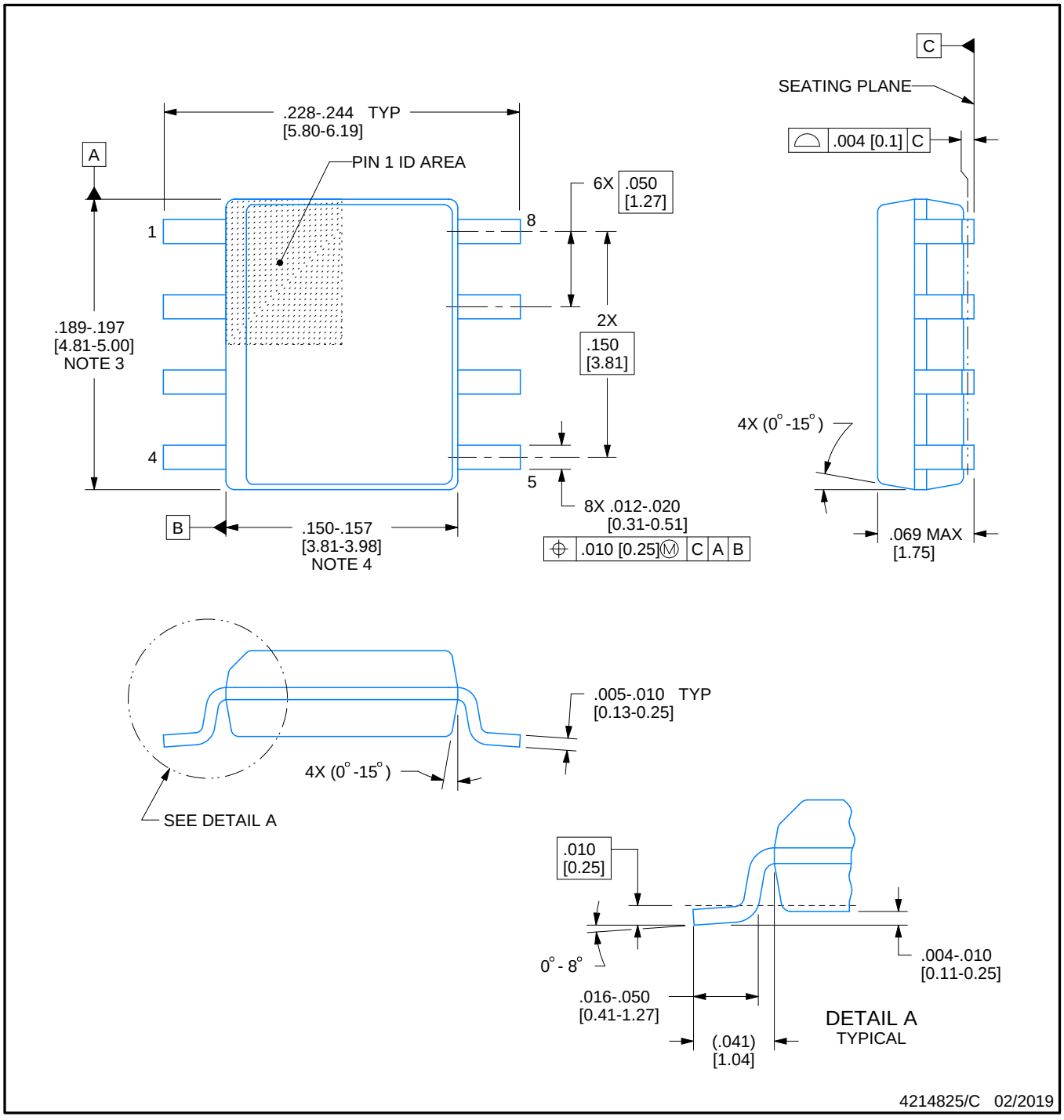


PACKAGE OUTLINE

D0008A

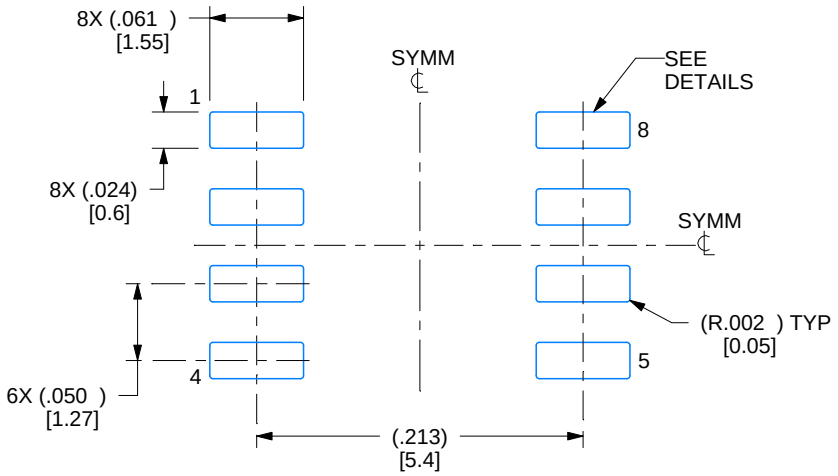
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

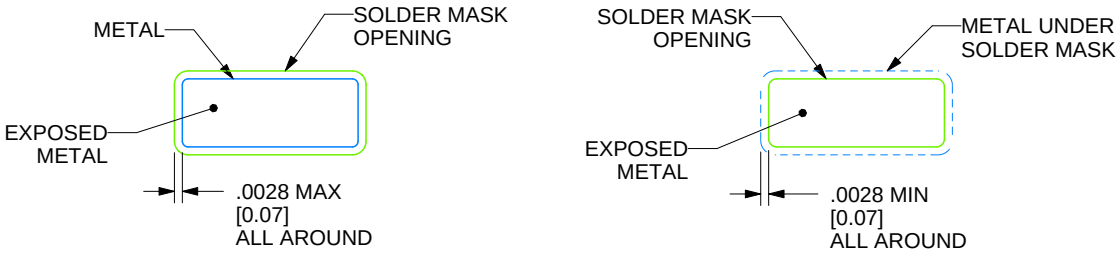


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

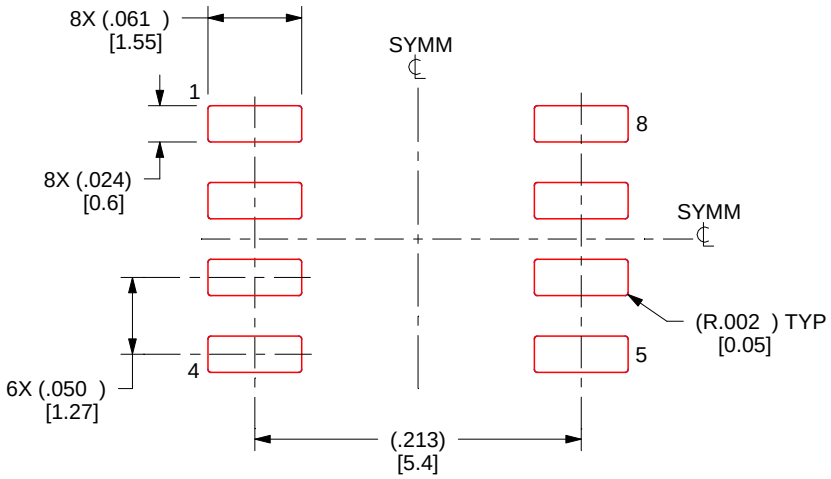
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025