

Very Low Noise, High-Speed, 12V CMOS Operational Amplifier

FEATURES

- **BANDWIDTH: 20MHz**
- **SLEW RATE: 30V/μs**
- **FAST 16-BIT SETTling TIME**
- **LOW NOISE: 6nV/√Hz (typ) at 100kHz**
- **EXCELLENT CMRR, PSRR, and A_{OL}**
- **RAIL-TO-RAIL OUTPUT**
- **CM RANGE INCLUDES GND**
- **THD+N: 0.0003% (typ) at 1kHz**
- **QUIESCENT CURRENT: 5.5mA/ch (max)**
- **SUPPLY VOLTAGE: 4V to 12V**
- **SHUTDOWN MODE (OPAx726): 6μA/ch**

APPLICATIONS

- **OPTICAL NETWORKING**
- **TRANSIMPEDANCE AMPLIFIERS**
- **INTEGRATORS**
- **ACTIVE FILTERS**
- **A/D CONVERTER BUFFERS**
- **I/V CONVERTER FOR DACs**
- **PORTABLE AUDIO**
- **PROCESS CONTROL**
- **TEST EQUIPMENT**

OPA725 RELATED PRODUCTS

FEATURES	PRODUCT
10MHz, 16V, 16V/μs, 8.5nV/√Hz at 1kHz	TLC080
8MHz, 36V, FET Input, 20V/μs, 8.5nV/√Hz at 1kHz	OPA132
100MHz, 5.5V, Precision Transimpedance Amplifier	OPA380
500MHz, ±5V, FET Input, 290V/μs, 7nV/√Hz at 100kHz	OPA656
7MHz, 12V, RRIO, 10V/μs, 30nV/√Hz at 10kHz	OPA743
16-Bit, 250kSPS, 4-Channel, Parallel Output ADC	ADS8342

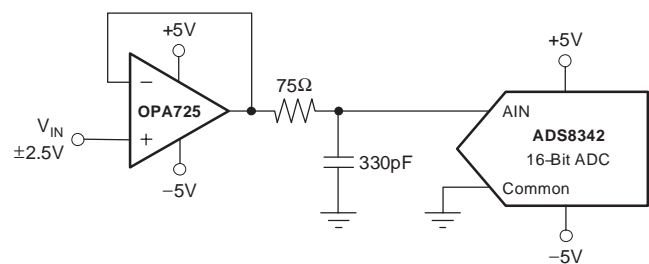
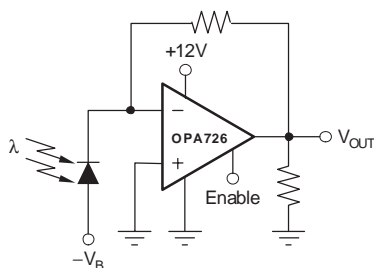
DESCRIPTION

The OPA725 and OPA726 series op amps use a state-of-the-art 12V analog CMOS process, and combine outstanding ac performance with low bias current and excellent CMRR, PSRR, and A_{OL}. The 20MHz Gain-Bandwidth (GBW) Product is achieved by using a proprietary and patent-pending output stage design. These characteristics allow excellent 16-bit settling times for driving 16-bit Analog-to-Digital converters (ADCs).

Excellent ac characteristics, such as 20MHz GBW, 30V/μs slew rate and 0.0003% THD+N make the OPA725 and OPA726 well-suited for communication, high-end audio, and active filter applications. With a bias current of less than 200pA, they are well-suited for use as transimpedance (I/V-conversion) amplifiers for monitoring optical power in ONET applications.

The OPA725 and OPA726 op amps can be used in single-supply applications from 4V up to 12V, or dual-supply from ±2V to ±6V. The output swings to within 150mV of the rails, maximizing dynamic range. The shutdown versions (OPAx726) reduce the quiescent current to less than 6μA and feature a reference pin for easy shutdown operation with standard CMOS logic in dual-supply applications.

The OPA725 (single) is available in SOT23-5 and SO-8 packages, and the OPA2725 (dual) is available in MSOP-8 and SO-8 packages. The OPA726 (single with shutdown) is available in MSOP-8 and SO-8. The OPA2726 (dual with shutdown) is available in MSOP-10. All versions are specified for operation from -40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Non-Shutdown						
OPA725	SOT23-5	DBV	-40°C to +125°C	OALI	OPA725AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA725AIDBVR	Tape and Reel, 3000
OPA725	SO-8	D	-40°C to +125°C	OPA725A	OPA725AID	Rails, 100
"	"	"	"	"	OPA725AIDR	Tape and Reel, 2500
OPA2725	SO-8	D	-40°C to +125°C	OPA2725A	OPA2725AID	Rails, 100
"	"	"	"	"	OPA2725AIDR	Tape and Reel, 2500
OPA2725	MSOP-8	DGK	-40°C to +125°C	BGM	OPA2725AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2725AIDGKR	Tape and Reel, 2500
Shutdown						
OPA726	SO-8	D	-40°C to +125°C	OPA726A	OPA726AID	Rails, 100
"	"	"	"	"	OPA726AIDR	Tape and Reel, 2500
OPA726	MSOP-8	DGK	-40°C to +125°C	BHC	OPA726AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA726AIDGKR	Tape and Reel, 2500
OPA2726	MSOP-10	DGS	-40°C to +125°C	BHB	OPA2726AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2726AIDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

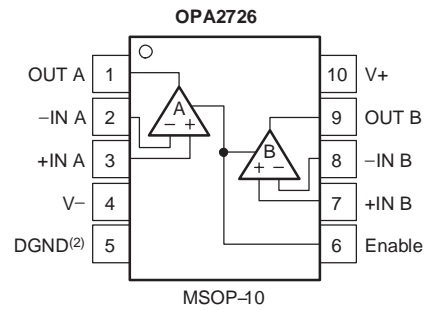
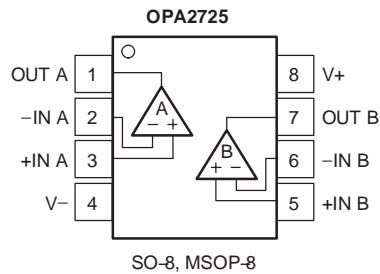
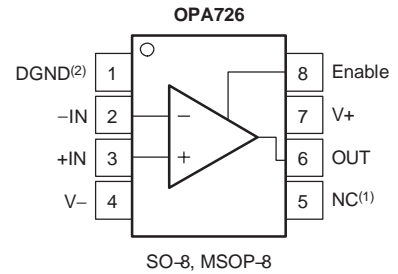
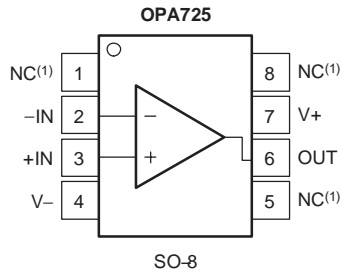
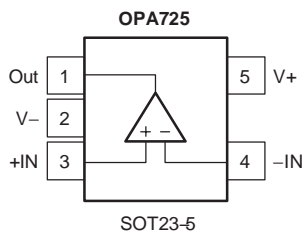
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+13.2V
Signal Input Terminals, Voltage(2)	-0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short Circuit(3)	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	1000 V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS



(1) NC denotes no internal connection.

(2) DGND = reference voltage for Enable Reference pin. Voltage on this pin will be the voltage to which the Enable Reference pin is referenced.

ELECTRICAL CHARACTERISTICS: $V_S = +4V$ to $+12V$ or $V_S = \pm 2V$ to $\pm 6V$

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+125^\circ C$.

At $T_A = +25^\circ C$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA725, OPA726, OPA2725, OPA2726			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage V_{OS}	$V_S = \pm 6V, V_{CM} = 0V$		1.2	3	mV
OPA725, OPA726	$V_S = \pm 6V, V_{CM} = 0V$		1.5	5	mV
OPA2725, OPA2726			4		$\mu V/^\circ C$
Drift			30	100	$\mu V/V$
vs Power Supply	$V_S = \pm 2V$ to $\pm 6V, V_{CM} = V-$			150	$\mu V/V$
Over Temperature					
Channel Separation, DC			1		$\mu V/V$
INPUT BIAS CURRENT					
Input Bias Current I_B			30	200	pA
Over Temperature			See Typical Characteristics		
Input Offset Current I_{OS}			10	50	pA
NOISE					
Input Voltage Noise, $f = 0.1Hz$ to $10Hz$	$V_S = \pm 6V, V_{CM} = 0V$		10		μV_{PP}
Input Voltage Noise Density, $f = 10kHz$	$V_S = \pm 6V, V_{CM} = 0V$		10		nV/\sqrt{Hz}
Input Voltage Noise Density, $f = 100kHz$	$V_S = \pm 6V, V_{CM} = 0V$		6		nV/\sqrt{Hz}
Input Current Noise Density, $f = 1kHz$	$V_S = \pm 6V, V_{CM} = 0V$		2.5		fA/\sqrt{Hz}
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		(V-)		(V+) - 2	V
Common-Mode Rejection Ratio $CMRR$	$(V-) \leq V_{CM} \leq (V+) - 2V$	88	94		dB
Over Temperature	$(V-) \leq V_{CM} \leq (V+) - 2V$	84			dB
	$(V-) \leq V_{CM} \leq (V+) - 3V$	94	100		dB
Over Temperature	$(V-) \leq V_{CM} \leq (V+) - 3V$	84			dB
INPUT IMPEDANCE					
Differential			$10^{11} 5$		ΩpF
Common-Mode			$10^{11} 4$		ΩpF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}					
OPA725, OPA726	$R_L = 100k\Omega, 0.15V < V_O < (V+) - 0.15V$	110	120		dB
Over Temperature	$R_L = 100k\Omega, 0.15V < V_O < (V+) - 0.15V$	100			dB
OPA2725, OPA2726	$R_L = 100k\Omega, 0.175V < V_O < (V+) - 0.175V$	110	120		dB
Over Temperature	$R_L = 100k\Omega, 0.175V < V_O < (V+) - 0.175V$	100			dB
OPA725, OPA726	$R_L = 1k\Omega, 0.25V < V_O < (V+) - 0.25V$	106	116		dB
Over Temperature	$R_L = 1k\Omega, 0.25V < V_O < (V+) - 0.25V$	96			dB
OPA2725, OPA2726	$R_L = 2k\Omega, 0.25V < V_O < (V+) - 0.25V$	106	116		dB
Over Temperature	$R_L = 2k\Omega, 0.25V < V_O < (V+) - 0.25V$	96			dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	$C_L = 20pF$				
Gain-Bandwidth Product			20		MHz
Slew Rate	$G = +1$		30		V/ μs
Settling Time, 0.1%	$V_S = \pm 6V, 5V$ Step, $G = +1$		350		ns
0.01%	$V_S = \pm 6V, 5V$ Step, $G = +1$		450		ns
Overload Recovery Time	$V_{IN} \cdot \text{Gain} > V_S$		50		ns
Total Harmonic Distortion + Noise	$V_S = \pm 6V, V_{OUT} = 2V_{RMS}, R_L = 600\Omega, G = +1, f = 1kHz$		0.0003		%

ELECTRICAL CHARACTERISTICS: $V_S = +4V$ to $+12V$ or $V_S = \pm 2V$ to $\pm 6V$ (continued)

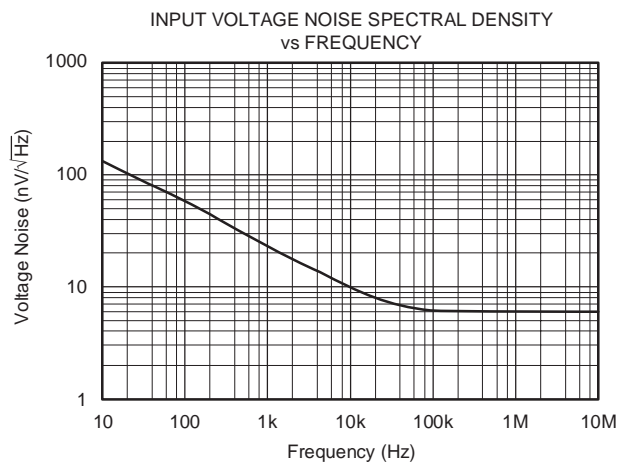
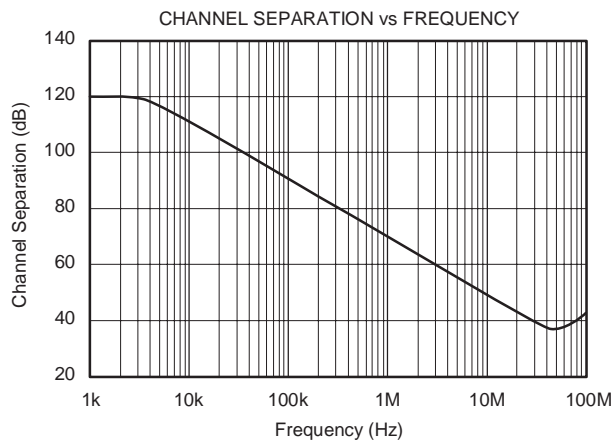
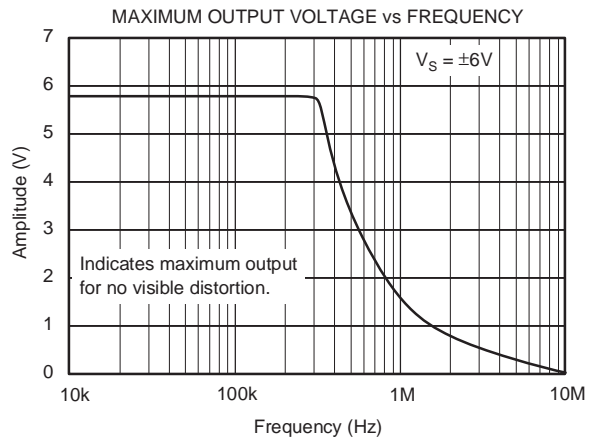
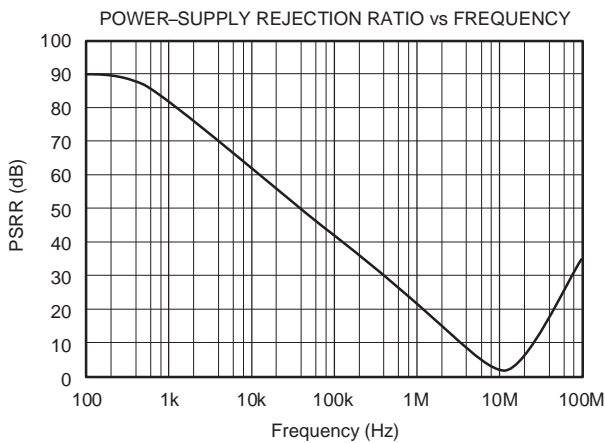
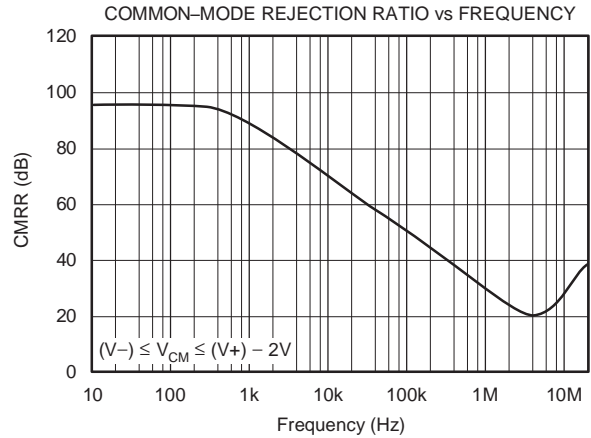
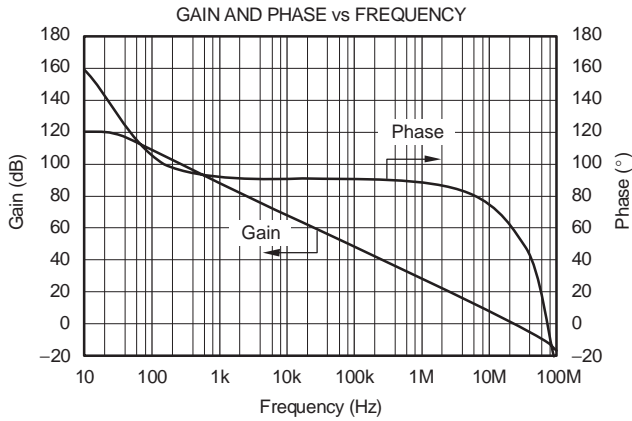
Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA725, OPA726, OPA2725, OPA2726			UNIT
		MIN	TYP	MAX	
OUTPUT					
Voltage Output Swing from Rail OPA725, OPA726 Over Temperature	$R_L = 100\text{k}\Omega$, $A_{OL} > 110\text{dB}$ $R_L = 100\text{k}\Omega$, $A_{OL} > 100\text{dB}$		100	150	mV
OPA2725, OPA2726 Over Temperature	$R_L = 100\text{k}\Omega$, $A_{OL} > 110\text{dB}$ $R_L = 100\text{k}\Omega$, $A_{OL} > 100\text{dB}$		125	175	mV
OPA725, OPA726 Over Temperature	$R_L = 1\text{k}\Omega$, $A_{OL} > 106\text{dB}$ $R_L = 1\text{k}\Omega$, $A_{OL} > 96\text{dB}$		200	250	mV
OPA2725, OPA2726 Over Temperature	$R_L = 2\text{k}\Omega$, $A_{OL} > 106\text{dB}$ $R_L = 2\text{k}\Omega$, $A_{OL} > 96\text{dB}$		200	250	mV
Output Current I_{OUT}	$ V_S - V_{OUT} < 1V$		40		mA
Short-Circuit Current I_{SC}			± 55		mA
Capacitive Load Drive C_{LOAD}		See Typical Characteristics			
Open-Loop Output Impedance	$f = 1\text{MHz}$, $I_O = 0$		40		Ω
ENABLE/SHUTDOWN (OPA_x726)					
t_{OFF}			5		μs
t_{ON}			30		μs
Enable Reference (DGND) Voltage Range V_{DGND}		V^-		$(V^+) - 2$	V
V_L (shutdown)				$< V_{DGND} + 0.8V$	V
V_H (amplifier is active)		$> V_{DGND} + 2V$			V
Input Disable Current	Ref Pin = Enable Pin = V^-		5		μA
I_{QSD} (per amplifier)			6	15	μA
POWER SUPPLY					
Specified Voltage Range V_S		4		12	V
Operating Voltage Range V_S			3.5 to 13.2		V
Quiescent Current (per amplifier) I_Q	$I_O = 0$		4.3	5.5	mA
Over Temperature				6	mA
TEMPERATURE RANGE					
Specified Range		-40		125	$^\circ\text{C}$
Operating Range		-55		125	$^\circ\text{C}$
Storage Range		-55		150	$^\circ\text{C}$
Thermal Resistance θ_{JA}					
SOT23-5			200		$^\circ\text{C/W}$
MSOP-8, MSOP-10, SO-8			150		$^\circ\text{C/W}$

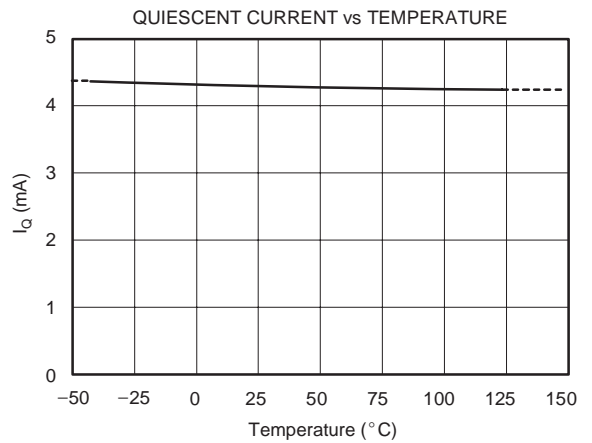
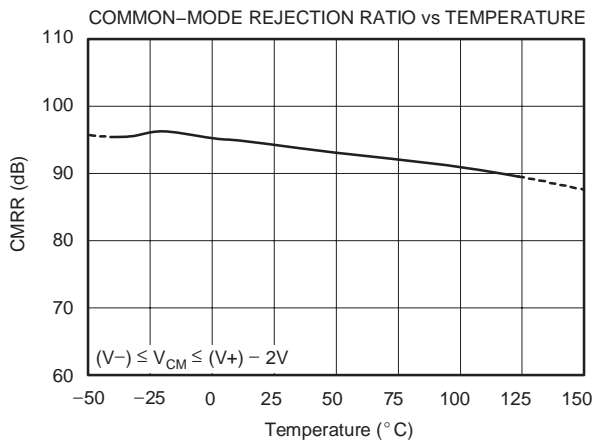
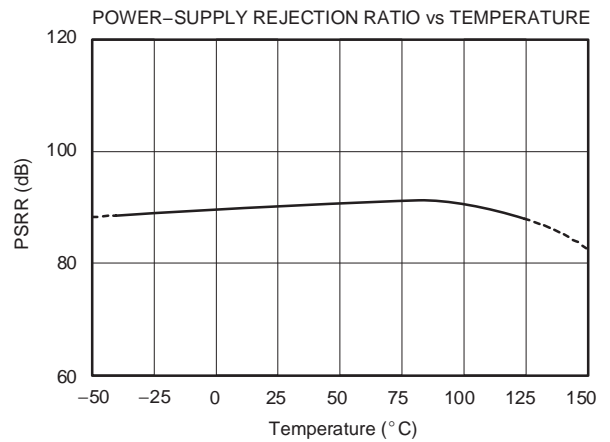
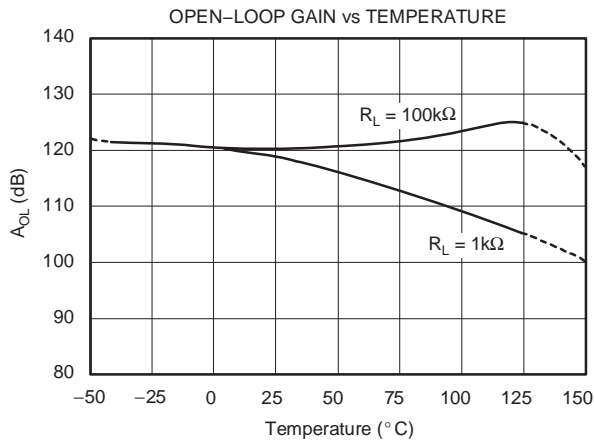
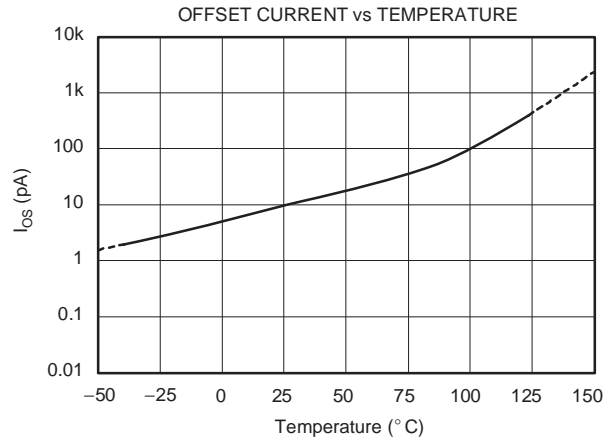
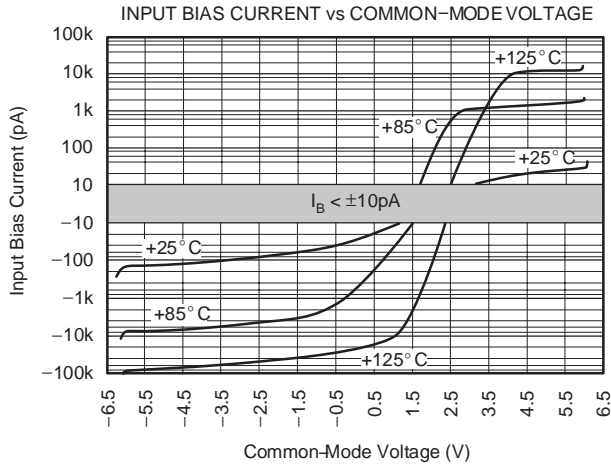
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



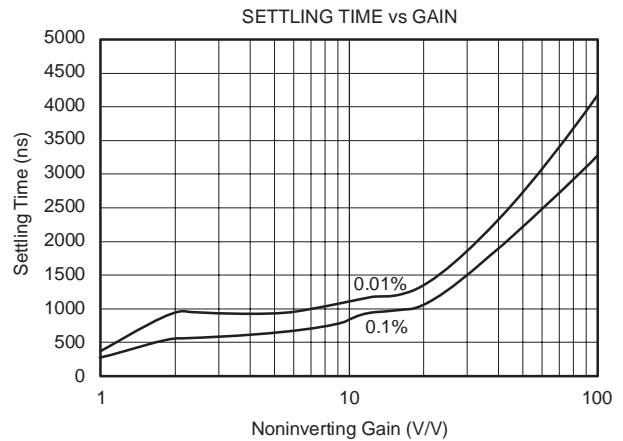
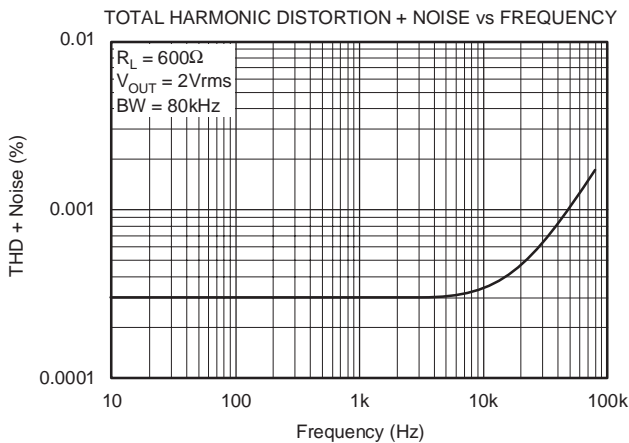
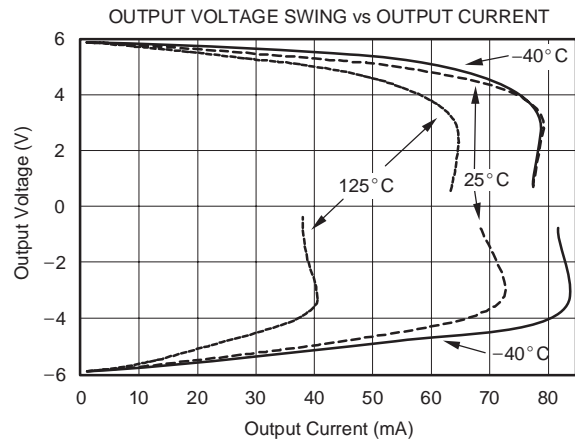
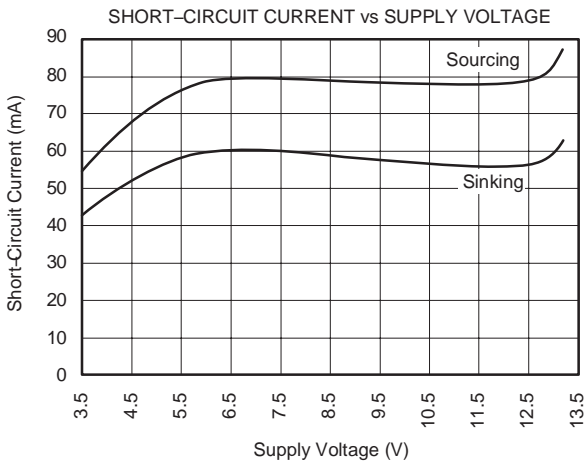
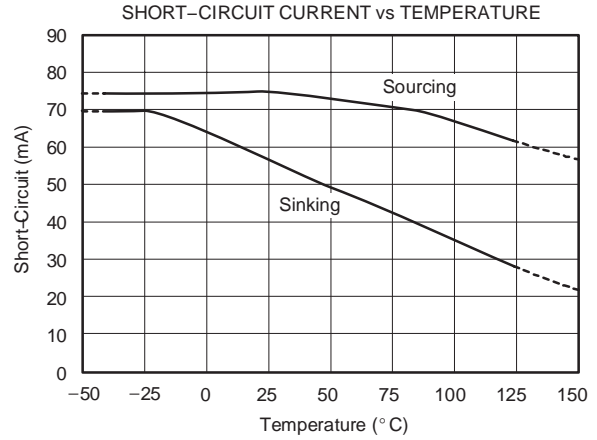
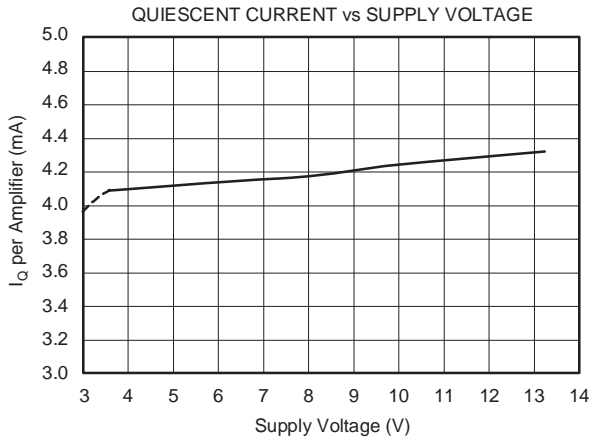
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



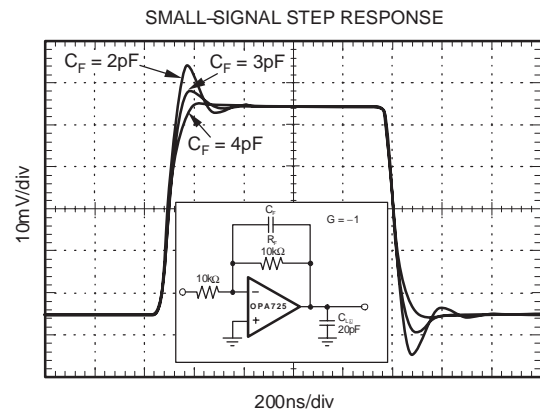
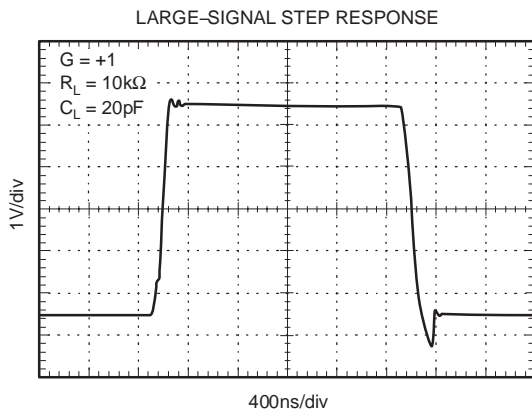
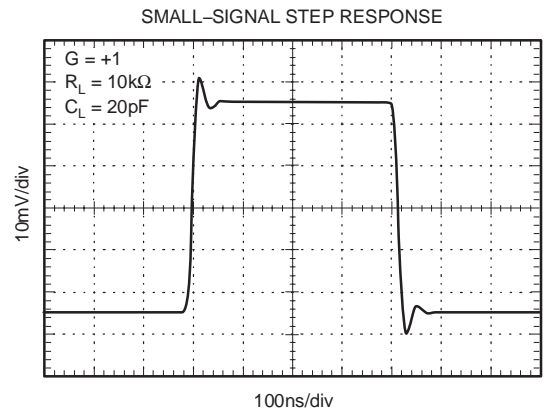
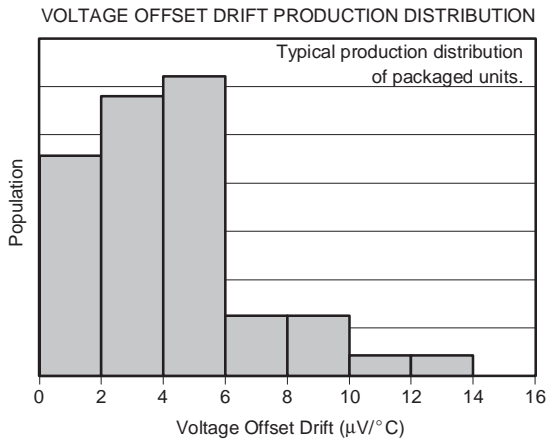
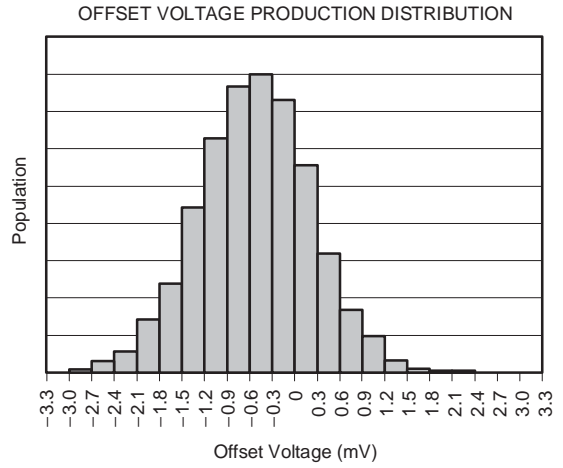
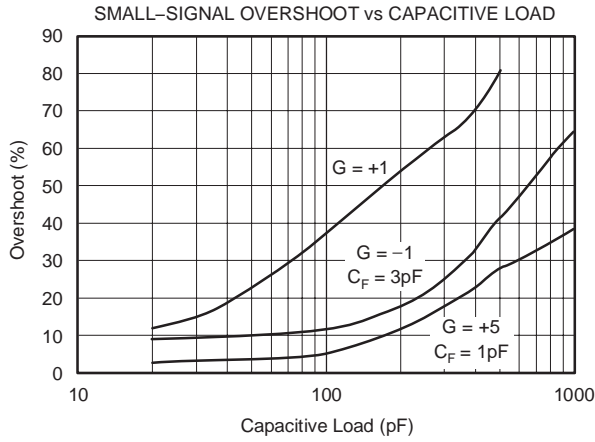
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



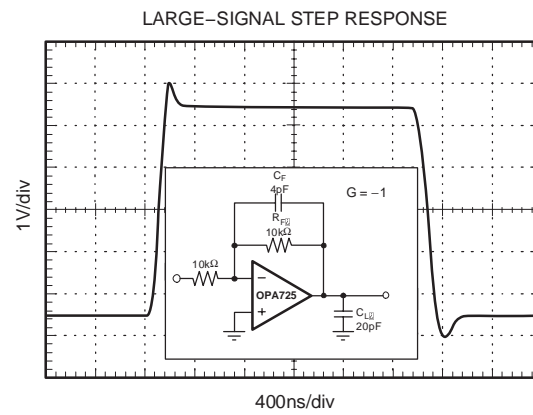
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

OPA725 and OPA726 series 20MHz CMOS op amps have a fast slew rate, low noise, and excellent PSRR, CMRR, and A_{OL} . These op amps can operate on typically 4.3mA quiescent current from a single (or split) supply in the range of 4V to 12V ($\pm 2V$ to $\pm 6V$), making them highly versatile and easy to use. They are stable in a unity-gain configuration.

Power-supply pins should be bypassed with 1nF ceramic capacitors in parallel with 1 μ F tantalum capacitors.

OPERATING VOLTAGE

OPA725 series op amps are specified from 4V to 12V supplies over a temperature range of -40°C to $+125^{\circ}\text{C}$. They will operate well in $\pm 5V$ or $+5V$ to $+12V$ power-supply systems. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

ENABLE/SHUTDOWN

OPA725 series op amps require approximately 4.3mA quiescent current. The enable/shutdown feature of the OPA726 allows the op amp to be shut off to reduce this current to approximately 6 μ A.

The enable/shutdown input is referenced to the Enable Reference Pin, DGND (see Pin Configurations). This pin can be connected to logic ground in dual-supply op amp configurations to avoid level-shifting the enable logic signal, as shown in Figure 1.

The Enable Reference Pin voltage, V_{DGND} , must not exceed $(V+) - 2V$. It may be set as low as $V-$. The amplifier is enabled when the Enable Pin voltage is greater than $V_{DGND} + 2V$. The amplifier is disabled (shutdown) if the Enable Pin voltage is less than $V_{DGND} + 0.8V$. The Enable Pin is connected to internal pull-up circuitry and will enable the device if left unconnected.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA725 and OPA726 series extends from $V-$ to $(V+) - 2V$.

Common-mode rejection is excellent throughout the input voltage range from $V-$ to $(V+) - 3V$. CMRR decreases somewhat as the common-mode voltage extends to $(V+) - 2V$, but remains very good and is tested throughout this range. See the Electrical Characteristics table for details.

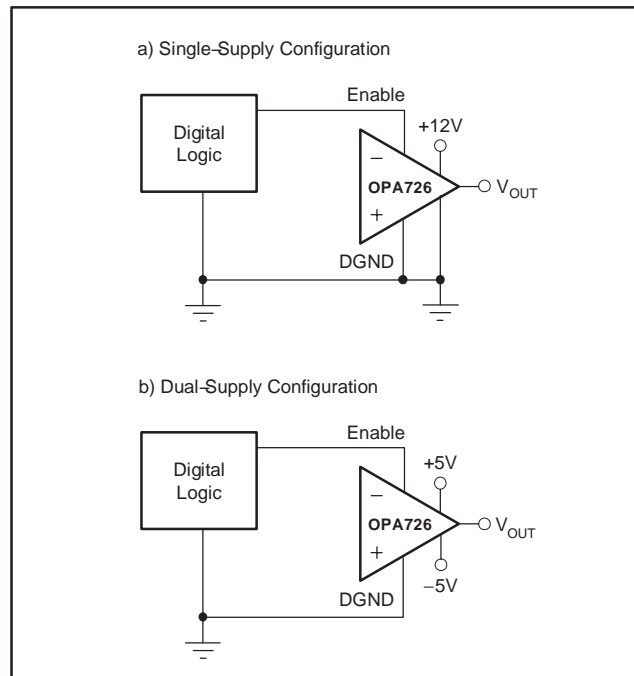


Figure 1. Enable Reference Pin Connection for Single- and Dual-Supply Configurations

INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor in series with the op amp, as shown in Figure 2. The OPA725 series features no phase inversion when the inputs extend beyond supplies, if the input is current limited.

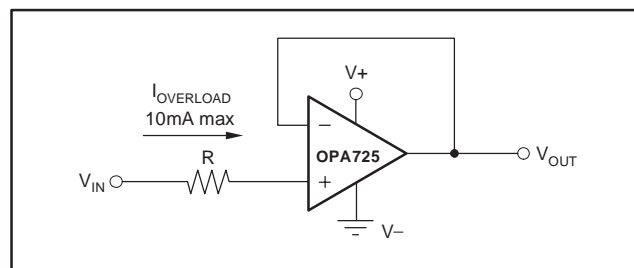


Figure 2. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving heavy loads connected to any point between $V+$ and $V-$. For light resistive loads ($> 100\text{k}\Omega$), the output voltage can swing to 150mV (175mV for dual) from the supply rail, while still maintaining excellent linearity ($A_{OL} > 110\text{dB}$). With $1\text{k}\Omega$ ($2\text{k}\Omega$ for dual) resistive loads, the output is specified to swing to within 250mV from the supply rails with excellent linearity (see the Typical Characteristics curve *Output Voltage Swing vs Output Current*).

CAPACITIVE LOAD AND STABILITY

Capacitive load drive is dependent upon gain and the overshoot requirements of the application. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see the Typical Characteristics curve *Small-Signal Overshoot vs Capacitive Load*).

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC accuracy.

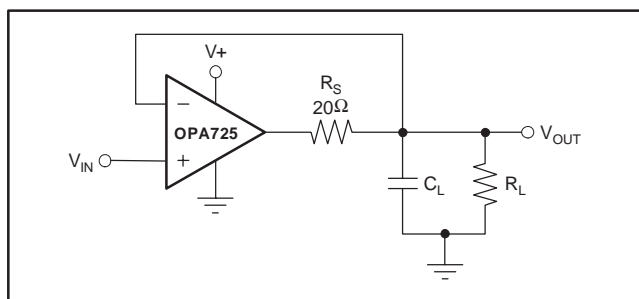


Figure 3. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

DRIVING FAST 16-BIT ADCs

The OPA725 series is optimized for driving fast 16-bit ADCs such as the ADS8342. The OPA725 op amps buffer the converter input capacitance and resulting charge injection, while providing signal gain. Figure 4 shows the OPA725 in a single-ended method of interfacing to the ADS8342 16-bit, 250kSPS, 4-channel ADC with an input range of $\pm 2.5\text{V}$. The OPA725 has demonstrated excellent settling time to the 16-bit level within the 600ns acquisition time of the ADS8342. The RC filter, shown in Figure 4, has been carefully tuned for best noise and settling performance. It may need to be adjusted for different op amp configurations. Please refer to the ADS8342 data sheet (available for download at www.ti.com) for additional information on this product.

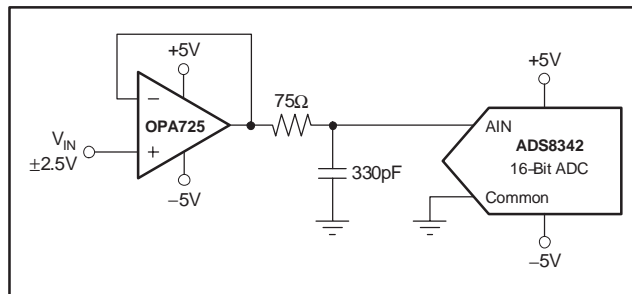


Figure 4. OPA725 Driving an ADC

TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA725 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 5, are the expected diode capacitance (C_D), which should include the parasitic input common-mode and differential-mode input capacitance ($4\text{pF} + 5\text{pF}$ for the OPA725); the desired transimpedance gain (R_F); and the GBW for the OPA725 (20MHz). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_F includes the stray capacitance of R_F , which is 0.2pF for a typical surface-mount resistor.

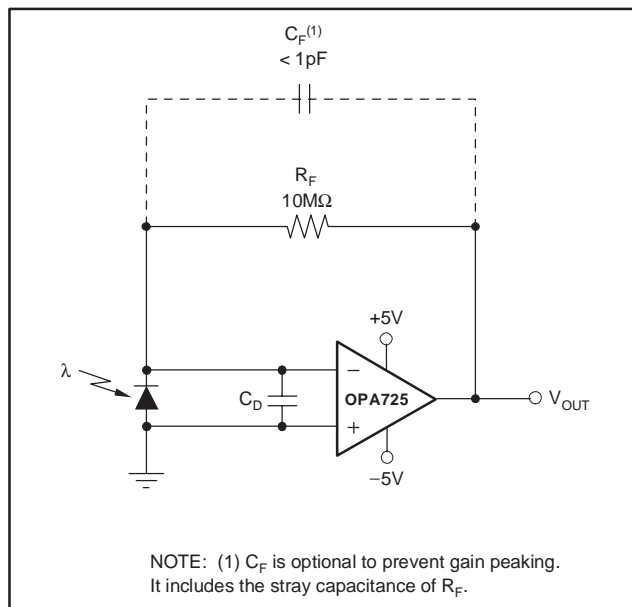


Figure 5. Dual-Supply Transimpedance Amplifier

To achieve a maximally-flat, 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA354 (100MHz GBW), OPA300 (180 MHz GBW), OPA355 (200MHz GBW), or OPA656, OPA657 (400MHz GBW) may be used.

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. (Refer to Figure 6.) This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.

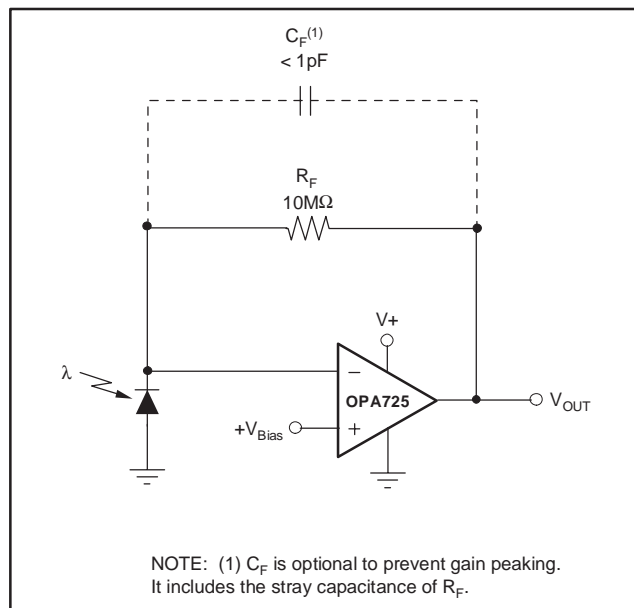


Figure 6. Single-Supply Transimpedance Amplifier

For additional information, refer to Application Bulletin SBOA055, *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.

OPTIMIZING THE TRANSIMPEDANCE CIRCUIT

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select R_F to create the total required gain. Using a lower value for R_F and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by R_F increases with the square-root of R_F , whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the R_F to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download at the TI web site.

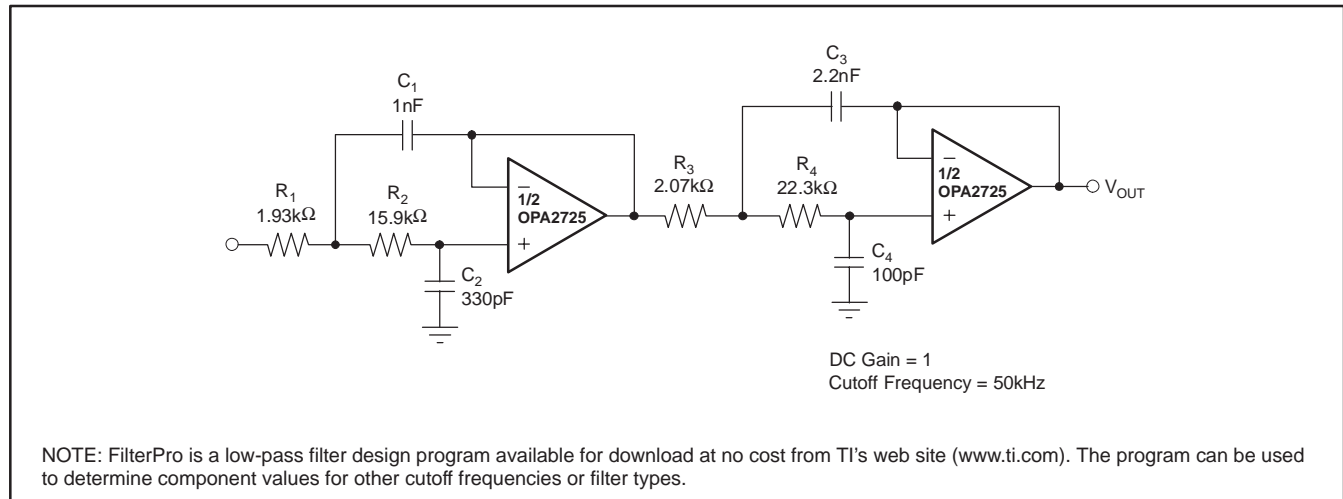


Figure 7. Four-Pole Butterworth Sallen-Key Low-Pass Filter

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2725AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2725A
OPA2725AID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2725A
OPA2725AIDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2725A
OPA2725AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BGM
OPA2725AIDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BGM
OPA2725AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BGM
OPA2725AIDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BGM
OPA2725AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2725A
OPA2725AIDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2725A
OPA2726AIDGST	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BHB
OPA2726AIDGST.B	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHB
OPA2726AIDGSTG4	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHB
OPA725AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 725A
OPA725AID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 725A
OPA725AIDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OALI
OPA725AIDBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OALI
OPA725AIDBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OALI
OPA725AIDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OALI
OPA725AIDBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OALI
OPA725AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 725A
OPA725AIDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 725A
OPA726AID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 726A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA726AID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 726A
OPA726AIDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 726A
OPA726AIDG4.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 726A
OPA726AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BHC
OPA726AIDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHC
OPA726AIDGKTG4	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BHC

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2725AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA725AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA725AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA725AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2725AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA725AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA725AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA725AIDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2725AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2725AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2725AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA725AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA725AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA726AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA726AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA726AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA726AIDG4.B	D	SOIC	8	75	506.6	8	3940	4.32

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025