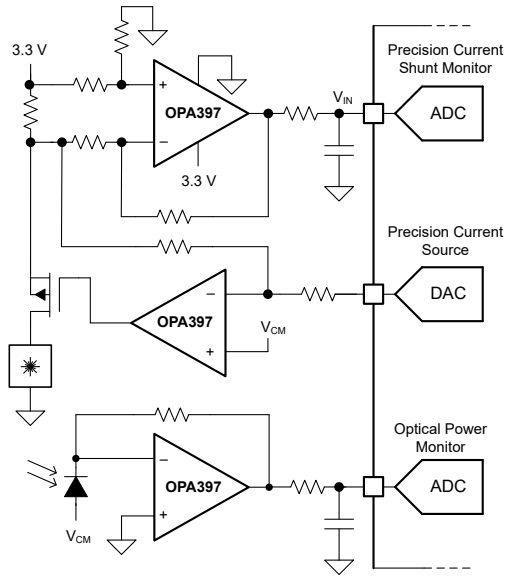
OPAx397 Precision, Low-Offset-Voltage, Low-Noise, Low-Input-Bias-Current, Rail-to-Rail I/O, e-trim™ Operational Amplifiers

1 Features

- Low offset voltage: ±60µV (maximum)
- Low-drift: ±0.18µV/°C
- Low input bias current: 10fA
- Low noise: 4.4nV/√Hz at 10kHz
- Low 1/f noise: 2µV_{PP} (0.1Hz to 10Hz)
- Low supply voltage operation: 1.7V to 5.5V
- Low quiescent current: 1.22mA
- Fast settling: 0.75µs (1V to 0.1%)
- Fast slew rate: 4.5V/µs
- High output current: +65/-55mA short circuit
- Gain bandwidth: 13MHz
- Rail-to-rail input and output
- Specified temperature range: –40°C to +125°C
- EMI/RFI filtered inputs

2 Applications

- Multiparameter patient monitor
- Electrocardiogram (ECG)
- Chemistry/gas analyzer
- Optical module
- Analog input module
- Process analytics (pH, gas, concentration, force and humidity)
- Gas detector
- Analog security camera
- Merchant DC/DC
- Pulse oximeter
- Inter-DC interconnect (long-haul, submarine)
- Data acquisition (DAQ)



OPAx397 Applications in Optical Modules

3 Description

The OPAx397 family of operational amplifiers (OPA397, OPA2397, and OPA4397) features ultra-low offset, offset drift, and input bias current with rail-to-rail input and output operation. In addition to precision dc accuracy, the ac performance is optimized for low noise and fast-settling transient response. These features make the OPAx397 an excellent choice for driving high-precision analog-to-digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs).

The OPAx397 feature TI's e-trim™ operational amplifier technology to achieve ultra-low offset voltage and offset voltage drift without any input chopping or auto-zero techniques. This technique enables ultra-low input bias current for sensor inputs or photodiode current-to-voltage measurements, creating high-performance transimpedance stages for optical modules or medical instrumentation.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE
OPA397	Single	DCK (SC70, 5)	2.0mm × 2.1mm
		DBV (SOT-23, 5)	2.9mm × 2.8mm
OPA2397	Dual	DGK (VSSOP, 8)	3.0mm × 4.9mm
		D (SOIC, 8)	4.9mm × 6.0mm
OPA4397	Quad	PW (TSSOP, 14)	5.0mm × 6.4mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.

Table of Contents

4 Pin Configuration and Functions

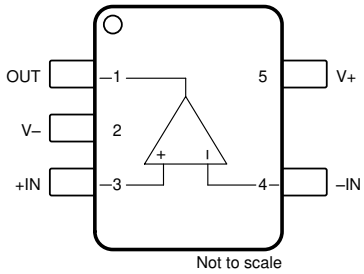


Figure 4-1. OPA397 DBV Package
5-Pin SOT-23
(Top View)

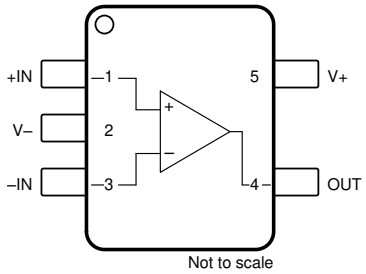


Figure 4-2. OPA397 DCK Package
5-Pin SC70
(Top View)

Table 4-1. Pin Functions: OPA397

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DBV (SOT-23)	DCK (SC70)		
–IN	4	3	Input	Inverting input
+IN	3	1	Input	Noninverting input
OUT	1	4	Output	Output
V–	2	2	Power	Negative (lowest) power supply
V+	5	5	Power	Positive (highest) power supply

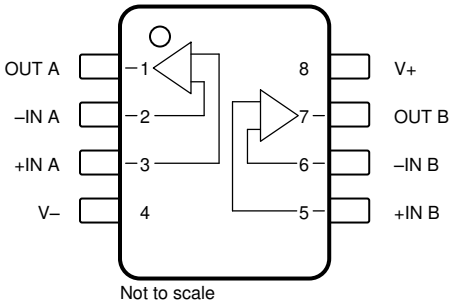


Figure 4-3. OPA2397 DGK and D Packages
8-Pin SOIC and DGK Package
8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2397

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
+IN A	3	Input	Noninverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply

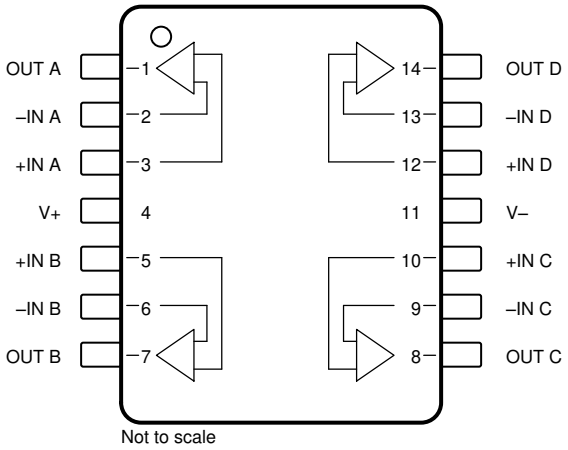


Figure 4-4. OPA4397 PW Package
14-Pin TSSOP
(Top View)

Table 4-3. Pin Functions: OPA4397

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
+IN A	3	Input	Noninverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN B	5	Input	Noninverting input, channel B
–IN C	9	Input	Inverting input, channel C
+IN C	10	Input	Noninverting input, channel C
–IN D	13	Input	Inverting input, channel D
+IN D	12	Input	Noninverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V–	11	Power	Negative (lowest) power supply
V+	4	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device is not specified to be fully
functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T_A	Specified temperature	Specified temperature	–40		+125	°C

5.4 Thermal Information OPA397

THERMAL METRIC(1)		OPA397		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	220.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	124.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	72.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	46.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	72.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information OPA2397

THERMAL METRIC(1)		OPA2397		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.7	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.2	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.8	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.4	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information OPA4397

THERMAL METRIC(1)		OPA4397	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics

at T_A = 25°C, V_S = 1.7V to 5.5V (single-supply) or V_S = ±0.85V to ±2.75V (dual-supply), R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.0V			±10	±60	µV
			V_{CM} = (V+) – 200mV		±20	±100	
			T_A = –40°C to +125°C[1]			±200	
		V_{CM} = V–, T_A = –40°C to +125°C[1]				±125	
			OPA2397DGK			±180	
dV_{OS}/dT	Input offset voltage drift	V_S = 5.0V	T_A = 0°C to 85°C		±0.16		µV/°C
			T_A = –40°C to +125°C[1]			±1	
			V_{CM} = 5.0V, T_A = –40°C to +125°C[1]		±0.18	±1.5	
PSRR	Power supply rejection ratio	V_{CM} = V–				±30	µV/V
			T_A = –40°C to +125°C[1]			±80	
INPUT BIAS CURRENT							
I_B	Input bias current[1]				±0.01	±1	pA
		T_A = –40°C to +85°C				±10	
		T_A = –40°C to +125°C				±50	
I_{OS}	Input offset current[1]				±0.01	±0.8	pA
		T_A = –40°C to +85°C				±5	
		T_A = –40°C to +125°C				±30	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			2.0		$µV_{PP}$
			V_{CM} = (V+) – 0.3V		3.2		
e_N	Input voltage noise density	f = 10Hz			42		$nV/\sqrt{Hz}$
			V_{CM} = (V+) – 0.3V		80		
		f = 1kHz			6.5		
			V_{CM} = (V+) – 0.3V		10.4		
		f = 10kHz			4.4		
			V_{CM} = (V+) – 0.3V		5.8		
i_N	Input current noise density	f = 1kHz	OPA397		70		$fA/\sqrt{Hz}$
			OPA2397, OPA4397		25		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			V–		V+	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5V		75	120		dB
			T_A = –40°C to +125°C		113		
		(V–) < V_{CM} < (V+), T_A = –40°C to +125°C[1]		66	97		
			V_S = 5.5V	88	111		
INPUT CAPACITANCE							
Z_{ID}	Differential				10^{13} || 2.8		Ω || pF
Z_{ICM}	Common-mode				10^{13} || 3.5		Ω || pF

5.7 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 1.7V to 5.5V (single-supply) or V_S = ±0.85V to ±2.75V (dual-supply), R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5V	(V–) + 50mV < V_{OUT} < (V+) – 50mV	115	132		dB
			(V–) + 100mV < V_O < (V+) – 100mV, R_L = 2kΩ	110	128		
			(V–) + 100mV < V_{OUT} < (V+) – 100mV, R_L = 2kΩ, T_A = –40°C to +125°C(1)	100			
		V_S = 1.7V	(V–) + 50mV < V_{OUT} < (V+) – 50mV, V_{CM} = (V+) – 1.15V	106	124		
			(V–) + 100mV < V_{OUT} < (V+) – 100mV, R_L = 2kΩ, V_{CM} = (V+) – 1.15V	106	124		
			(V–) + 100mV < V_{OUT} < (V+) – 100mV, R_L = 2kΩ, V_{CM} = (V+) – 1.15V, T_A = –40°C to +125°C(1)	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	A_V = 1000V/V			13		MHz
SR	Slew rate	4V step, gain = +1	falling		4.5		V/µs
			rising		3.5		
	Phase margin	C_L = 100pF	OPA397		45		°
			OPA2397, OPA4397		35		
t_S	Settling time	To 0.1%, 2V step, gain = +1			0.75		µs
		To 0.01%, 2V step, gain = +1			1		
	Overload recovery time	V_{IN} × gain > V_S			0.45		µs
THD+N	Total harmonic distortion + noise	V_{OUT} = 1V_{RMS}, gain = +1, f = 1kHz, V_{CM} = (V–) + 1.5V			–112		dB
					0.00025		%
OUTPUT							
	Voltage output swing from both rails	V_S = 1.7V				20	mV
			R_L = 2kΩ			30	
		V_S = 5.5V				20	
			R_L = 2kΩ			35	
I_{SC}	Short-circuit current	Sinking, V_S = 5.5V			–55		mA
		Sourcing, V_S = 5.5V			65		
R_O	Open-loop output impedance	f = 1MHz			120		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			1.22	1.4	mA
			T_A = –40°C to +125°C(1)			1.5	

(1) Specification established from device population bench system measurements across multiple lots.

5.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

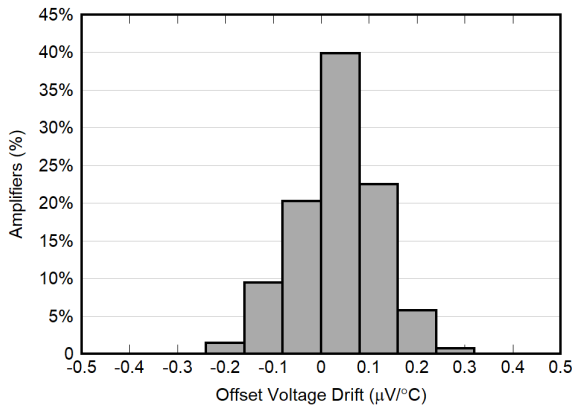


Figure 5-1. Offset Voltage Distribution

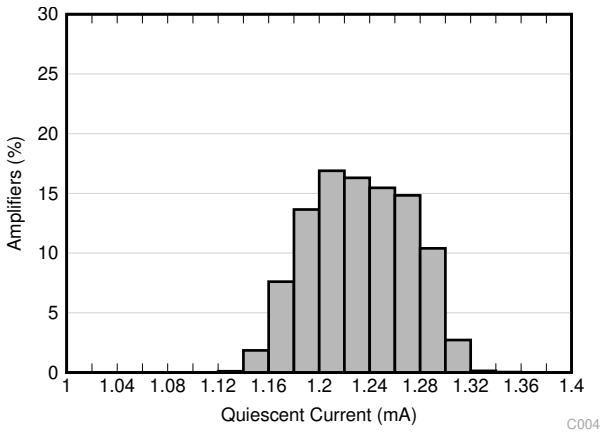


Figure 5-2. Quiescent Current Distribution

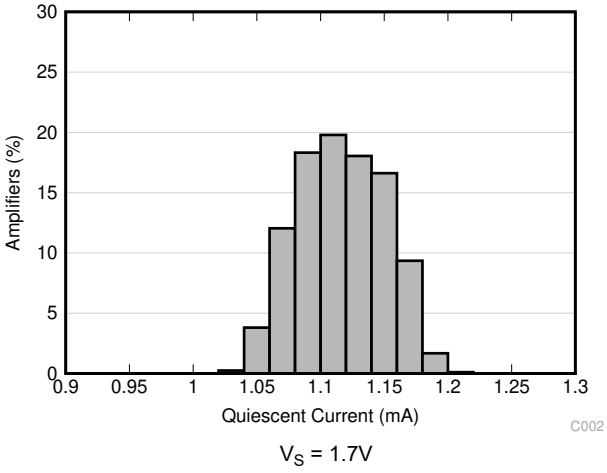


Figure 5-3. Quiescent Current Distribution

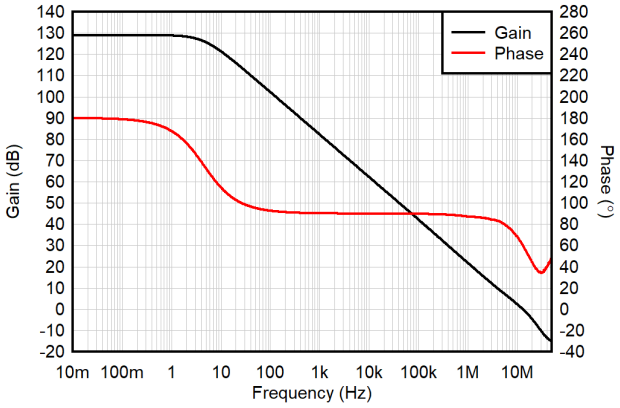


Figure 5-4. Open-Loop Gain and Phase vs Frequency

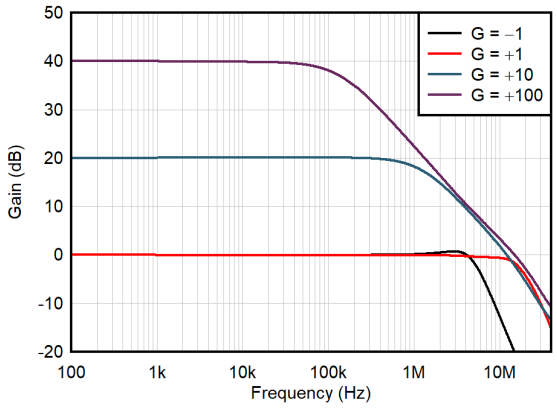


Figure 5-5. Closed-Loop Gain and Phase vs Frequency

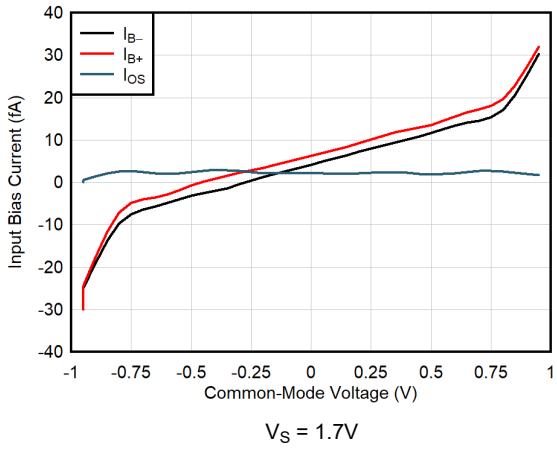


Figure 5-6. Input Bias Current vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

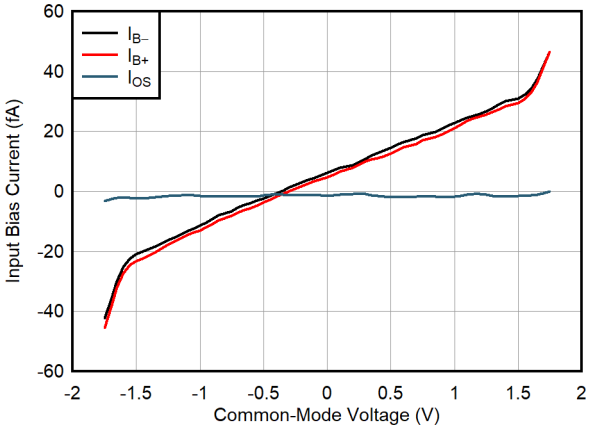


Figure 5-7. Input Bias Current vs Common-Mode Voltage

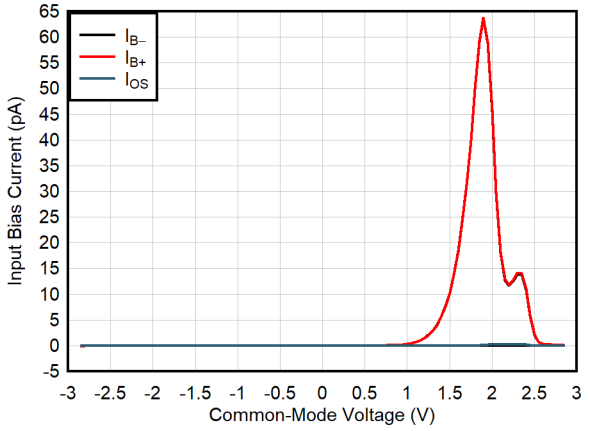


Figure 5-8. Input Bias Current vs Common-Mode Voltage

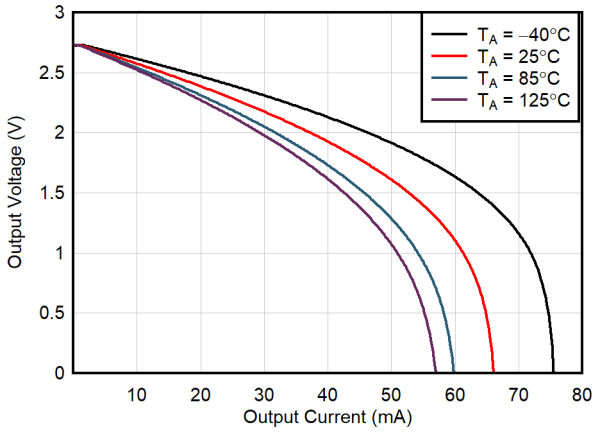


Figure 5-9. Output Voltage Swing vs Output Current (Sourcing)

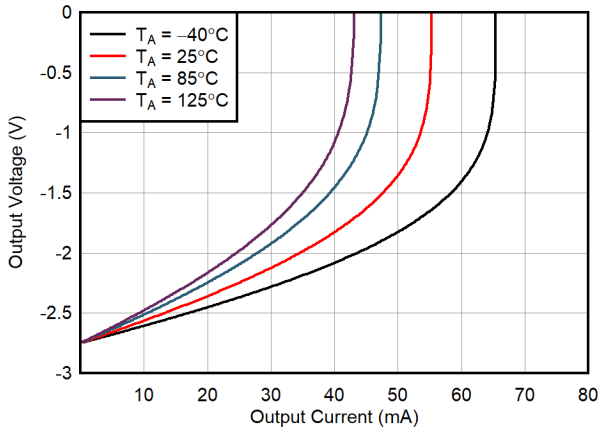


Figure 5-10. Output Voltage Swing vs Output Current (Sinking)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

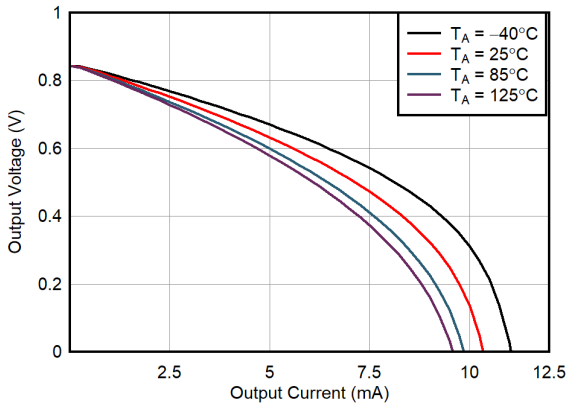


Figure 5-11. Output Voltage Swing vs Output Current (Sourcing)

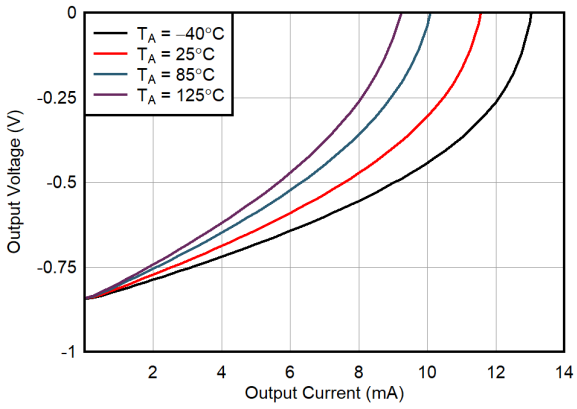


Figure 5-12. Output Voltage Swing vs Output Current (Sinking)

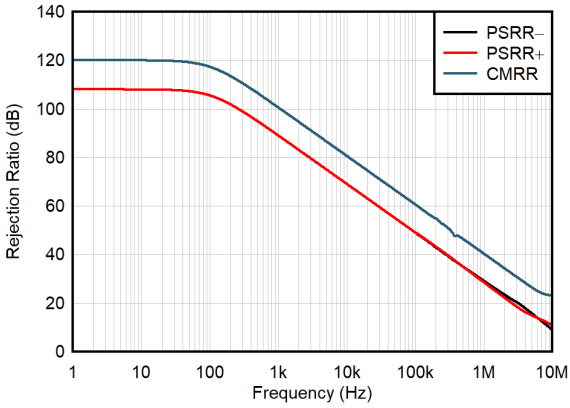


Figure 5-13. CMRR and PSRR vs Frequency

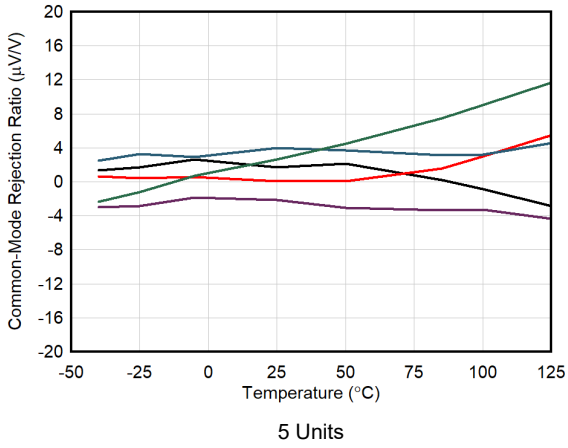


Figure 5-14. CMRR vs Temperature

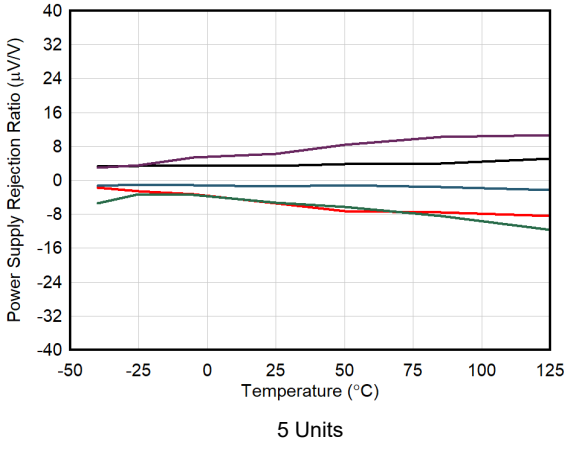


Figure 5-15. PSRR vs Temperature

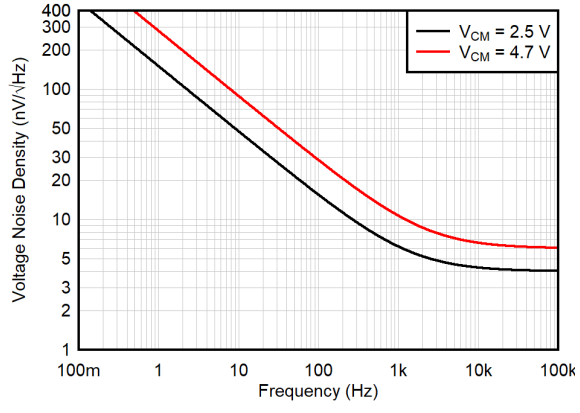
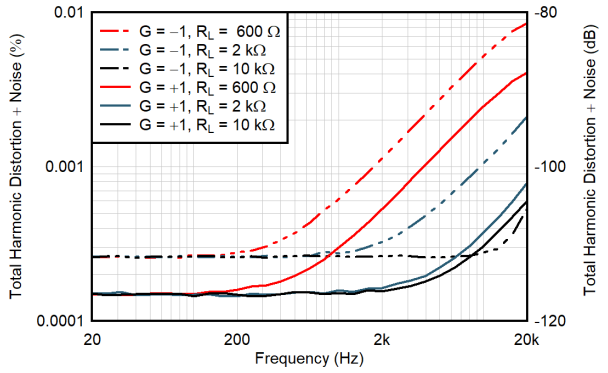


Figure 5-16. Voltage Noise vs Frequency

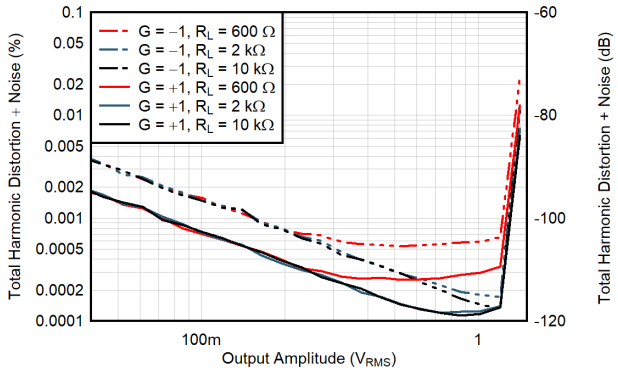
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



V_{OUT} = 1V_{RMS}

Figure 5-17. THD+N Ratio vs Frequency



f = 1kHz

Figure 5-18. THD+N vs Output Amplitude

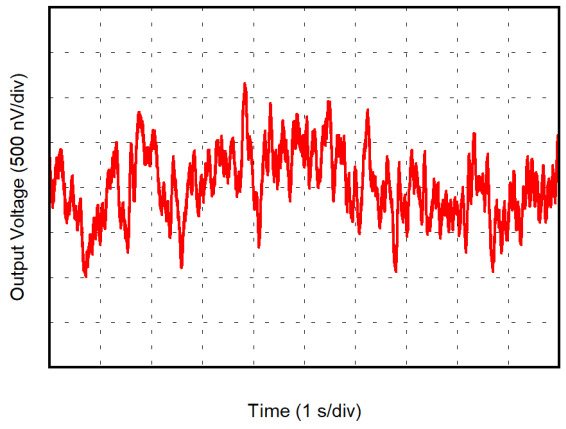
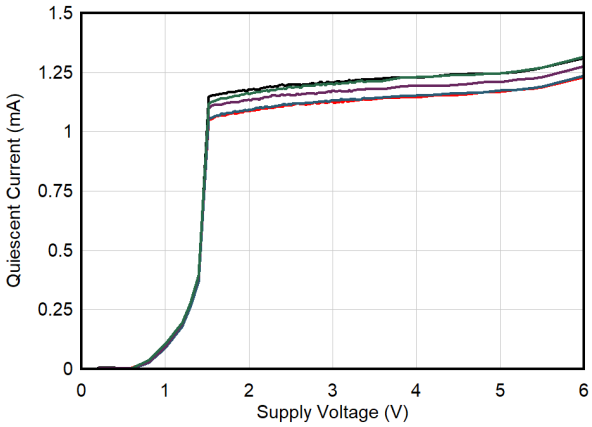
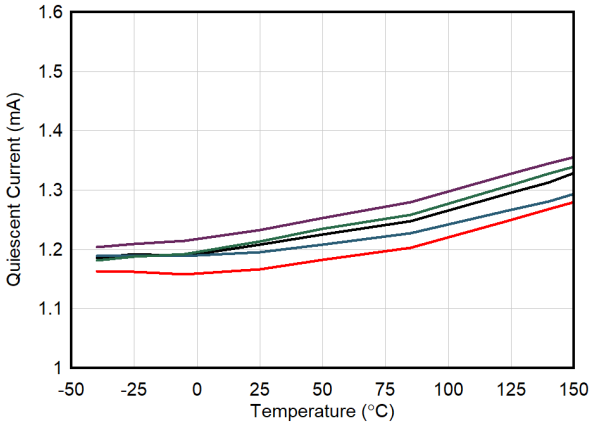


Figure 5-19. 0.1Hz to 10Hz Noise



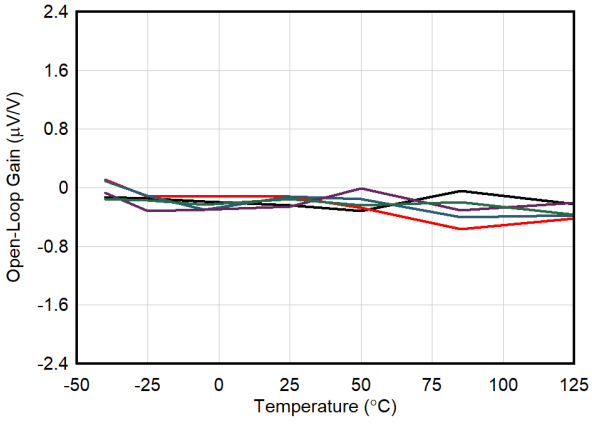
5 Units

Figure 5-20. Quiescent Current vs Supply Voltage



5 Units

Figure 5-21. Quiescent Current vs Temperature



5 Units

Figure 5-22. Open-Loop Gain vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

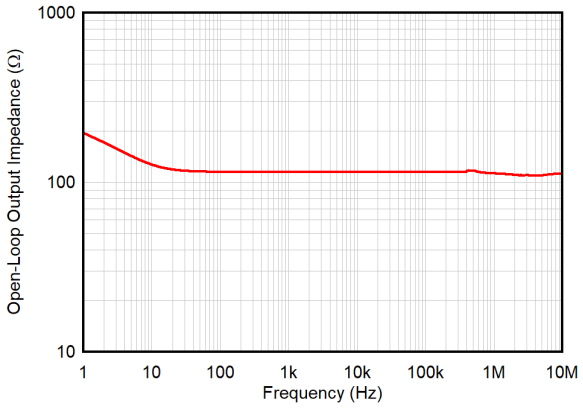


Figure 5-23. Open-Loop Output Impedance vs Frequency

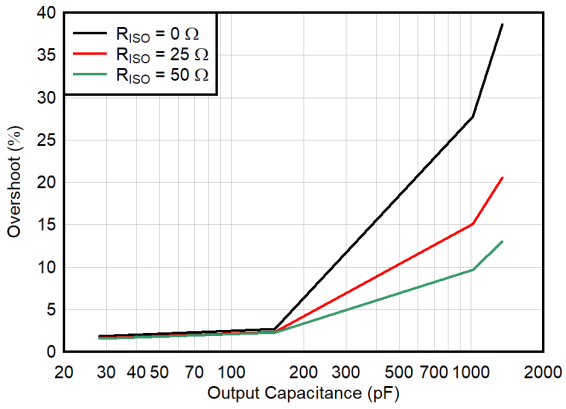


Figure 5-24. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

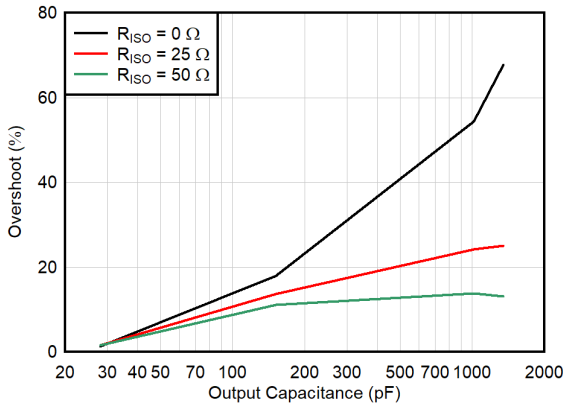


Figure 5-25. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

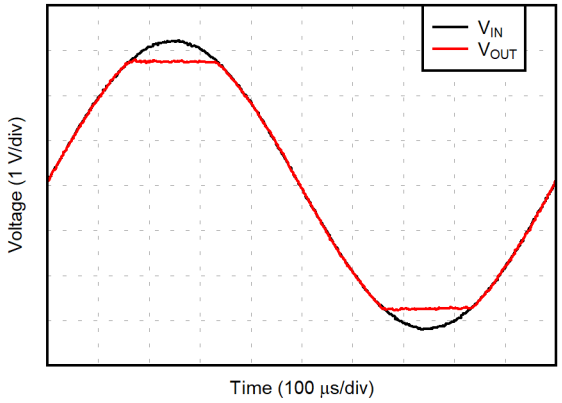


Figure 5-26. No Phase Reversal

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

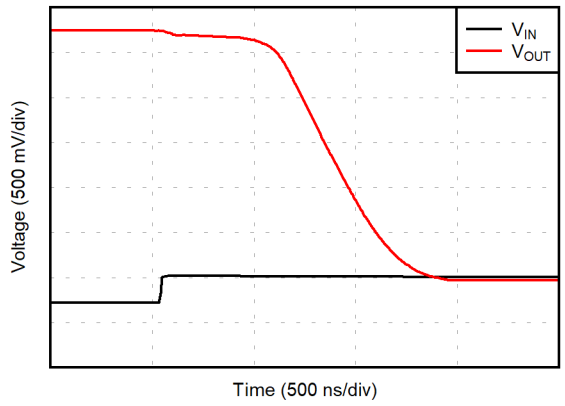


Figure 5-27. Positive Overload Recovery

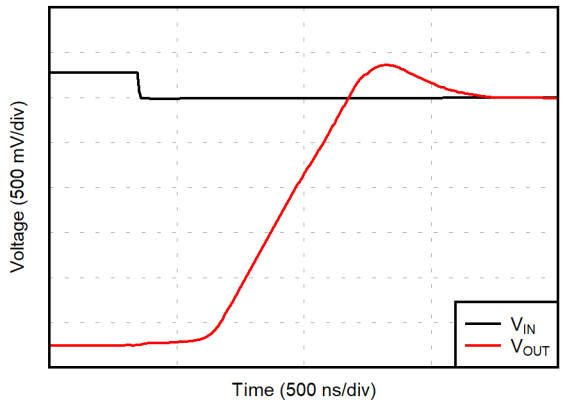


Figure 5-28. Negative Overload Recovery

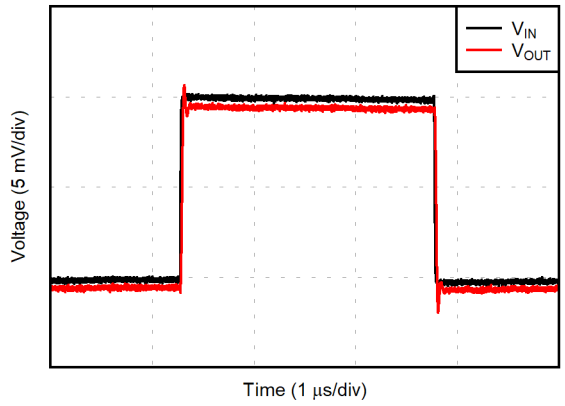


Figure 5-29. Small-Signal Step Response (10mV Step)

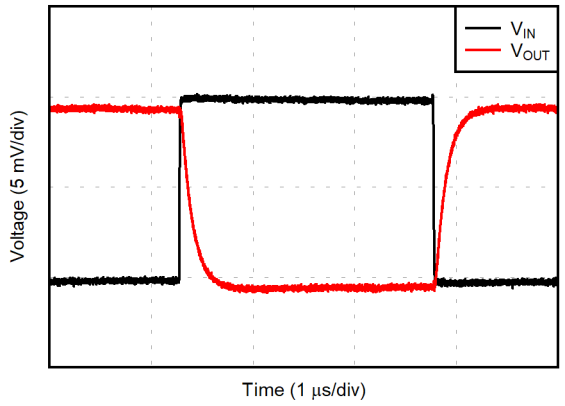


Figure 5-30. Small-Signal Step Response (10mV Step)

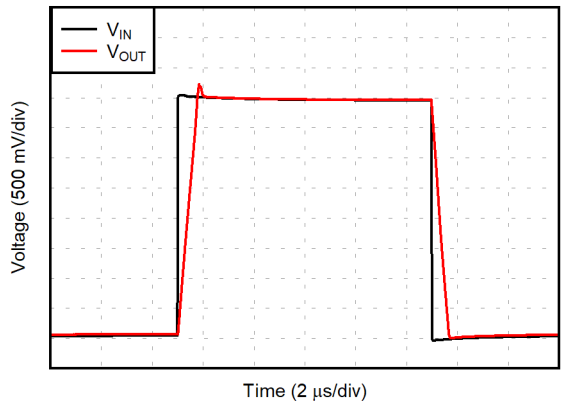


Figure 5-31. Large-Signal Step Response (4V Step)

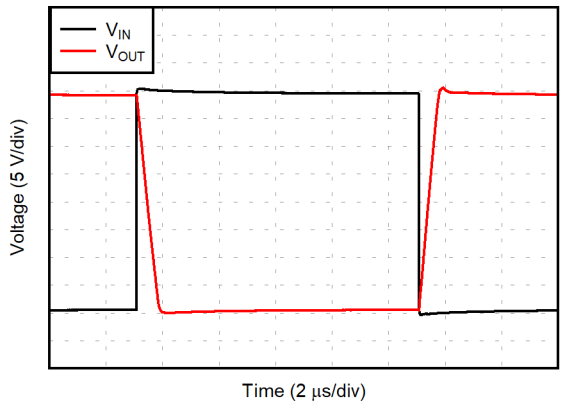


Figure 5-32. Large-Signal Step Response (4V Step)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

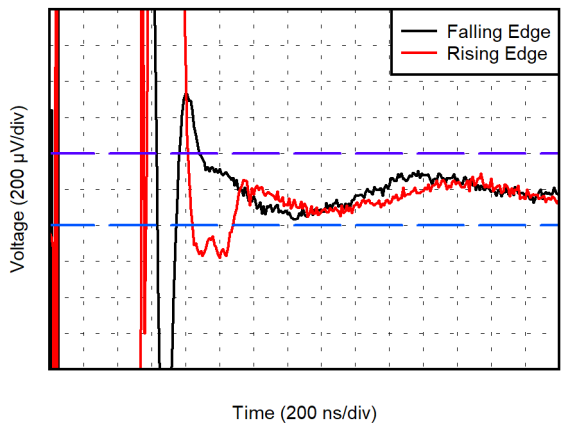


Figure 5-33. Settling Time

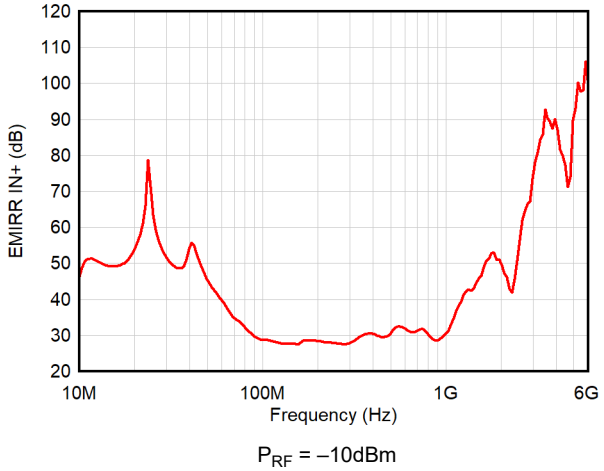


Figure 5-34. EMIRR vs Frequency

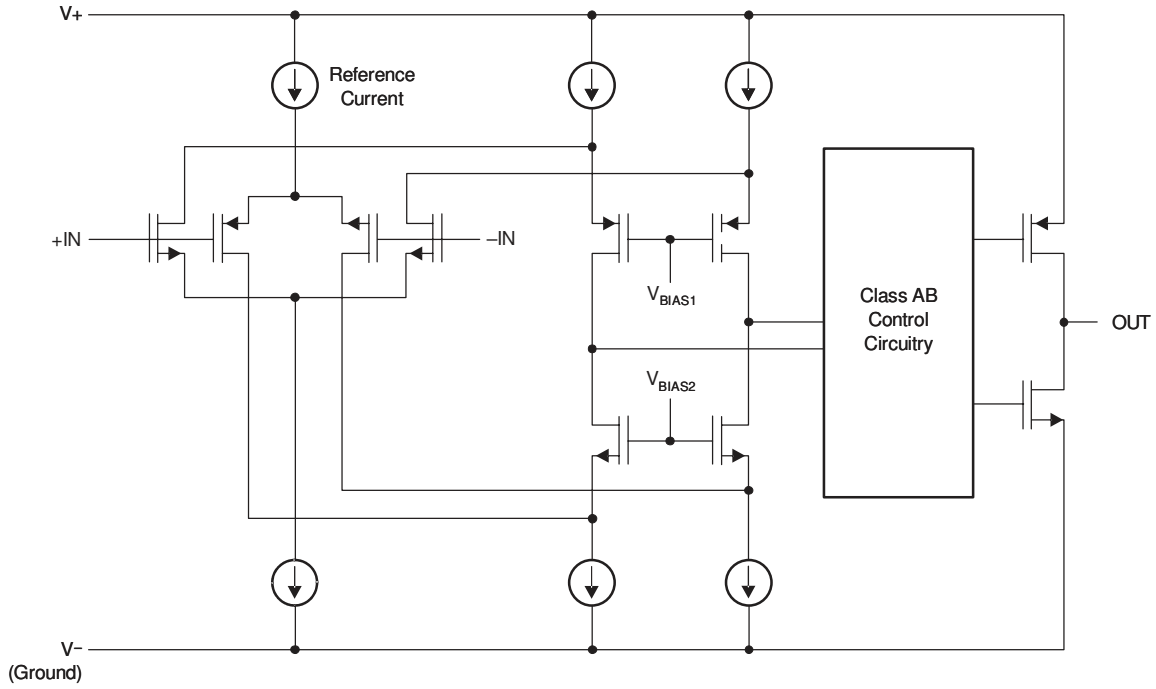
6 Detailed Description

6.1 Overview

The OPAx397 is a family of low offset, low-noise e-trim operational amplifiers (op amps) that uses a proprietary offset trim technique. These op amps offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx397 operate from 1.7V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve extremely low input bias current, wide input and output voltage ranges, high loop gain, and low, flat output impedance in small package options. The OPAx397 strengths also include 13MHz bandwidth, 4.4nV/$\sqrt{\text{Hz}}$ noise spectral density, and low 1/f noise. These features make the OPAx397 an exceptional choice for interfacing with sensors, photodiodes, and high-performance analog-to-digital converters (ADCs).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Operating Voltage

The OPAx397 family can be used with single or dual supplies from an operating range of V_S = 1.7V (±0.85V) up to 5.5V (±2.75V). The offset voltage is trimmed at 5.0V, however, the device maintains ultra-low offset voltages down to V_S = 1.7V.

Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics*.

6.3.2 Low Input Bias Current

The typical input bias current of the OPAx397 is extremely low (typically 10fA). Input bias current is dominated by leakage current from the ESD protection diodes, which is proportional to the area of the diode. The OPAx397 is able to achieve ultra-low input bias current as a result of modern process technology and advanced electrostatic discharge (ESD) protection design that minimizes the area of the diode.

In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in the forward-biasing of the ESD cells. Figure 6-1 shows the equivalent circuit.

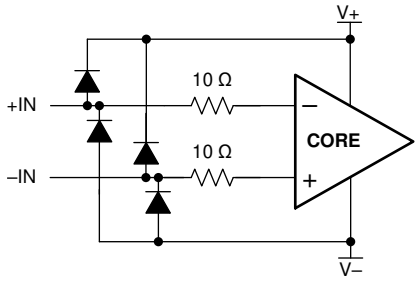


Figure 6-1. Equivalent Input Circuit

6.4 Device Functional Modes

The OPAx397 family is operational when the power-supply voltage is greater than 1.7V (±0.85V). The maximum specified power-supply voltage for the OPAx397 is 5.5V (±2.75V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx397 is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary e-trim operational amplifier technology gives the benefit of low input offset voltage over time and temperature, along with ultra-low input bias current. The OPAx397 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range to the supply rail, with low offset across the supply range, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx397 precision amplifiers are designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

7.2 Typical Application

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA397 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 7-1 shows the schematic.

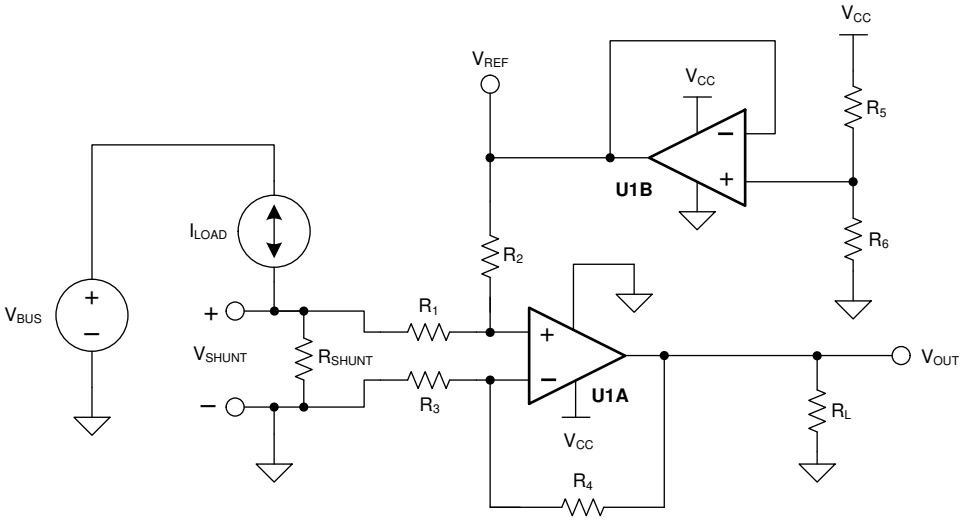


Figure 7-1. Bidirectional Current-Sensing Schematic

7.2.1 Design Requirements

This design example has the following requirements:

- Supply voltage: 3.3V
- Input: –1A to +1A
- Output: 1.65V ±1.54V (110mV to 3.19V)

7.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100mV and maximum load current of 1A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100mV to +100mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA397, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPA397 has a typical offset voltage of merely ±0.25µV (±5µV maximum).

Given a symmetric load current of –1A to +1A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA397 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA397 given a 3.3V supply.

$$-100\text{mV} < V_{CM} < 3.4\text{V} \tag{3}$$

$$100\text{mV} < V_{OUT} < 3.2\text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5:

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\text{ V} - 100\text{ mV}}{100\text{ m}\Omega \times [1\text{ A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 is 1kΩ. 15.4kΩ is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the calculated gain of the difference amplifier is 15.4V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors are selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

7.2.3 Application Curve

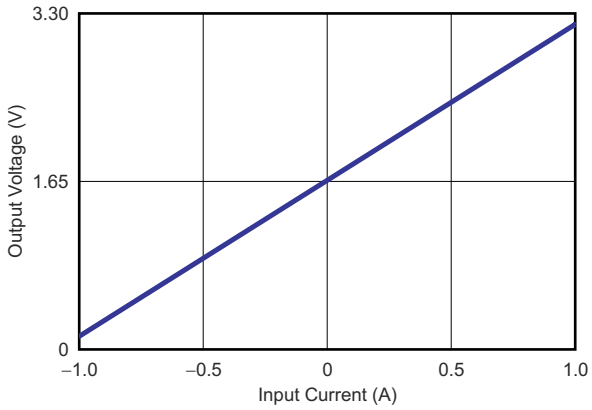


Figure 7-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

7.3 Power Supply Recommendations

The OPAx397 are specified for operation from 1.7V to 5.5V (±0.85V to ±2.75V).

CAUTION

Exceeding supply voltages listed in the *Absolute Maximum Ratings* table can permanently damage the device.

7.4 Layout

7.4.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short, and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by making sure these potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Use guard traces to minimize leakage current when ultra-low bias current is required.
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1µV/°C or higher, depending on materials used.

7.4.2 Layout Example

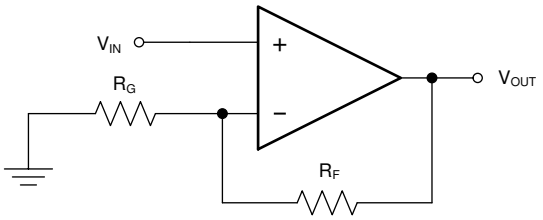


Figure 7-3. OPA397 Layout Schematic

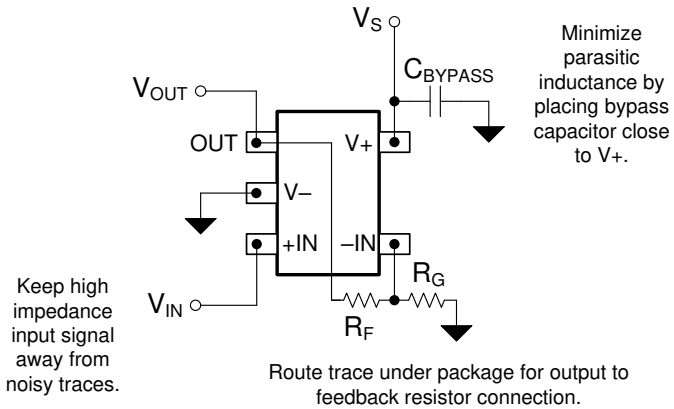


Figure 7-4. OPA397 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Amplifier Input Common-Mode and Output-Swing Limitations* application note
- Texas Instruments, *Offset Correction Methods: Laser Trim, e-Trim™, and Chopper* application brief

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

e-trim™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2021) to Revision A (April 2025)	Page
• Changed the status of the following packages from preview to active: DCK (SC70, 5), D (SOIC, 8), DGK (VSSOP, 8), and PW (TSSOP, 14)	1
• Changed Figure 6-4, *Open-Loop Gain and Phase vs Frequency*	9
• Changed Figure 6-5, *Closed-Loop Gain and Phase vs Frequency*	9

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2397DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3BQS
OPA2397DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2397D
OPA397DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JXT
OPA397DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

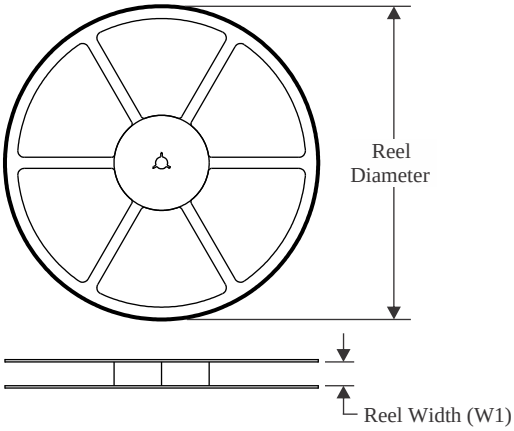
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

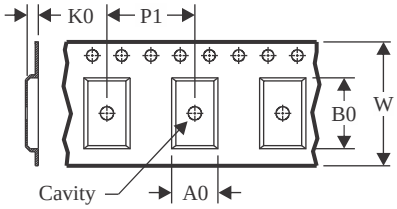
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

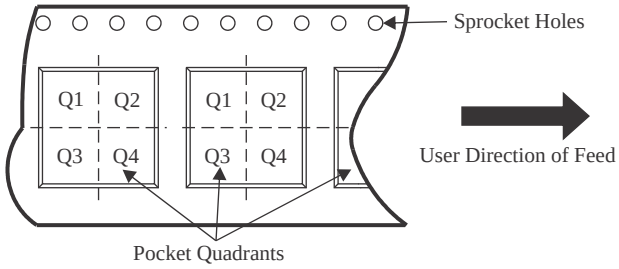


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

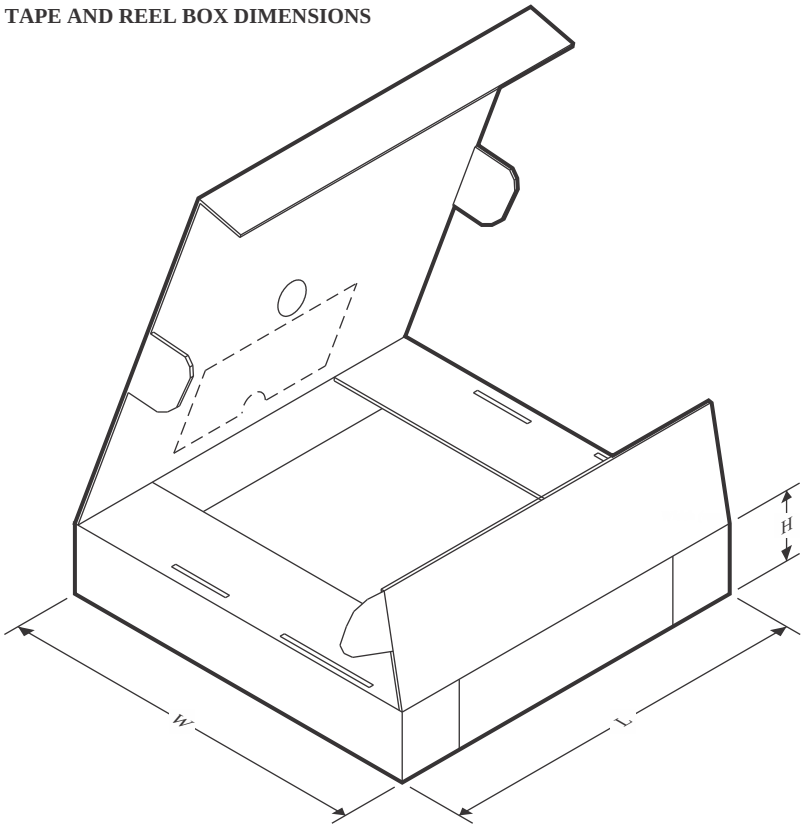
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2397DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2397DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA397DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA397DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA397DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA397DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

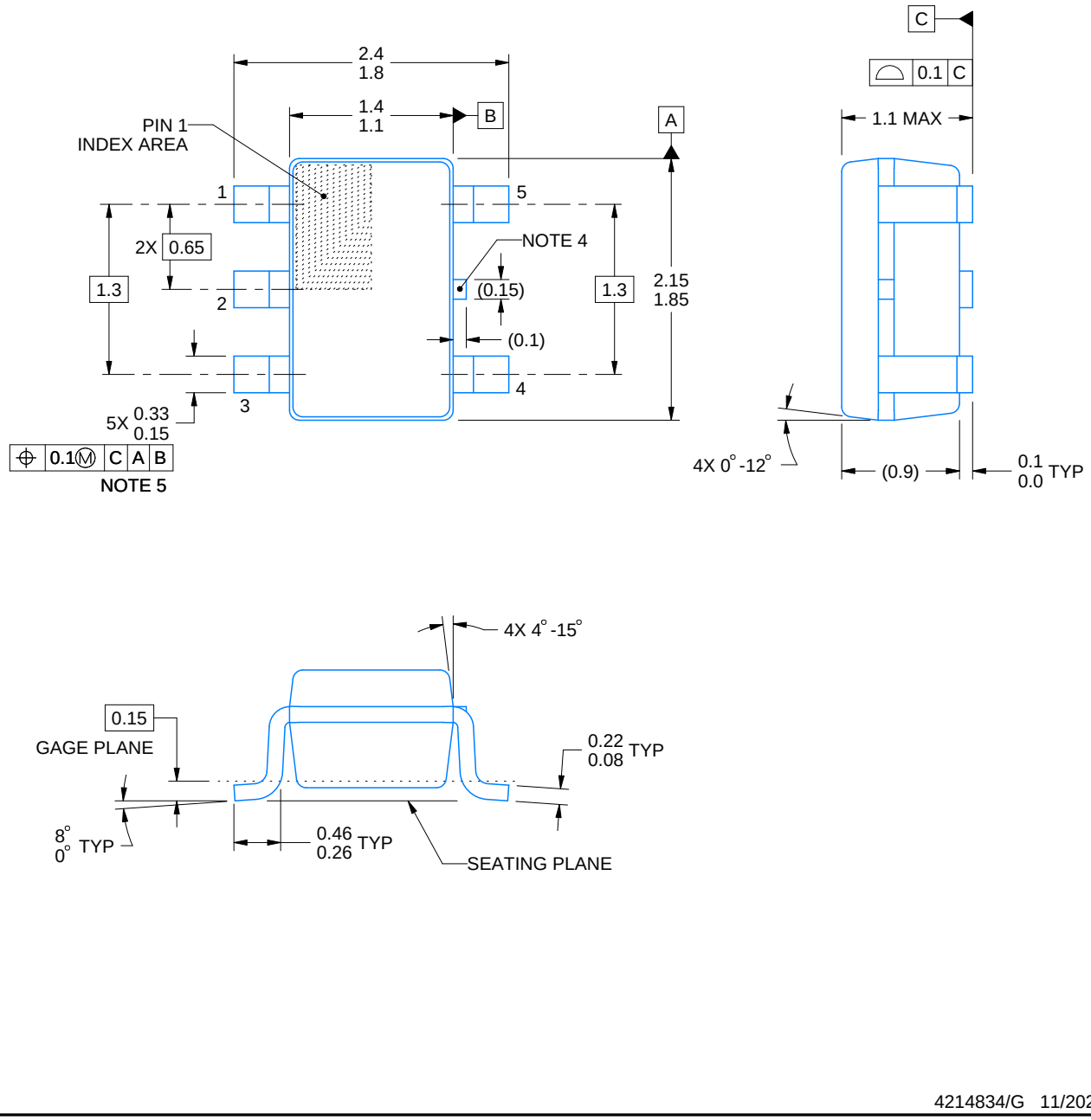
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2397DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2397DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA397DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA397DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA397DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA397DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

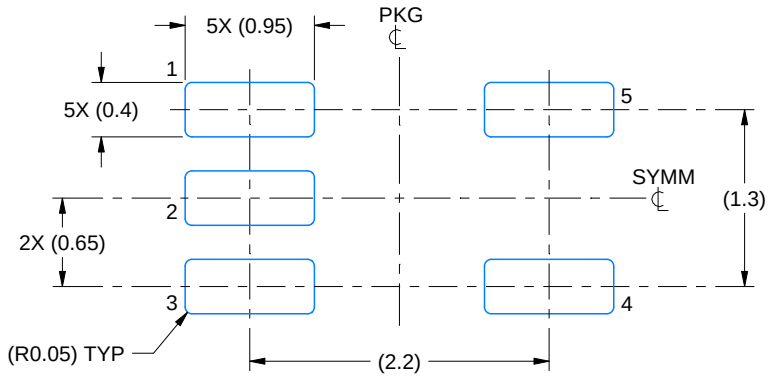
SMALL OUTLINE TRANSISTOR



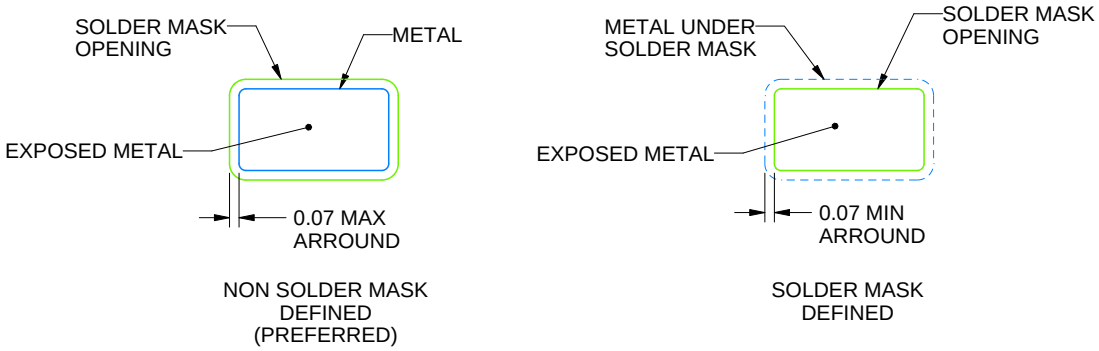
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

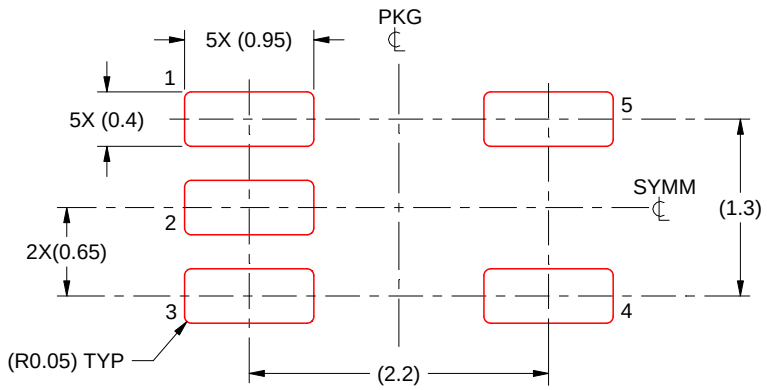


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

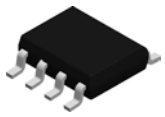


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

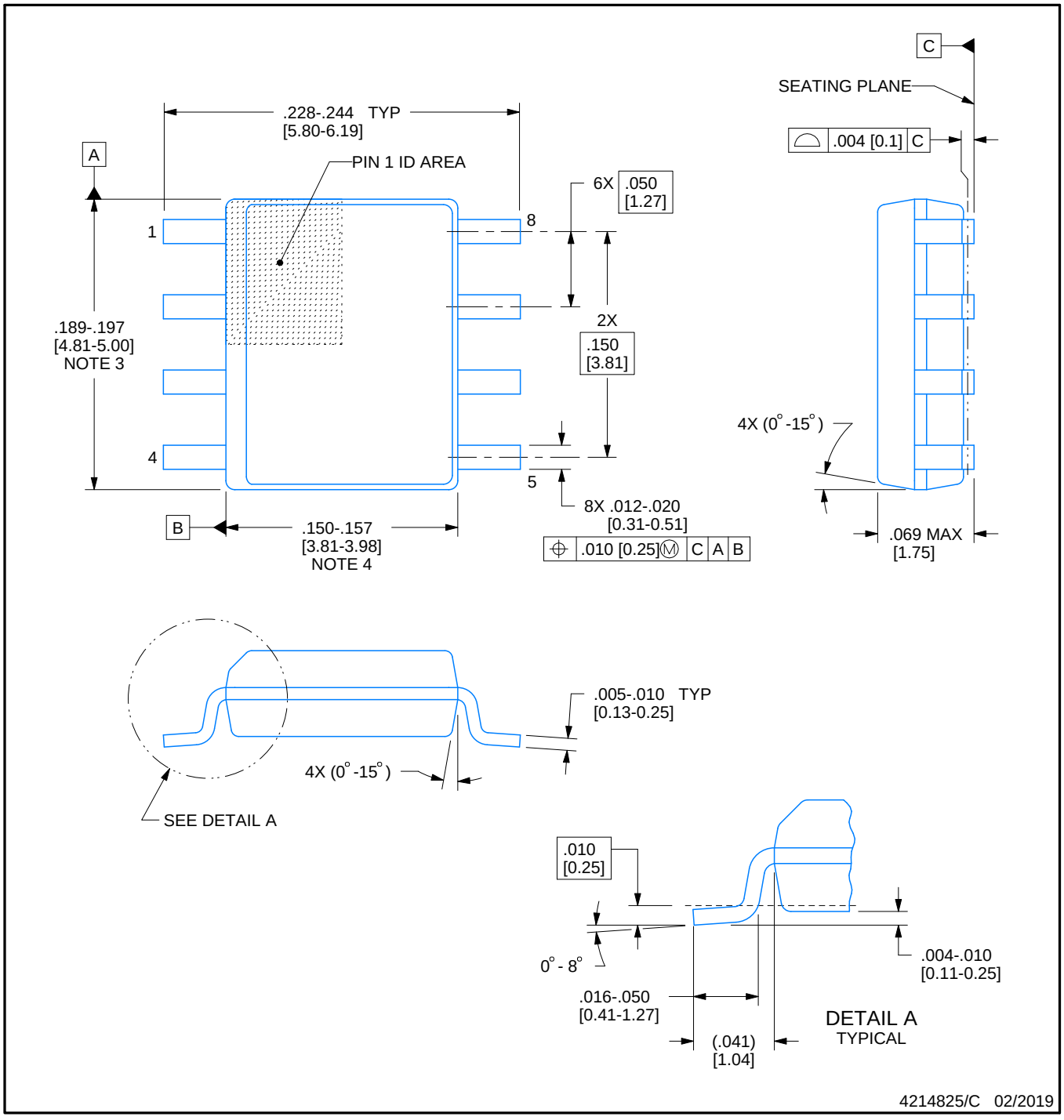


PACKAGE OUTLINE

D0008A

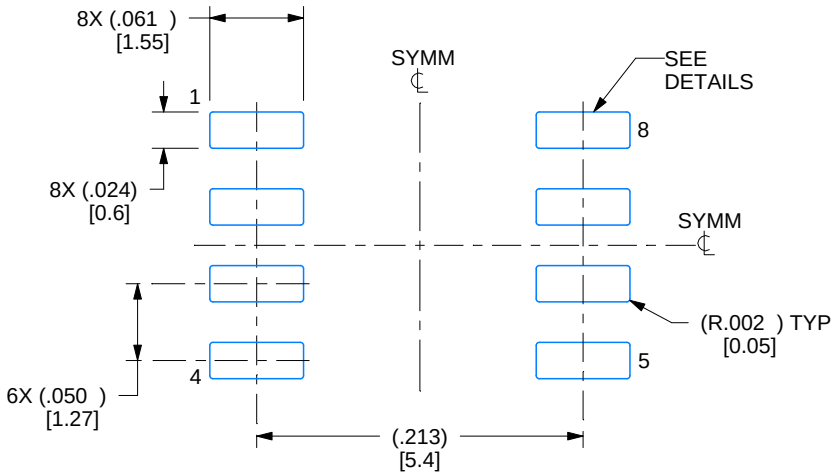
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

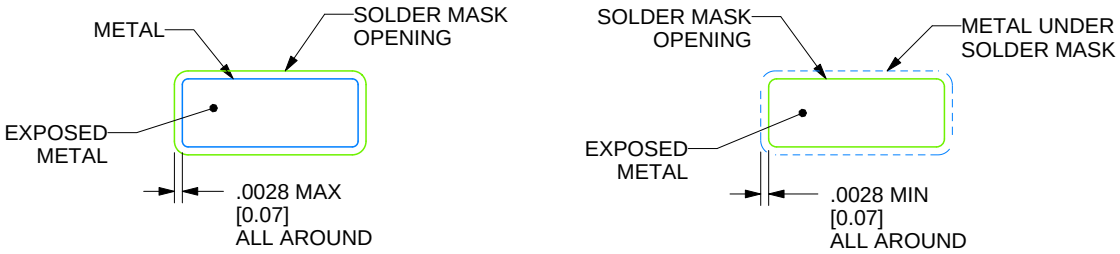


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

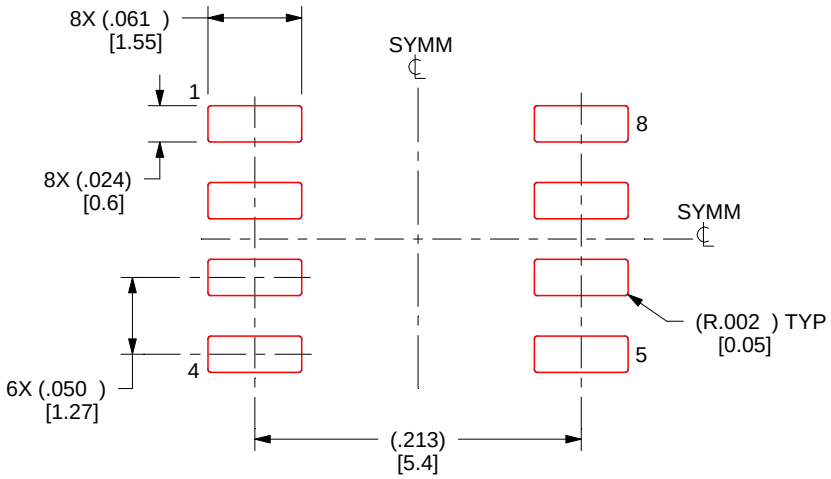
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

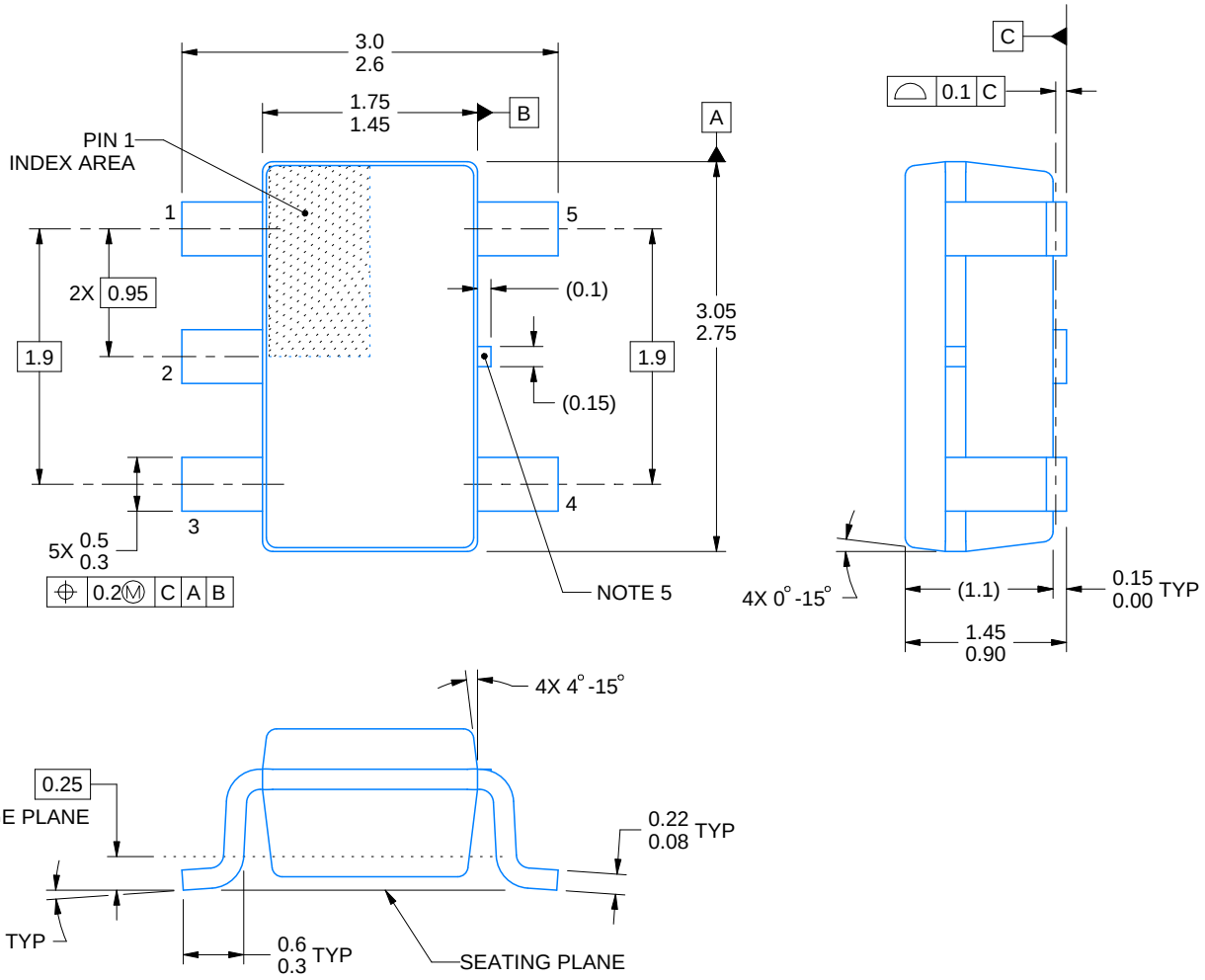
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

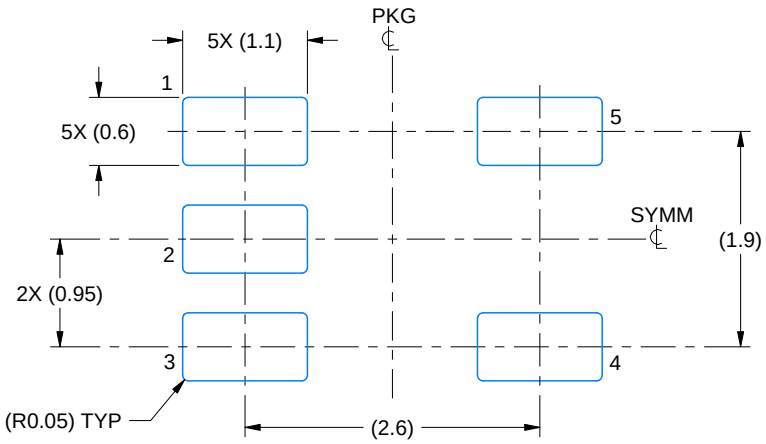
SMALL OUTLINE TRANSISTOR



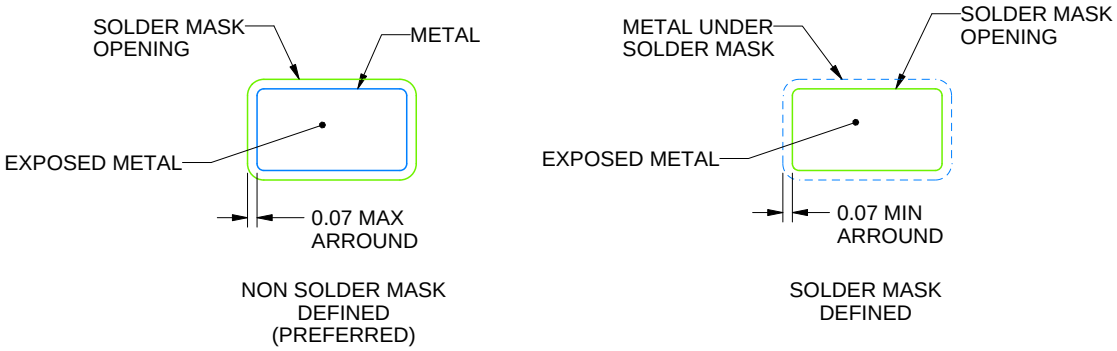
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

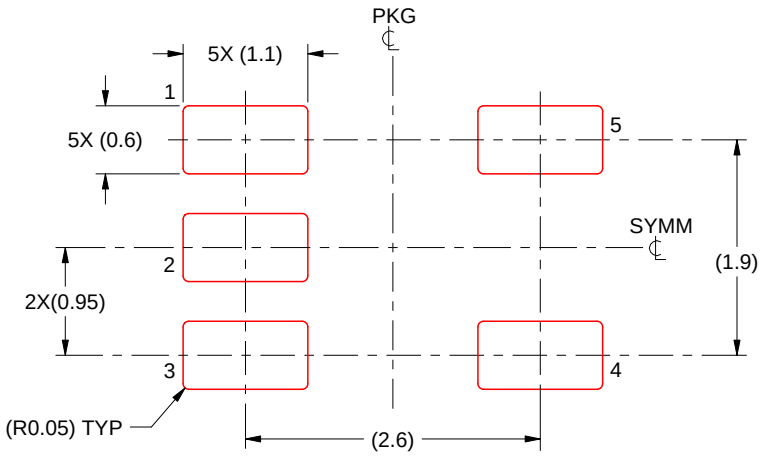


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

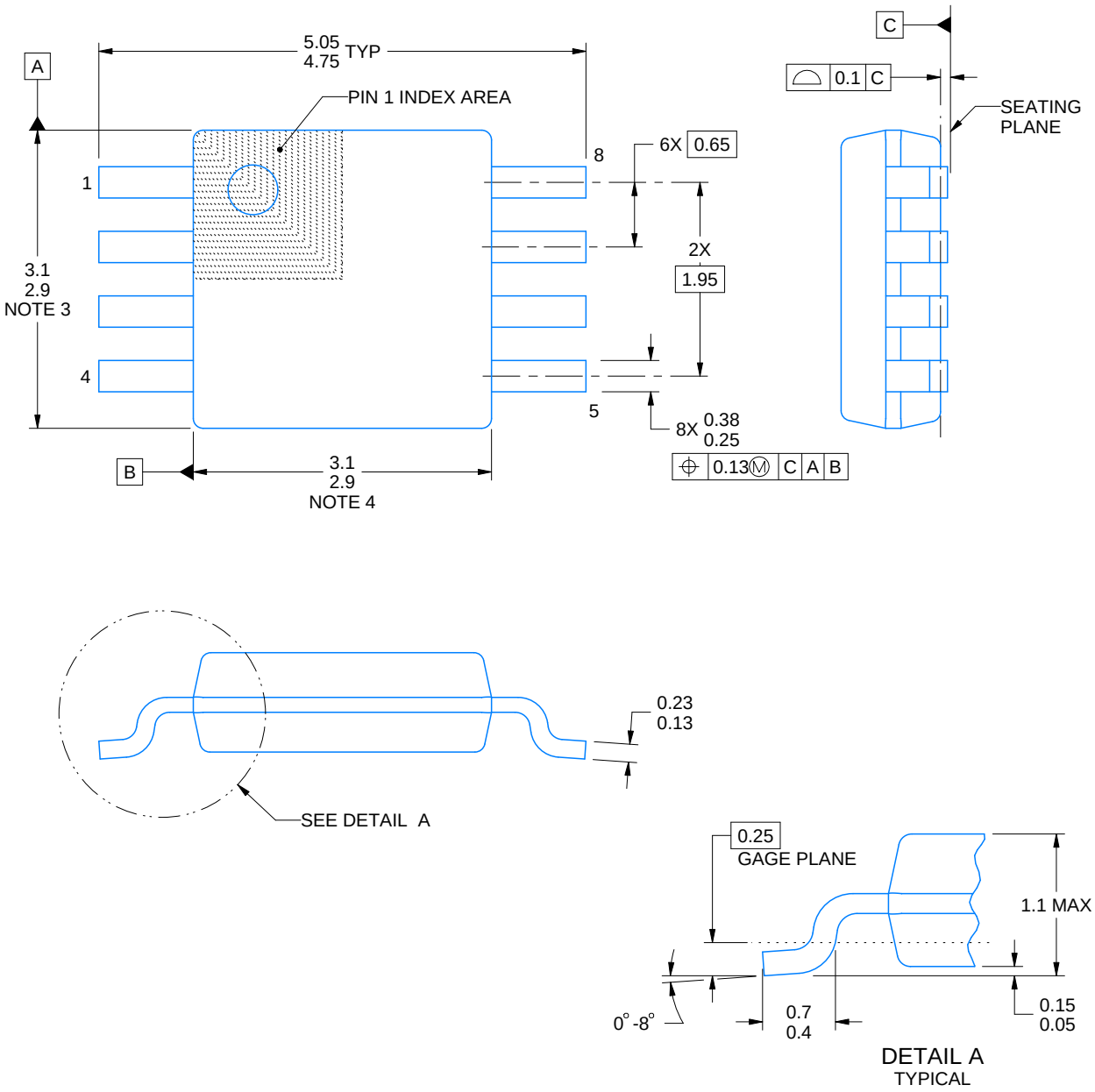
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

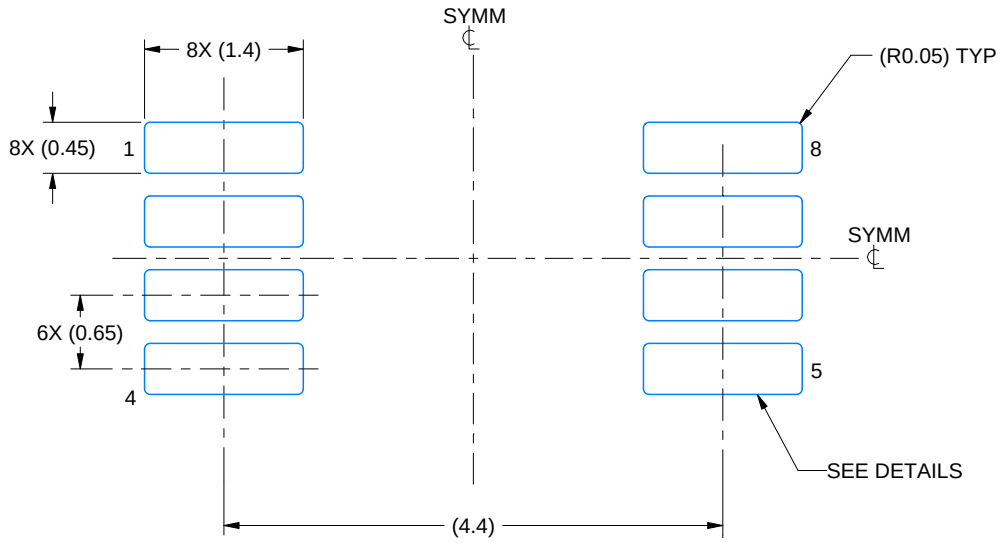
SMALL OUTLINE PACKAGE



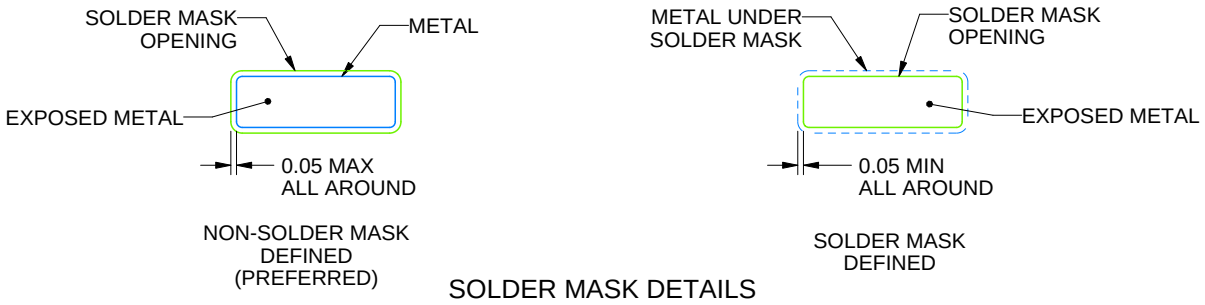
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

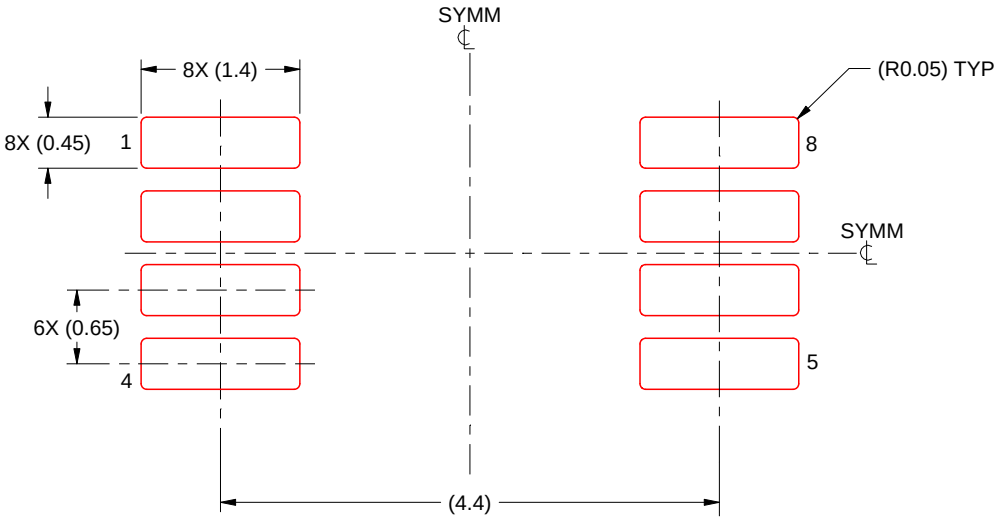


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025